USB Type-C Port Controller

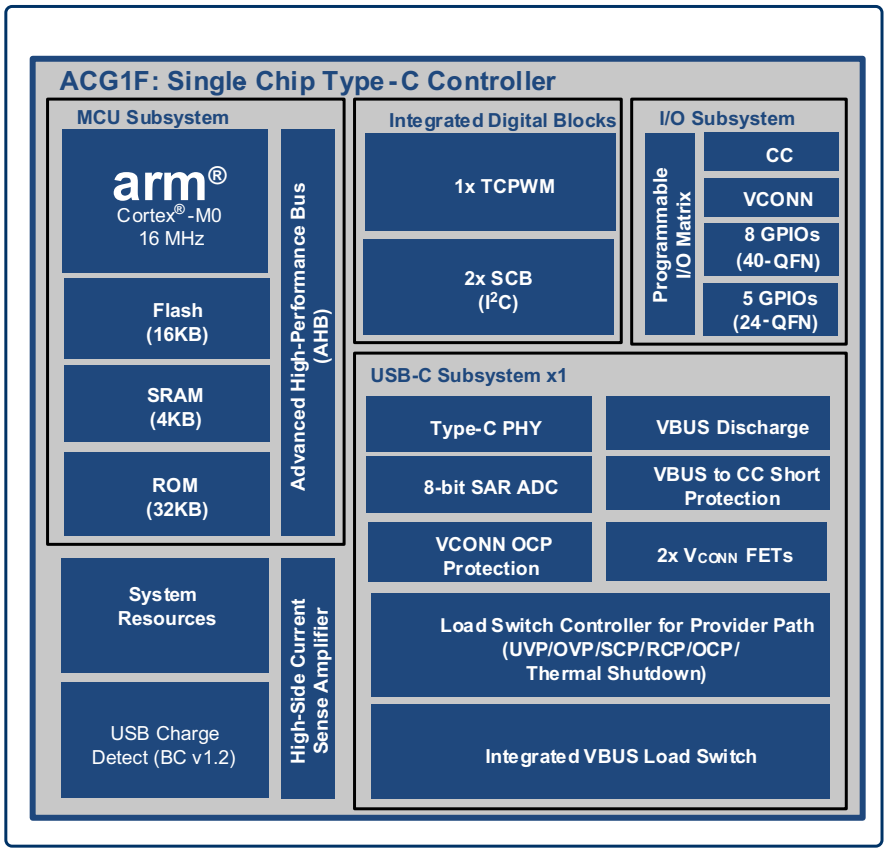
General Description

ACG1F (Type-A to Type-C Generation - 1 FET) is a single-port USB Type-C controller that complies with the latest USB Type-C specifications. ACG1F provides a complete USB Type-C control solution for notebooks and desktops. It can also be used in devices required to convert legacy Type-A data port to Type-C data port. ACG1F uses Cypress' proprietary M0S8 technology with a 32-bit Arm® Cortex®-M0 processor with 16-KB flash and integrates a Type-C controller (no Power Delivery) and a VBUS load switch (5 V/3A).

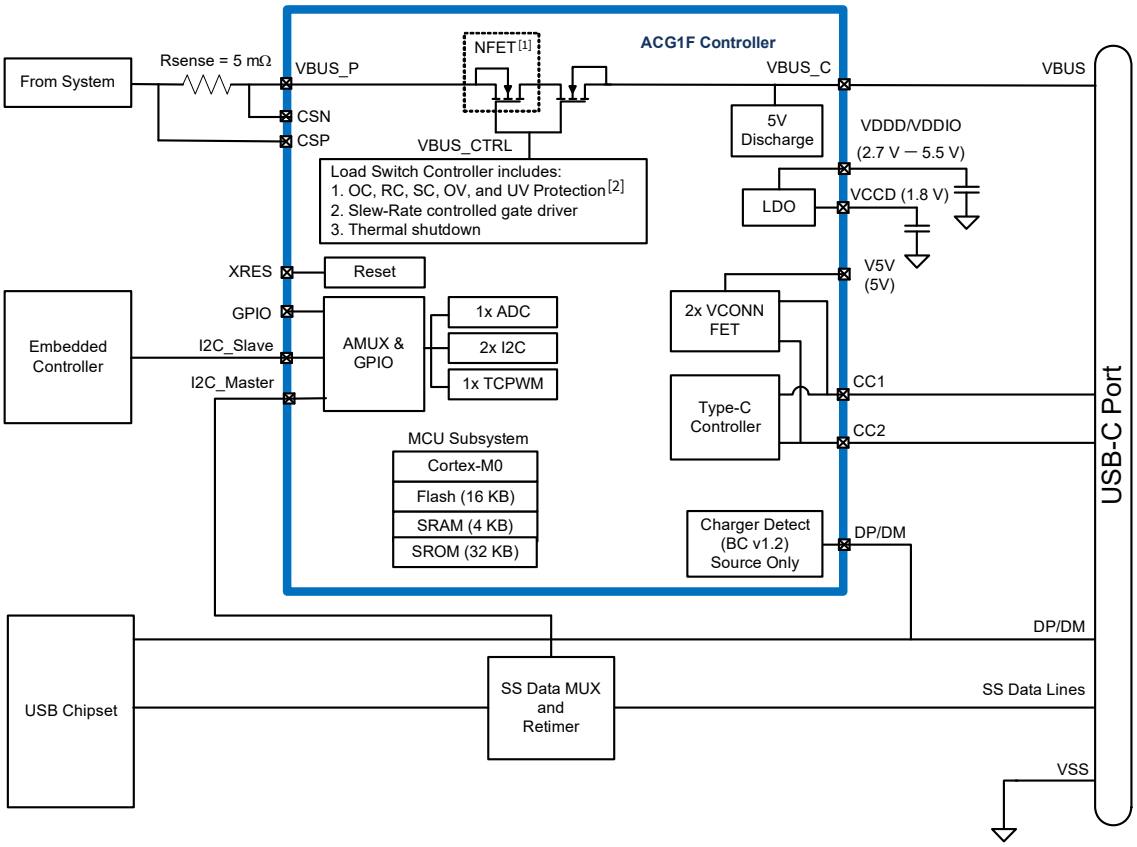
Features

- **USB Type-C Support**
  - Integrated Type-C controller supporting Type-C v1.3
  - Integrated 2x VCONN FET with OCP to power EMCA cable
- **Integrated VBUS Load Switch Controller**
  - Integrated VBUS load switch supports
    - 5 V/3A VBUS NFET
    - RDSon of load switch: 45-mΩ (typ) for 40-QFN, 15-mΩ (typ) for 24-QFN
  - Slew rate control turn-ON on the provider VBUS switch
  - Configurable hardware-controlled VBUS overvoltage protection (OVP), overcurrent protection (OCP), and reverse current protection (RCP)
  - VBUS high-side current sense amplifier across external precision series resistance (Rsense) of 5 mΩ.
  - Over temperature thermal shutdown
  - VBUS to CC short circuit protection up to 20 V
- **2x I^2C**
  - Supports USB Type-C Connector System Software Interface (UCSI) over I^2C interface
  - Controls external high-speed redriver/retimer mux interface over I^2C
- **Legacy Charging**
  - Integrated Charge Detect: BC v1.2
- **32-bit MCU Subsystem**
  - 16-MHz Arm Cortex-M0 CPU
  - 16-KB Flash
  - 4-KB SRAM
  - 32-KB SROM
- **Packages**
  - 40-QFN, 0.5-mm pitch
  - 24-QFN, 0.5-mm pitch
  - Supports industrial temperature range (–40 °C to +85 °C)

Logic Block Diagram



Functional Block Diagram



Notes
1. This NFET is available in the 40-QFN part only.
2. RC protection only available in 40-QFN part.

Table of Contents

1 Functional Overview

1.1 USB Type-C Subsystem

This subsystem provides the interface to the Type-C USB port and comprises the following:

- USB-PD Physical Layer (only Rp terminations and Line-Comparators)
- VCONN FETs
- ADC
- Undervoltage, overvoltage, and reverse-current protection on VBUS
- High-side current sense amplifier for VBUS with OCP and short-circuit protection (SCP)
- VBUS Discharge
- Gate Driver for VBUS NFET
- Charger Detect

1.1.1 USB-PD Physical Layer

The USB Type-C subsystem contains the USB-PD physical layer block and supporting circuits. The USB-PD Physical Layer consists of only two Deep Sleep comparators that are used to detect Type-C attach/detach, CC line activity events, and determine the voltage range on the chosen CC line. In addition, the block includes Rp termination and their switches as required by the USB Type-C spec. The Rp termination is implemented using current sources to indicate the current profiles supported by DFP.

1.1.2 VCONN FET

ACG1F has power supply input V5V pin for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs in ACG1F to power either CC1 or CC2 pins. These FETs are capable of sourcing maximum of 1.0W on the CC1 or CC2 pin to power active EMCA cables. At any given time, only one of the VCONN FETs shall be ON. The floating V5V pin should not cause ACG1F to malfunction and draw more current.

1.1.3 ADC

ACG1F has one low-footprint 8-bit SAR ADC available for general purpose A-D conversion applications in the chip. The ADC can be accessed from the GPIOs through an on-chip analog mux.

1.1.4 Undervoltage and Overvoltage Protection on VBUS

The chip implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The thresholds for both OCP and UVOV are made programmable.

1.1.5 High-side Current Sense Amplifier for VBUS

The chip supports the programmable threshold VBUS current sensing through the VBUS path. External resistor (5 mΩ) placed in the connector VBUS path connects to the chip, and the drop across this resistor is monitored to sense the magnitude of current.

1.1.6 VBUS Reverse Current Protection

ACG1F restricts reverse current to zero on the VBUS provider path when Type-C VBUS is greater than VIN (provider voltage before the VBUS NFET). ACG1F reacts quickly (less then 1 µs - Typ) and turns off the VBUS provider NFET.

1.1.7 VBUS Discharge

The chip supports 21.5-V VBUS discharge circuitry inside the 40-QFN package and 5-V VBUS discharge circuitry inside the 24-QFN package. After cable removal detection, the chip will discharge the residual charge and bring the floating VBUS back to 0.8 V.

1.1.8 VBUS Load Switch

ACG1F has an integrated VBUS provider load switch, which includes OVP, OCP, SCP, RCP protection, and high-side current sense amplifier. ACG1F supports thermal protection where the load switch is turned OFF when the on-chip temperature rises above the threshold temperature and turns ON the load switch when the device temperature falls below threshold temperature.

1.1.9 Gate Driver for VBUS NFET

ACG1F has an integrated gate driver to drive NFETs on the VBUS provider path.

1.1.10 Charger Detect

The chip implements battery charger emulation (source) for USB BC.1.2.

1.1.11 High-Voltage Tolerant CC Lines

The chip supports high-voltage tolerant CC lines. In the case of CC short to VBUS through connectors, these lines will be protected internally.

1.1.12 Reverse Current Protection (RCP)

ACG1F controller supports RCP in 40-QFN package. ACG1F integrates the RCP circuitry that has the capability of sensing reverse current that lasts for more than 10 µs and protects the system by shutting down the Gate automatically upon detection of such events. ACG1F provides RCP circuitry that can detect reverse current flow from connector VBUS_C to provider VBUS_P. The RCP event is recognized whenever VBUS_C > VBUS_P while provider FET is ON, causing current to flow from connector VBUS to provider VBUS. After recognizing the RCP event, the provider FET is shut down thus isolating the provider and connector VBUS. ACG1F has three distinct mechanisms to detect the reverse current as shown in **Figure 1-1**.

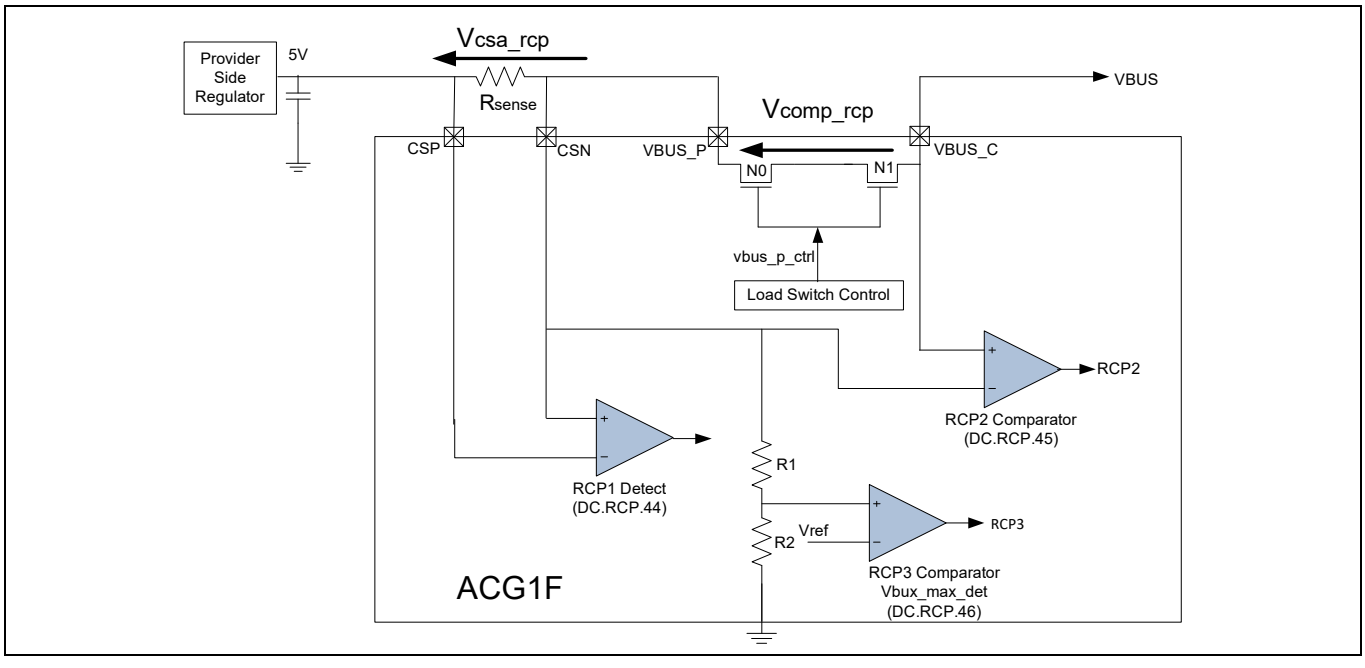


Figure 1-1 RCP Mechanism

- Mechanism 1: A comparator senses the voltage drop across external Rsense through pins CSP and CSN. This comparator signals an RCP event whenever CSN > CSP by the Vcsa_rcp voltage given in **Table 6-23**. The output of this comparator RCP1 is shown in **Figure 1-1**.
- Mechanism 2: A comparator senses the voltage drop across provider FET through CSN and VBUS pin of ACG1F. This comparator signals an RCP event whenever VBUS > CSN by the Vcomp_rcp voltage given in **Table 6-23**. The output of this comparator RCP2 is shown in **Figure 1-1**.
- Mechanism 3: A comparator senses the 33.33% voltage of the CSN pin and compares it against Vref = 1.79 V for 5-V provider VBUS application. This comparator signals an RCP event whenever CSN voltage goes above Vbus_-max_det voltage given in **Table 6-23** for a 5-V application. The output of this comparator RCP3 is shown in **Figure 1-1**. Note that Vref is programmable and the voltage divider has an option to use 25% or 33.33% value which is configurable only through firmware. To change the Vref value to 25%, contact local Cypress Sales Representative.

  When any one of the three comparator outputs show an RCP event, then the provider FET is turned OFF.

1.2 MCU and Memory

1.2.1 CPU

The Cortex M0 in ACG1F is part of a 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for ACG1F has 4 break-point (address) comparators and two watchpoint (data) comparators.

1.2.2 Flash

The 16-KB integrated Flash memory shall store the firmware implementing Type-C functionality. The 16-KB flash shall support in-system firmware upgrade through the SWD or I^2C interface A section of Flash can be used for storing Device/System power parameters. The flash row size is 64 Bytes.

1.2.3 SROM

The 32-KB SROM contains boot and configuration routines. The SROM will also be used for storing frequently-used functionalities in the firmware.

1.2.4 SRAM

The 4-KB RAM is used under software control to store temporary status of system variables and parameters.

2 Power System Overview

ACG1F operates on a single power-supply input VDDD with a valid range of (2.7 V–5.5 V). In addition, there is a V5V supply pin that sources the VCONN supply to the Type-C connector; the valid levels on the V5V supply can range from 4.85 V–5.5 V. V5V does not power the chip. The V5V supply support operation over 4.85 V–5.5 V while the VDDD input supports operation over 2.7 V–5.5 V. ACG1F has two different power modes: Active and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. VDDD should be shorted to VDDIO at system level. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1-µF capacitor for the regulator stability only. The VCCD pin is not supported as a power supply.

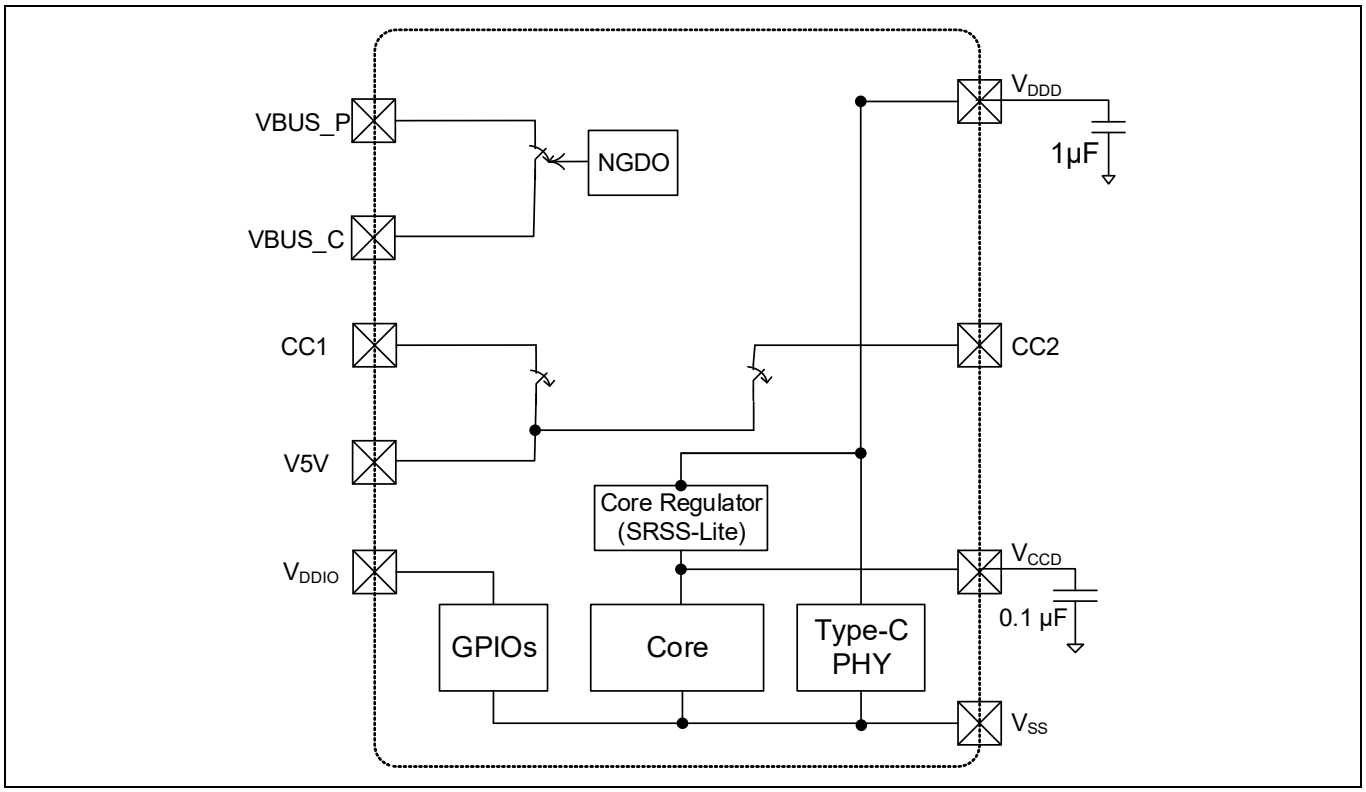


Figure 2-1 ACG1F Power System

2.1 Power Modes

Table 2-1 lists the power modes of the device, accessible and observable by the user.

Table 2-1 ACG1F Power Modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
DEEP SLEEP	Main regulator and most hard-IPs are shut down. DeepSleep regulator powers logic, but only low-frequency clock is available.
SCAN	System is in Scan mode. Scan mode is entered by applying DFT key during XRES and exited by applying something other than the DFT key (at least one bit).

2.2 Peripherals

ACG1F has two SCBs, which can each implement only an I^2C.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU.

The SCB blocks support 8-deep FIFOs for Receive and Transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA. Data throughput is not a critical consideration for I^2C.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes. The I^2C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I^2C speeds are guaranteed by using appropriate pull-up resistor values depending on VDDD, bus capacitance, and resistor tolerance. For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I^2C bus specification and user manual (the latest revision is available at **www.nxp.com**).

One of the SCB (typically SCB1) blocks is used to implement the Host Processor Interface (HPI) slave, which allows an external MCU to control the firmware operation.

The HPI I^2C slave address is configurable using the I2C_CFG_EC pin for ACG1F 40-QFN as shown in **Table 2-2**. The default address for ACG1F 24-QFN will be 0x66.

Table 2-2 I^2C Slave Address Configuration

I2C_CFG_EC Configuration	I^2C Slave
Floating	0x60
Pulled up with 1 kΩ	0x64
Pulled down with 1 kΩ	0x62

2.3 Timer/Counter/PWM Block (TCPWM)

The timer block of ACG1F supports one timer or counter or pulse-width modulator. The timer is available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

2.4 GPIO

The ACG1F die has eight GPIOs in 40-QFN and five GPIOs in 24-QFN including the I^2C and SWD pins, which can also be used as GPIOs. The GPIO block shall implement the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control.

During power-on and reset, the blocks are forced to the Disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals, such as the USB Type-C port, are also fixed in order to reduce internal multiplexing complexity. Data Output Registers and Pin State Registers store, respectively, the values to be driven on the pins and the states of the pins themselves. The pins can be configured by programming of registers through software for each digital I/O Port.

Every I/O pin can generate an interrupt if so enabled and each I/O Port has an Interrupt Request (IRQ) and Interrupt Service Routine (ISR) Vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the High-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The I/Os (on data bus) do not draw current on power down.

3 Pinouts

Table 3-1 24-QFN Pin List

Group Name	Pin Name	Port	Pin	Description
USB Type-C	CC1	Analog	24	USB PD connector detect/Configuration Channel 1
	CC2	Analog	22	USB PD connector detect/Configuration Channel 2
Mux	DPLUS	Analog	13	USB 2.0 DP for BC1.2
	DMINUS	Analog	12	USB 2.0 DM for BC1.2
VBUS OCP	CSP	Analog	17	Current Sense Positive Input for VBUS side external Rsense
	CSN	Analog	18	Current Sense Negative input for other side of external Rsense
GPIOs and Serial Interfaces		P0.0	19	SWD Clock / SCB2 I^2C Data / GPIO
		P0.3	20	GPIO
		P0.4	21	SWD Data / SCB2 I^CC clock / GPIO
		P1.1	2	SCB1 I^2C Data / GPIO
		P1.2	3	SCB1 I^2C clock / GPIO
Reset	XRES	Analog	1	Reset input
Power	VBUS_C	Power	7, 8, 9, 10	Connector VBUS Output from Power NFET
	VBUS_P	Power	11	Provider VBUS Input to Power NFET (Same as CSN at system Level)
	VDDD	Power	15	Supply for the System
	VCCD	Power	16	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	V5V	Power	23	Supply for VCONN FET of Type-C
Ground	VSS	Ground	4, 5, 14	Ground
EPAD	VBUS_P	Power	–	Provider VBUS Input to Power NFET (Same as CSN at system Level)

Table 3-2 40-QFN Pin List

Group Name	Pin Name	Port	Pin	Description
USB Type-C	CC1	Analog	9	USB PD connector detect/Configuration Channel 1
	CC2	Analog	7	USB PD connector detect/Configuration Channel 2
Mux	DPLUS	Analog	28	USB 2.0 DP for BC1.2
	DMINUS	Analog	27	USB 2.0 DM for BC1.2
VBUS OCP	CSP	Analog	1	Current Sense Positive Input for VBUS side external Rsense
	CSN	Analog	40	Current Sense Negative input for other side of external Rsense
GPIOs and Serial Interfaces		P0.0	2	SWD Clock / GPIO
		P0.1	3	SCB2 I^2C Data / GPIO
		P0.2	4	SCB2 I^2C Clock / GPIO
		P0.3	5	GPIO
		P0.4	6	SWD Data / GPIO
		P1.0	15	Embedded Controller interrupt / GPIO
		P1.1	16	SCB1 I^2C Data / GPIO
		P1.2	17	SCB1 I^2C Clock / GPIO
Reset	XRES	Analog	10	Reset input
Power	VBUS_C	Power	21, 22, 23	Connector VBUS Output from Power NFET
	VBUS_P	Power	24, 25, 26	Provider VBUS Input to Power NFET (Same as CSN at system Level)
	VDDD	Power	31	Supply for the System
	VDDIO	Power	32	At system-level short the VDDD to VDDIO
	VCCD	Power	33	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	V5V	Power	8	Supply for VCONN FET of Type-C
EPAD	VSS	Ground	–	Ground

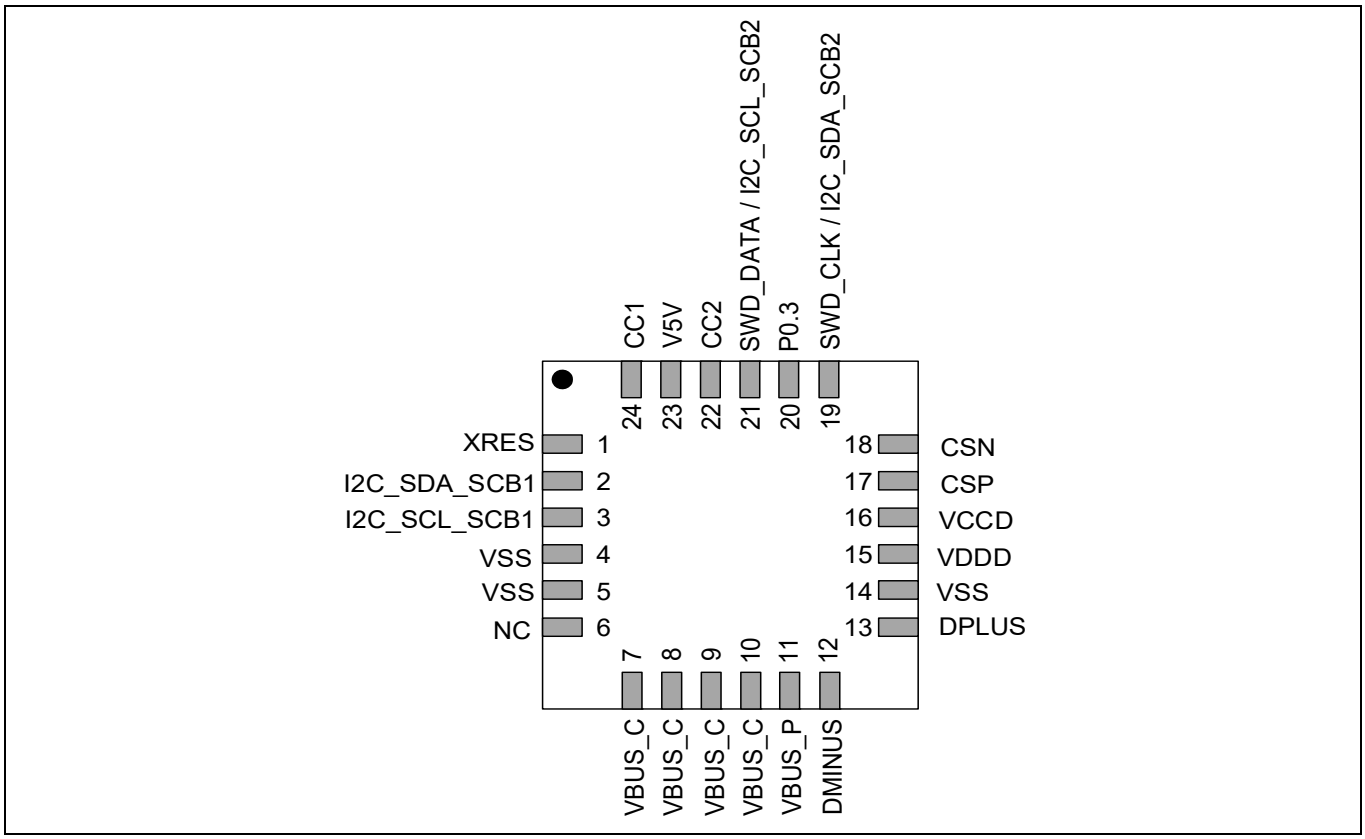


Figure 3-1 24-Pin QFN Pinout

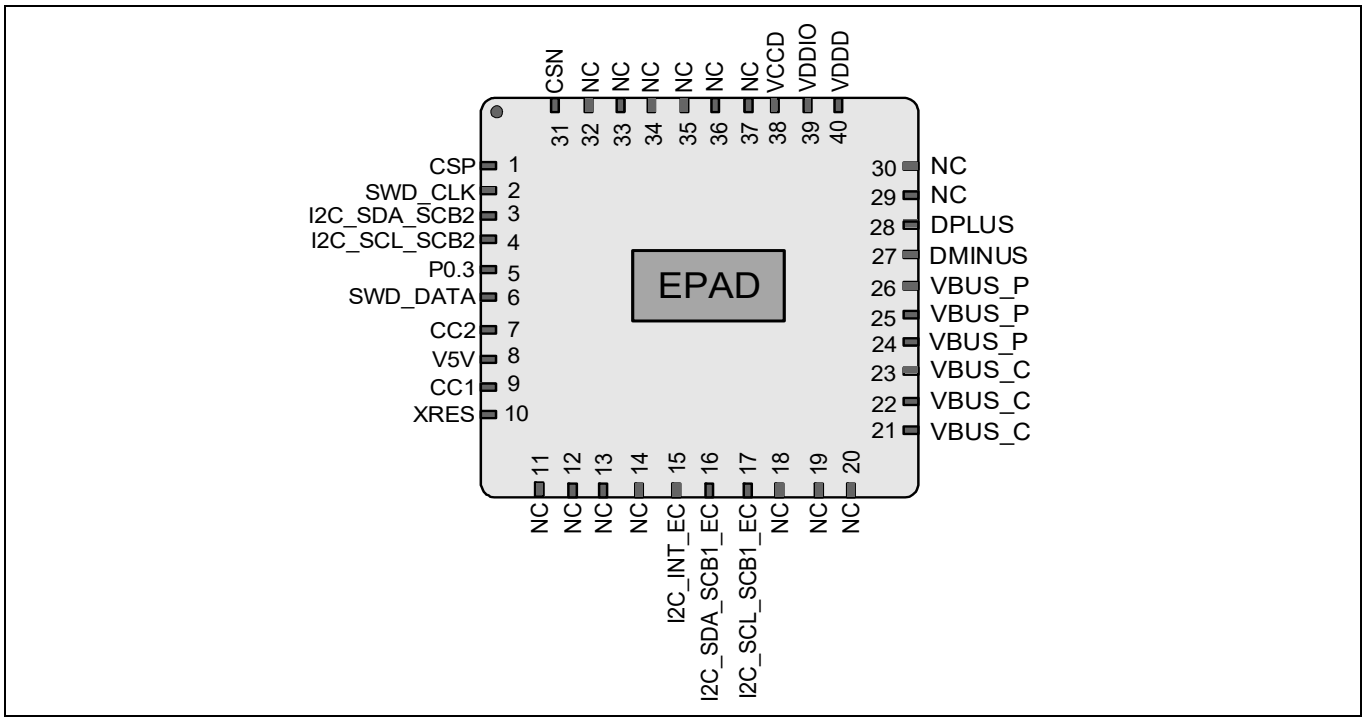


Figure 3-2 40-Pin QFN Pinout

4 Application Diagrams

Figure 4-1 illustrates a Type-C port DFP application diagram using ACG1F. The Type-C port can be used as a Type-A to Type-C converter. The ACG1F device communicates with the embedded controller (EC) over I^2C bus, which manages the ACG1F operation. It also updates external analog mux Controller via I^2C to route the Super-Speed signals coming from the Type-C port to the USB host. The ACG1F device supports battery charger detection (BC 1.2) through USB 2.0 DPLUS and DMINUS lines of the Type-C receptacle which is connected to the controller and to the DPLUS and DMINUS lines of the USB Host controller. ACG1F offers VBUS Short protection on CC lines. The ACG1F device has integrated VCONN FETs for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. The integrated VBUS load switch is used for providing power over VBUS. The 5-mΩ resistor between the 5-V supply and provider FETs is used for overcurrent detection on the VBUS.

Figure 4-1 illustrates Single Port Type-C port DFP application diagram using CYAC1126-40LQXIT.

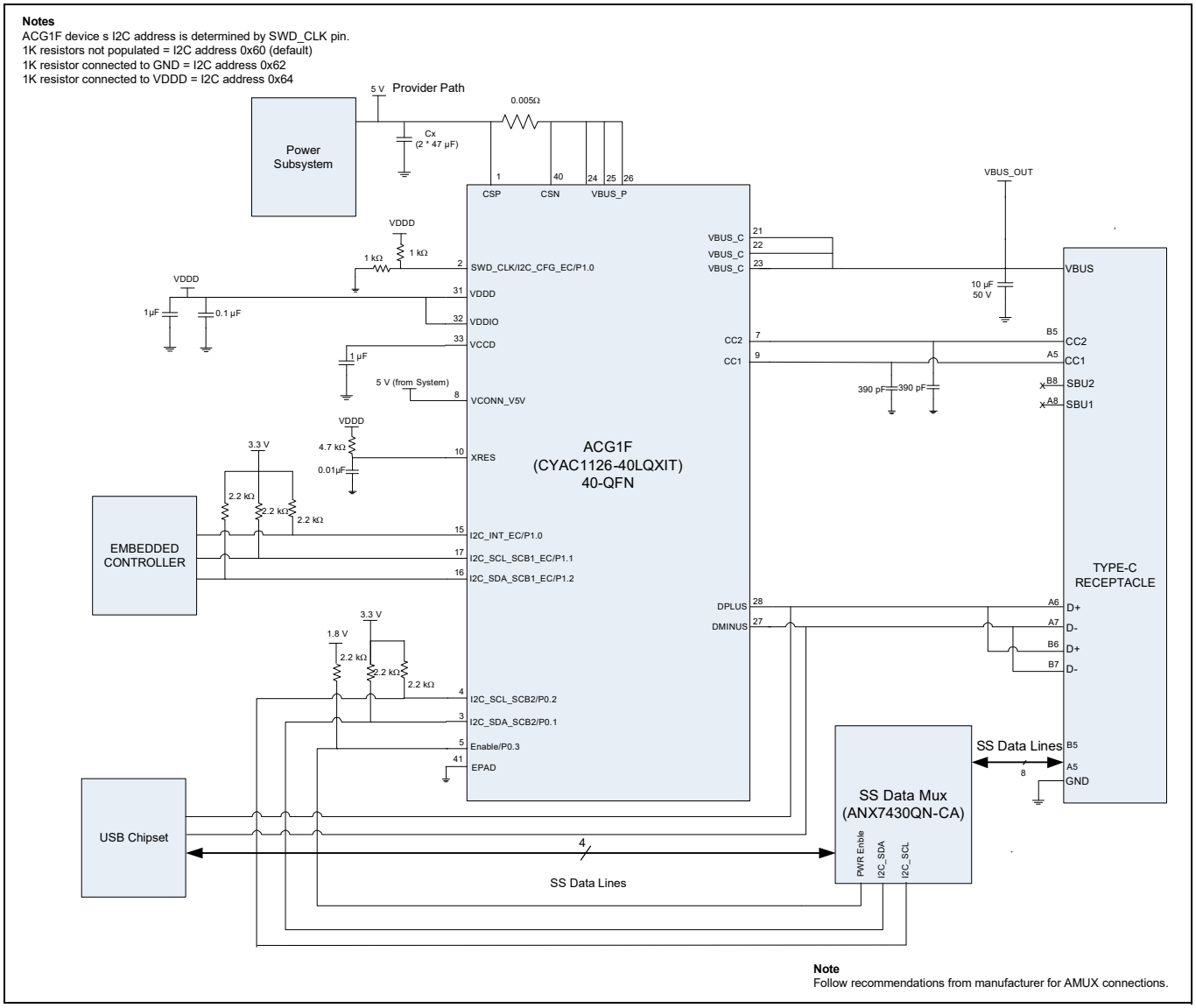


Figure 4-1 ACG1F in Single Port USB Type-C Notebook Application using CYAC1126- 40LQXIT

Figure 4-2 illustrates single port Type-C port DFP application diagram using CYAC1126-24LQXIT.

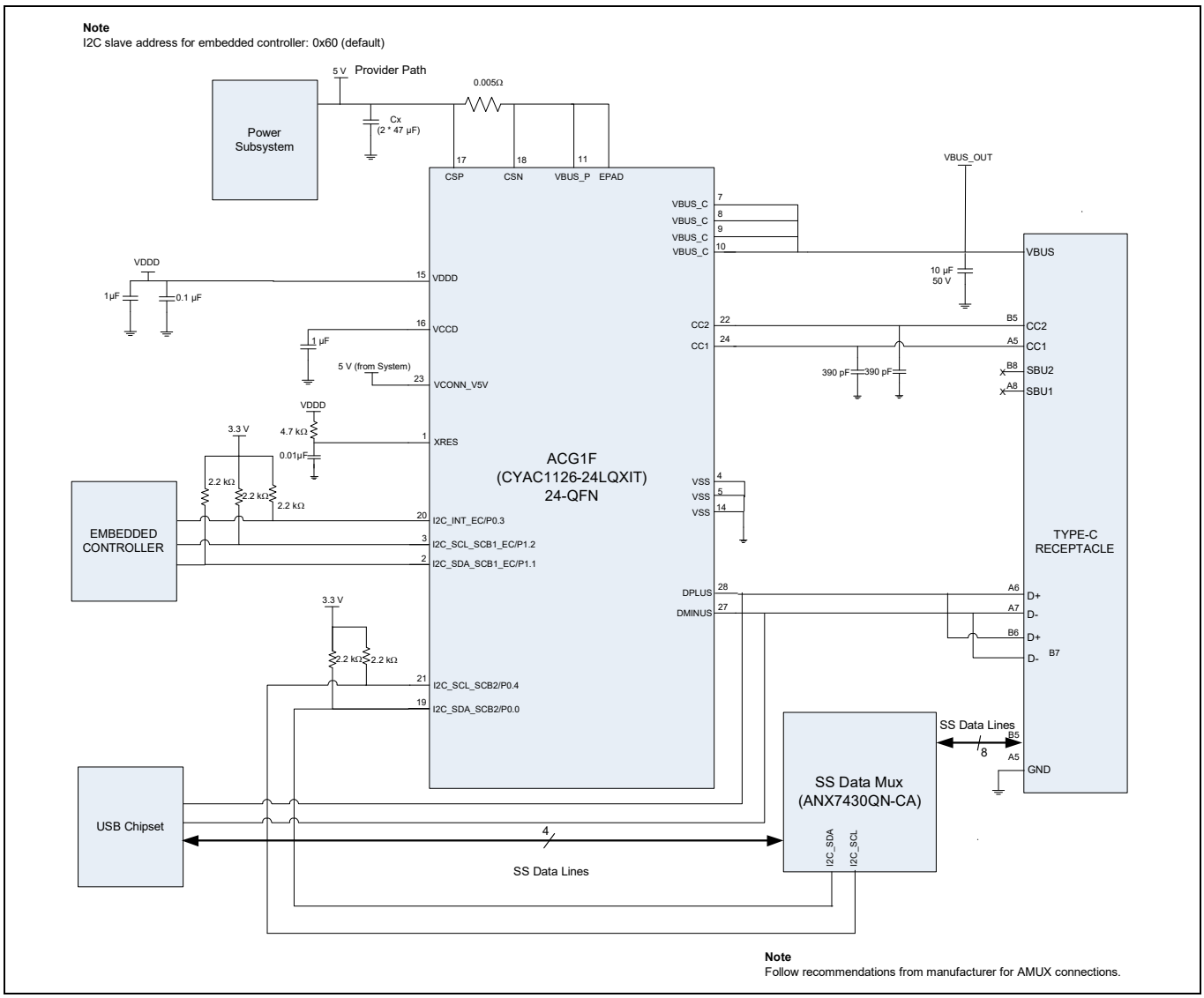


Figure 4-2 ACG1F in Single Port USB Type-C Notebook Application using CYAC1126- 24LQXIT

5 Device Configuration Parameters

ACG1F supports the following configuration parameters, which can be modified using EZ-PD configuration utility.

Table 5-1 ACG1F Device Configuration Parameters

Parameter	Options	Description
Rp_Supported	**Bitmap of Rp Supported by ACG1F**	
	Rp for default USB Current	Enable or disable
	Rp for 1.5A USB Current	Enable or disable
	Rp for 3.0A USB Current	Enable or disable
VConn_Enable	**Vconn Enable Parameters**	
	Enable options	Yes – Turn ON VConn only if Ra termination is seen. No – Turn ON VConn even if Ra termination is not seen.
VBUS_OVP	**VBUS Over Voltage Protection Parameters**	
	Enable	Can be enabled or disabled
	Threshold	Voltage threshold percentage above the contract voltage to trigger the fault.
	Debounce	Fault event debounce period in µs [0 – 255]
	Retry Count	Number of times to retry recovery from fault [0 – 255].
VBUS_OCP	**VBUS Over Current Protection Parameters**	
	Enable	Can be enabled or disabled
	Threshold	Current threshold percentage above the contract current to trigger the fault.
	Debounce	Fault event debounce period in µs [0 – 255]
	Retry Count	Number of times to retry recovery from fault [0 – 255].
VBUS_SCP	**VBUS Short Circuit Protection Parameters**	
	Enable	Can be enabled or disabled
	Threshold	Threshold is fixed to 6A.
	Debounce	Fault event debounce period in µs [0 – 255]
	Retry Count	Number of times to retry recovery from fault [0 – 255].
VBUS_RCP	**VBUS Reverse Current Protection Parameters**	
	Enable	Can be enabled or disabled
	Retry Count	Number of times to retry recovery from fault [0 – 255].
Vconn_OCP	**Vconn Over Current Protection Parameters**	
	Enable	Can be enabled or disabled
	Debounce	Fault event debounce period in µs [0 – 255]
VBUS_OTP	**VBUS Over Temperature Protection Parameters**	
	Enable	Can be enabled or disabled
	Therm_type	CCGx internal bipolar junction transistor (BJT)
	Cutoff_val	Reading/temperature at which device operation should be cut-off. Expressed in °C for internal BJT.
	Restart_val	Reading/temperature at which normal operation should be resumed.
Battery Charging	**Battery Charging Source Mode of Operation**	
	BC 1.2 Enable	Can be enabled or disabled

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{5V_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	–40 °C to +85 °C T_A, Absolute maximum
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	–40 °C to +85 °C T_A, Absolute maximum
$V_{BUS\_P\_MAX}$	Max Provider V_{BUS} in the system	–	–	6	V	–40 °C to +85 °C T_A
$V_{BUS\_C\_MAX}$ (40-QFN)	Max Connector side VBUS in the system with 40-QFN package	–	–	24	V	–40 °C to +85 °C T_A peaks up to 30 V for duration less than 1 µs at room temperature.
$V_{BUS\_C\_MAX}$ (24-QFN)	Max Connector side VBUS in the system with 24-QFN package	–	–	6	V	–40 °C to +85 °C T_A
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	V_{DDD}	V	–
V_{GPIO_ABS}	Inputs to GPIO	–0.5	–	V_{DDIO} + 0.5	V	–
$V_{DP\text{-}DM\_abs}$	Inputs to DPLUS and DMINUS	–0.5	–	V_{DDD} + 0.5	V	–
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM_VBUS	Electrostatic discharge human body model for VBUS_C, VBUS_P pins	500	–	–	V	Only applicable to VBUS_C, VBUS_P pins
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	Charged Device Model ESD
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	Applicable for all pins except CC1, CC2, VBUS_C, and VBUS_P pins
ESD_HBM_CC	Electrostatic discharge human body model for CC1, CC2 pins	1100	–	–	V	Only applicable to CC1, CC2 pins
LU	Pin current for latch-up	–200	–	200	mA	–
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins	–	–	24	V	–

6.2 Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

Table 6-2 DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR#2	V_{BUS_P}	Provider V_{BUS} from the system	4.0	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR#2B	V_{BUS_C}	Connector VBUS from the system	–	–	V_{BUS_P}	V	–40 °C to +85 °C T_A
SID.PWR#26	V5V	Power supply for V_{CONN}	4.85	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR24	V_{CCD}	Output voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	I_{DD}	Supply current	–	10	–	mA	T_A = 25 °C, no I/O sourcing current, CPU at 16 MHz
SID.PWR#7	$V_{DDWRITE}$	Supply voltage for flash write	2.7	–	5.5	V	–40 °C to +85 °C T_A, All V_{DDD}.
SID.PWR#13	V_{DDIO}	Supply voltage for I/O	V_{DDD}	–	V_{DDD}	V	–40 °C to +85 °C T_A, All V_{DDD}
SID.PWR#15	C_{EFC}	External Regulator voltage bypass for V_{CCD}	80	100	120.0	nF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor for V_{DDD}	–	1	–	µF	X5R ceramic or better
SID.PWR#27	C_{EXV}	Power supply decoupling capacitor for V5V, V_{DDIO}	–	0.1	–	µF	X5R ceramic or better
SID.PWR#18	V_{GPIO_ABS}	Inputs to GPIO	-0.5	–	V_{DDIO}+0.5	V	Absolute Maximum
SID.PWR#18A	$V_{DP\text{-}DM\_ABS}$	Inputs to DPLUS and DMINUS	-0.5	–	V_{DDD}+0.5	V	Absolute Maximum
SID.PWR#19	I_{GPIO_ABS}	Current per GPIO	-25.0	–	25	mA	Absolute Maximum
SID.PWR#19A	$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > V_{DDD} and min for V_{IL} < V_{SS}	-0.5	–	0.5	mA	Absolute Maximum current injection per pin
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep Mode	–	35	–	µs	–
SID.PWR#50	$V_{CC\_PIN\_ABS}$	Max voltage on CC1 & CC2 pins	–	–	24	V	Absolute Maximum
Current Consumption for ACG1F in Deep Sleep Mode. Typical values measured at 25 °C.							
SID_DS1	I_{DD_DS1}	V_{DDD} = 3.3 V. CC wakeup on, Type-C not connected	–	150	–	µA	Power source = V_{DDD}, Type-C Not attached, CC enabled for wakeup. Rp connection should be enabled for PD port.
SID_DS3	I_{DD_DS2}	V_{DDD} = 3.3 V. CC wakeup on, with CSA/UVOV On	–	500	–	µA	I_{DD_DS1}+ CC ON, CSA/UVOV ON

Table 6-2 DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V. I^2C Wakeup and WDT on.	–	150	–	µA	V_{DDD} = 3.3 V, T_A = 25 °C
SID307	I_{DD_XR}	Supply current while XRES asserted	–	50	–	µA	Power Source = V_{DDD} = 3.3 V, Type-C not attached, T_A = 25 °C

6.2.1 CPU

Table 6-3 CPU Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	16	MHz	All V_{DDD}
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	Guaranteed by characterization
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	
SYS.FES#1	T_{PWR_RDY}	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

6.2.2 GPIO

Table 6-4 GPIO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	0.7 × V_{DDIO}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = –4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = –1mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#35A	$V_{OL\_I2C\_2}$	Output low voltage	–	–	0.4	V	I_{OL} = 3 mA, V_{DDIO} > 2 V
SID.GIO#35B	$V_{OL\_I2C\_3}$	Output low voltage	–	–	0.6[3]	V	I_{OL} = 6 mA, V_{DDIO} > 1.71 V
SID.GIO#35C	V_{OL1_20mA}	Output low voltage	–	–	0.4	V	I_{OL} = 20 mA, V_{DDIO} > 3.0 V, Applicable for overvoltage-tolerant pins only
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA (IOL_LED) at 3-V V_{DDIO}
SID.GIO#5	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#6	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDIO}
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL	15	40	–	mV	V_{DDIO} > 2.7 V. Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	V_{DDIO} < 4.5 V
SID.GIO#44A	$V_{HYSCMOS55}$	Input hysteresis CMOS	200	–	–	mV	V_{DDIO} > 4.5 V

Note
3. To drive full bus load at 400 kHz, 6-mA I_{OL} is required at 0.6-V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.

Table 6-5 GPIO AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#46	T_{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#47	T_{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#48	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.3 V ≤ V_{DDIO} ≤ 5.5 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#49	F_{GPIO_OUT2}	GPIO F_{OUT}; 1.7 V ≤ V_{DDIO} ≤ 3.3 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#50	F_{GPIO_OUT3}	GPIO F_{OUT}; 3.3 V ≤ V_{DDIO} ≤ 5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25-pF load
SID.GIO#51	F_{GPIO_OUT4}	GPIO F_{OUT}; 1.7 V ≤ V_{DDIO} ≤ 3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load
SID.GIO#52	F_{GPIO_IN}	GPIO input operating frequency; 1.7 V ≤ V_{DDIO} ≤ 5.5 V.	–	–	16	MHz	90/10% V_{IO}

6.2.3 XRES

Table 6-6 XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	0.05× V_{DDIO}	–	mV	Guaranteed by characterization

6.3 Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

6.3.1 Pulse Width Modulation (PWM) for GPIO Pins

Table 6-7 PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 16 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

6.3.2 I^2C

Table 6-8 Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.3.3 Memory

Table 6-9 Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.MEM#4	T_{ROW_WRITE}	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	T_{ROW_ERASE}	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	25 °C to 55 °C, All V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	Guaranteed by design
SID180	$T_{DEVPROG}$	Total device program time	–	–	25	s	Guaranteed by design
SID.MEM#6	F_{END}	Flash endurance	100k	–	–	cycles	–
SID182	F_{RET1}	Flash retention, $T_A \leq 55$ °C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, $T_A \leq 85$ °C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, $T_A \leq 105$ °C, 10K P/E cycles	3	–	–	years	–

6.4 System Resources

6.4.1 Power-on-Reset (POR) with Brown Out

Table 6-10 Imprecise Power On Reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	Guaranteed by characterization

Table 6-11 Precise Power-on Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	Guaranteed by characterization
SID.CLK#6	SR_POWER	Power supply slew rate	0.40	–	67	V/ms	On power-up and power-down

6.4.2 SWD Interface

Table 6-12 SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.SWD#1	F_SWDCLK1	$3.3\ V \le V_{DDIO} \le 5.5\ V$	–	–	5	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	$1.8\ V \le V_{DDIO} \le 3.3\ V$	–	–	5	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

6.4.3 Internal Main Oscillator

Table 6-13 IMO AC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	$2.7\ V \le V_{DDD} < 5.5\ V$. $-25\ °C \le T_A \le 85\ °C$.
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–
SID.CLK#1	F_{IMO}	IMO frequency	–	48	–	MHz	–

6.4.4 Internal Low-speed Oscillator

Table 6-14 ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

6.4.5 PD

Table 6-15 PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID.DC.acg1f.cc.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.acg1f.cc.6	Idac_1p5a	Source current for 1.5A @ 5-V advertisement	165.6	–	194.4	µA	–
SID.DC.acg1f.cc.7	Idac_3a	Source current for 3A @ 5-V advertisement	303.6	–	356.4	µA	–
SID.DC.acg1f.cc.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.acg1f.cc.11	DFP_default_0p2	CC Voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.acg1f.cc.12	DFP_1.5A_0p4	CC Voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.acg1f.cc.13	DFP_3A_0p8	CC Voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.acg1f.cc.14	DFP_3A_2p6	CC Voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.acg1f.cc.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.acg1f.cc.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–

6.4.6 Analog-to-Digital Converter

Table 6-16 ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generated from Deep Sleep reference

6.4.7 Charger Detect

Table 6-17 Charger Detect DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
DC.CHGDET.1	VDAT_REF	Data detect voltage in charger detect mode	250	–	400	mV	–
DC.CHGDET.2	VDM_SRC	Dn voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.3	VDP_SRC	Dp voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.4	IDM_SINK	Dn sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.5	IDP_SINK	Dp sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.6	IDP_SRC	Data contact detect current source	7	–	13	µA	–
DC.CHGDET.32	RDM_UP	Dp/Dn pull-up resistance	0.9	–	1.575	kΩ	–
DC.CHGDET.31	RDM_DWN	Dp/Dn pull-down resistance	14.25	–	24.8	kΩ	–
DC.CHGDET.29	RDAT_LKG	Data line leakage on Dp/Dn	300	–	500	kΩ	–
DC.CHGDET.34	VSETH	Logic Threshold	1.26	–	1.54	V	–
DC.acg1f.dpdm.14	RDCP_DAT	Dedicated charging port resistance across DP and DN	–	–	40	Ω	

6.4.8 CSA

Table 6-18 CSA DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.csa_scp.42	SCP_6A	Short circuit current detect @ 6A	–	±10	–	%	–
DC.csa_scp.43	SCP_10A	Short circuit current detect @10A	–	±10	–	%	–
OP.csa_scp.11	Rsense	External sense register	–	5	–	mΩ	1% accuracy
DC.csa_scp.44	Iocp_1A	OCP Trip threshold for 1A with Rsense = 5 mΩ	–	130 ±20%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
	Iocp_1A	OCP Trip threshold for 1A with Rsense = 10 mΩ	–	130 ±10%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
DC.csa_scp.45	Iocp_5A	OCP Trip threshold for 2A, 3A, 4A and 5A contracts with Rsense = 5/10 mΩ	–	130 ±10%	–	%	2A, 3A, 4A, and 5A PD contracts OCP set at 130% of contract value OR user programmable
DC.rcp_scp.7a	I_csainn_lk	CSP pin input leakage when RCP and CSA blocks are OFF	–	–	10	µA	For provider V_{BUS} = 5 V

Table 6-18 CSA DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.rcp_scp.6a	I_csainp_lk	CSN pin input leakage when RCP and CSA blocks are OFF	–	–	80	µA	For provider V_{BUS} = 5 V
DC.sys.1	I_CSP_RCP_ON_CSA_OFF	CSP pin current when RCP block is ON and SCP is OFF	–	–	20	µA	For provider V_{BUS} = 5 V
DC.sys.2	I_CSN_RCP_ON_CSA_OFF	CSN pin current when RCP block is ON and SCP is OFF	–	–	100	µA	For provider V_{BUS} = 5 V
DC.sys.3	I_CSP_CSA_ON	CSP pin current when RCP block is OFF and SCP is ON	–	–	30	µA	For provider V_{BUS} = 5 V
DC.sys.4	I_CSN_CSA_ON	CSN pin current when RCP block is OFF and SCP is ON	–	–	100	µA	For provider V_{BUS} = 5 V
DC.sys.5	I_CSP_RCP_ON_CSA_ON	CSP pin current when RCP block is ON and SCP is ON	–	–	50	µA	For provider V_{BUS} = 5 V. Guaranteed by design.
DC.sys.6	I_CSP_RCP_ON_CAS_ON	CSN pin current when RCP block is ON and SCP is ON	–	–	120	µA	For provider V_{BUS} = 5 V. Guaranteed by design.

6.4.9 V_{BUS} UV/OV

Table 6-19 V_{BUS} UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy in active mode using bandgap reference	–	±3	–	%	–
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy in deep sleep mode using deep sleep reference	–	±5	–	%	–
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4s	–15	–	15	mV	–

6.4.10 VCONN Switch

Table 6-20 VCONN Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
DC.acg1f.20VCONN.1	Ron	Switch ON resistance at V5V = 5 V with 215-mA load current	–	1.4	2	Ω	–
DC.acg1f.20VCONN.9	I_{OCP}	Overcurrent detection range for CC1/CC2	550	–	–	mA	–
DC.acg1f.20VCONN.10	OVP_threshold	CC1, CC2 overvoltage protection detection threshold above V_{DDD} or V5V, whichever is higher	200	–	1200	mV	–
DC.acg1f.20VCONN.11	OVP_hysteresis	Overvoltage detection hysteresis	50	–	200	mV	Guaranteed by design
DC.acg1f.20VCONN.12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	80	mA	–
DC.acg1f.20VCONN.14	OVP_threshold_on	Overvoltage detection threshold above V5V of CC1/2, with CC1 or CC2 switch enabled. Same threshold triggers reverse current protection circuit	200	–	700	mV	–

Table 6-21 VCONN Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.acg1f.20VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	200	µs	–
AC.acg1f.20VCONN.2	T_{OFF}	VCONN switch turn-off time	–	–	3	µs	Guaranteed by design

6.4.11 V_{BUS}

Table 6-22 V_{BUS} Discharge Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID.VBUS.DISC.1	Ron1	20-V NMOS ON resistance	1500	–	3000	Ω	–
SID.VBUS.DISC.2	Ron2	20-V NMOS ON resistance	750	–	1500	Ω	–
SID.VBUS.DISC.3	Ron3	20-V NMOS ON resistance	500	–	1000	Ω	–
SID.VBUS.DISC.4	Ron4	20-V NMOS ON resistance	375	–	750	Ω	–
SID.VBUS.DISC.5	Ron5	20-V NMOS ON resistance	300	–	600	Ω	–

6.4.12 Provider NFET RCP

Table 6-23 Provider NFET RCP DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
DC.RCP.44	V_{CSA_RCP}	Voltage across external Rsense between CSP/CSN for which RCP condition detected (CSN higher than CSP by Vcsa_rcp)	–	2	6	mV	–
DC.RCP.45	V_{COMP_RCP}	Voltage across V_{BUS} and CSN pins for which RCP condition is detected	20	–	130	mV	–
DC.RCP.46	$V_{BUS\_MAX\_DET}$	Voltage on CSN pad during provider FET ON (source) for which RCP condition is triggered (this threshold is user programmable)	–	5.375	–	V	–

Table 6-24 Provider NFET RCP AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.RCP_SYS.1	T_{OFF_RCP}	Provider NFET switching off after reverse current detect through provider FET (for 20 V hot plug-in)	–	1	–	µs	V_{BUS} = 5 V/3A, Provider path ON, 47 µF ceramic cap on V_{BUS_P} pin
AC.RCP_SYS.2	$T_{RCP\_deassert}$	Time taken to detect RCP out of fault	–	55	80	µs	V_{BUS} falls below CSN and start NGDO enable

Table 6-25 VBUS Provider DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.ngdo_fet_sys.1	RDSon-1fet	FET RDSon (24-QFN)	–	15	–	mΩ	NFET Driver is ON
DC.ngdo_fet_sys.1a	RDSon-2fet	FET RDSon (40-QFN)	–	45	55	mΩ	NFET Driver is ON; 3A load current, short-duration pulse, –40 °C to +55°C TA
DC.ngdo_fet_sys.2	Isw	Continuous current	–	–	3	A	–

Table 6-26 VBUS Provider AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.ngdo_fet_sys.1	T_{on}	V_{BUS} Low to High (10% to 90%)	–	5	–	ms	0.8 to 4.5 V transition, system-level (with 10 Ω load on VBUS_C)
AC.ngdo_fet_sys.2	$T_{off\text{-}fault}$	FET turn-off time - Under fault condition of SCP/RCP	–	1	–	µs	–
AC.ngdo_fet_sys.3	T_{off}	VBUS High to Low (90% to 10%) - Under normal condition	–	7	–	µs	0.8 to 4.5 V transition, system-level with external FET (with 10 Ω load on VBUS_C)
AC.ngdo_fet_sys.4	OT_{Sth_OFF}	Overtemperature shutdown threshold OFF	–	125	–	°C	–
AC.ngdo_fet_sys.5	OT_{Sth_ON}	Overtemperature shutdown threshold ON	–	90	–	°C	–

7 Hardware Design Guidelines

This section provides hardware design guidelines for designing a USB Type-C controller for DFP applications using ACG1F.

Following are the guidelines:

1. **ESD and EMI/EMC Protection**
2. **TVS Diode on VBUS_C Pin**
3. **Power Supply Noise Suppression**
4. **Placement of Bulk and Decoupling Capacitors**
5. **Placement of Power and Ground Planes**
6. **Voltage Regulation**
7. **Power Domain Routing**
8. **Routing of Type-C (USB Data and CC) Lines**
9. **Routing of CSP and CSN Lines**

7.1 ESD and EMI/EMC Protection

Ferrite beads are not mandatory for all Type-C applications but are recommended to be connected between the USB Type-C Connector's Shield and the system's GND pin (in the place of resistor R81) (see **Figure 7-1**) to prevent the transmission of electrical stress from the Type-C connector to the ACG1F device.

ESD protection diodes (D15, D16, and D17) are recommended to be connected to VBUS, USB D+, and USB D- lines for protection above 2 kV as shown in **Figure 7-1**. The ESD Diodes should meet the requirement of IEC61000-4-2 and have low input capacitance.

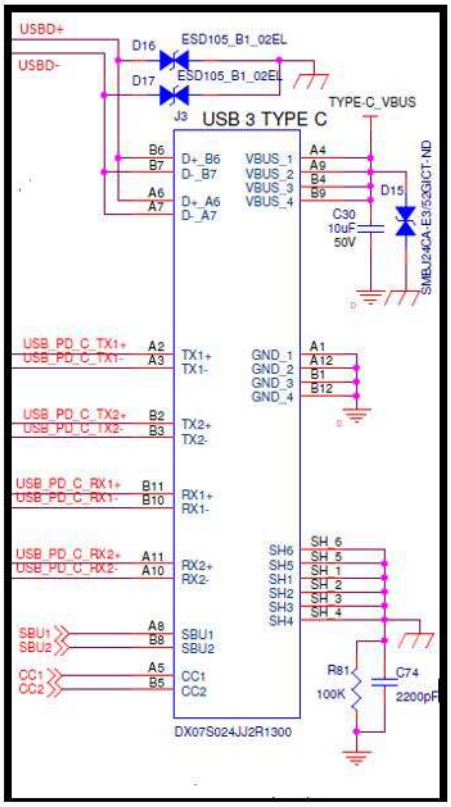


Figure 7-1 ESD and EMC Protection

7.2 TVS Diode on VBUS_C Pin

It is recommended to connect TVS diode (SMBJ24CA-E3/52) on the VBUS_C pin if the maximum voltage at this pin can go above 24 V. This is for protection from high voltage spikes that can appear during VBUS_C hot plug-in to 24 V.

7.3 Power Supply Noise Suppression

Power supply noise can be suppressed by using decoupling capacitors to power supply pins VBUS_C, VBUS_P, VDDD, VDDIO, VCCD, and V5V pins as shown in **Figure 7-2**. A 390-pF decoupling capacitor should be connected to CC lines (CC1, CC2) to maintain the signal quality at the signaling rate of 300 kHz. The CSP pin requires a capacitance of 50 µF for optimal performance of ACG1F during SCP and RCP events. Noise suppression diagram shown in **Figure 7-2** is for a single port controller, ACG1F.

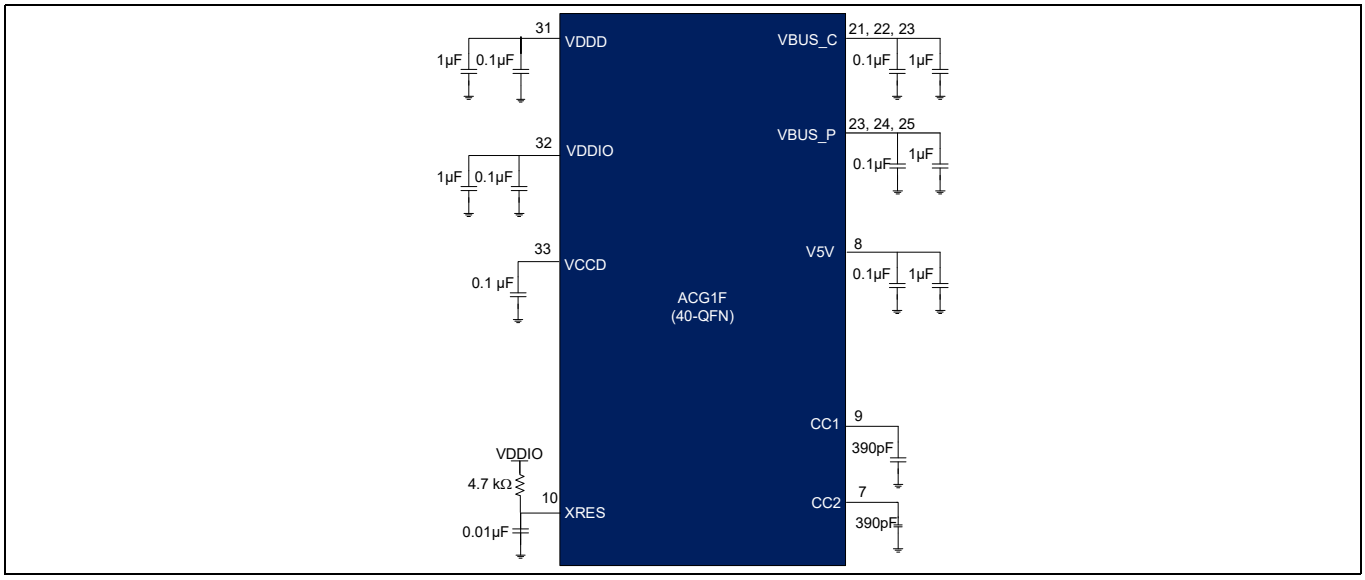


Figure 7-2 Noise Suppression on ACG1F

7.4 Placement of Bulk and Decoupling Capacitors

This section explains the hardware design guidelines for USB Type-C DFP controller application using ACG1F and provides recommendations for component placement and routing power signals and USB signals.

- Place decoupling capacitors close to the power pins of the respective CCG controller for high- and low-frequency noise filtering, as shown in **Figure 7-3**.
- Place the bulk capacitor, which acts as a local power supply, close to the power supply input and output headers and voltage regulators. Filter power inputs and outputs near the power headers to reduce the electrical noise. Ceramic or tantalum capacitors are recommended; electrolytic capacitors are not suitable for bulk capacitance.

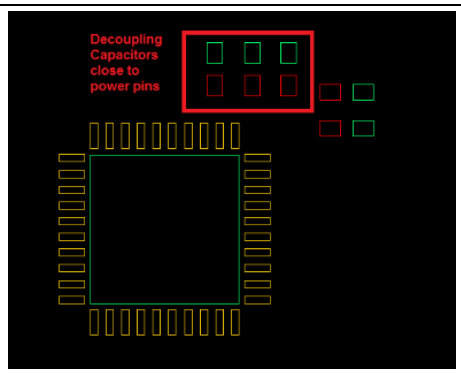


Figure 7-3 Placement of Bulk and Decoupling Capacitors

7.5 Placement of Power and Ground Planes

- Use a high-performance substrate material for PCBs. The system may carry maximum current up to 5 A. Therefore, it is required to construct PCBs with 2-ounce (oz) copper thickness. Minimum recommended space between copper elements is 8 mil (0.203 mm).
- Use dedicated planes for power and ground. Use of dedicated planes reduces jitter on USB signals and helps minimize the susceptibility to EMI and RFI.
- Use cutouts on the power plane if more than one voltage is required on the board (for example, 2.5 V, 3.3 V, 5.0 V).
- Place the power plane near the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing the electromagnetic radiation.
- Do not split or cut the ground plane. Splitting it increases the electrical noise and jitter on USB signals. Ground planes should be continuous. A discontinuous ground plane leads to larger inductance due to longer return current paths, which can increase EMI radiation. Also, multiple split grounds can cause increased crosstalk.

7.6 Voltage Regulation

The following points must be considered while selecting voltage regulators to reduce electrical emissions and prevent regulation problems during USB suspend:

- Select voltage regulators that have minimum load current less than the board's load current during USB suspend. If the current drawn on the regulator is less than the regulator's minimum load current, then the output voltage may change.
- Place voltage regulators so they straddle split VCC planes; this reduces emissions.

7.7 Power Domain Routing

- Power traces should be routed with a minimum of 40 mils trace width to reduce inductance.
- Keep the power traces short.
- Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Make the power trace width the same dimension as the power pad. To connect power pins to the power plane, place the vias very close to the power pads. This helps in minimizing the stray inductance and IR drop on the line.
- The EPAD (Exposed PAD) for 40-QFN should be soldered onto an exposed ground pad provided in the PCB.
- If a switched-mode power supply is used, power traces should be far away from signal traces to avoid addition of power noise on signal or keep ground traces in between the signal traces.

7.8 Routing of Type-C (USB Data and CC) Lines

USB SuperSpeed lines from the Host controller are connected to the Type-C port through a multiplexer. Ensure care while routing USB data and CC lines to achieve good signal quality and reduced emission. Improper layouts lead to poor signal quality specifically on the USB signaling, which may lead to enumeration failure of Super-Speed USB devices connected at Type-C port of the notebook.

7.8.1 Guidelines for Routing USB Data Lines

- Keep USB SuperSpeed traces as short as possible. Ensure that these traces have a nominal differential characteristic impedance of 90 Ω.
- Match the differential SS pair trace lengths within 0.12 mm (5 mils).
- Match the Hi-Speed (Dp and Dn) signal trace lengths within 1.25 mm (50 mils).
- Adjust the High-Speed signal trace lengths near the USB receptacle, if necessary.
- Select a grounded coplanar waveguide (CPWG) system as a transmission line method, as shown in **Figure 7-4**.

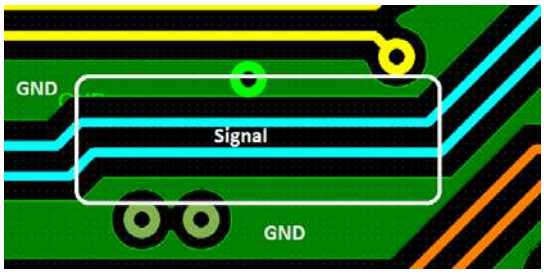


Figure 7-4 PWG Example

- Minimize the use of vias.

7.8.2 Guidelines for Routing Type-C (VBUS, GND, and CC) Lines

- Group the VBUS pins together (all VBUS pins are brought out to the same plane using vias) as shown in **Figure 7-5**.

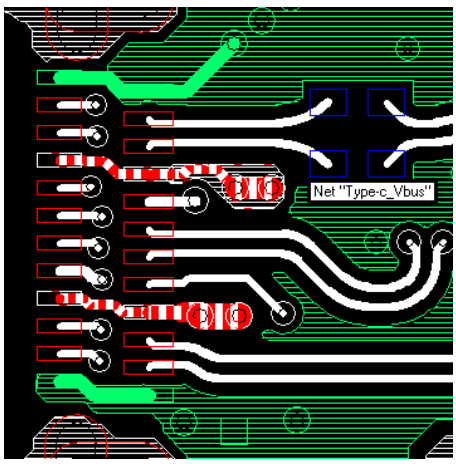


Figure 7-5 All VBUS Pins are Grouped Together

- Similarly, group the GND pins together (all GND pins are brought out to the same plane using vias).
- Place GND plane adjacent and below CC (CC1, CC2) lines. Traces from CC pins must be routed with a minimum of 20 mils trace width for VCONN operation.

7.9 Routing of CSP and CSN Lines

- CSP and CSN must be of shorter length
- The signals must be routed as differential pair to the external Rsense resistor, as shown in **Figure 7-6**.

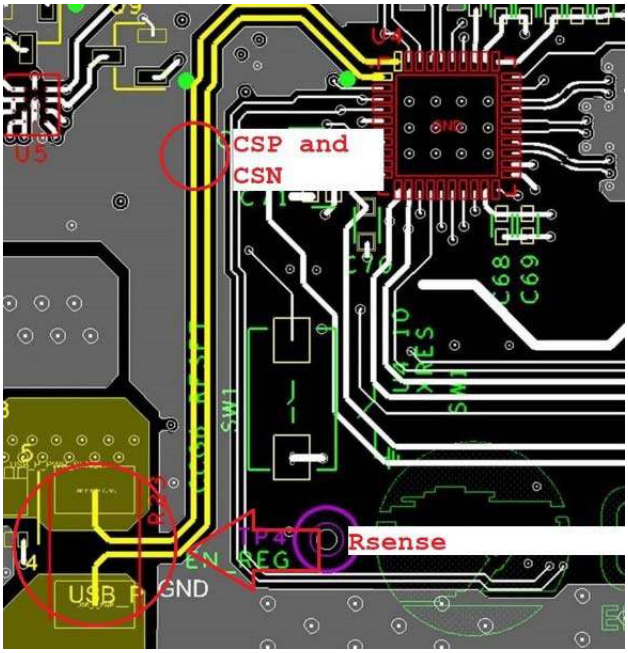


Figure 7-6 Routing of CSP and CSN Traces to Rsense Resistor

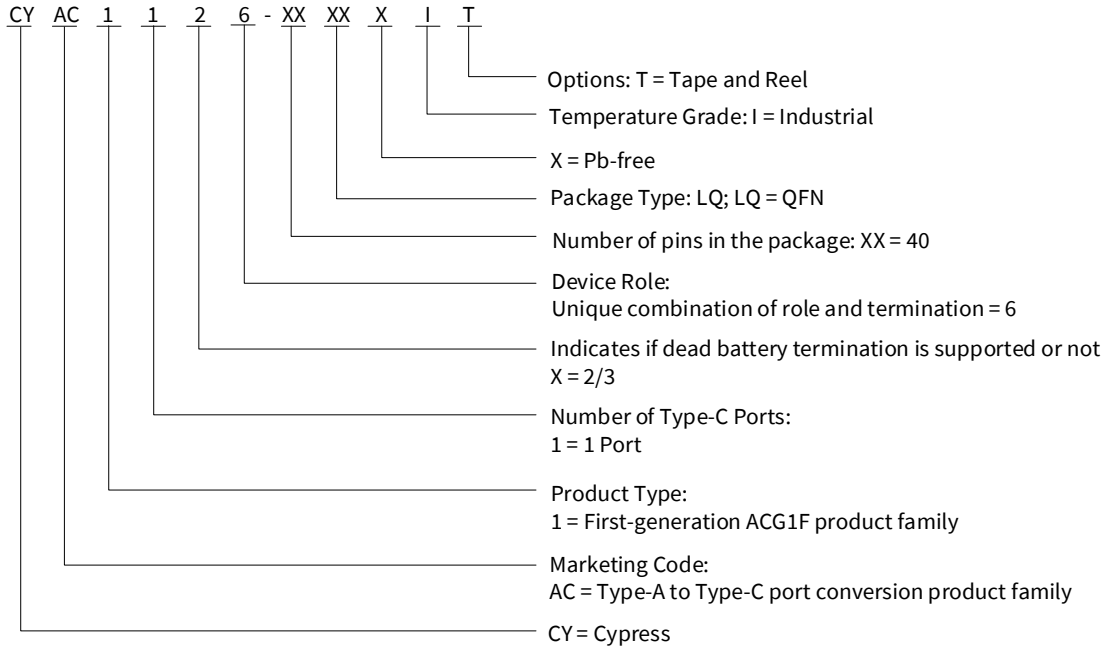
8 Ordering Information

Table 8-1 lists the ACG1F part numbers and features.

Table 8-1 ACG1F Ordering Information

Part Number	Application	Type-C Ports	Dead battery Termination	VBUS_C_MAX Voltage	Role	Package
CYAC1126-24LQXI/T	Notebooks, Desktops	1	No	6 V	DFP	24-QFN
CYAC1126-40LQXI/T	Notebooks, Desktops	1	No	24 V	DFP	40-QFN

8.1 Ordering Code Definitions



9 Packaging

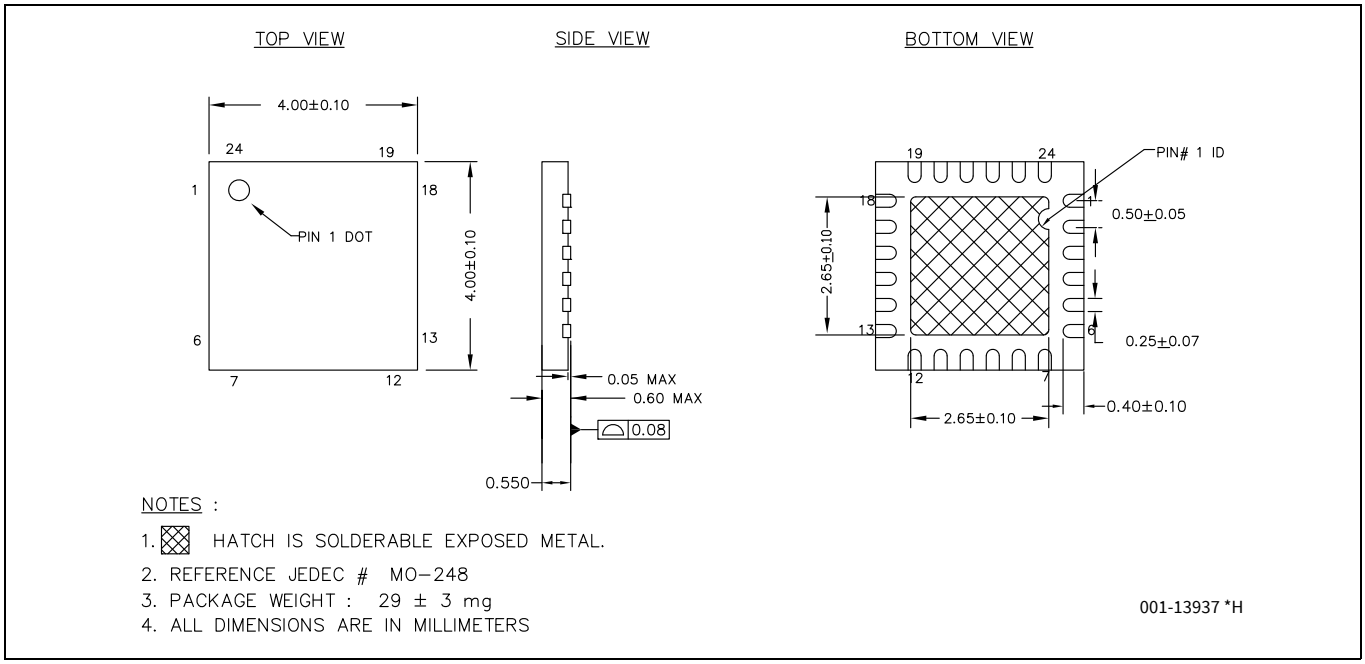


Figure 9-1 24-Pin QFN Package Outline

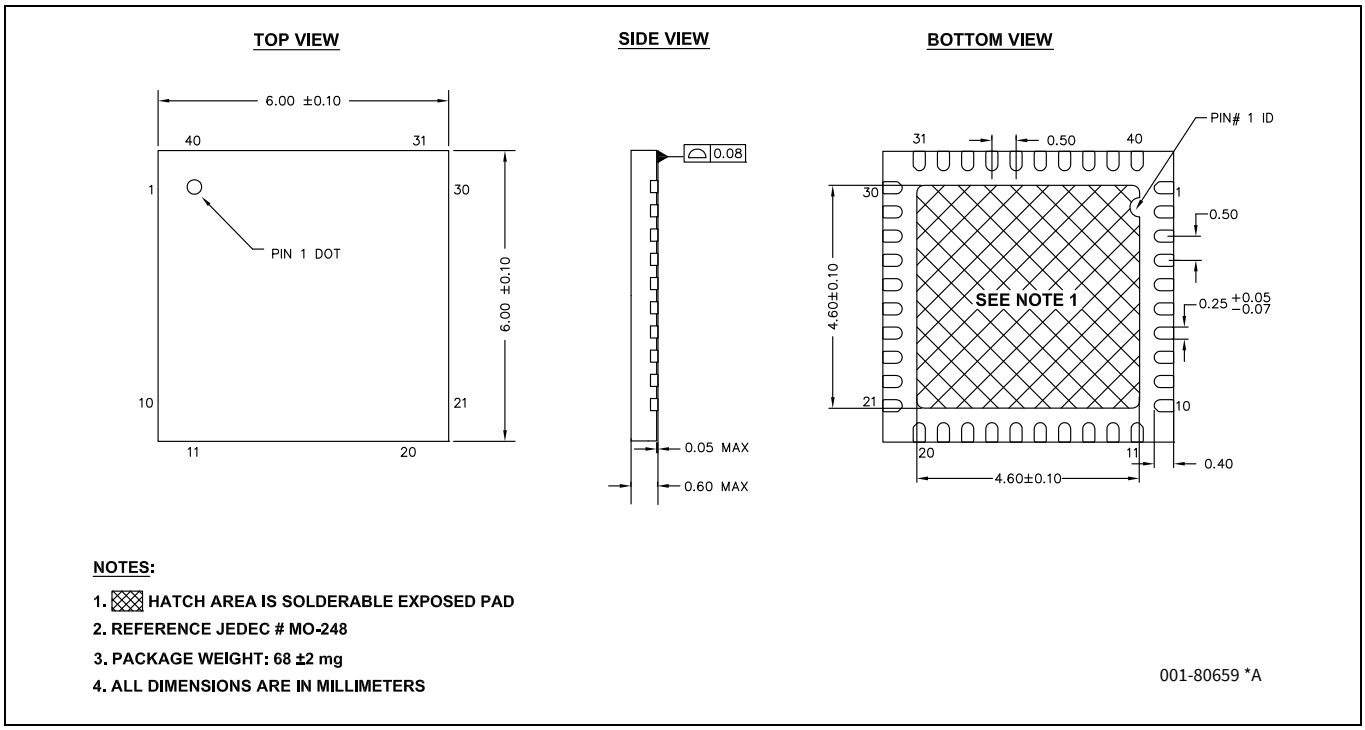


Figure 9-2 40-Pin QFN Package Outline

10 Acronyms

Table 10-1 Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BOD	Brown out Detect
CC	configuration channel
CPU	central processing unit
CPWG	coplanar waveguide
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
CSA	current sense amplifier
CSN	current sense negative
CSP	current sense positive
DFP	downstream facing port
DFT	design for test
DP	DisplayPort, digital display interface developed by Video Electronics Standards Association
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DM	data minus
DRP	dual role power
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
EPAD	exposed PAD
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
HPI	host processor interface
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
IPOR	imprecise power-on reset
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit

Table 10-1 Acronyms Used in this Document *(continued)*

Acronym	Description
NC	no connect
NGDO	NFET gate driver output
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWG	planar wave guide
PWM	pulse-width modulator
RAM	random-access memory
RCP	reverse current protection
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SCP	short circuit protection
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read only memory
SS Data Lines	superspeed data lines
SWD	serial wire debug, a test protocol
TCPWM	timer counter pulse-width modulator
TBT	Thunderbolt, hardware interface standard for peripherals developed by Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol

Table 10-1 Acronyms Used in this Document *(continued)*

Acronym	Description
UCSI	USB Type-C Connector System Software Interface
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, ACG1F pins used to connect to a USB port
USB PD	USB power delivery
UVP	under voltage protection
XRES	external reset I/O pin

11 Document Conventions

11.1 Units of Measure

Table 11-1 Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision History

Document version	Date of release	Description of changes
**	2019-02-13	Initial release
*A	2019-03-29	Added **Functional Overview**, **Power System Overview**, **Pinouts**, **Ordering Information**, and **Packaging** sections.
*B	2019-05-13	Updated Copyright information. Updated **Features**, **Absolute Maximum Ratings**, and **Device-Level Specifications**. Updated **Table 6-25**, **Table 6-26**, and **Table 8-1**. Removed the following tables: VBUS Gate Driver AC Specifications VBUS Gate Driver DC Specifications
*C	2019-07-04	Added VBUS to CC short circuit protection in **Features**. Updated **I2C Slave Address Configuration**. Updated T_{ON} parameter description and conditions. Added Errata**Revision History**.
*D	2019-10-30	Added **Application Diagrams**, **Hardware Design Guidelines**, **Device Configuration Parameters**, **High-Voltage Tolerant CC Lines**, and **Reverse Current Protection (RCP)**. Updated **Acronyms**. Removed Errata. Updated **Table 6-25**: Updated RDS parameter spec. Updated **Table 6-1**: Updated Description for $V_{BUS\_C\_MAX\ (40\text{-}QFN)}$. Updated **Table 6-2**: Updated Description for SID.PWR#1.
*E	2020-02-07	Updated the Max value of DC.RCP.45 in the **Table 6-23**. Completing the Sunset review.
*F	2021-06-21	Updated to Infineon template. Updated **Table 6-1** and **Table 6-2**: Updated value of $V_{CC\_PIN\_ABS}$ from 6V to 24V. Updated **Table 6-11**: Added SR_POWER power supply slew rate parameter. Updated **Figure 9-1** (spec 001-13937 *G to *H) in **Packaging**. Updated Copyright information.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-06-21
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Go to www.cypress.com/support

Document reference
002-26356 Rev. *F

IMPORTANT NOTICE
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.