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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR

2SK3367

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3367 is N-Channel MOS Field Effect Transistor designed for DC/DC converter application of notebook computers.

FEATURES

- Low on-resistance
 $R_{DS(on)1} = 9.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 18 \text{ A)}$
 $R_{DS(on)2} = 12.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 18 \text{ A)}$
 $R_{DS(on)3} = 14.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 18 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2800 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3367	TO-251 (MP-3)
2SK3367-Z	TO-252 (MP-3Z)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 36	A
Drain Current (Pulse) ^{Note}	$I_{D(pulse)}$	± 144	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	40	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

Note $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$

THERMAL RESISTANCE

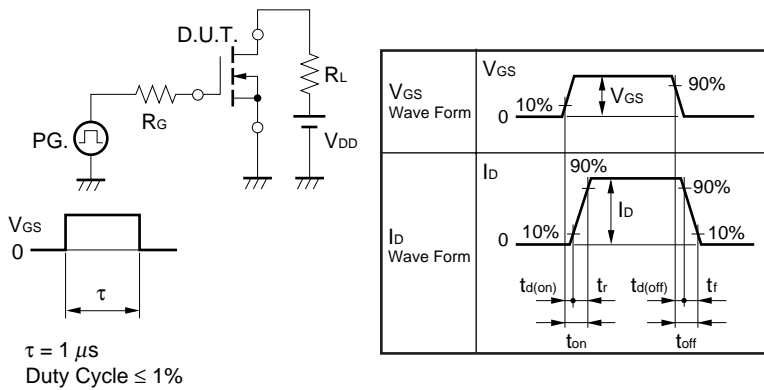
Channel to case Thermal Resistance	$R_{th(ch-C)}$	3.13	$^\circ\text{C/W}$
Channel to ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

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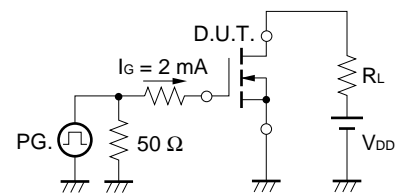
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 18 A		7.3	9.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 18 A		9.0	12.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 18 A		9.7	14.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 18 A	13	26		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		2800		pF
Output Capacitance	C _{oss}			880		pF
Reverse Transfer Capacitance	C _{rss}			400		pF
Turn-on Delay Time	t _{d(on)}	I _D = 18 A, V _{GS} = 10 V, V _{DD} = 15 V, R _G = 10 Ω		75		ns
Rise Time	t _r			1130		ns
Turn-off Delay Time	t _{d(off)}			165		ns
Fall Time	t _f			210		ns
Total Gate Charge	Q _G	I _D = 36 A, V _{DD} = 24 V, V _{GS} = 10 V		49		nC
Gate to Source Charge	Q _{GS}			10		nC
Gate to Drain Charge	Q _{GD}			14		nC
Body Diode forward Voltage	V _{F(S-D)}	I _F = 36 A, V _{GS} = 0 V		0.95		V
Reverse Recovery Time	t _{rr}	I _F = 36 A, V _{GS} = 0 V		45		ns
Reverse Recovery Charge	Q _{rr}		di/dt = 100 A/μs		50	

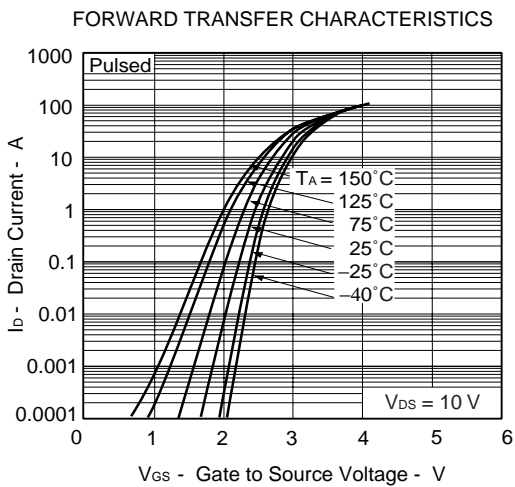
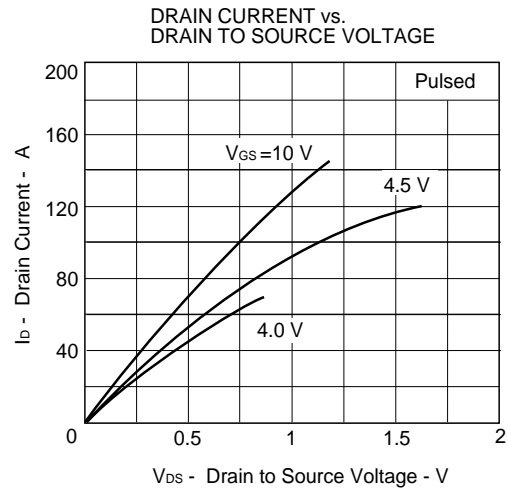
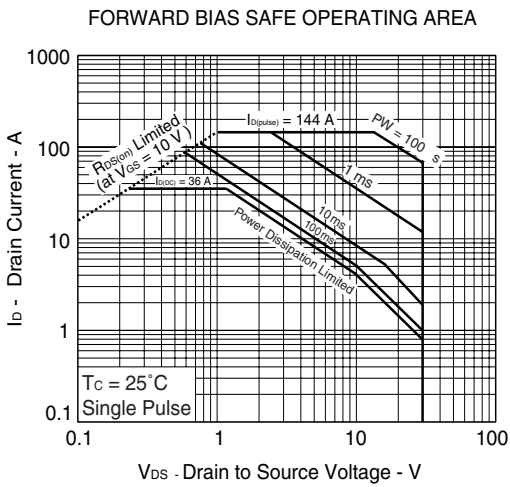
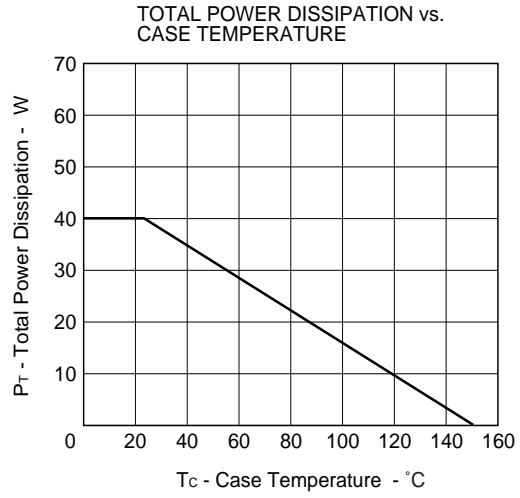
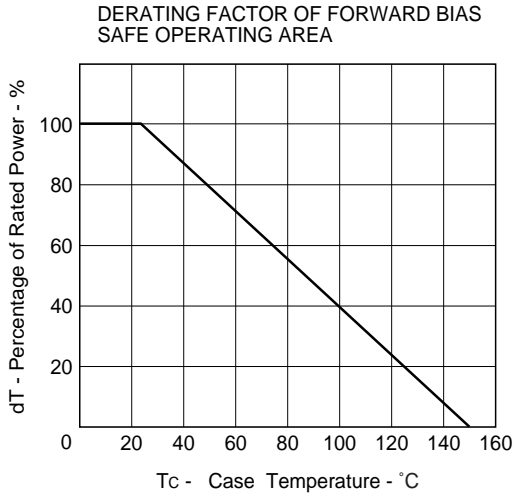
TEST CIRCUIT 1 SWITCHING TIME



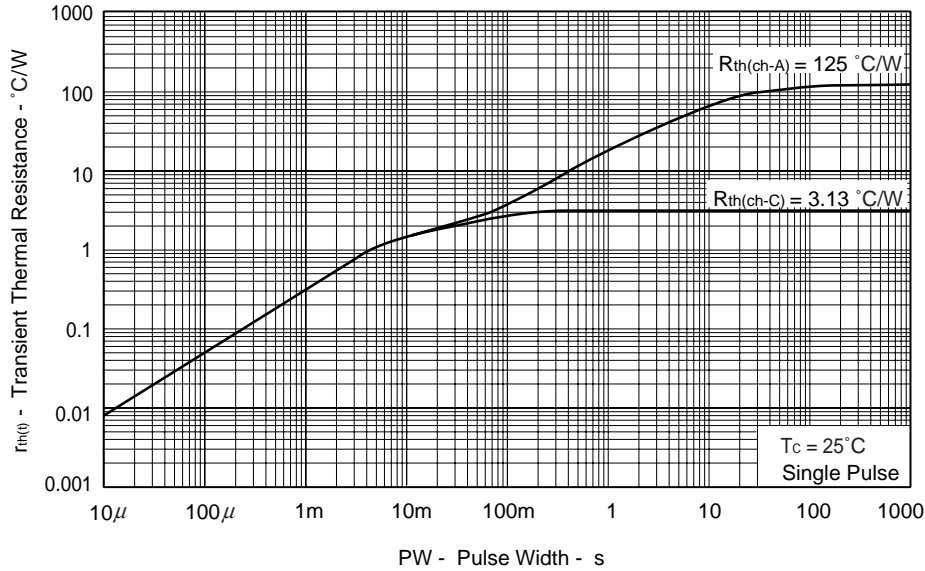
TEST CIRCUIT 2 GATE CHARGE



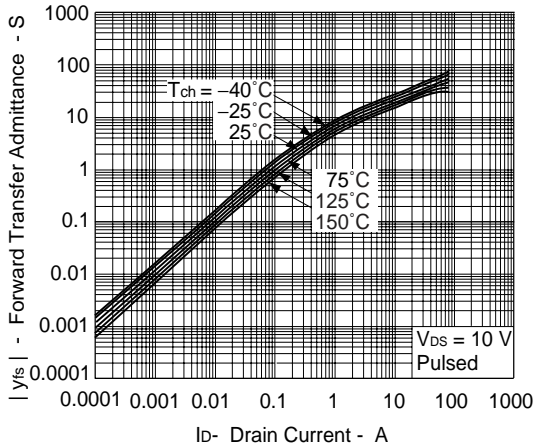
TYPICAL CHARACTERISTICS (T_A = 25°C)



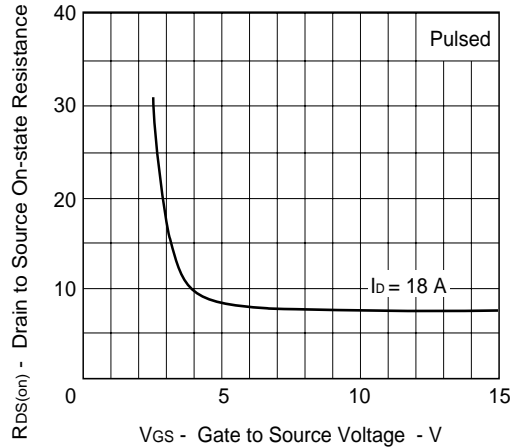
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



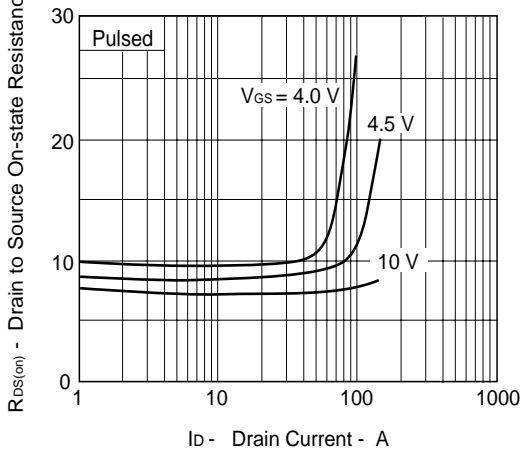
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



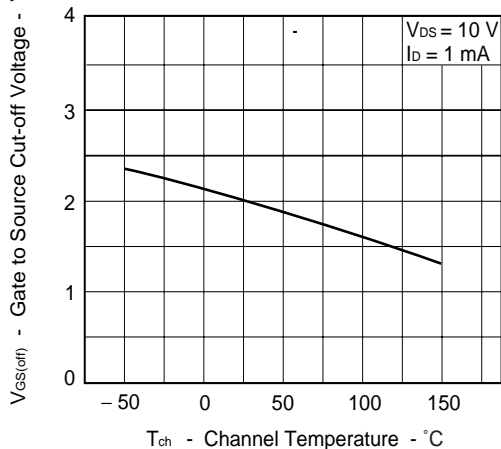
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



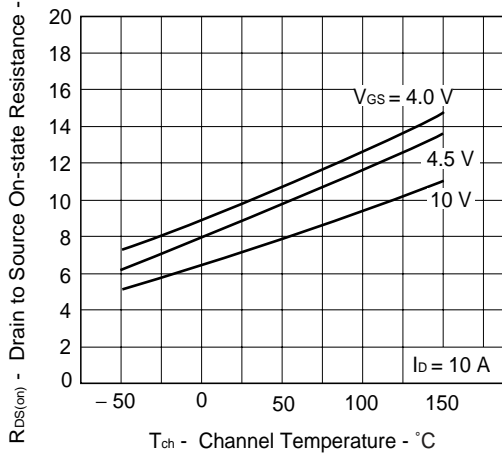
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



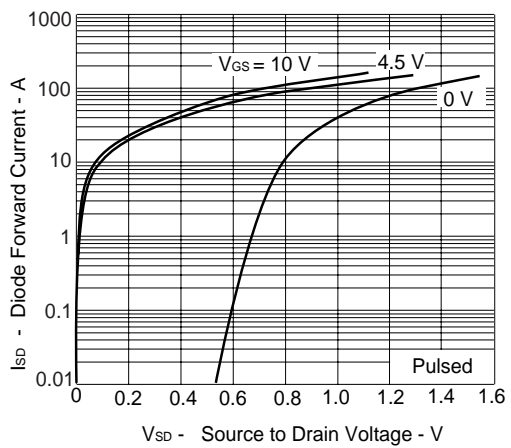
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



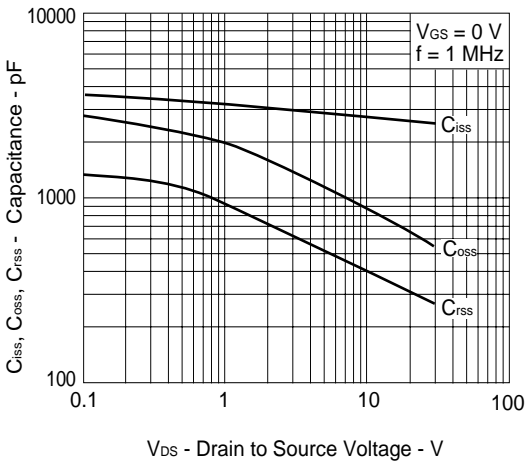
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



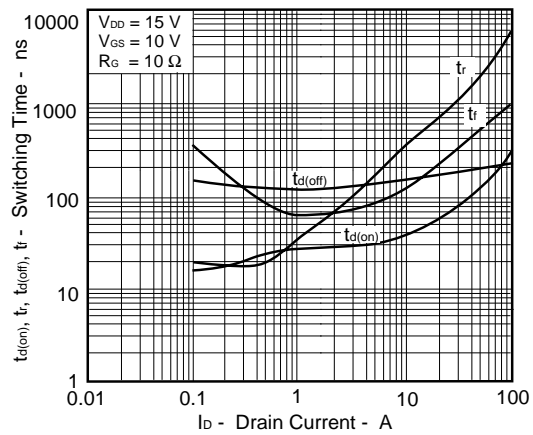
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



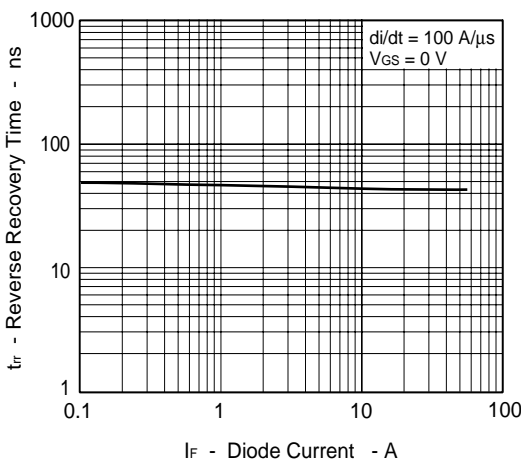
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



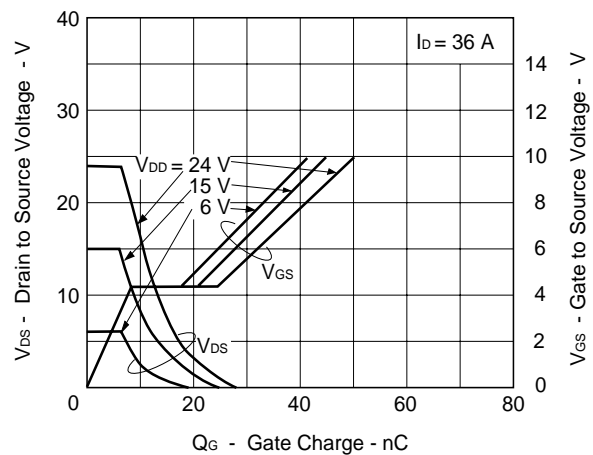
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

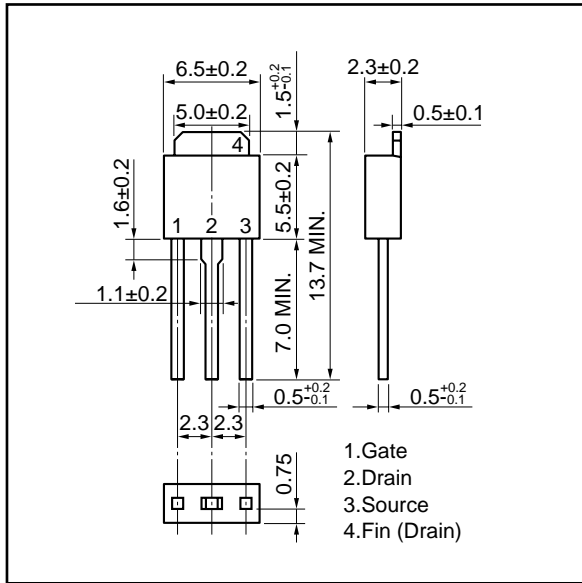


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

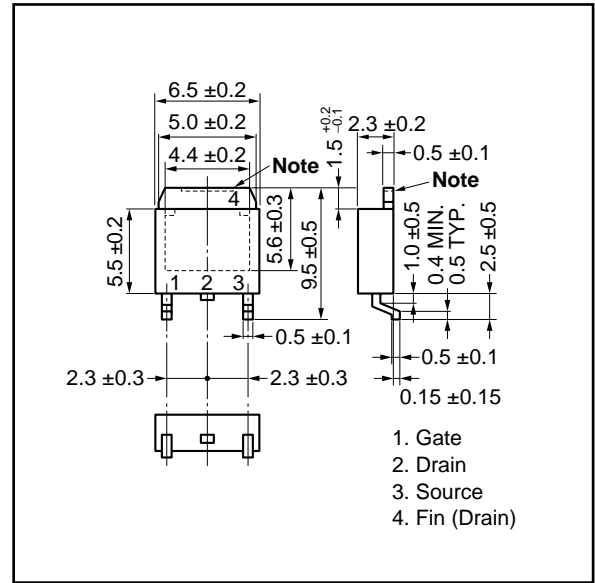


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

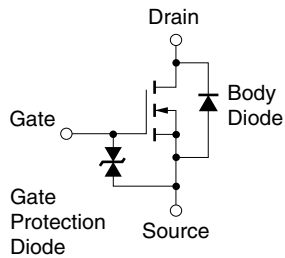


<R> 2) TO-252 (MP-3Z)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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