One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADP2121 6 MHz, Step-Down Converter

FEATURES

600 mA, 6 MHz, synchronous, step-down dc-to-dc converter[1]
Tiny ceramic inductor and capacitors
Input voltage range: 2.3 V to 5.5 V (VIN = 2.9 V to 5.5 V for ADP2121-2.3-EVALZ)
Fixed output voltages: 1.8 V, 1.82 V, 1.85 V, 1.875 V, and 2.3 V
Automatic power-saving mode
Jumper-selectable shutdown/enable
Jumper-selectable operating mode for the desired optimization at light loads
Automatic PFM/PWM switching for high efficiency
Fixed PWM for improved transient performance

GENERAL DESCRIPTION

The ADP2121 evaluation board is a complete 6 MHz, low quiescent current, step-down dc-to-dc converter application capable of producing up to a 600 mA output current at the 1.8 V, 1.82 V, 1.85 V, 1.875 V, and 2.3 V fixed output voltages. The converter operates with an input voltage in the 2.3 V to 5.5 V range. At high load currents, the device uses a voltage regulating pulse-width modulation (PWM) mode that maintains a constant frequency with excellent stability and transient response. For light load currents, the state of the MODE pin determines the operating mode of the converter. In forced PWM mode, the converter continues operating in PWM for light loads. In auto mode, the ADP2121 can automatically enter a power saving mode that uses pulse-frequency modulation (PFM) to reduce the effective switching frequency and ensure the longest battery life in portable applications. The evaluation board demonstrates the operation and performance of the ADP2121 as well as its compatibility with tiny ceramic components for a small area solution.

This user guide includes I/O descriptions, setup instructions, the evaluation board schematic, and the printed circuit board (PCB) layout drawings for the ADP2121 evaluation board.

Complete specifications for the ADP2121 are available in the ADP2121 data sheet available from Analog Devices, Inc., and should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD LAYOUT

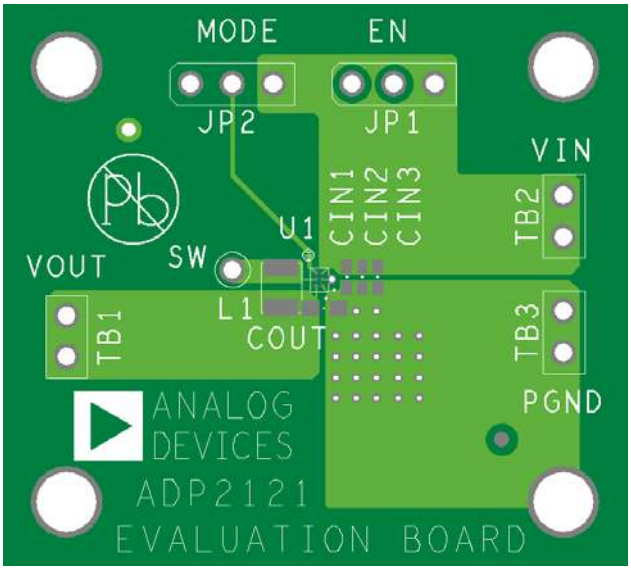

Figure 1. ADP2121 Evaluation Board Top Layer

[1] Guaranteed by design. The maximum output current guarantee for 2.3 V to 2.5 V increases linearly from 300 mA to 500 mA. The maximum output current guarantee for 2.5 V to 2.7 V increases linearly from 500 mA to 600 mA. For greater than 2.7 V, the maximum output current guarantee is 600 mA.

TABLE OF CONTENTS

Features 1
General Description 1
Evaluation Board Layout 1
Revision History 2
Evaluation Board Overview 3
Input/Output Connectors 3
Evaluation Setup 4
Performance Evaluation 4
Evaluation Board Schematic and Layout 5
Layout Guidlines 5
Application Note 5
Ordering Information 6
Bill of Materials 6

REVISION HISTORY

10/10—Revision 0: Initial Version

EVALUATION BOARD OVERVIEW

The ADP2121 evaluation board is fully assembled and tested. The following sections describe the various connectors on the board, the proper evaluation setup, and the testing capabilities of the evaluation board.

INPUT/OUTPUT CONNECTORS

EN Jumper (JP1)

The EN connector enables or disables the converter. Use one of the following methods to control the state of the EN pin. Do not leave the EN pin floating.

- Disable the converter by using a jumper to connect the left-most pins of JP1. The jumper connects the EN pin to GND, effectively disabling the converter (see Figure 2).

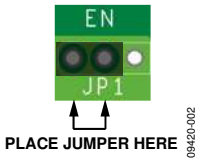

Figure 2. SD Jumper Position

- Enable the converter by using a jumper to connect the right most pins of JP1. The jumper connects the EN pin to VIN, effectively enabling the converter (see Figure 3).

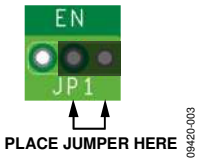

Figure 3. EN Jumper Position

- Directly control the EN pin by connecting an external device to the center pin of JP1 (see Figure 4). Apply a voltage between GND and VIN.

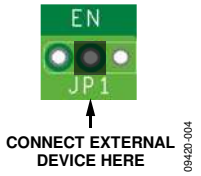

Figure 4. EN Pin Direct Connection

MODE Jumper (JP2)

The MODE connector controls the operating mode of the ADP2121. Use one of the following methods to select between automatic PFM/PWM switching and forced PWM operation. Do not leave the MODE pin floating. The MODE pin is not designed for dynamic control and should not be changed after the ADP2121 is enabled.

- Place the converter in auto mode by using a jumper to connect the left most pins of JP2. The jumper connects the MODE pin to GND to use the power save mode with automatic transition between PFM and PWM mode (see Figure 5).

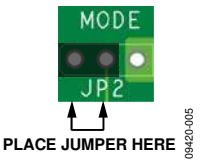

Figure 5. Auto Mode Jumper Position

- Place the converter in forced PWM mode by using a jumper to connect the right most pins of JP2. The jumper connects the MODE pin to VIN, effectively forcing the converter to remain in PWM mode, regardless of the size of the applied load (see Figure 6).

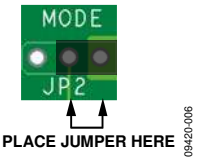

Figure 6. PWM Mode Jumper Position

- Control the voltage applied to the MODE pin directly by connecting an external device to the center pin of JP2 (see Figure 7). Apply a voltage between GND and VIN.

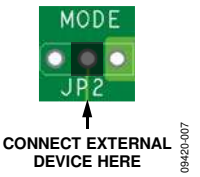

Figure 7. MODE Pin Direct Connection

VOUT Test Bus (TB1)

The VOUT test bus provides access to the regulated output voltage and the FB (feedback) pin of the part. A load of up to 600 mA can be applied to this bus.

VIN Test Bus (TB2)

The VIN test bus connects the positive input supply voltage to the VIN pin. Connect the power supply to this bus and keep the wires as short as possible to minimize EMI transmission.

PGND Test Bus (TB3)

The PGND test bus is the power ground connection for the part and the external components via the GND pin. Attach ground connections from external equipment to this bus.

SW Test Point (TP1)

The SW test point allows access to the switch node (SW pin) of the ADP2121 to monitor the switching behavior. An LC filter is connected to this pin on the board. Connect a BNC cable to measure the switching frequency to this test point.

EVALUATION SETUP

Follow these setup instructions to ensure proper operation of the ADP2121 evaluation board:

1. Connect the positive input supply to VIN.
2. Connect the input supply ground to PGND.
3. Connect the desired load between VOUT and PGND. For VIN = 2.3 V to 2.5 V, the maximum load the ADP2121 can deliver increases linearly from 300 mA to 500 mA. For VIN = 2.5 V to 2.7 V, the maximum load increases linearly from 500 mA to 600 mA. Above VIN = 2.7 V, the ADP2121 can supply up to 600 mA.
4. Connect EN to enable or disable the converter and MODE to select between auto mode and PWM mode.
5. Apply a VIN between 2.3 V and 5.5 V (6.0 V absolute maximum.)

PERFORMANCE EVALUATION

The resulting oscilloscope waveforms and typical performance characteristics for the following tests are provided in the ADP2121 data sheet.

Line Regulation

The line regulation is observed and measured by monitoring the output voltage at VOUT while varying the input voltage applied to VIN.

Load Regulation

The load regulation is observed and measured by monitoring the output voltage at VOUT while sweeping the applied load between VOUT and PGND. To minimize voltage drop, use short, low resistance wires, especially for heavy loads.

Output Accuracy

The output accuracy is verified by monitoring the output voltage at VOUT while testing both the line and load regulation.

Efficiency

The efficiency, η, is calculated by comparing the input power to the output power.

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}$$

PFM/PWM Transition

To observe the PFM/PWM transition, place the converter in auto mode. Connect an oscilloscope to the SW test point and vary the load current applied to VOUT between 70 mA and 170 mA (typical). The PFM/PWM transition point varies with the input voltage applied to VIN. Hysteresis exists in the load transition point to prevent oscillation between modes and is evident in the different values seen for the rising and the falling load sweeps.

Output Voltage Ripple

The output voltage ripple is visible by placing an oscilloscope across the output capacitor (COUT.) Set the oscilloscope to ac coupling or apply a dc offset for proper resolution.

Line Transient

Generate a high speed transient in the voltage applied to VIN and observe the behavior of the evaluation board at the SW test point and the VOUT test bus. To see the most accurate load transient waveform, place a probe directly on the output capacitor terminal with a short path to ground to limit noise and stray inductance.

Load Transient

Generate a fast transient in the current applied to VOUT and observe the behavior of the evaluation board at the SW test point and the VOUT test bus. To see the most accurate load transient waveform, place a probe directly on the output capacitor terminal with a short path to ground to limit noise and stray inductance.

Oscillator Frequency

The oscillator frequency is measured by connecting an oscilloscope to the SW test point with the converter in PWM mode.

Inductor Current

The inductor current is accessible by removing one side of the inductor from its pad and connecting a current loop in series. Place an oscilloscope current probe on the loop to view the current waveform.

EVALUATION BOARD SCHEMATIC AND LAYOUT

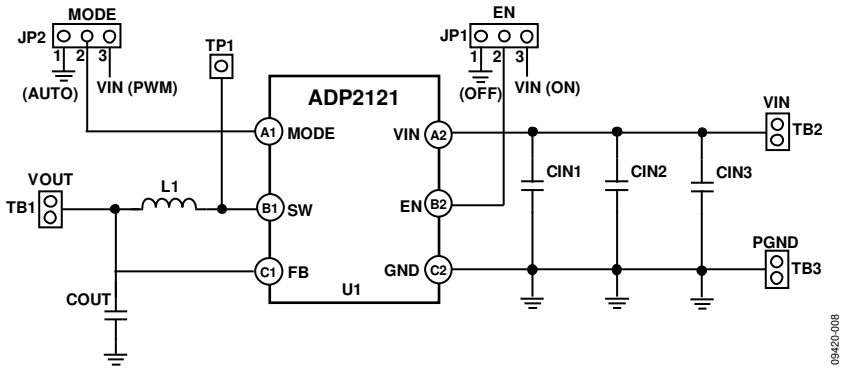

Figure 8. ADP2121 Evaluation Board Schematic

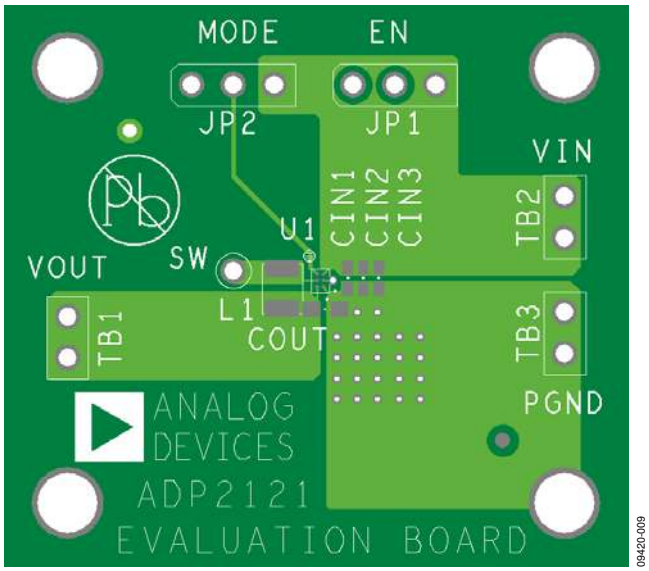

Figure 9. PCB Top Layer

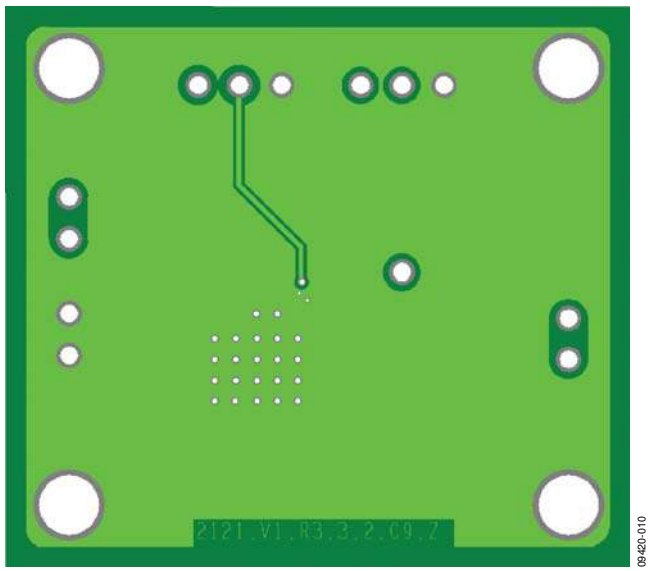

Figure 10. PCB Bottom Layer

LAYOUT GUIDLINES

For high efficiency, good regulation, and stability with the ADP2121, a well-designed PCB layout is essential. Use the following guidelines when designing PCBs:

- Keep the low ESR input capacitor, CIN, close to VIN and GND.
- Keep high current traces as short and as wide as possible.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.
- Keep the low ESR output capacitor, COUT, close to the FB and GND pins of the ADP2121. Long trace lengths from the part to the output capacitor add series inductance and may cause instability or increased ripple.

APPLICATION NOTE

It is recommended that the VIN pin be bypassed with a 2.2 µF or larger ceramic input capacitor if a supply line has a distributed capacitance of at least 10 µF. If not, at least a 10 µF capacitor is recommended on the input supply pin. The input capacitor can be increased without any limit for improved input voltage filtering.

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Manufacturer	Part Number
1	U1	6-ball wafer level chip scale package [WLCSP], step-down converter, V_{OUT} = 1.8 V	Analog Devices, Inc.	ADP2121ACBZ-1.8-R7
1	U1	6-ball wafer level chip scale package [WLCSP], step-down converter, V_{OUT} = 1.82 V	Analog Devices, Inc.	ADP2121ACBZ-1.82R7
1	U1	6-ball wafer level chip scale package [WLCSP], step-down converter, V_{OUT} = 1.85 V	Analog Devices, Inc.	ADP2121ACBZ-1.85R7
1	U1	6-ball wafer level chip scale package [WLCSP], step-down converter, V_{OUT} = 1.875 V	Analog Devices, Inc.	ADP2121ACBZ-1875R7
1	U1	6-ball wafer level chip scale package [WLCSP], step-down converter, V_{OUT} = 2.3 V	Analog Devices, Inc.	ADP2121ACBZ-2.3-R7
1	CIN1	Capacitor, MLCC, 2.2 µF, 6.3 V, 0402, X5R	Murata Manufacturing Co. Ltd.	GRM155R60J225ME95D
3	CIN2, CIN3, COUT	Capacitor, MLCC, 4.7 µF, 6.3 V, 0402, X5R	Murata Manufacturing Co. Ltd.	GRM155R60J475ME87D
1	L1	Inductor, 0.47 µH, 1.1 A, 0805	Murata Manufacturing Co. Ltd.	LQM21PNR47MC0D
1	TP1	Headers, 0.100 in, single, straight, 1-pin	Sullins Connector Solutions	PBC01SAAN[1]
3	TB1, TB2, TB3	Headers, 0.100 in, single, straight, 2-pin	Sullins Connector Solutions	PBC02SAAN[1]
2	JP1, JP2	Headers, 0.100 in, single, straight, 3-pin	Sullins Connector Solutions	PBC03SAAN[1]
2	JP1, JP2	Conn jumper shorting gold	Sullins Connector Solutions	SSC02SYAN

[1] Alternatively, PBC36SAAN can be purchased and cut as necessary.

NOTES

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG09420-0-10/10(0)

www.analog.com