AK7736A

Audio/HF DSP with 2Ch SRC

GENERAL DESCRIPTION

The AK7736A is a highly integrated audio digital signal processor with integrated 2ch SRC. It includes internal memories for digital audio processing, that allows surround effect process, time alignment and parametric equalizing. More over, the AK7736A can process both data and filter coefficients as floating point data so that high accuracy IIR/FIR filter performance can be achieved easily. The AK7736A can operate a hands-free software by AKM as well as sound processing, by programs downloaded via the microprocessor interface.

FEATURES

□ **DSP Block**
- **Word length: 24-bit**
- **Machine Cycle: 8.1 ns (2560step/fs; fs = 48kHz)**
- **Step fs=48kHz: Maximum 2560 step**
  fs=8kHz: Maximum 15360step
  fs=16kHz: Maximum 7680step
- **Multiplication: 20 x 24 → 44-bit (Double precision arithmetic available)**
- **Divider 20 / 20 → 20-bit (floating point normalization function)**
- **ALU: 48-bit arithmetic and logic operation (overflow margin 4-bit)**
- **Shift: Multiple DBUS ±15bit Shift with indirect shifting function**
- **Program RAM (PRAM): 6144word x 36-bit**
- **Coefficient RAM (CRAM): 4096word x 24-bit**
- **Data RAM (DRAM): 4096 x 24-bit (Variable Bank Size)**
- **Offset Register (OFREG): 32word x 15-bit**
- **Delay RAM (DLRAM): 16384word x 24-bit (Variable Bank Size)**
- **Register: 48-bit × 4 (ACC) [ALU]**
  24-bit × 12 (TMP) [DBUS connection]
  24-bit × 6 level stack (PTMP) [DBUS connection]

□ **Stereo 24-bit SRC**
-SRC: FSI=8kHz~96kHz / FSO=8kHz~96kHz (FSO/FSI = 0.167~6.0)

□ **Mono 24-bit Simple SRC**
-FSCONV: FSI=44.1kHz~48kHz / FSO=8kHz~16kHz

□ **Digital Interface Input/Output**
- **8ch Serial Data Inputs**
- **8ch Serial Data Outputs**
- **Sampling Frequency: 8~96kHZ**

□ **Microcontroller Interface: SPI, I^2CBUS (400kHz Fast-Mode)**

□ **PLL**

□ **Power Supply:**
-VDD 3.0~3.6V typ 3.3V (Internal Regulator)
-TVDD 1.7~3.6V (1~8pin)

□ **Operating Temperature Range: -40°C ~ 85°C**

□ **Package: 48pin LQFP**

■ Block Diagram

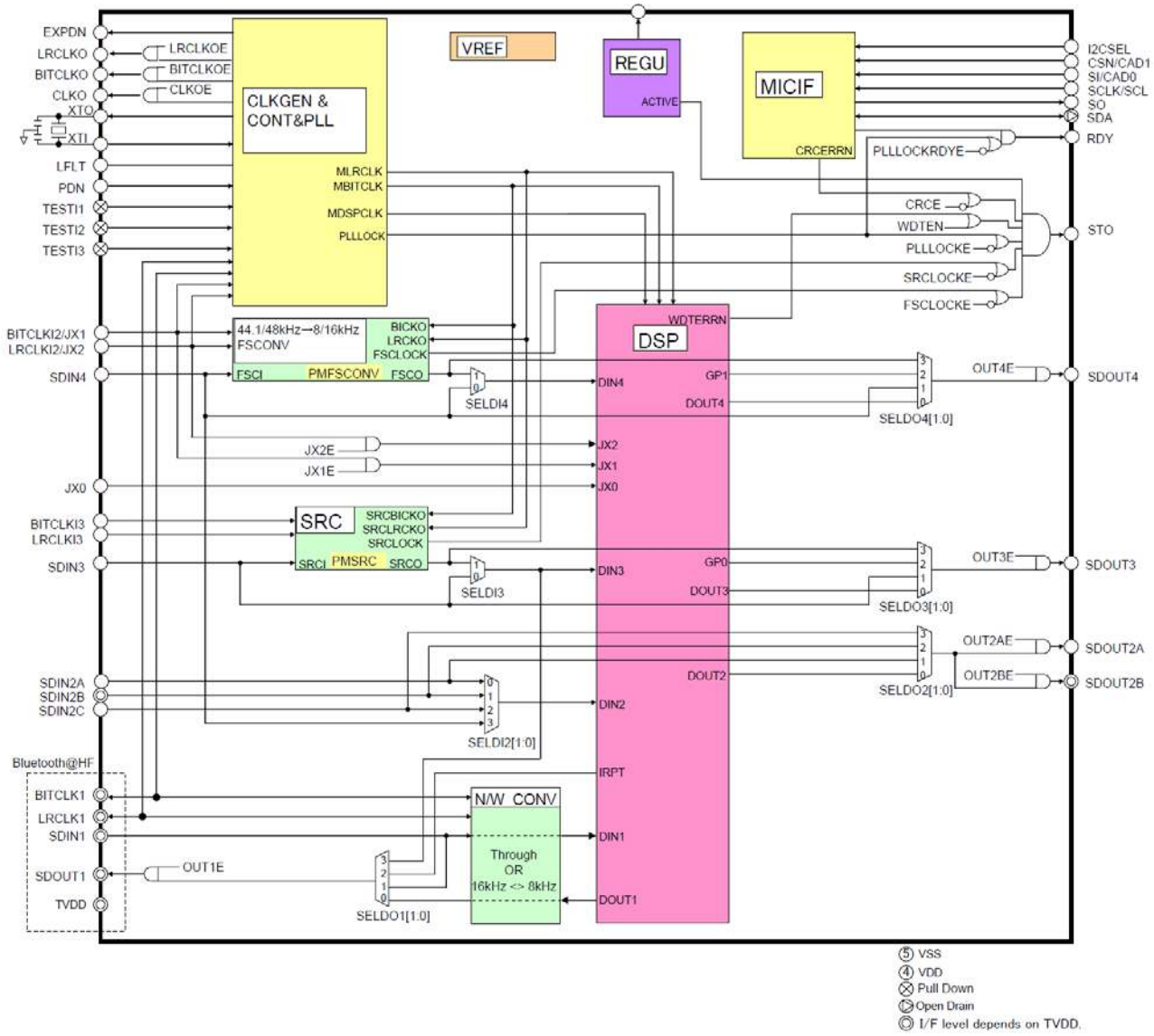


Figure 1. Block Diagram

Note 1. Refer to the section “4. When Using N/W Converter” for N/W CONV block.

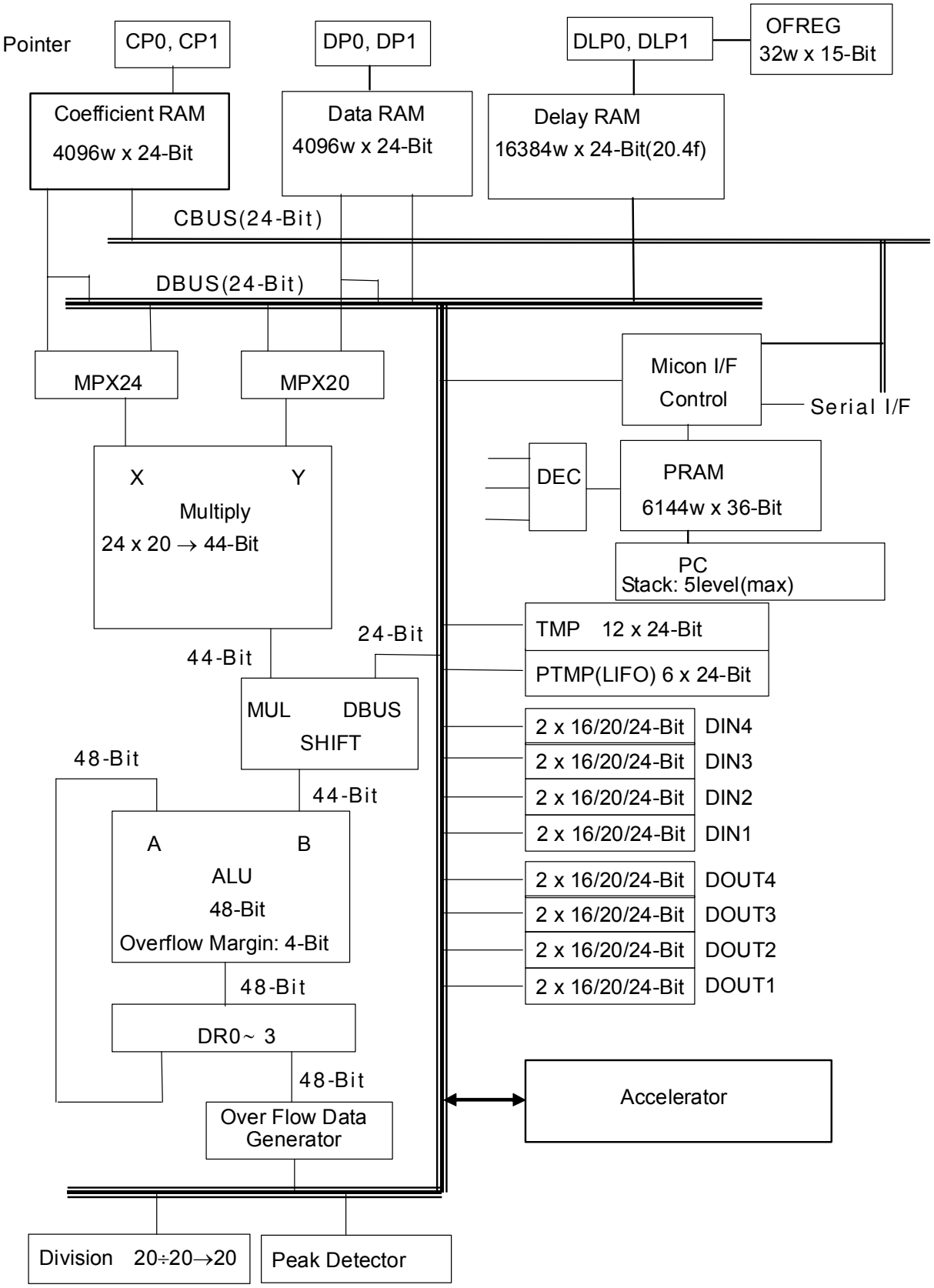
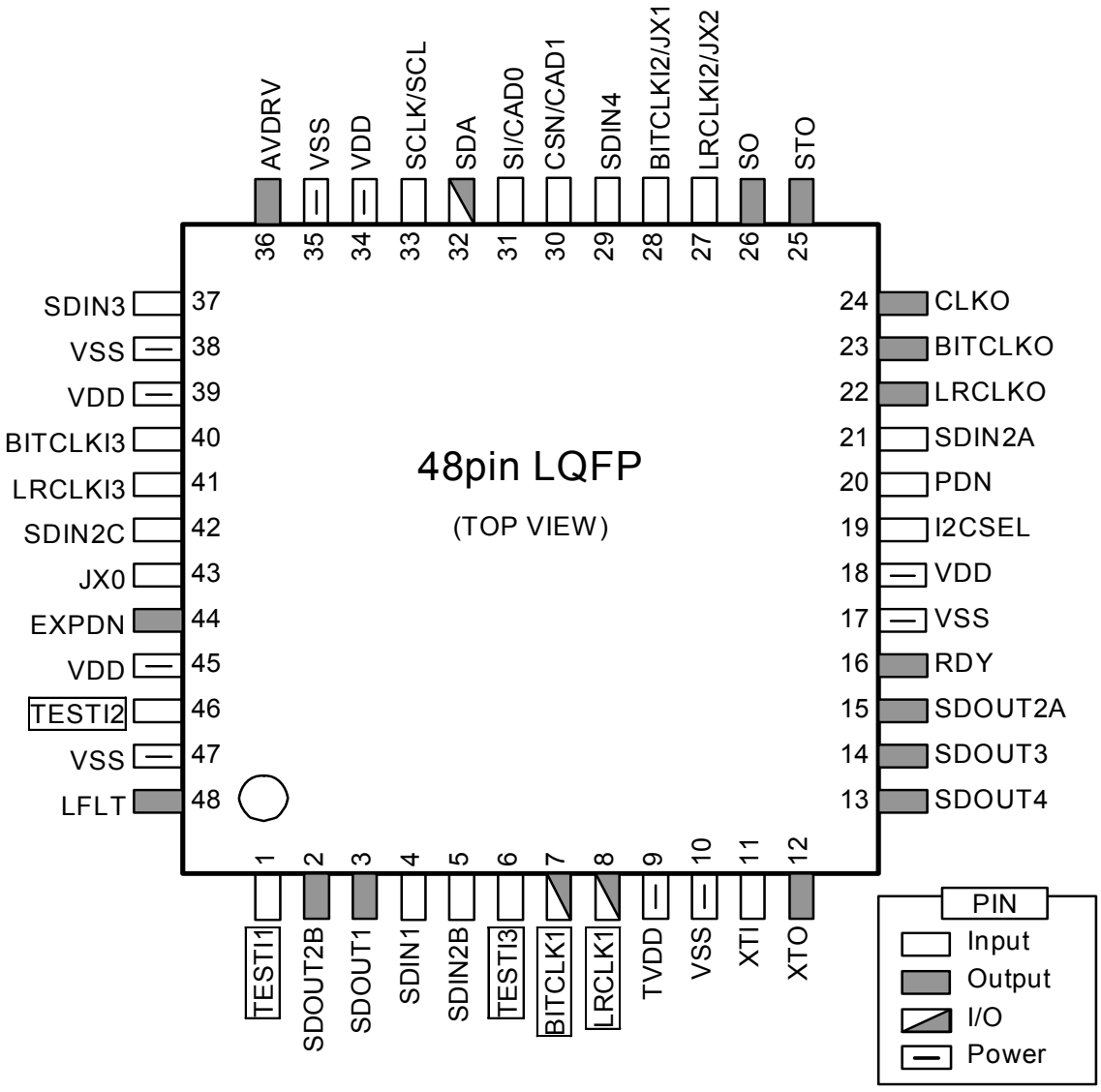


Figure 2. AK7736A Main DSP Block Diagram

■ Ordering Guide

AK7736AVQ	-40 ~ +85°C	48pin LQFP (0.5mm pitch)
AKD7736A	Evaluation Board for AK7736A	

■ Pin Layout



Note) **** is an Internal pull-down pin. ***: Pin Name

PIN/FUNCTION

No	Name	I/O	Function	Classification
1	TESTI1	I	Test Pin (Internal pull-down) This pin must be connected to VSS.	Test
2	SDOUT2B	O	Serial Data2 B Output Pin	Serial Data
3	SDOUT1	O	Serial Data1 Output Pin	
4	SDIN1	I	Serial Data1 Input Pin	Serial Data
5	SDIN2B	I	Serial Data2 B Input Pin	
6	TESTI3	I	Test Pin (Internal pull-down) This pin must be connected to VSS	Test
7	BITCLK1	I/O	Serial Bit Clock Pin 1 (Internal pull-down)	System Clock
8	LRCLK1	I/O	LR Channel Select Clock Pin 1 (Internal pull-down)	
9	TVDD	-	Power Supply Pin for 1pin-8pin I/O **1.7~3.6V**	Power Supply
10	VSS	-	Ground Pin 0V	
11	XTI	I	Crystal Oscillator Input Pin Connect a crystal oscillator between this pin and the XTO pin, or input an external clock to the XTI pin.	System Clock
12	XTO	O	Crystal Oscillator Output Pin When a crystal oscillator is used, connect it between XTI and XTO. When an external clock is used, leave this pin open.	
13	SDOUT4	O	Serial Data4 Output Pin	Serial Data
14	SDOUT3	O	Serial Data3 Output Pin	
15	SDOUT2A	O	Serial Data2 A Output Pin	
16	RDY	O	RDY Pin	Status
17	VSS	-	Ground Pin 0V	Power Supply
18	VDD	-	Power Supply Pin **3.0~3.6V** (typ. 3.3V)	
19	I2CSEL	I	I^2C BUS Select Pin I2CSEL= "L": SPI Interface I2CSEL= "H": I2CBUS Interface I2CSEL should be connected to "L" (VSS) or "H" (VDD).	I^2C
20	PDN	I	Power Down N Pin The AK7736A is powered-down by this pin. This pin must be set to "L" when power-up the AK7736A	Power Down
21	SDIN2A	I	Serial Data2 A Input Pin	Serial Data
22	LRCLKO	O	LR Channel Select Clock Pin	System Clock
23	BITCLKO	O	Serial Bit Clock Output Pin	
24	CLKO	O	Clock Output Pin	Clock Output
25	STO	O	Status Output Pin	Status
26	SO	O	Control Data Output Pin for Microprocessor Interface Hi-Z output when the CSN pin = "H"	Microprocessor Interface
27	LRCLKI2	I	LR Channel Select Clock Pin 2 (for FSCONV)	System Clock
	JX2	I	External Conditional Jump Pin 2	Conditional Input
28	BITCLKI2	I	Serial Bit Clock Input Pin 2 (for FSCONV)	System Clock
	JX1		External Conditional Jump Pin 1	Conditional Input
29	SDIN4	I	Serial Data4 Input Pin	Serial Data

30	CSN	I	Microprocessor Interface Request N Pin (I2CSEL pin= "L") Set this pin to "H" when not interfacing to a microprocessor or during power-down.	Microprocessor Interface
	CAD1	I	I^2CBUS Address Pin 1 (I2CSEL pin= "H")	I^2C
31	SI	I	Serial Data Input Pin for Microprocessor Interface Set this pin to "L" when not using.	Microprocessor Interface
	CAD0	I	I^2C BUS Address Pin 0 (I2CSEL pin= "H")	I^2C
32	SDA	O	Control Data Input /Output Pin (I2CSEL pin= "L") "Hi-Z" Output. This pin must be open when the I2CSEL pin = "L".	Open
		I/O	Control Data Input /Output Pin (I2CSEL pin= "H") SDA: I^2C BUS Interface	I^2C
33	SCLK	I	Control Data Clock Pin for Microprocessor Interface (I2CSEL pin = "L") Set this pin to "H" when no clock is input.	Microprocessor Interface
	SCL	I	Control Data Clock Pin (I2CSEL pin= "H") SCL: I^2C BUS Interface	I^2C
34	VDD	-	Power Supply Pin **3.0~3.6V** (typ. 3.3V)	Power Supply
35	VSS	-	Ground Pin 0V	
36	AVDRV		AVDRV pin Connect a 1μF capacitor between this pin and the VSS pin (No. 35). No external circuits should be connected to this pin.	Analog Output
37	SDIN3	I	Serial Data3 Input Pin	Serial Data
38	VSS	-	Ground Pin 0V	Power Supply
39	VDD	-	Power Supply Pin **3.0~3.6V** (typ. 3.3V)	
40	BITCLKI3	I	Serial Bit Clock Input Pin 3 (for SRC)	System Clock
41	LRCLKI3	I	LR Channel Select Clock Pin 3 (for SRC)	
42	SDIN2C	I	Serial Data2 C Input Pin	Serial Data
43	JX0	I	External Conditional Jump Pin 0	Conditional Input
44	EXPDN	O	Power Down Signal Output Pin	Power Down
45	VDD	-	Power Supply Pin **3.0~3.6V** (typ. 3.3V)	Power Supply
46	TESTI2	I	Test Pin (internal pull-down) This pin must be connected to VSS.	Test
47	VSS	-	Ground Pin 0V	Power Supply
48	LFLT	O	PLL RC Component Connect Pin Connect C=12nF between this pin and No.47 (VSS) pin.	Analog Output

Note 2. All digital input pins must not be allowed to float
Note 3. The I2CSEL pin must be fixed to "L" (VSS) or "H" (TVDD).

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately:

Pin Name	**Setting**
Output Pins	Leave Open
Input/Output Pins	
SDA	Leave Open
LRCLK1	Connect to VSS
BITCLK1	Connect to VSS
Input Pins	Connect to VSS

■ **Output pin Status in Power-down Mode (PDN pin = "L")**

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
2	SDOUT2B	O	"L" Output	22	LRCLKO	O	"L" Output
3	SDOUT1	O	"L" Output	23	BITCLKO	O	"L" Output
7	BITCLK1	I/O	Input	24	CLKO	O	"L" Output
8	LRCLK1	I/O	Input	25	STO	O	"L" Output
12	XTO	O	"H" Output	26	SO	O	"Hi-Z" Output
13	SDOUT4	O	"L" Output	32	SDA	I/O	"Hi-Z" Output
14	SDOUT3	O	"L" Output	44	EXPDN	O	"L" Output
15	SDOUT2A	O	"L" Output	48	LFLT	O	"L" Output
16	RDY	O	"L" Output				

■ **Relationship between the I2CSEL Pin and the SDA Pin**

	I2CSEL	PDN	SDA
SPI Interface	L	L	Hi-Z
	L	H	Hi-Z
I2CBUS support	H	L	"Hi-Z" → pull-up
	H	H	function

ABUSOLUTE MAXIMUM RATINGS

(VSS=0V: All voltages are with respect to ground)

Parameter	Symbol	min	max	Unit
Power Supply				
TVDD	TVDD	-0.3	4.3	V
VDD	VDD	-0.3	4.3	V
Input Current (except for power supply pin)	IIN	–	±10	mA
Digital Input Voltage (1pin-8pin)	VINDT	-0.3	(TVDD+0.3)	V
Digital Input Voltage (except 1pin-8pin)	VIND	-0.3	(VDD+0.3)	
Operating Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATION CONDITION

(VSS=0V: All voltages are with respect to ground.)

Parameter	Symbol	min	typ	max	Unit
Power Supply					
TVDD	TVDD	1.7	1.8	3.6	V
VDD	VDD	3.0	3.3	3.6	V

Note 4. The TVDD pin is the power supply pin for pin number 1 ~ 8 pins.

Note 5. The power-up sequence with VDD and TVDD is not critical. The PDN pin should be held "L" when power is supplied. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

Note 6. Do not turn off the power supply of the AK7736A with the power supply of the surrounding device turned on. VDD must not exceed the pull-up of SDA and SCL of I2C BUS. (The diode exists for VDD in the SDA and SCL pins.)

ELECTRIC CHARACTERISTICS

■ SRC Characteristics

1) SRC

(Ta= -40°C~85°C; TVDD=1.8V, VDD=3.3V; VSS=0V; data = 24bit; measurement bandwidth = 20Hz~FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Unit
Resolution				24	Bits
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO	8		96	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=44.1kHz/48kHz			-112		dB
FSO/FSI=44.1kHz/96kHz			-111		dB
FSO/FSI=48kHz/44.1kHz			-112		dB
FSO/FSI=48kHz/96kHz			-113		dB
FSO/FSI=48kHz/8kHz			-111	-103	dB
FSO/FSI=16kHz/48kHz			-113		dB
FSO/FSI=16kHz/44.1kHz			-100		dB
FSO/FSI=8kHz/48kHz			-113		dB
FSO/FSI=8kHz/44.1kHz			-95		dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=44.1kHz/48kHz			113		dB
FSO/FSI=44.1kHz/96kHz			113		dB
FSO/FSI=48kHz/44.1kHz			113		dB
FSO/FSI=48kHz/96kHz			113		dB
FSO/FSI=48kHz/8kHz		108	113		dB
FSO/FSI=16kHz/48kHz			113		dB
FSO/FSI=16kHz/44.1kHz			113		dB
FSO/FSI=8kHz/48kHz			111		dB
FSO/FSI=8kHz/44.1kHz			114		dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)					
FSO/FSI=44.1kHz/48kHz			115		dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

2) FSCONV

(Ta= -40°C ~85°C; TVDD=1.8V, VDD=3.3V; VSS=0V; data = 24bit; measurement bandwidth = 20Hz~FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Unit
Resolution				24	Bits
Input Sample Rate	FSI	44.1		48	kHz
Output Sample Rate	FSO	8		16	kHz
THD+N (Input= 1kHz, 0dBFS)					
FSO/FSI=16kHz/48kHz			-114		dB
FSO/FSI=16kHz/44.1kHz			-95		dB
FSO/FSI=8kHz/48kHz			-115		dB
FSO/FSI=8kHz/44.1kHz			-97		dB
Dynamic Range (Input= 1kHz, -60dBFS)					
FSO/FSI=16kHz/48kHz			114		dB
FSO/FSI=16kHz/44.1kHz			114		dB
FSO/FSI=8kHz/48kHz			114		dB
FSO/FSI=8kHz/44.1kHz			114		dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted)					
FSO/FSI=8kHz/48kHz			117		dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		0.363	-

Note 7. Input signal frequency bandwidth of FSCONV must be attenuated more than 4kHz when the output sampling rate is 8kHz, or must be attenuated more than 8kHz when the output sampling rate is 16kHz.

■ DC Characteristics

(Ta= -40°C ~85°C, VSS=0V, VDD=3.0~3.6V, TVDD=1.7~3.6V)

Parameter	Symbol	min	typ	max	Unit
High Level Input Voltage 1 (Note 8)	VIH1	80%TVDD			V
Low Level Input Voltage 1 (Note 8)	VIL1			20%TVDD	V
High Level Input Voltage 2 (Note 9)	VIH2	80%VDD			V
Low Level Input Voltage 2 (Note 9)	VIL2			20%VDD	V
SCL, SDA High Level Input Voltage	VIH3	70%VDD			V
SCL, SDA Low Level Input Voltage	VIL3			30%VDD	V
High Level Output Voltage 1 Iout= -100µA (Note 8)					
1.7 ≤ TVDD < 3.0	VOH1	TVDD-0.3			V
3.0 ≤ TVDD ≤ 3.6	VOH1	TVDD-0.5			
Low Level Output Voltage 1 Iout=100µA (Note 8)					
1.7 ≤ TVDD < 3.0	VOL1			0.3	V
3.0 ≤ TVDD ≤ 3.6	VOL1			0.5	
High Level Output Voltage 2 Iout= -100µA (Note 9)	VOH2	VDD-0.5			V
Low Level Output Voltage 2 Iout=100µA (Note 9)	VOL2			0.5	V
SDA Low Level Output Voltage Iout=3mA	VOL3			0.4	V
Input Leak Current (Note 10)	Iin			±10	µA
Input Leak Current with pulled-down (Note 11)	Iid		81		µA

Note 8. TESTI1, SDOUT2B, SDOUT1, SDIN1, SDIN2B, TESTI3, BITCLK1 and LRCLK1 pins. 1pin-8pin.
Note 9. Except 1pin-8pin, SDA and SCL pins
Note 10. Pull-down pins, and the XTI pin is not included.
Note 11. LRCLK1, BITCLK1, TESTI1, TESTI2 and TESTI3 pins are internal pulled-down pin. (typ. 40.7kΩ)

■ Current Consumption

(Ta=25°C, VSS=0V, VDD=3.0~3.6V(typ=3.3V, max=3.6V), TVDD=1.7~3.6V(typ=1.8V, max=3.6V))

	Parameter	min	typ	max	Unit
Normal Operation Mode (Note 12)	TVDD		0.3	0.5	mA
	VDD		31	50	mA
Power-down Mode	TVDD		0.01		µA
(PDN = L)	VDD		1		µA

Note 12. The current consumption changes depending on the system frequency and contents of the DSP program.

DIGITAL FILTER CARACTERISTICS

■ SRC Block

(Ta= -40°C~85°C, VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS =0V)

Parameter		Symbol	min	typ	max	Unit
Passband -0.01dB	0.980≤FSO/FSI≤6.000	PB	0		0.4583FSI	kHz
	0.900≤FSO/FSI<0.990	PB	0		0.4167FSI	kHz
	0.533≤FSO/FSI<0.909	PB	0		0.2182FSI	kHz
	0.490≤FSO/FSI<0.539	PB	0		0.2177FSI	kHz
	0.450≤FSO/FSI<0.495	PB	0		0.1948FSI	kHz
	0.225≤FSO/FSI<0.455	PB	0		0.1312FSI	kHz
Passband -0.50dB	0.167≤FSO/FSI<0.227	PB	0		0.0658FSI	kHz
Stopband	0.980≤FSO/FSI≤6.000	SB	0.5417FSI			kHz
	0.900≤FSO/FSI<0.990	SB	0.5021FSI			kHz
	0.533≤FSO/FSI<0.909	SB	0.2974FSI			kHz
	0.490≤FSO/FSI<0.539	SB	0.2812FSI			kHz
	0.450≤FSO/FSI<0.495	SB	0.2604FSI			kHz
	0.225≤FSO/FSI<0.455	SB	0.1802FSI			kHz
	0.167≤FSO/FSI<0.227	SB	0.0970FSI			kHz
Passband Ripple	0.225≤FSO/FSI≤6.000	PR			±0.01	dB
	0.167≤FSO/FSI<0.227	PR			±0.50	dB
Stopband Attenuation	0.450≤FSO/FSI≤6.000	SA	95.2			dB
	0.167≤FSO/FSI<0.455	SA	90.0			dB
Group Delay (Ts=1/fs) (Note 13)		GD		63		Ts

Note 13. This delay is the a period from the rising edge of LRCLKI3, just after the data is input, to the rising edge of LRCLKO, just before the data is output, when there is no phase difference between Input and Output signals.

■ FSCONV Block

(Ta= -40°C~85°C, VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS =0V)

Parameter		Symbol	min	typ	max	Unit
Passband -0.01dB	0.167≤FSO/FSI≤0.363	PB	0		0.1814FSI	kHz
Stopband	0.167≤FSO/FSI≤0.363	SB	0.8185FSI			kHz
Passband Ripple	0.167≤FSO/FSI≤0.363	PR			±0.005	dB
Stopband Attenuation	0.167≤FSO/FSI≤0.363	SA	94.0			dB
Group Delay (Ts=1/fsi) (Note 14)		GD		9		Ts

Note 7. Input signal frequency bandwidth of FSCONV must be attenuated more than 4kHz when the output sampling rate is 8kHz, or must be attenuated more than 8kHz when the output sampling rate is 16kHz.

Note 14. This delay is the a period from the rising edge of LRCLKI2, just after the data is input, to the rising edge of LRCLKO, just before the data is output, when there is no phase difference between Input and Output signals.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta= -40°C~85°C; VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS =0V; CL=20pF)

Parameter		Symbol	min	typ	max
a) with a Crystal Oscillator					
CKM[2:0]bits=0h	fXTI		11.2896 12.288		MHz
CKM[2:0]bits=1h	fXTI		16.9344 18.432		MHz
b) with an External Clock					
Duty Cycle		40	50	60	%
CKM[2:0]bits=0h,2h	fXTI	11.0	11.2896 12.288	12.4	MHz
CKM[2:0]bits=1h	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCLK1 Frequency (Note 15)	fs	8		96	kHz
BITCLK1 Frequency (Note 16)			32,48,64		fs
High Level Width Low Level Width	tBCLKH tBCLKL	64 64			ns ns
Frequency	fBCLK	0.23	3.072	6.2	MHz
LRCLKI2 Frequency (FSCONV) (Note 17)	fs	44.1		48	kHz
BITCLKI2 Frequency (FSCONV) (Note 18)			32,48,64,128		fs
High Level Width Low Level Width	tBCLKH tBCLKL	64 64			ns ns
Frequency	fBCLK	1.25	3.072	6.2	MHz
LRCLKI3 Frequency (SRC)	fs	8		96	kHz
BITCLKI3 Frequency (SRC)			32,48,64,128		fs
High Level Width Low Level Width	tBCLKH tBCLKL	32 32			ns ns
Frequency	fBCLK	0.23	3.072	12.4	MHz

Note 15. LRCLK1 frequency and sampling rate (fs) should be the same.
Note 16. When BITCLK1 is used as a master clock reference clock, it should be synchronized with LRCLK1, and its frequency should be fixed.
Note 17. fs=8~48kHz in CKM mode 4.
Note 18. 128fs is inhibited in CKM mode 4.

■ Power Down

(Ta= -40°C~85°C; VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS =0V)

Parameter	Symbol	min	typ	max	Unit
PDN (Note 19)	tRST	600			ns

Note 19. The PDN pin must be “L” when power up the AK7736A.

■ Serial Data Interface

(Ta= -40°C ~85°C; VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS =0V; CL=20pF)

Parameter		Symbol	min	typ	max	Unit
DSP Section Input SDIN1, 2A, 2B, 2C, 3, 4	(Note 20)					
Delay Time from BITCLK1 "↑" to LRCLK1	(Note 21)	tBLRD	20			ns
Delay Time from LRCLK1 to BITCLK1 "↑"	(Note 21)	tLRBD	20			ns
Serial Data Input Latch Setup Time		tBSIDS	80			ns
Serial Data Input Latch Hold Time		tBSIDH	80			ns
SRC Section Input SDIN3						
Delay Time from BITCLKI3 "↑" to LRCLKI3	(Note 22)	tBLRD	20			ns
Delay Time from LRCLKI3 to BITCLKI3 "↑"	(Note 22)	tLRBD	20			ns
Serial Data Input Latch Setup Time		tBSIDS	40			ns
Serial Data Input Latch Hold Time		tBSIDH	40			ns
FSCONV Section Input SDIN4	(Note 23)					
Delay Time from BITCLKI2 "↑" to LRCLKI2	(Note 24)	tBLRD	20			ns
Delay Time from LRCLKI2 to BITCLKI2 "↑"	(Note 24)	tLRBD	20			ns
Serial Data Input Latch Setup Time		tBSIDS	40			ns
Serial Data Input Latch Hold Time		tBSIDH	40			ns
Output SDOUT1, SDOUT2, SDOUT3, SDOUT4						
BITCLKO Frequency	(Note 25)	fBCLK		64		fs
BITCLKO Duty Factor	(Note 25)			50		%
Delay Time from BITCLKO "↓" to LRCLKO	(Note 26)	tMBL	-20		40	ns
Delay Time from LRCLK1 to Serial Data Output	(Note 27)	tLRD			80	ns
Delay Time from BITCLK1"↓" to Serial Data Output	(Note 28)	tBSOD			80	ns
Delay Time from LRCLKO to Serial Data Output	(Note 27)	tLRD			80	
Delay Time from BITCLKO "↓" to Serial Data Output	(Note 29)	tBSOD			80	
SDINn → SDOUTn (n=1, 2A, 2B, 2C, 3, 4)						
Delay Time from SDINn to SDOUTn Output		tIOD			60	ns

Note 20. In CKM mode 4, these are the time from LRCKLI2 or BITCLKI2.
Note 21. When BITCLK1 polarity is inverted, delay time is from BITCLK1 "↓".
Note 22. When BITCLKI3 polarity is inverted, delay time is from BITCLKI3 "↓".
Note 23. Except CKM mode 4.
Note 24. When BITCLKI2 polarity is inverted, delay time is from BITCLKI2 "↓".
Note 25. Except slave mode.
Note 26. When BCKOP bit = "1", delay time is from BITCLKO "↑".
Note 27. Except I^2S compatible mode.
Note 28. When BITCLK1 polarity is inverted, delay time is from BITCLK1 "↑".
Note 29. When BITCLKO polarity is inverted, delay time is from BITCLKO "↑".

■ Microprocessor Interface

(Ta= -40°C ~85°C; VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microprocessor Interface Signal					
SCLK Frequency	fSCLK			2.1	MHz
SCLK Low Level Width	tSCLKL	200			ns
SCLK High Level Width	tSCLKH	200			ns
Microprocessor → AK7736A					
CSN High Level Width	tWRQH	500			ns
From CSN "↑" to PDN "↑"	tRST	600			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	500			ns
From SCLK "↑" to CSN "↑"	tSCW	800			ns
SI Latch Setup Time	tSIS	200			ns
SI Latch Hold Time	tSIH	200			ns
AK7736A → Microprocessor					
Delay Time from SCLK "↓" to SO Output	tSOS			200	ns
Hold Time from SCLK "↑" to SO Output (Note 30)	tSOH	200			ns

Note 30. Except when input the eighth bit of the command code.

■ I²C-BUS Interface

(Ta= -40°C ~85°C; VDD=3.0~3.6V, TVDD=1.7~3.6V, VSS=0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I2C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

■ **Timing Diagram**

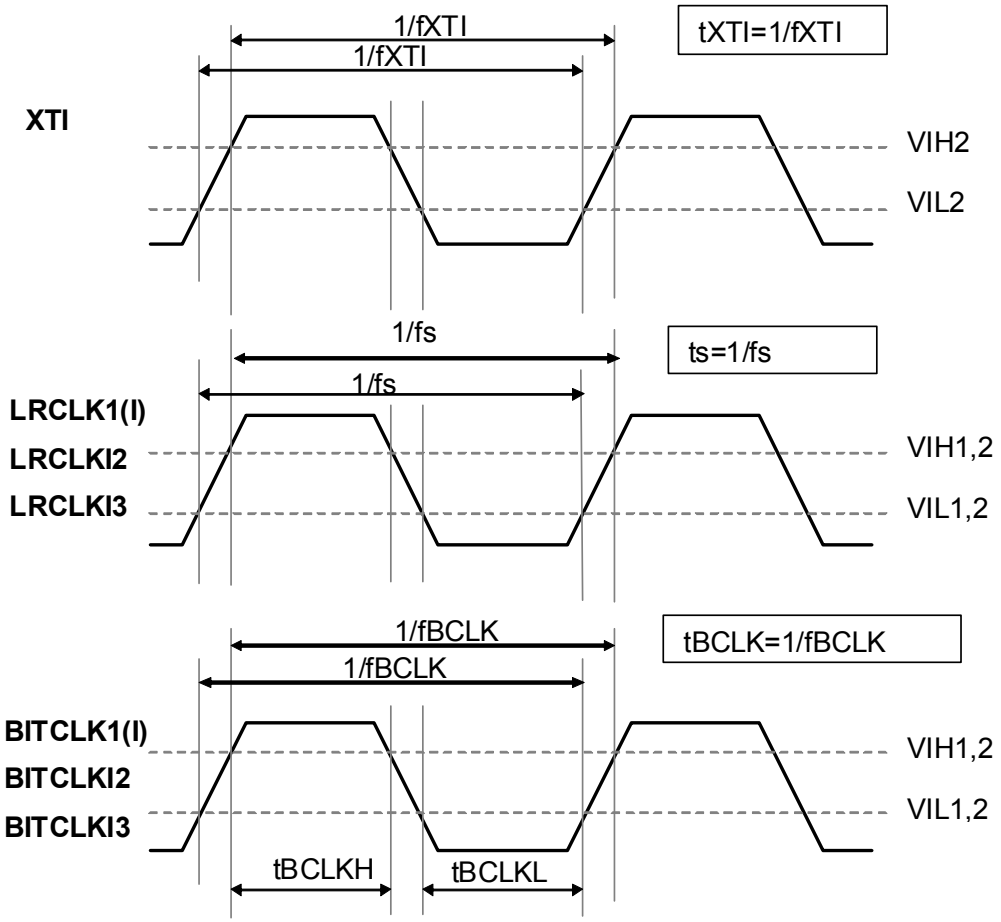


Figure 3. System Clock

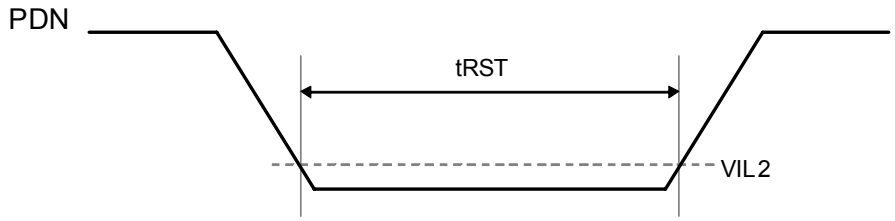


Figure 4. Power-down

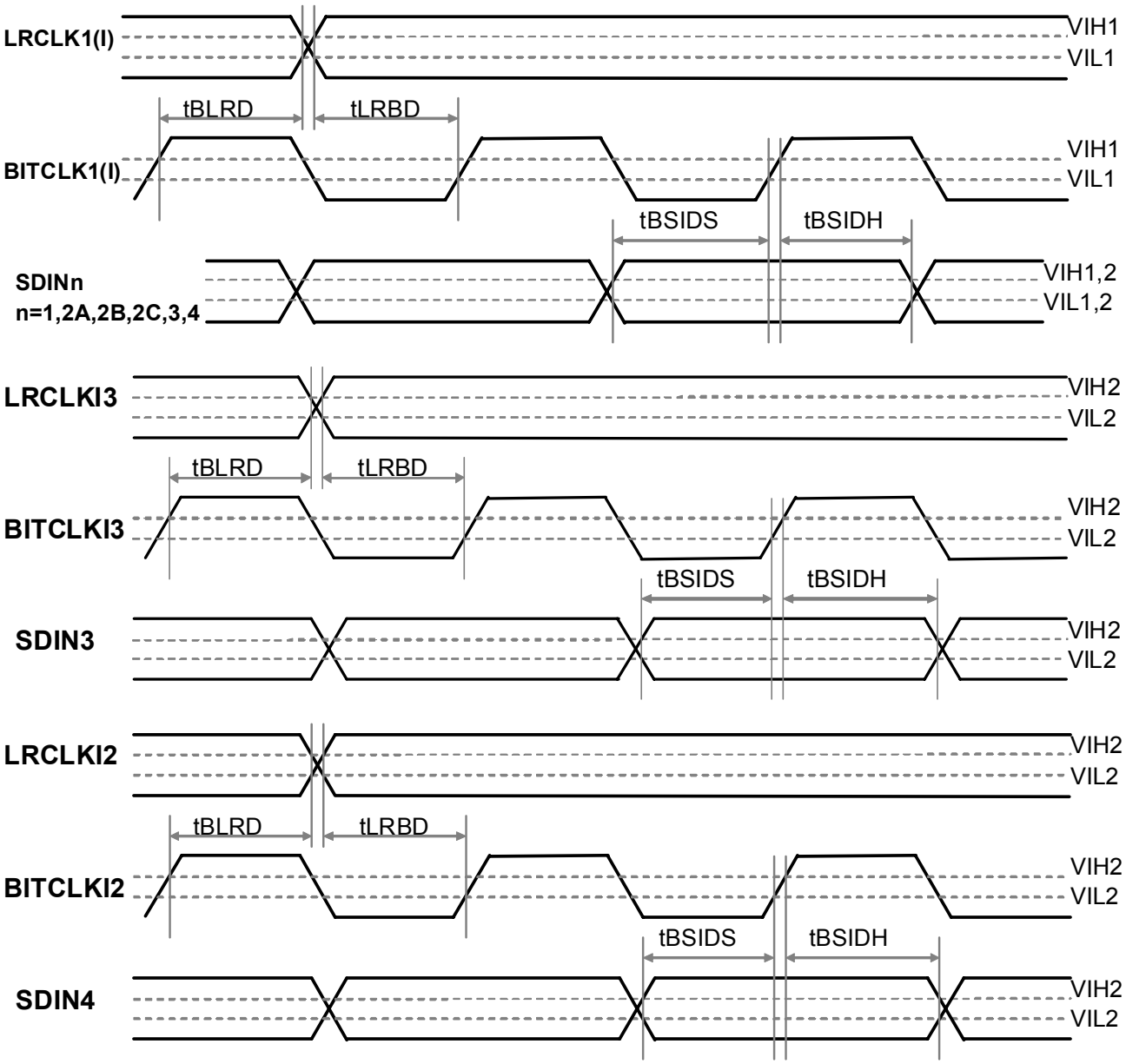


Figure 5. Slave Mode Input Interface

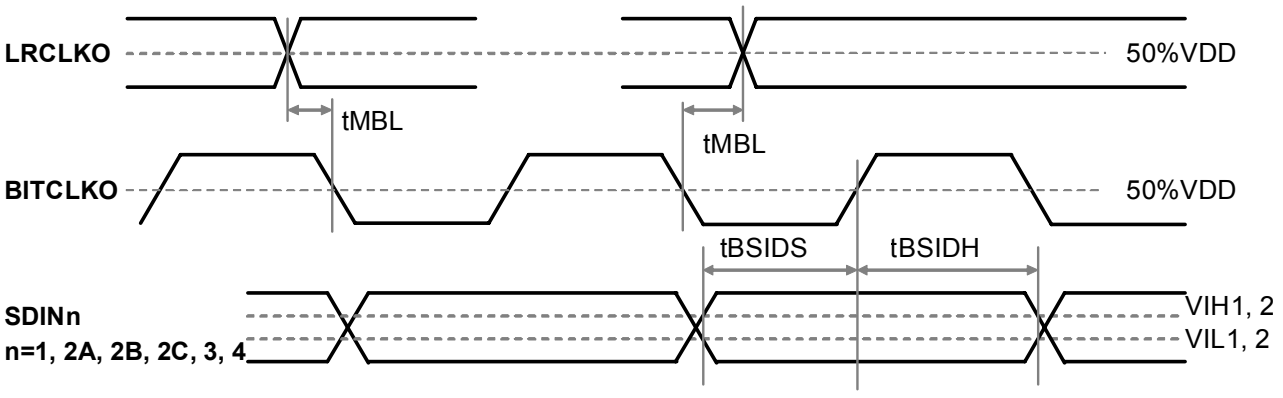


Figure 6. Master Mode Input Interface

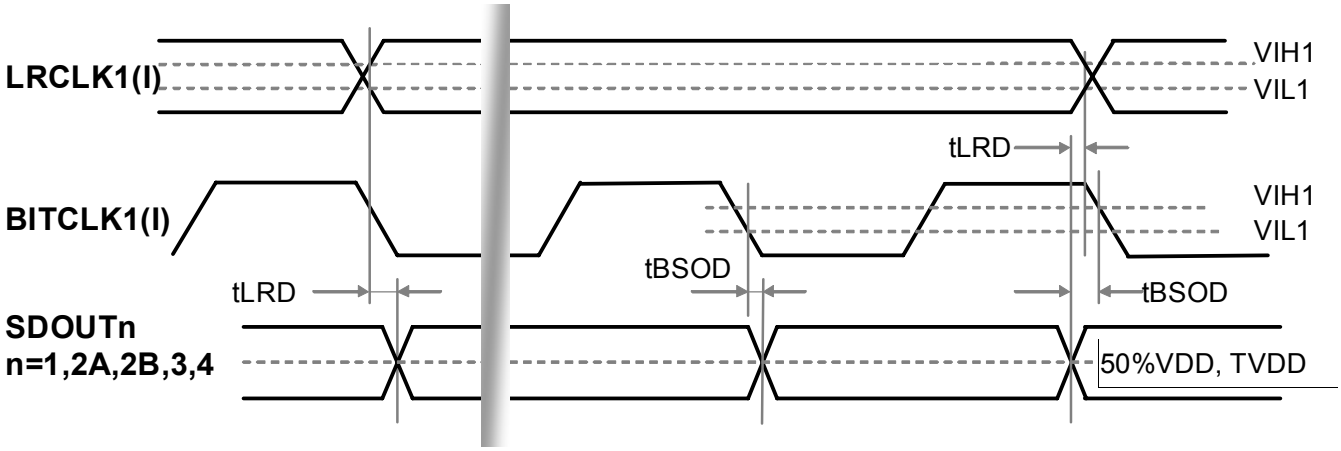


Figure 7. Slave Mode Output Interface

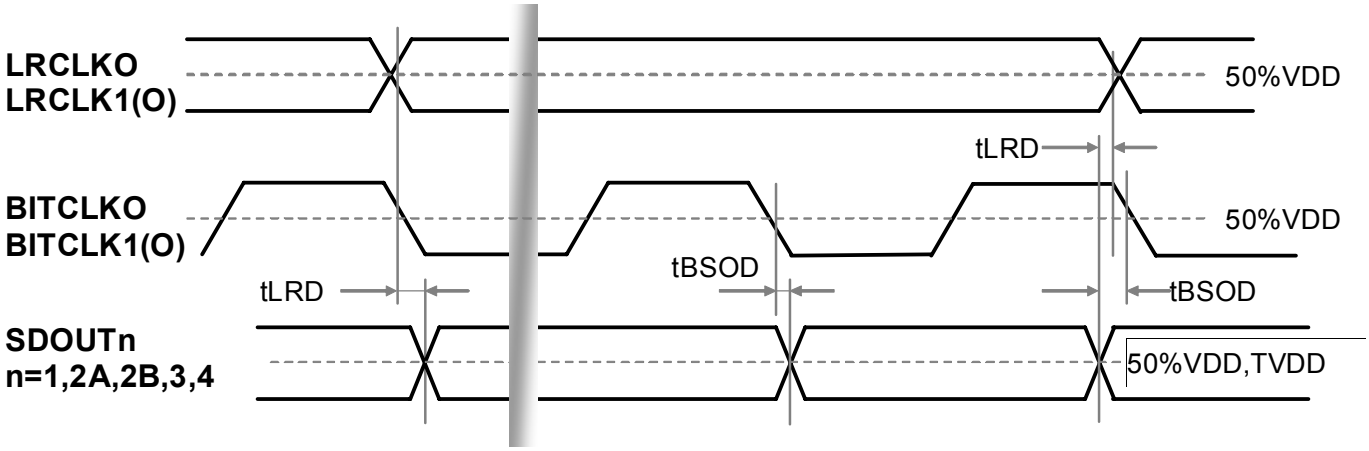


Figure 8. Master Mode Output Interface

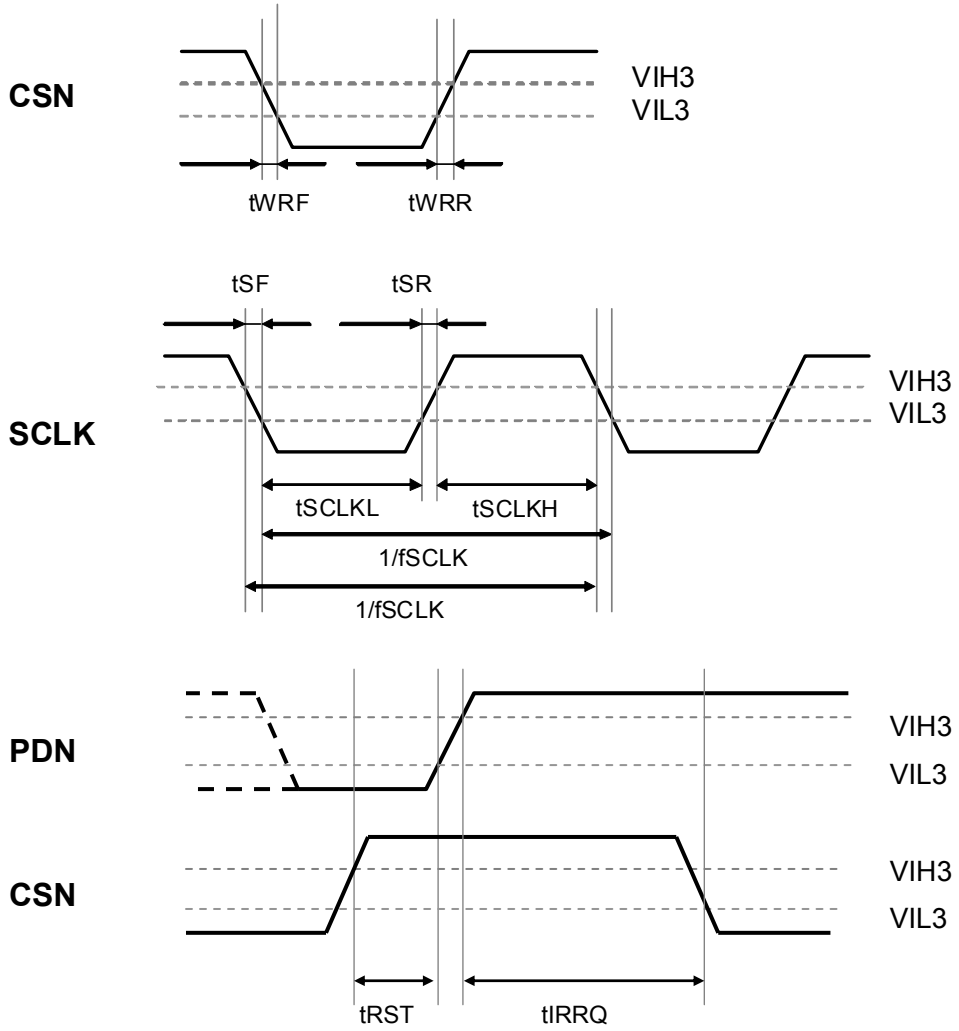


Figure 9. Microprocessor Interface Signal

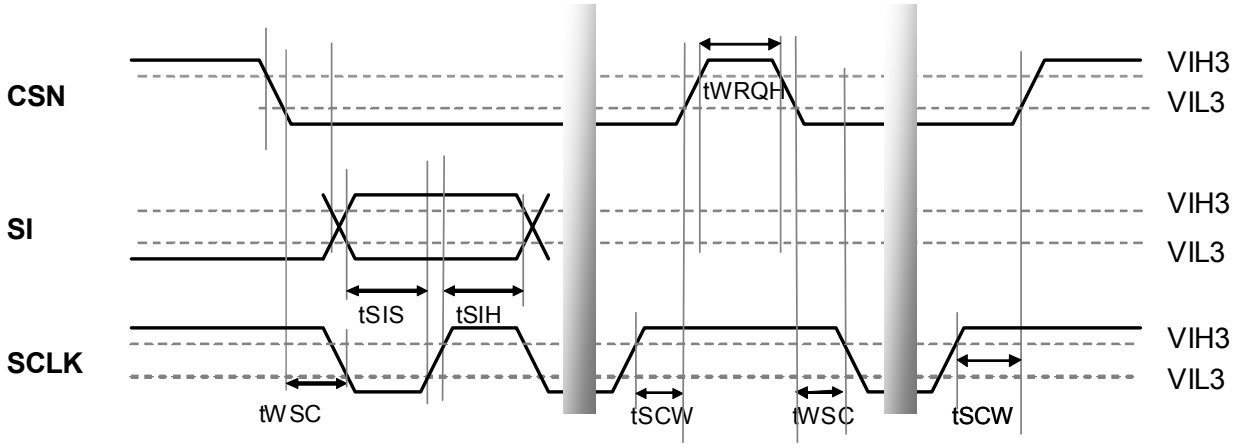


Figure 10. Microprocessor → AK7736A

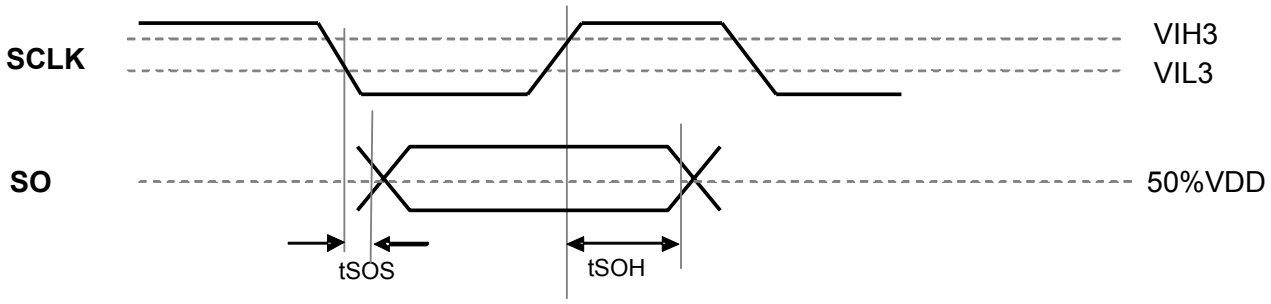


Figure 11. AK7736A → Microprocessor

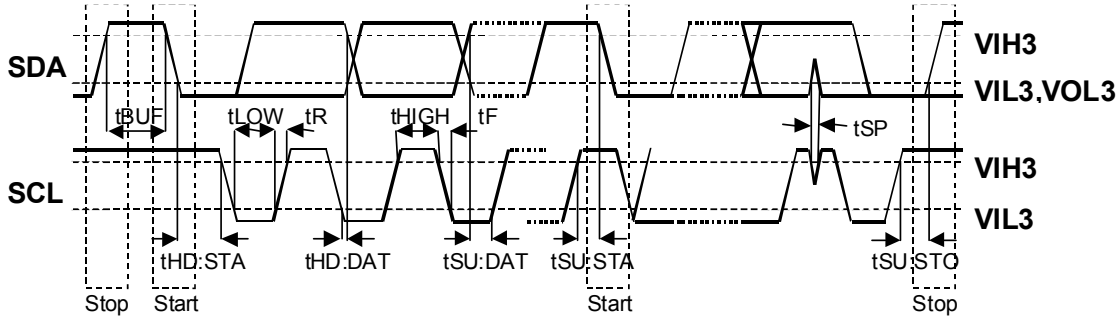
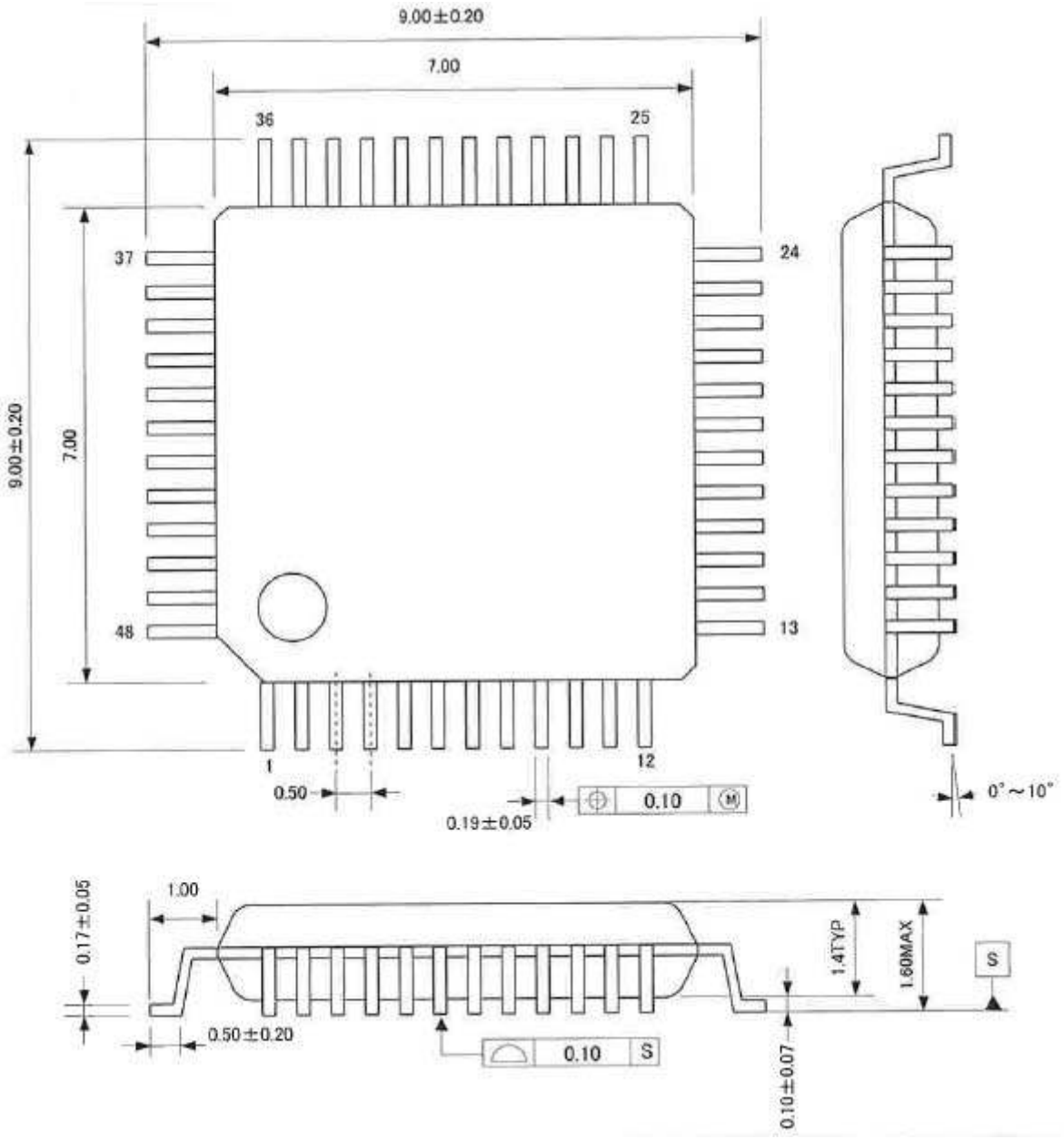


Figure 12. I^2C-BUS Interface

PACKAGE

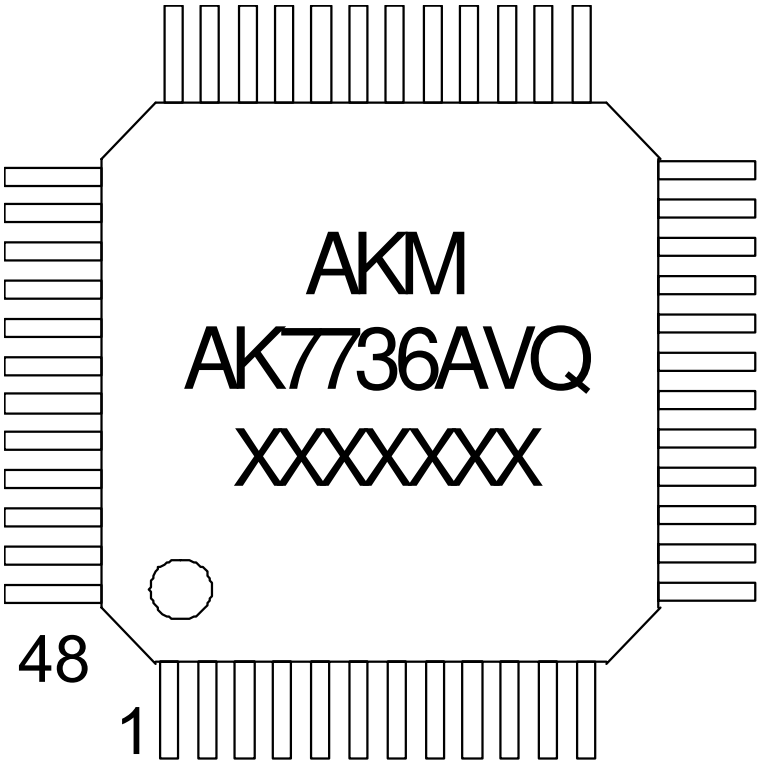
48pin LQFP (Unit mm)



■ Materials and Lead Specification

Package: Epoxy
Lead frame: Copper
Lead-finish: Soldering (Pb free) plate

MARKING



1) pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7736AVQ
4) Asahi Kasei Logo

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/12/17	00	First Edition		

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