SN74LV540A Octal Buffers/Drivers with 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Max t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Voltage operation on all ports
- I_{off} supports Partial-Power-Down Mode operation
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Tests and Measurements
- Industrial Transports
- Patient Monitoring
- Wireless Infrastructure
- Network Switches
- Automotive Infotainment

3 Description

The SN74LV540A device is an octal buffer/driver designed for 2 V to 5.5 V V_{CC} operation.

This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
SN74LV540A	RGY (VQFN, 20)	4.50 mm x 3.50 mm
	DB (SSOP, 20)	7.50 mm x 5.30 mm
	PW (TSSOP, 20)	6.50 mm x 4.40 mm
	DGV (TVSOP, 20)	5.00 mm x 4.40 mm
	DW (SOIC, 20)	12.80 x 7.50 mm
	NS (SOP, 20)	12.6 mm x 5.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

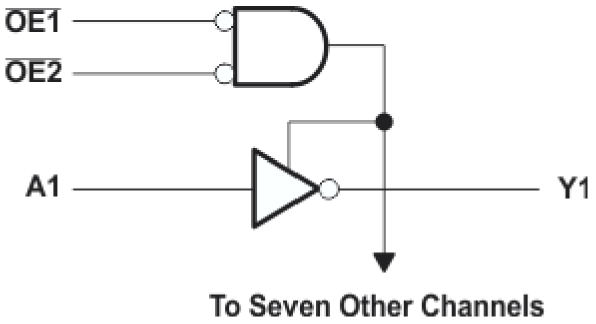

Figure 3-1. Simplified Schematic

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4 Revision History

Changes from Revision I (December 2014) to Revision J (March 2023) — Page

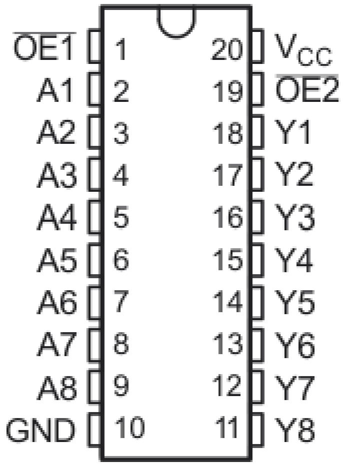
- Updated structural layout of document to current standard, updated *Features* section, and added NS package to *Package Information* table....1
- Added ± to values in *ESD Ratings* section....4
- Updated thermal values for PW package from RθJA = 102.8 to 128.2, RθJC(top) = 36.8 to 70.5, RθJB = 53.8 to 79.3, ΨJT =2.5 to 23.4, ΨJB = 53.3 to 78.9, all values in °C/W....5

Changes from Revision H (April 2005) to Revision I (December 2014) — Page

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Deleted *Ordering Information* table....1
- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. 5

5 Pin Configuration and Functions

SN74LV540A . . . DB, DGV, DW, NS, OR PW PACKAGE (TOP VIEW)



SN74LV540A . . . RGY PACKAGE (TOP VIEW)

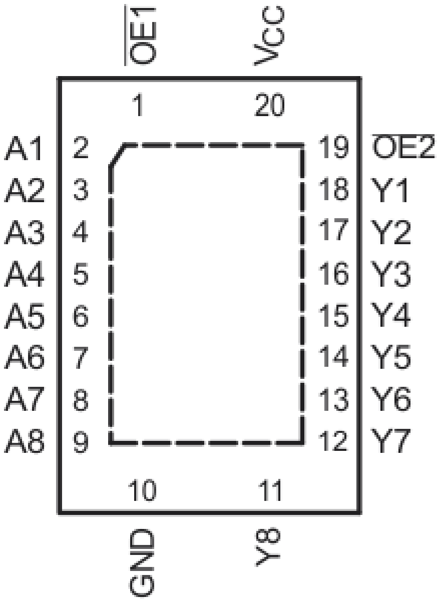


Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{\text{OE1}}$	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground Pin
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	$\overline{\text{OE2}}$	I	Output Enable 2
20	V_{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range[2]		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	7	V
V_O	Output voltage range applied in the high or low state[2] [3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±2000	
		Machine Model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN74LV540A		UNIT
			MIN	MAX	
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 2.3 V to 2.7 V		–2	mA
		V_{CC} = 3 V to 3.6 V		–8	
		V_{CC} = 4.5 V to 5.5 V		–16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 2.3 V to 2.7 V		2	mA
		V_{CC} = 3 V to 3.6 V		8	
		V_{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200	ns/V
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC(1)		SN74LV540A						UNIT
		DB	DGV	DW	NS	PW	RGY	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.0	116.1	79.8	77.1	128.2	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.7	31.3	45.8	43.6	70.5	43.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	57.6	47.4	44.6	79.3	12.9	
Ψ_{JT}	Junction-to-top characterization parameter	19.4	1.0	18.5	17.2	23.4	0.9	
Ψ_{JB}	Junction-to-board characterization parameter	50.8	56.9	47.0	44.2	78.9	12.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	7.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –50 µA	2 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V_{CC} – 0.1		V
	I_{OH} = –2 mA	2.3 V	2			2		2		
	I_{OH} = –8 mA	3 V	2.48			2.48		2.48		
	I_{OH} = –16 mA	4.5 V	3.8			3.8		3.8		
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I_{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I_{OL} = 8 mA	3 V			0.44		0.44		0.44	
	I_{OL} = 16 mA	4.5 V			0.55		0.55		0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5		±5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20		20		20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5		5		5	µA
C_i	V_I = V_{CC} or GND	3.3 V		2.5						pF
		5 V		2.5						

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		5.6(1)	12(1)	1	14.5	1	16	ns
t_{en}	$\overline{OE}$	Y			7.8(1)	17.4(1)	1	21	1	22.5	
t_{dis}	$\overline{OE}$	Y			5.7(1)	16(1)	1	19	1	20	
t_{pd}	A	Y	C_L = 50 pF		7.9	16.8	1	18.5	1	20	ns
t_{en}	$\overline{OE}$	Y			10.1	22.2	1	25.5	1	27	
t_{dis}	$\overline{OE}$	Y			8.1	22.3	1	25.5	1	26.5	
$t_{sk(o)}$						2		2		3	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		4.1(1)	7(1)	1	8.5	1	9.5	ns
t_{en}	$\overline{OE}$	Y			5.6(1)	10.5(1)	1	12.5	1	14	
t_{dis}	$\overline{OE}$	Y			4.2(1)	10.5(1)	1	12.5	1	13.5	
t_{pd}	A	Y	C_L = 50 pF		5.8	10.5	1	12	1	13	ns
t_{en}	$\overline{OE}$	Y			7.3	14	1	16	1	17.5	
t_{dis}	$\overline{OE}$	Y			5.8	15.4	1	17.5	1	18.5	
$t_{sk(o)}$						1.5		1.5		2	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	C_L = 15 pF		3[1]	5[1]	1	6	1	7	ns
t_{en}	$\overline{OE}$	Y			4.1[1]	7.2[1]	1	8.5	1		
t_{dis}	$\overline{OE}$	Y			2.9[1]	7[1]	1	8	1	9	
t_{pd}	A	Y	C_L = 50 pF		4.2	7	1	8	1	9	ns
t_{en}	$\overline{OE}$	Y			5.3	9.2	1	10.5	1	11.5	
t_{dis}	$\overline{OE}$	Y			3.5	8.8	1	10	1	11	
$t_{sk(o)}$						1		1		1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[1]		SN74LV540A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.3			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF,	f = 10 MHz	3.3 V	10	pF
		Outputs enabled			5 V	11	

6.11 Typical Characteristics

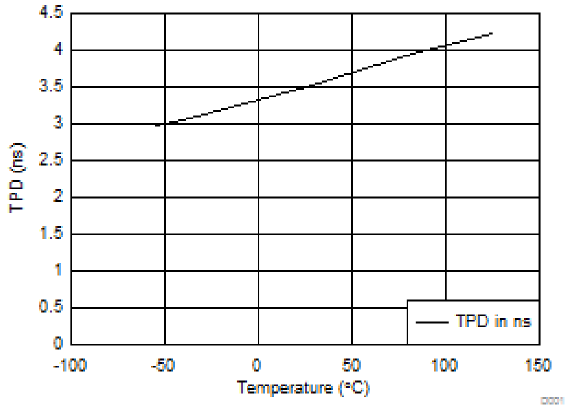


Figure 6-1. TPD vs Temperature

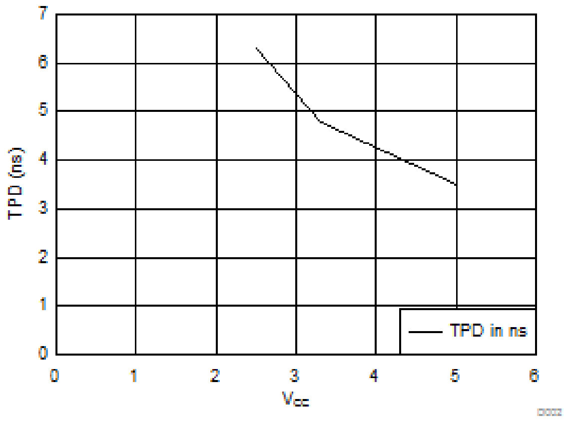
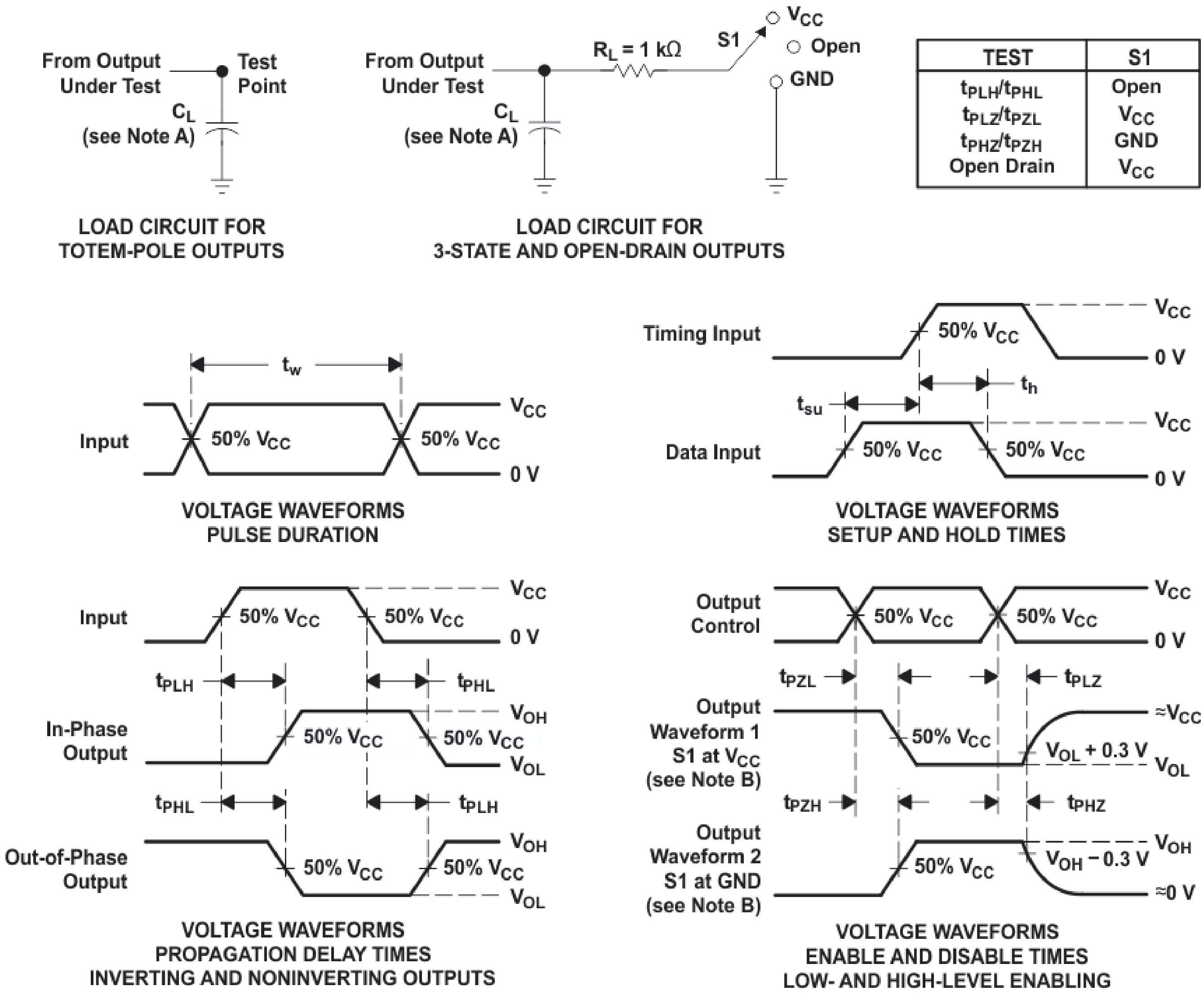


Figure 6-2. TPD vs V_{CC} at 25°C

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

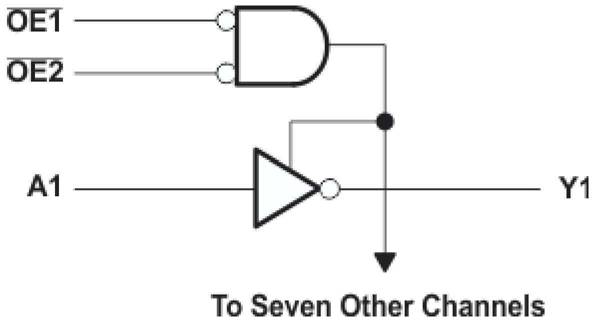
The SN74LV540A device is an octal buffer/driver designed for 2 V to 5.5 V V_{CC} operation.

This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that, if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down-voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing
- I_{off} feature
  - Allows voltages on the inputs and outputs when V_{CC} is 0 V

8.4 Device Functional Modes

Table 8-1. Function Table (Each Buffer/Driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV540A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC}. This feature makes it Ideal for translating down to the V_{CC} level. Figure 9-2 shows the reduction in ringing compared to higher drive parts such as AC.

9.2 Typical Application

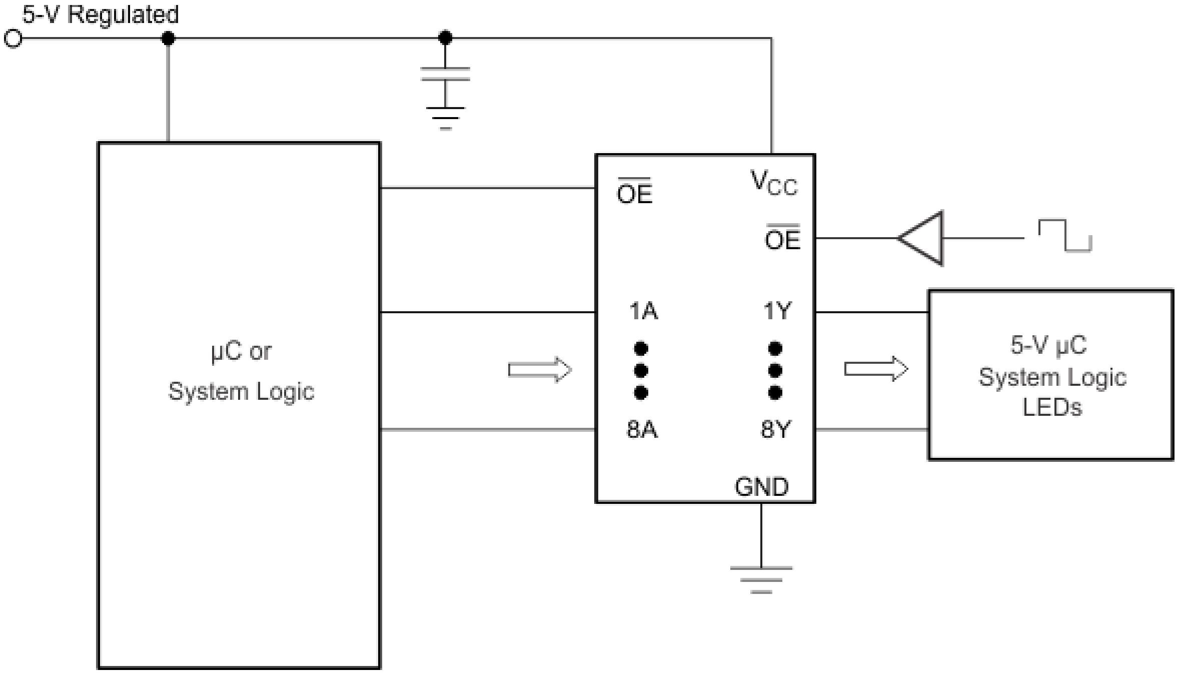


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
    - For rise time and fall time specifications, see Δt/ΔV in the *Recommended Operating Conditions* table.
    - For specified High and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
    - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
    - Load currents should not exceed 35 mA per output and 70 mA total for the part.
    - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

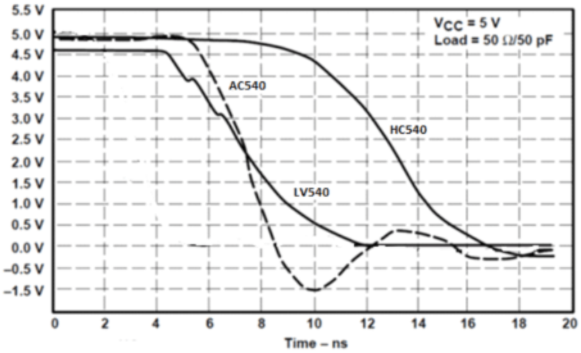


Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 9-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

9.4.2 Layout Example

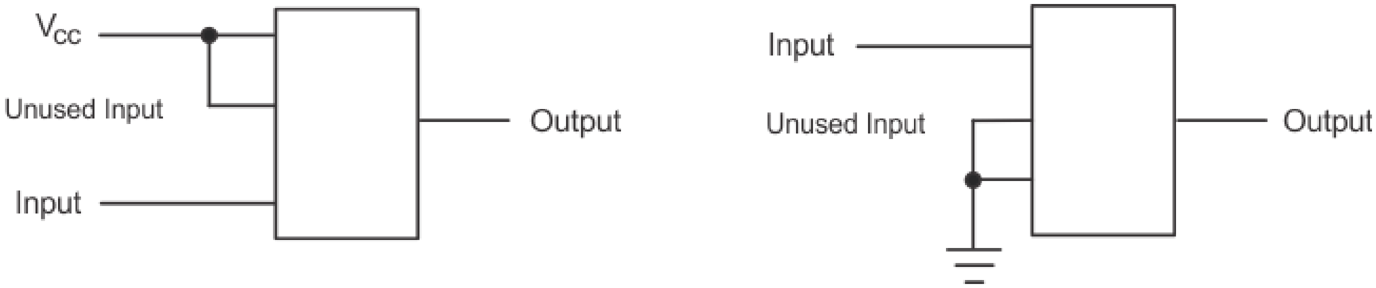


Figure 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV540A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV540ADB	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		LV540A	
SN74LV540ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A	Samples
SN74LV540ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A	Samples
SN74LV540ADW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A	
SN74LV540ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A	Samples
SN74LV540ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV540A	Samples
SN74LV540APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A	Samples
SN74LV540ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV540A	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

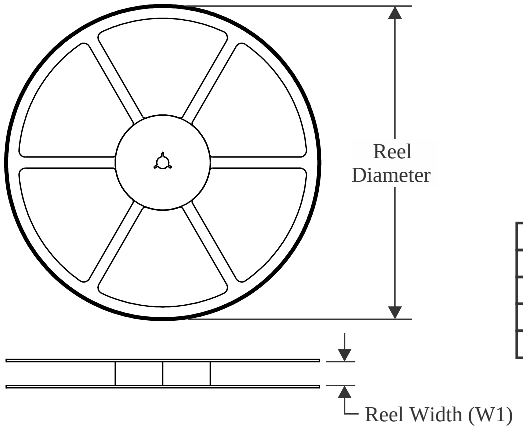
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

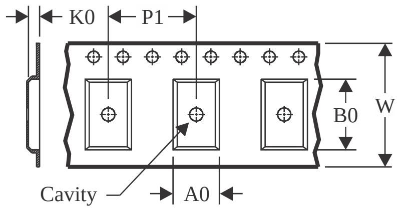
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

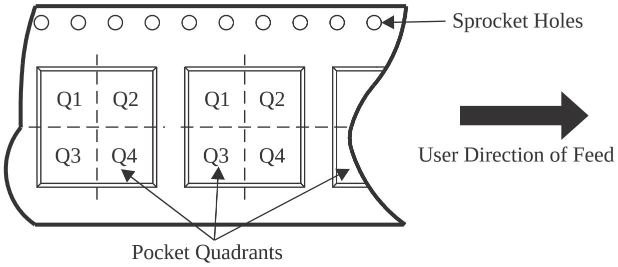


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

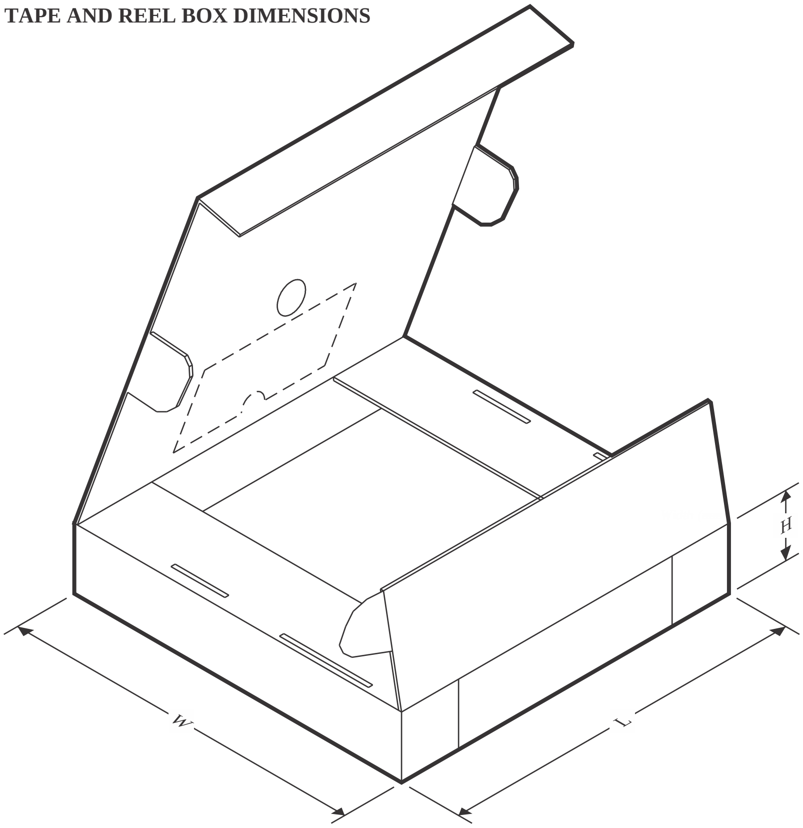
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV540ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV540ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV540ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV540ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV540APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV540ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

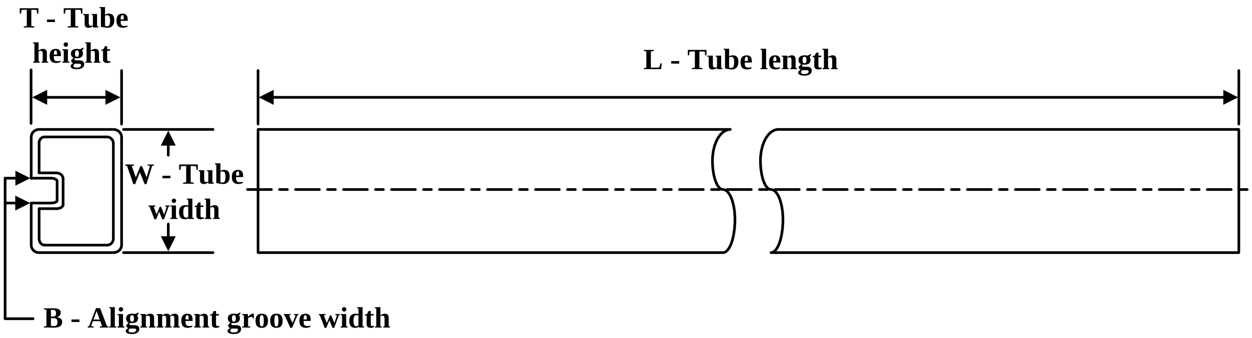
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

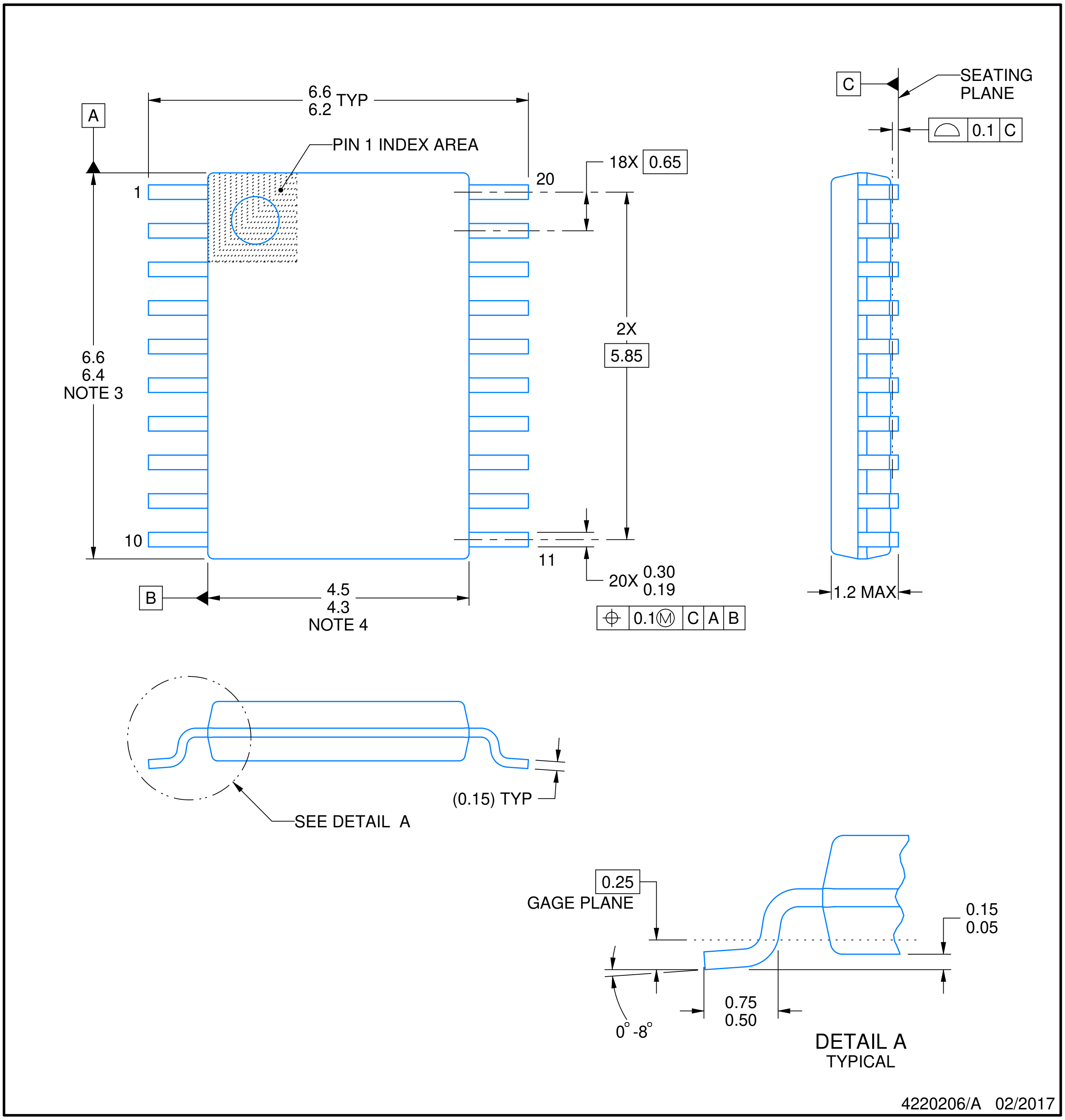
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV540ADBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74LV540ADGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74LV540ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LV540ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LV540APWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74LV540ARGYR	VQFN	RGY	20	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

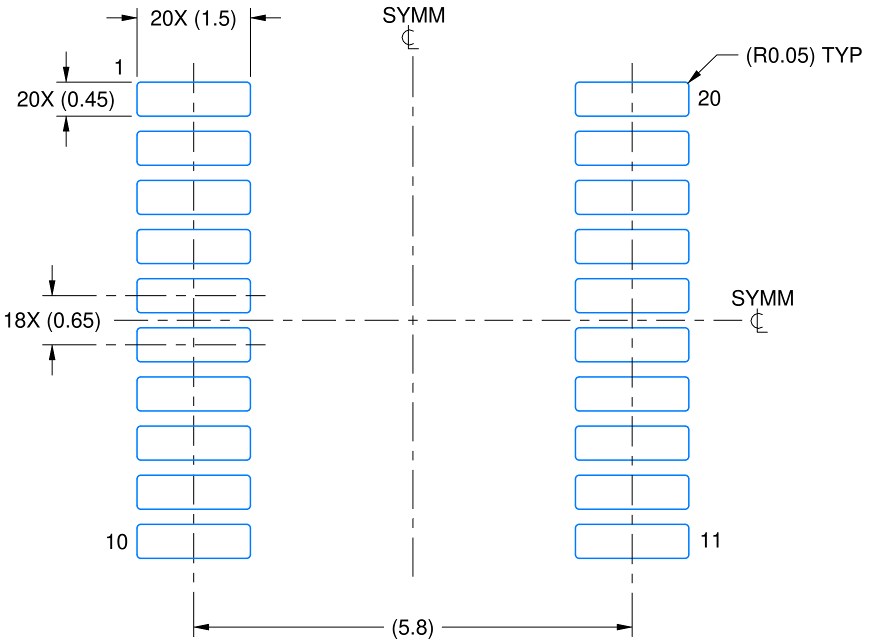
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV540ADW	DW	SOIC	20	25	507	12.83	5080	6.6



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

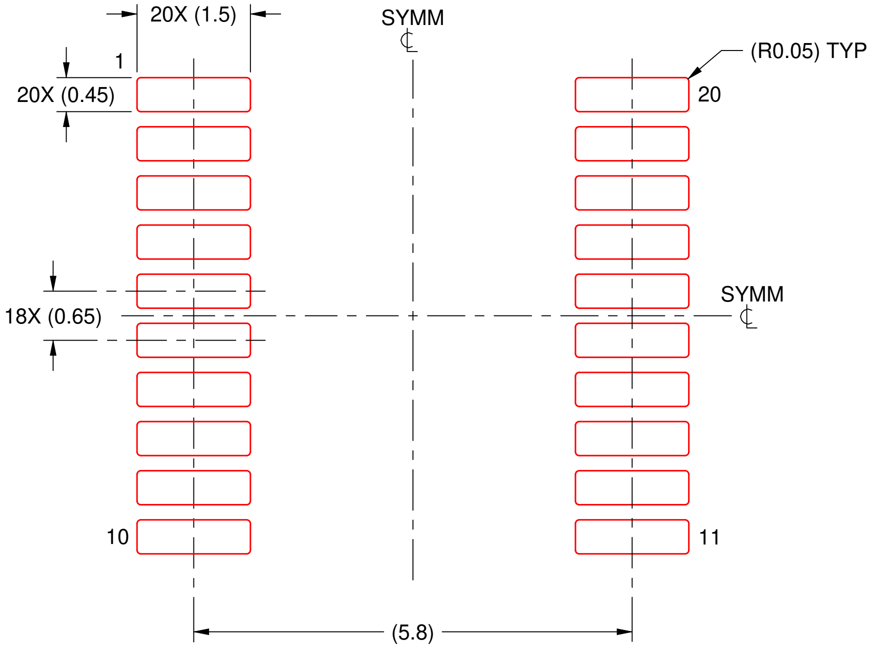
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

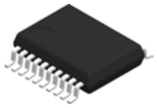


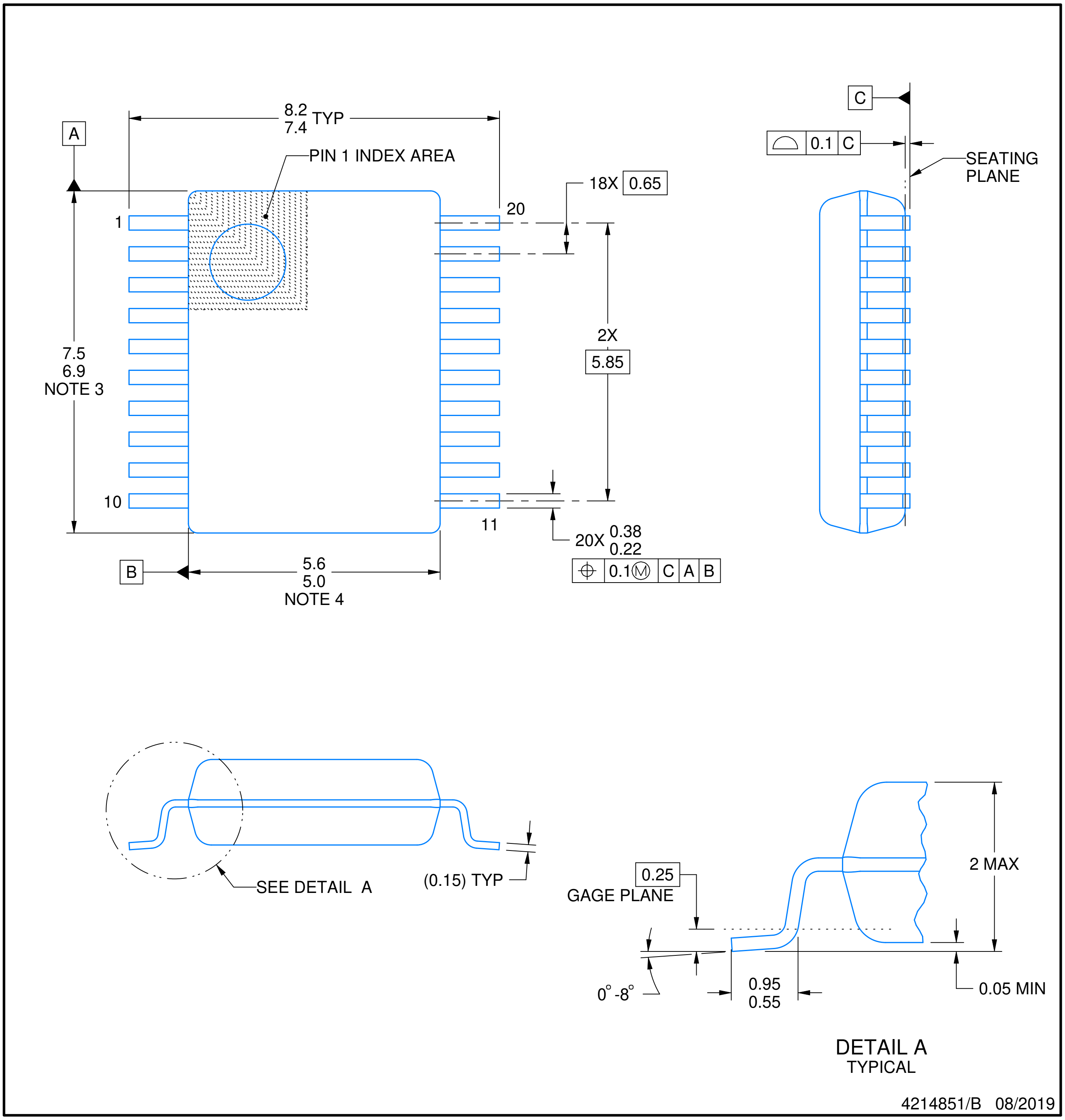
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

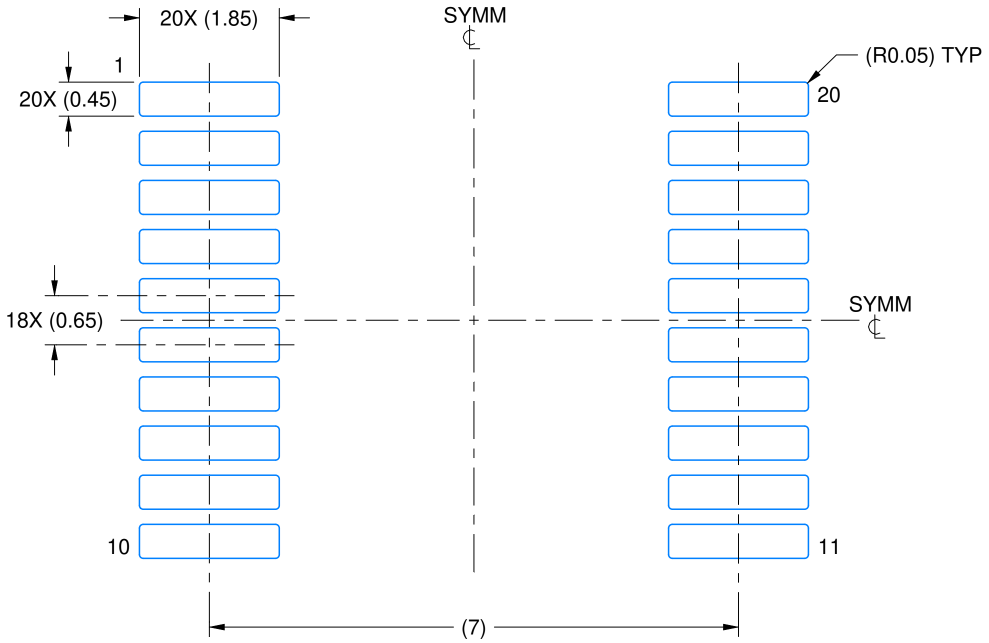
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.





NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

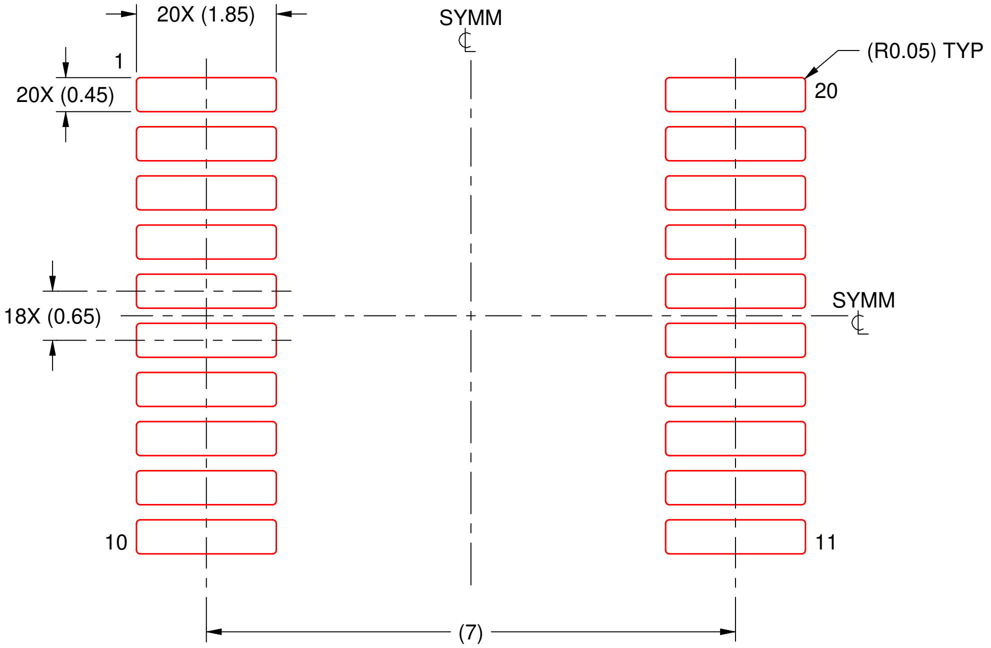
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

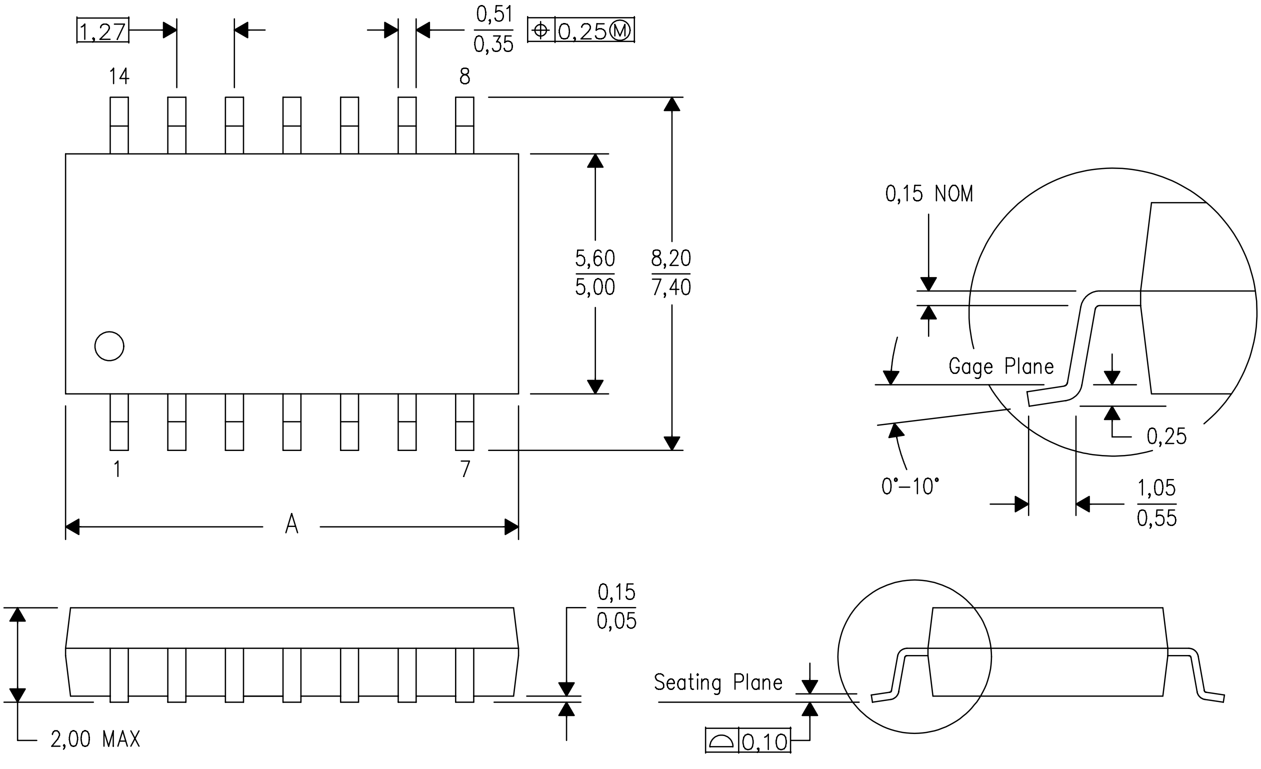
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



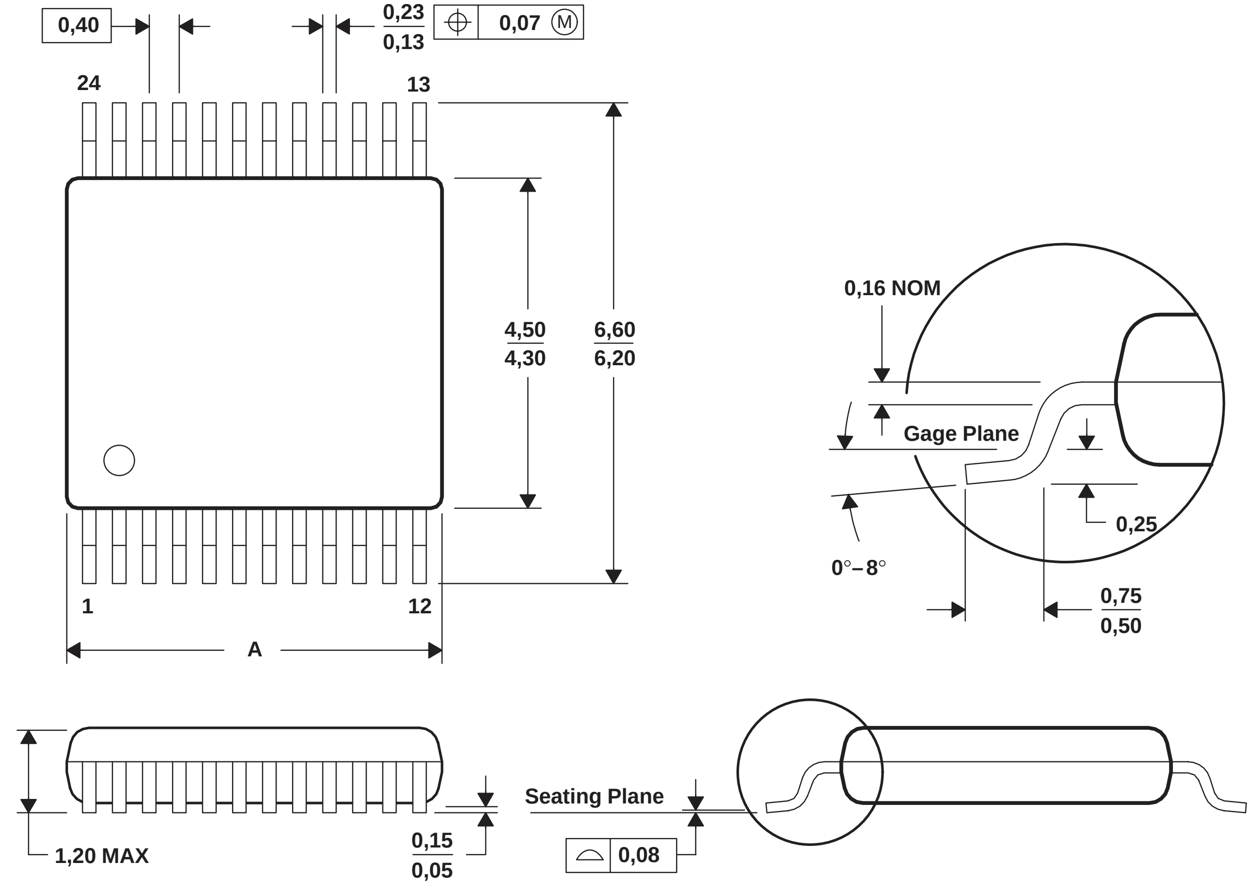
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

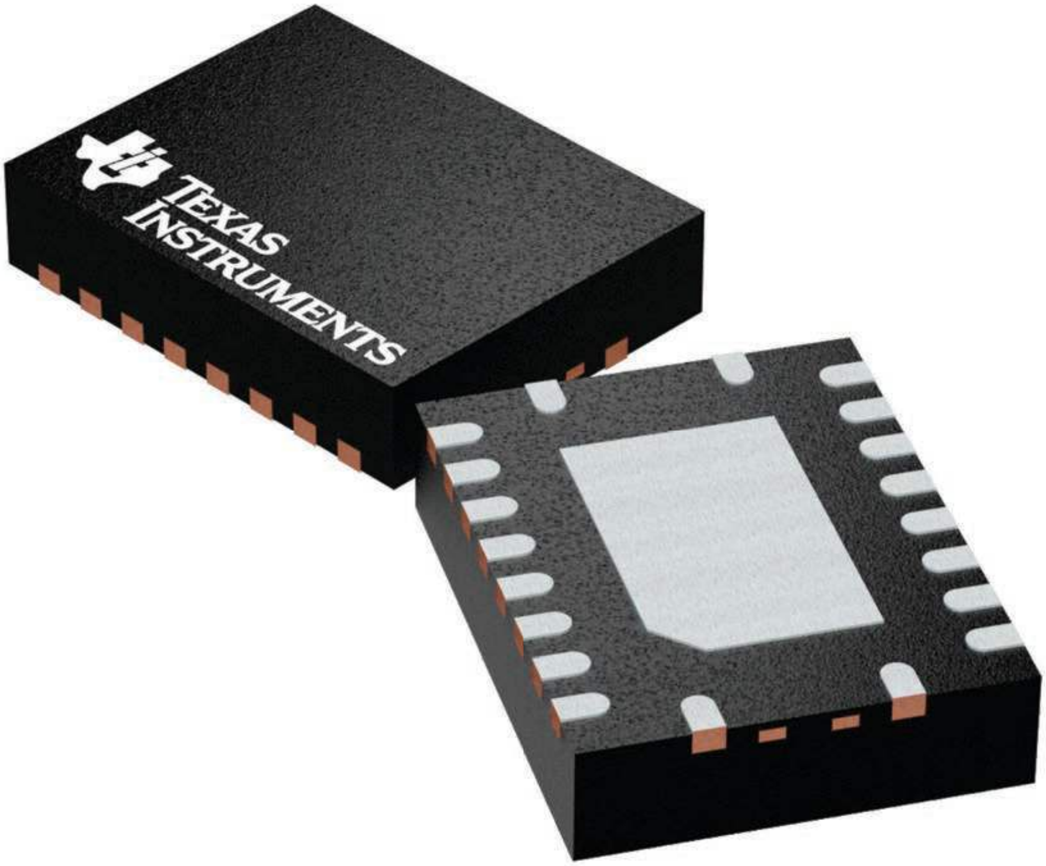
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

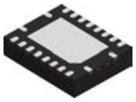
PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

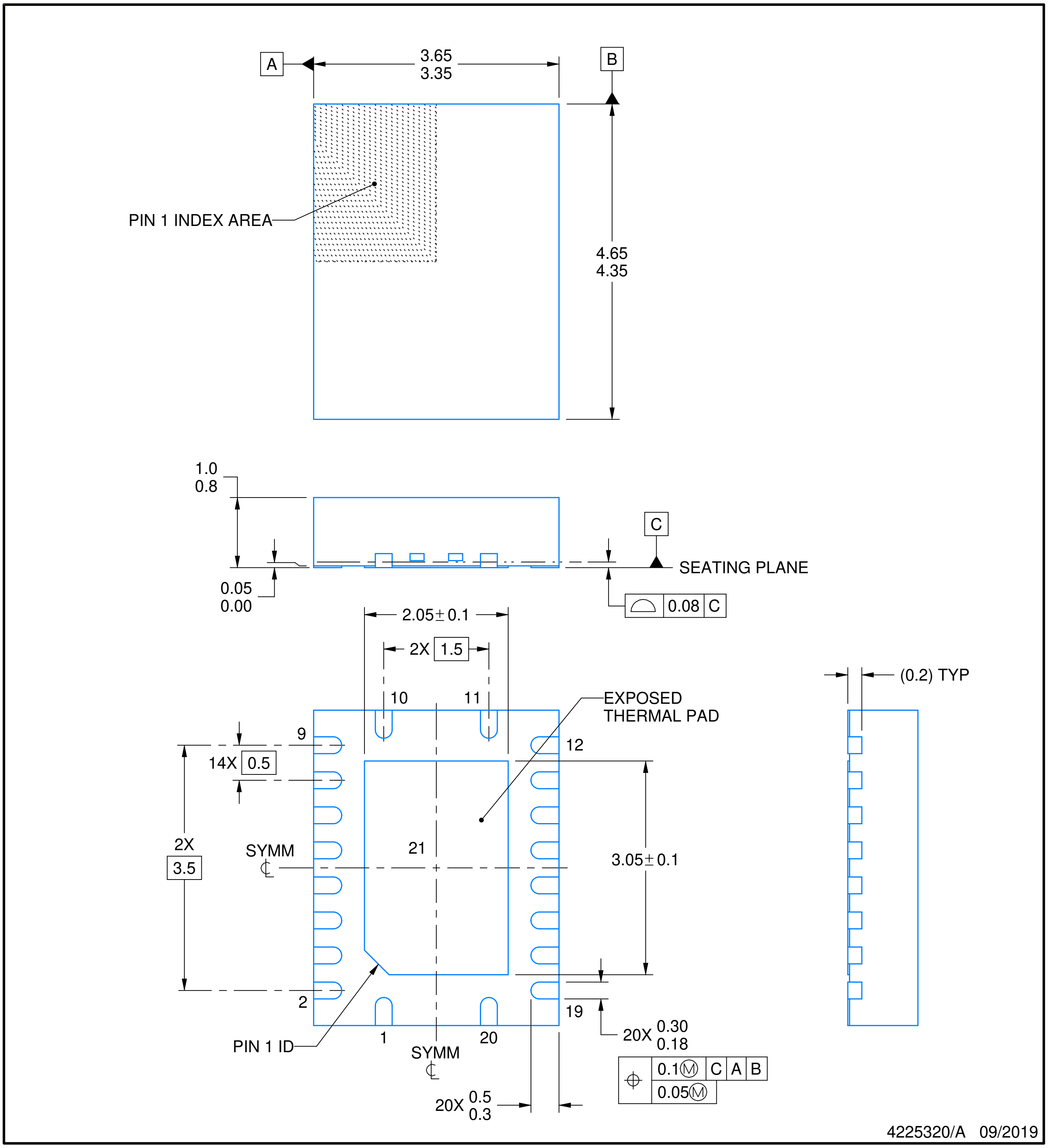
PACKAGE OUTLINE



RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

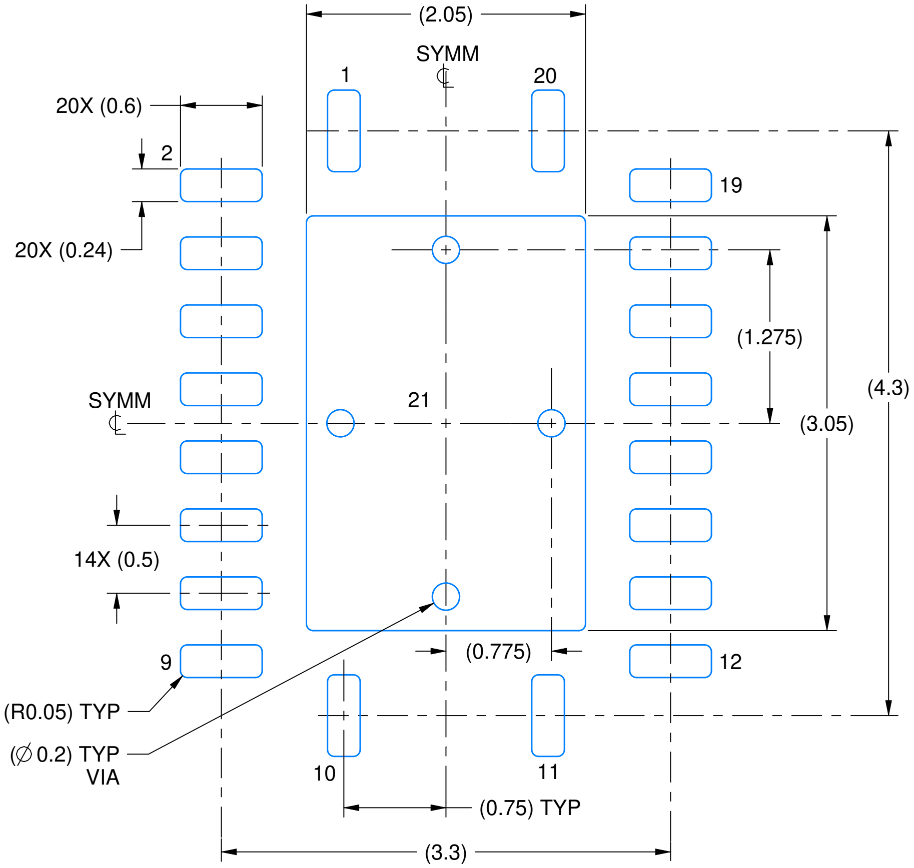


4225320/A 09/2019

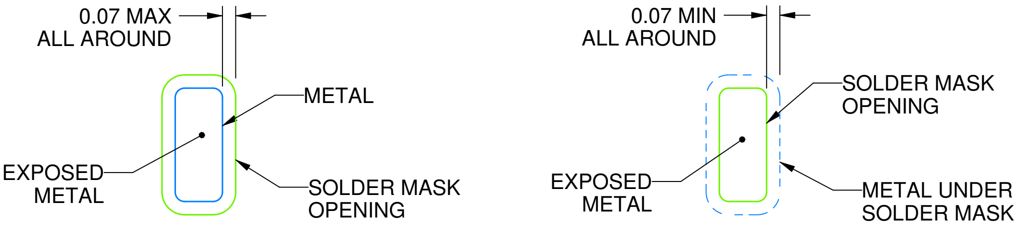
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



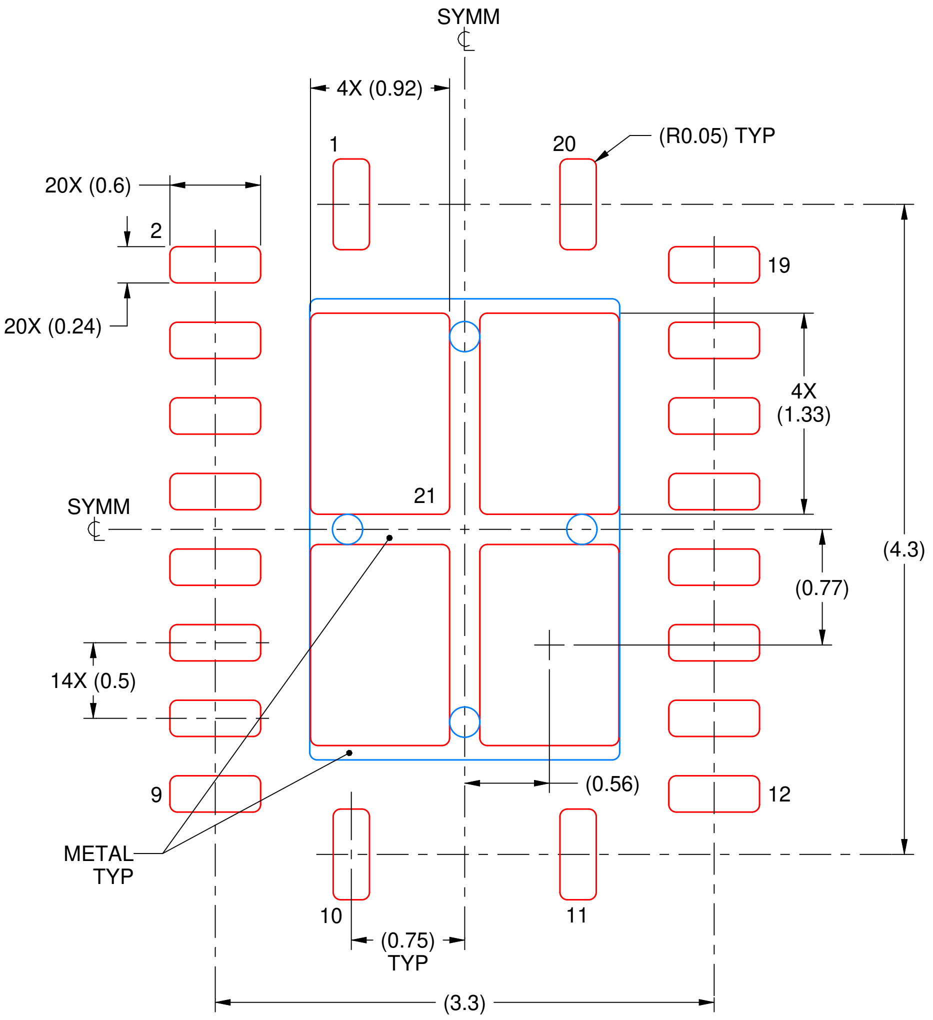
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

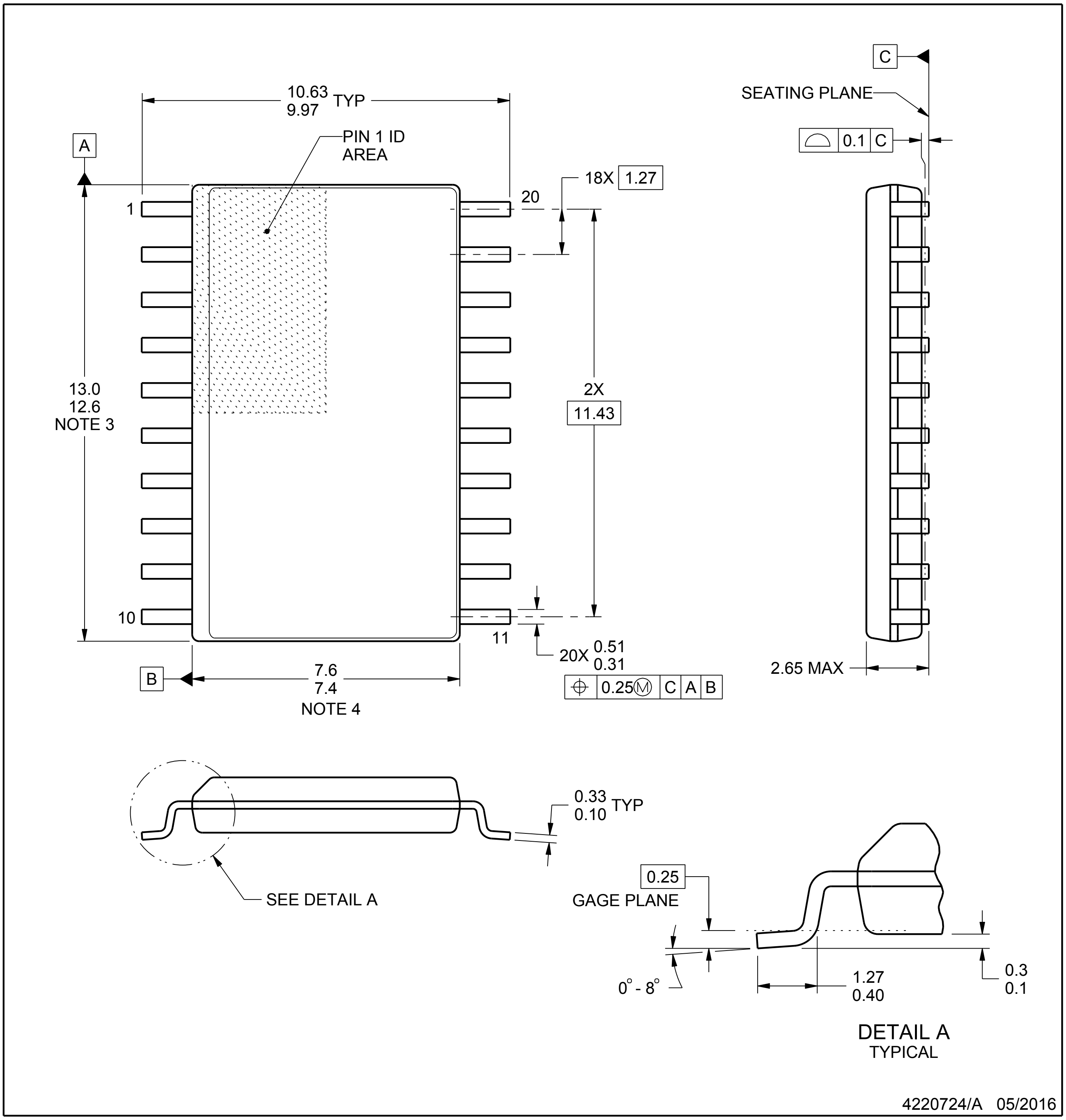
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DW0020A

SOIC - 2.65 mm max height

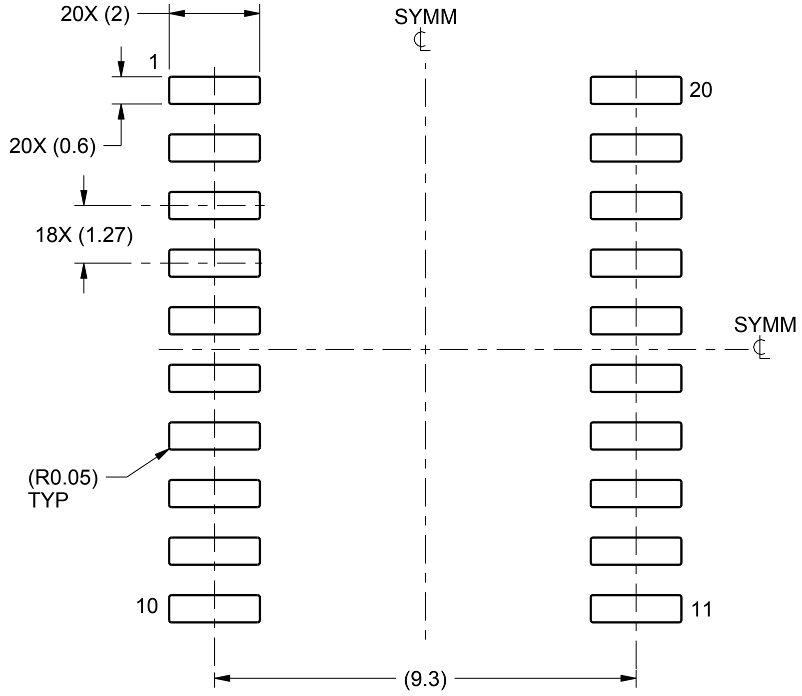
SOIC



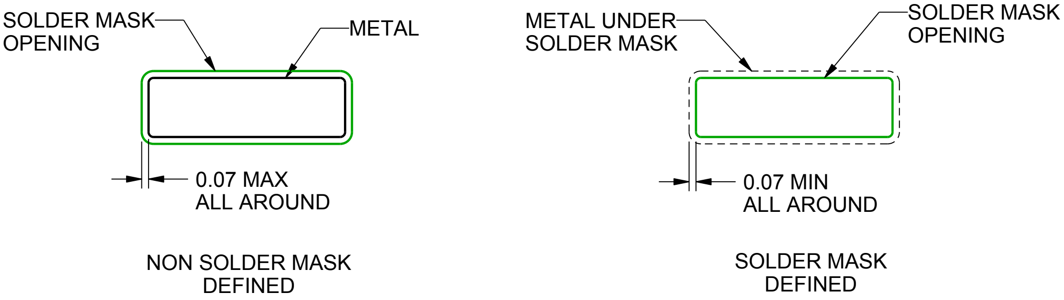
4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

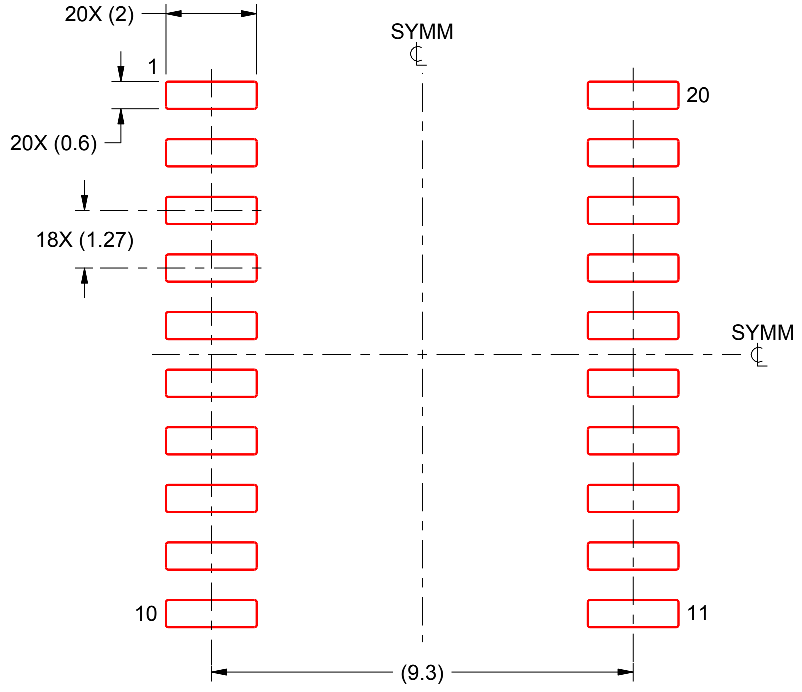


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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