Ultralow Power, 1.8 V, 3 mm × 3 mm, 2-Channel Capacitance Converter

AD7156

FEATURES

Ultralow power
- **Power supply voltage: 1.8 V to 3.6 V**
- **Operation power supply current: 70 μA typical**
- **Power-down current: 2 μA typical**

Fast response time
- **Conversion time: 10 ms per channel**
- **Wake-up time from serial interface: 300 μs**

Adaptive environmental compensation

2 capacitance input channels
- **Sensor capacitance (C_{SENS}): 0 pF up to 13 pF**
- **Sensitivity up to 3 fF**

2 modes of operation
- **Standalone with fixed settings**
- **Interfaced to a microcontroller for user-defined settings**

2 detection output flags

2-wire serial interface (I^2C-compatible)

Operating temperature: −40°C to +85°C

10-lead LFCSP package (3 mm × 3 mm × 0.8 mm)

APPLICATIONS

Buttons and switches
Proximity sensing
Contactless switching
Position detection
Level detection
Portable products

GENERAL DESCRIPTION

The AD7156 delivers a complete signal processing solution for capacitive sensors, featuring an ultralow power converter with fast response time.

The AD7156 uses an Analog Devices, Inc., capacitance-to-digital converter (CDC) technology, which combines features important for interfacing to real sensors, such as high input sensitivity and high tolerance of both input parasitic ground capacitance and leakage current.

The integrated adaptive threshold algorithm compensates for any variations in the sensor capacitance due to environmental factors like humidity and temperature or due to changes in the dielectric material over time.

By default, the AD7156 operates in standalone mode using the fixed power-up settings and indicates detection on two digital outputs. Alternatively, the AD7156 can be interfaced to a micro-controller via the serial interface, the internal registers can be programmed with user-defined settings, and the data and status can be read from the part.

The AD7156 operates with a 1.8 V to 3.6 V power supply. It is specified over the temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

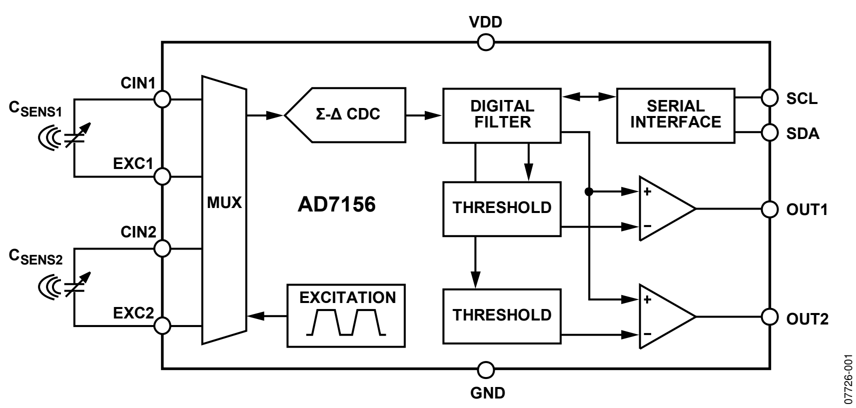

Figure 1.

Rev. 0

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REVISION HISTORY

10/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 1.8 V to 3.6 V, GND = 0 V, temperature range = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
CAPACITIVE INPUT					
Conversion Input Range, CIN to EXC[2, 3]	3.2	4		pF	4 pF input range
	1.6	2		pF	2 pF input range
	0.8	1		pF	1 pF input range
	0.4	0.5		pF	0.5 pF input range
Resolution[4, 5]		2.0		fF	4 pF input range
		1.6		fF	2 pF input range
		1.4		fF	1 pF input range
		1.0		fF	0.5 pF input range
Maximum Allowed Capacitance, CIN to GND[4, 6]		50		pF	See Figure 4, Figure 5, and Figure 6
Minimum Allowed Resistance, CIN to GND[4, 6]		10		MΩ	See Figure 10 and Figure 11
Maximum Allowed Serial Resistance[4, 6]		50		kΩ	See Figure 14
Gain Error	−20		+20	%	
Gain Deviation over Temperature[4]		0.5		%FSR	See Figure 17
Gain Matching Between Ranges[4]	−2		+2	%	
Offset Error[4]		50		fF	CIN and EXC pins disconnected
Offset Deviation over Temperature[4]		5		fF	CIN and EXC pins disconnected See Figure 16
Integral Nonlinearity (INL)[4]		0.05		%	
Channel-to-Channel Isolation[4]		60		dB	
Power Supply Rejection[4]		4		fF/V	
CAPDAC					
Full Range	10	12.5		pF	
Resolution (LSB)[4]		200		fF	
Differential Nonlinearity (DNL)[4]			0.25	LSB	
Auto-DAC Increment/Decrement[4, 7]	25		75	% of C_{IN} range	
EXCITATION					
Voltage[4, 7]		$\pm V_{DD}/2$		V	
Frequency		16		kHz	See Figure 18
Maximum Allowed Capacitance EXC to GND[4, 6]		1000		pF	See Figure 7, Figure 8, and Figure 9
Minimum Allowed Resistance EXC to GND[4, 6]		1		MΩ	See Figure 12 and Figure 13
LOGIC OUTPUTS (OUT1, OUT2)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −3 mA
Output High Voltage (V_{OH})	V_{DD} − 0.6			V	I_{SOURCE} = +3 mA
SERIAL INTERFACE INPUTS (SCL, SDA)					
Input High Voltage (V_{IH})	70			% of V_{DD}	
Input Low Voltage (V_{IL})			25	% of V_{DD}	
Input Leakage Current		±0.1	±5	µA	
Input Pin Capacitance		6		pF	
OPEN-DRAIN OUTPUT (SDA)					
Output Low Voltage (V_{OL})			0.4	V	I_{SINK} = −6.0 mA
Output High Leakage Current (I_{OH})		0.1	5	µA	$V_{OUT} = V_{DD}$

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}-to-GND Voltage	1.8		3.6	V	
I_{DD} Current[4, 8]		65	75	μA	$V_{DD} \leq 2.7$ V, see Figure 20
		70	85	μA	$V_{DD} = 3.6$ V, see Figure 20
I_{DD} Current Power-Down Mode[4, 8]		2	10	μA	$V_{DD} \leq 2.7$ V, see Figure 21
		2	17	μA	$V_{DD} = 3.6$ V, see Figure 21

[1] Capacitance units: 1 pF = 1×10^{-12} F; 1 fF = 10^{-15} F.
[2] The CAPDAC can be used to shift (offset) the input range. The total capacitance of the sensor can therefore be up to the sum of the CAPDAC value and the conversion input range. With the auto-DAC feature, the CAPDAC is adjusted automatically when the CDC input value is lower than 25% or higher than 75% of the CDC nominal input range.
[3] The maximum capacitance of the sensor connected between the EXCx and CINx pins is equal to the sum of the minimum guaranteed value of the CAPDAC and the minimum guaranteed input range.
[4] The maximum specification is not production tested but is supported by characterization data at initial product release.
[5] The resolution of the converter is not limited by the output data format or output data LSB (least significant bit) size, but by the converter and system noise level. The noise-free resolution is defined as level of peak-to-peak noise coming from the converter itself, with no connection to the CIN and EXC pins.
[6] These specifications are understood separately. Any combination of the capacitance to ground and serial resistance may result in additional errors, for example gain error, gain drift, offset error, offset drift, and power supply rejection.
[7] Specification is not production tested but is guaranteed by design.
[8] Digital inputs equal to V_{DD} or GND.

TIMING SPECIFICATIONS

V_{DD} = 1.8 V to 3.6 V, GND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = V_{DD}, temperature range = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CONVERTER					
Conversion Time[1]			20	ms	Both channels, 10 ms per channel.
Wake-Up Time from Power-Down Mode[2, 3]		0.3		ms	
Power-Up Time[2, 4]		2		ms	
Reset Time[2, 5]		2		ms	
SERIAL INTERFACE[6, 7]					See Figure 2.
SCL Frequency	0		400	kHz	
SCL High Pulse Width, t_{HIGH}	0.6			μs	
SCL Low Pulse Width, t_{LOW}	1.3			μs	
SCL, SDA Rise Time, t_R			0.3	μs	
SCL, SDA Fall Time, t_F			0.3	μs	
Hold Time (Start Condition), $t_{HD;STA}$	0.6			μs	After this period, the first clock is generated.
Setup Time (Start Condition), $t_{SU;STA}$	0.6			μs	Relevant for repeated start condition.
Data Setup Time, $t_{SU;DAT}$	0.1			μs	
Setup Time (Stop Condition), $t_{SU;STO}$	0.6			μs	
Data Hold Time (Master), $t_{HD;DAT}$	10			ns	
Bus-Free Time (Between Stop and Start Conditions), t_{BUF}	1.3			μs	

[1] Conversion time is 304 internal clock cycles for both channels (nominal clock 16 kHz); the internal clock frequency is equal to the specified excitation frequency.
[2] Specification is not production tested but is supported by characterization data at initial product release.
[3] Wake-up time is the maximum delay between the last SCL edge writing the configuration register and the start of conversion.
[4] Power-up time is the maximum delay between the V_{DD} crossing the minimum level (1.8 V) and either the start of conversion or when ready to receive a serial interface command.
[5] Reset time is the maximum delay between the last SCL edge writing the reset command and either the start of conversion or when ready to receive a serial interface command.
[6] Sample tested during initial release to ensure compliance.
[7] All input signals are specified with input rise/fall times = 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Output load = 10 pF.

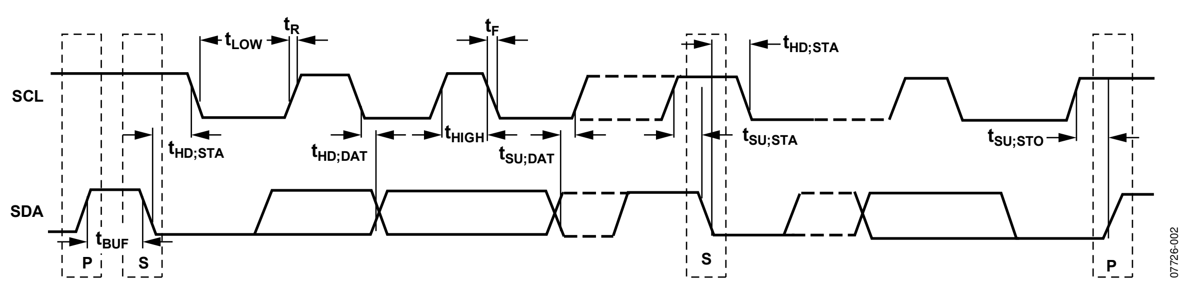


Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

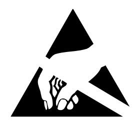
T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Positive Supply Voltage V_{DD} to GND	−0.3 V to +3.9 V
Voltage on Any Input or Output to GND	−0.3 V to V_{DD} + 0.3 V
ESD Rating	
ESD Association Human Body Model, S5.1	4 kV
Field-Inducted Charged Device Model	500 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
LFCSP Package	
θ_{JA}, Thermal Impedance to Air	49°C/W
θ_{JC}, Thermal Impedance to Case	3°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260(0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

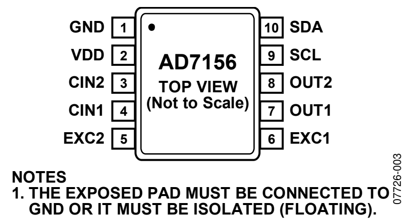


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Pin.
2	VDD	Power Supply Voltage. This pin should be decoupled to GND using a low impedance capacitor, such as a 0.1 μF X7R multilayer ceramic capacitor.
3	CIN2	CDC Capacitive Input Channel 2. The measured capacitance (sensor) is connected between the EXC2 pin and the CIN2 pin. If not used, this pin can be left open circuit or be connected to GND. When a conversion is performed on Channel 2, the CIN2 pin is internally connected to a high impedance input of the Σ-Δ modulator. When a conversion is performed on the other channel or in idle mode or power-down mode, the CIN2 pin is internally disconnected and left floating by the part.
4	CIN1	CDC Capacitive Input Channel 1. The measured capacitance (sensor) is connected between the EXC1 pin and the CIN1 pin. If not used, this pin can be left open circuit or be connected to GND. When a conversion is performed on Channel 1, the CIN1 pin is internally connected to a high impedance input of the Σ-Δ modulator. When a conversion is performed on the other channel or in idle mode or power-down mode, the CIN1 pin is internally disconnected and left floating by the part.
5	EXC2	CDC Excitation Output Channel 2. The measured capacitance is connected between the EXC2 pin and the CIN2 pin. If not used, this pin should be left as an open circuit. When a conversion is performed on Channel 2, the EXC2 pin is internally connected to the output of the excitation signal driver. When a conversion is performed on the other channel or in idle mode or power-down mode, the EXC2 pin is internally connected to GND.
6	EXC1	CDC Excitation Output Channel 1. The measured capacitance is connected between the EXC1 pin and the CIN1 pin. If not used, this pin should be left as an open circuit. When a conversion is performed on Channel 1, the EXC1 pin is internally connected to the output of the excitation signal driver. When a conversion is performed on the other channel or in idle mode or power-down mode, the EXC1 pin is internally connected to GND.
7	OUT1	Logic Output Channel 1. A high level on this output indicates proximity detected on CIN1.
8	OUT2	Logic Output Channel 2. A high level on this output indicates proximity detected on CIN2.
9	SCL	Serial Interface Clock Input. This pin connects to the master clock line and requires a pull-up resistor if not provided elsewhere in the system.
10	SDA	Serial Interface Bidirectional Data. This pin connects to the master data line and requires a pull-up resistor if not provided elsewhere in the system.

TYPICAL PERFORMANCE CHARACTERISTICS

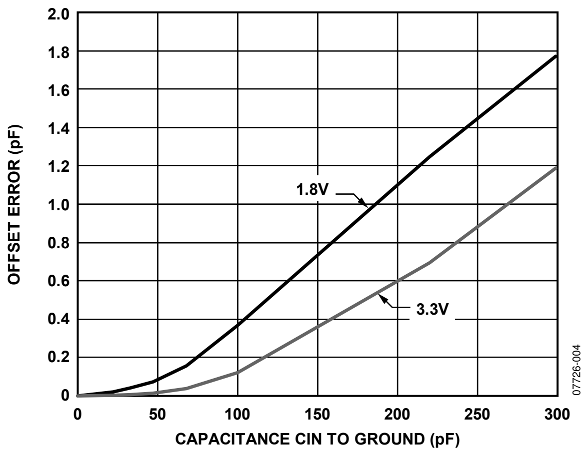


Figure 4. Capacitance Input Offset Error vs. Capacitance CIN to GND, V_{DD} = 1.8 V and 3.3 V, EXC Pin Open Circuit

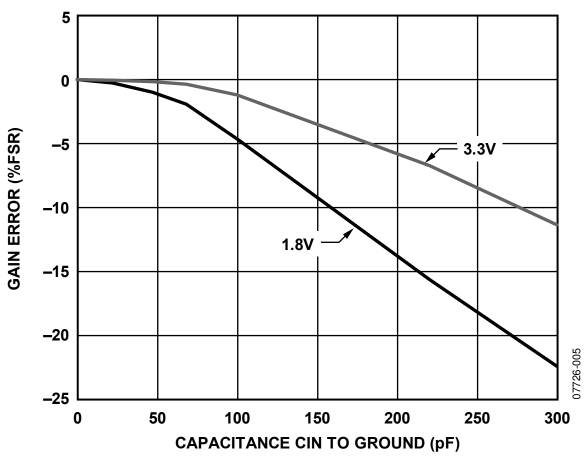


Figure 5. Capacitance Input Gain Error vs. Capacitance CIN to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

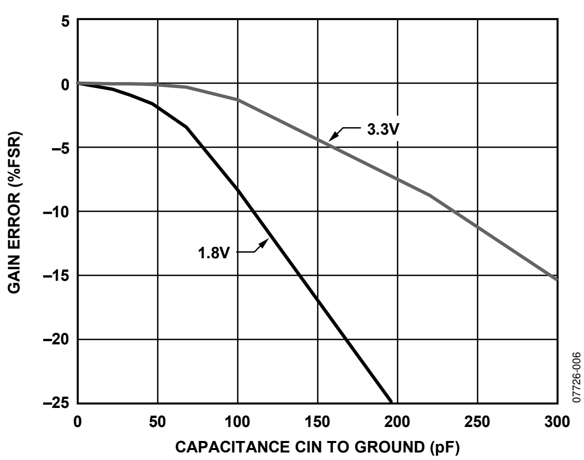


Figure 6. Capacitance Input Gain Error vs. Capacitance CIN to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 9 pF

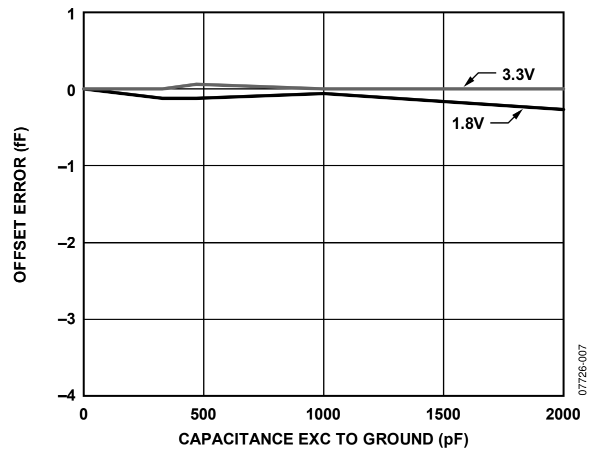


Figure 7. Capacitance Input Offset Error vs. Capacitance EXC to GND, V_{DD} = 1.8 V and 3.3 V, CIN Pin Open Circuit

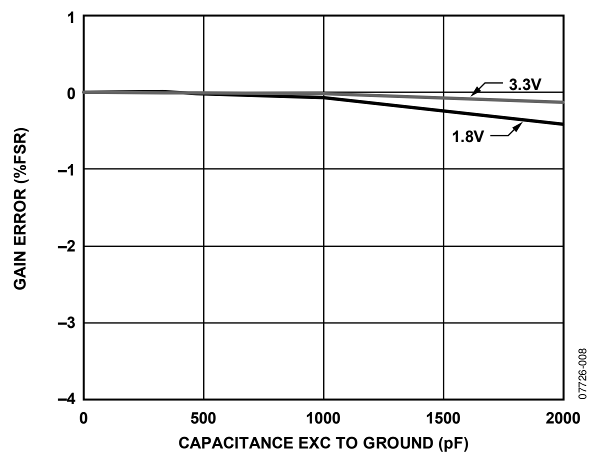


Figure 8. Capacitance Input Gain Error vs. Capacitance EXC to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

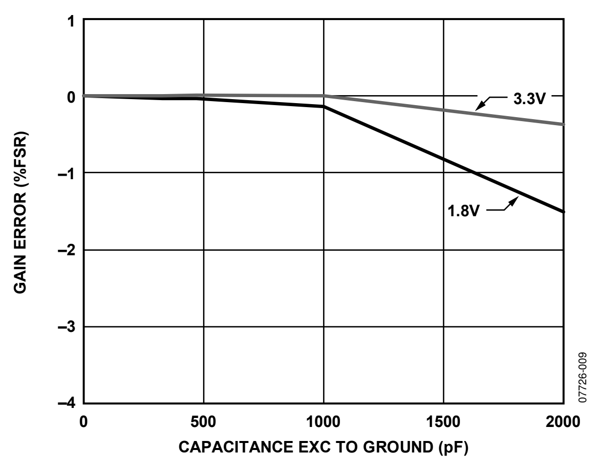


Figure 9. Capacitance Input Gain Error vs. Capacitance EXC to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 9 pF

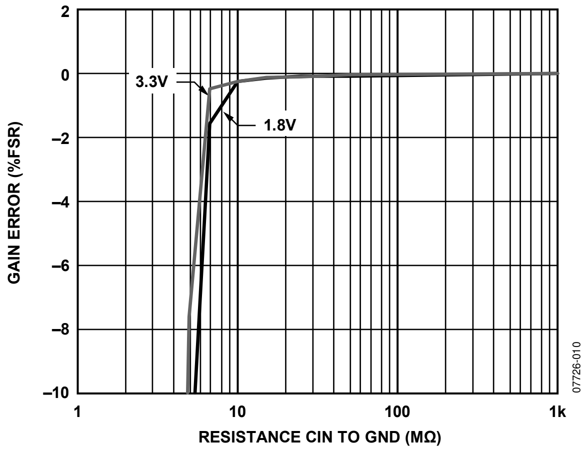


Figure 10. Capacitance Input Gain Error vs. Resistance CIN to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

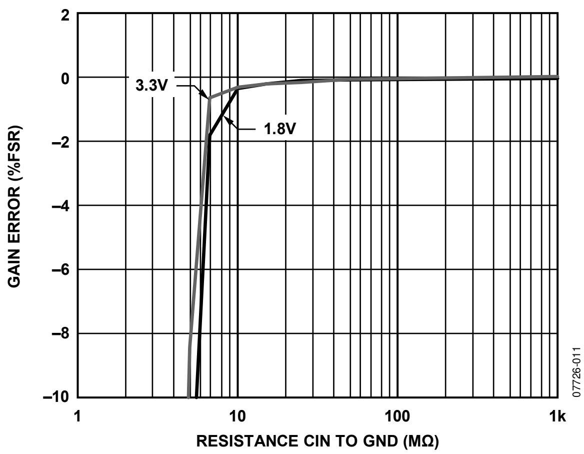


Figure 11. Capacitance Input Gain Error vs. Resistance CIN to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 9 pF

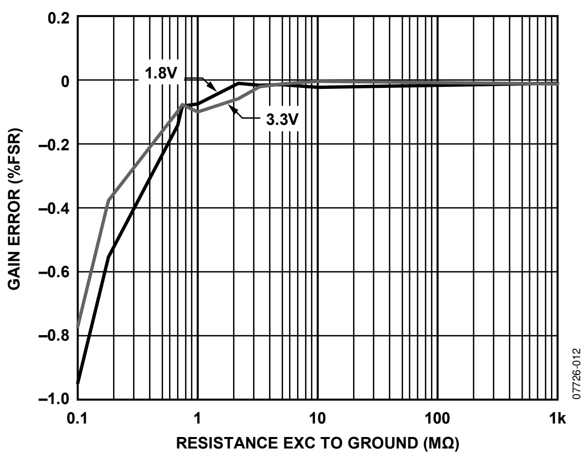


Figure 12. Capacitance Input Gain Error vs. Resistance EXC to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

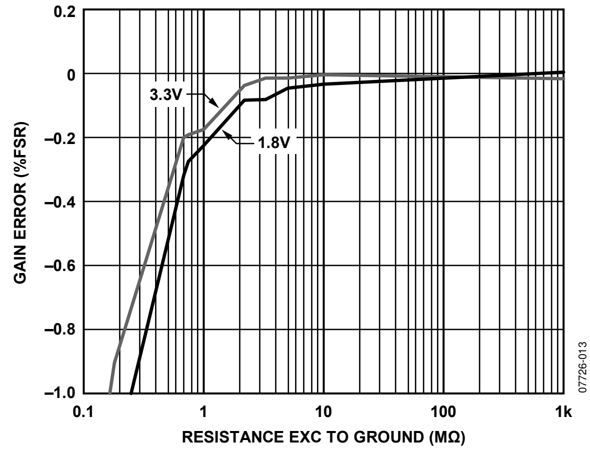


Figure 13. Capacitance Input Gain Error vs. Resistance EXC to GND, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 9 pF

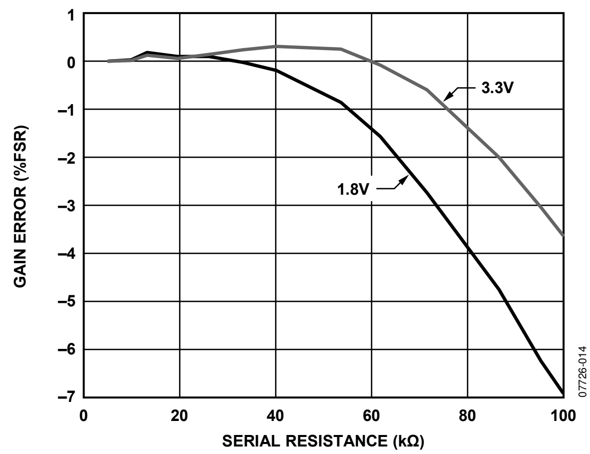


Figure 14. Capacitance Input Gain Error vs. Serial Resistance, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

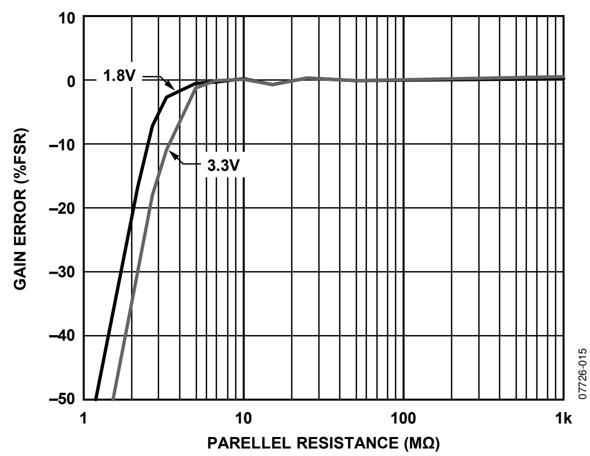


Figure 15. Capacitance Input Gain Error vs. Parallel Resistance, V_{DD} = 1.8 V and 3.3 V, CIN to EXC = 3 pF

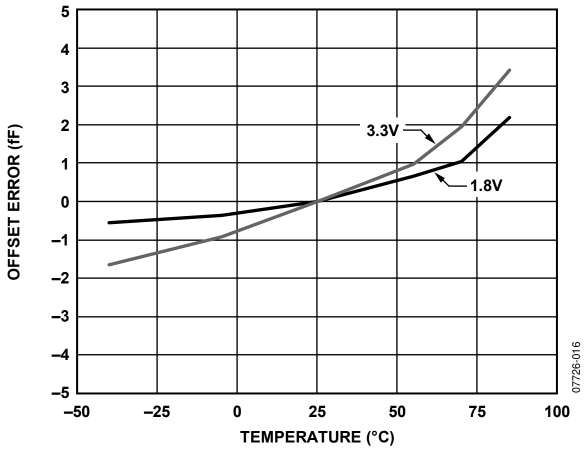


Figure 16. Capacitance Input Offset Error vs. Temperature, V_{DD} = 1.8 V and 3.3 V, CIN and EXC Pins Open Circuit

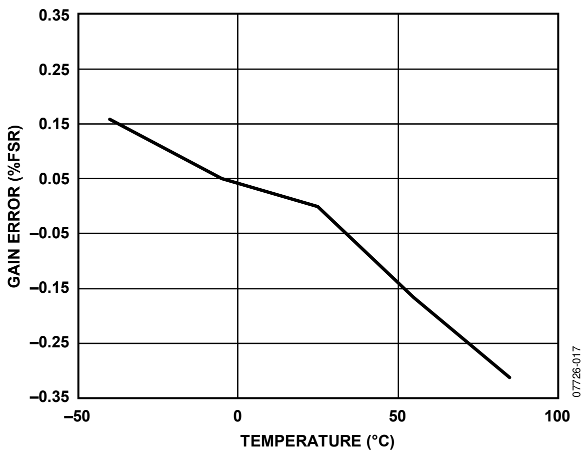


Figure 17. Capacitance Input Gain Error vs. Temperature, V_{DD} = 2.7 V, CIN to EXC = 4 pF

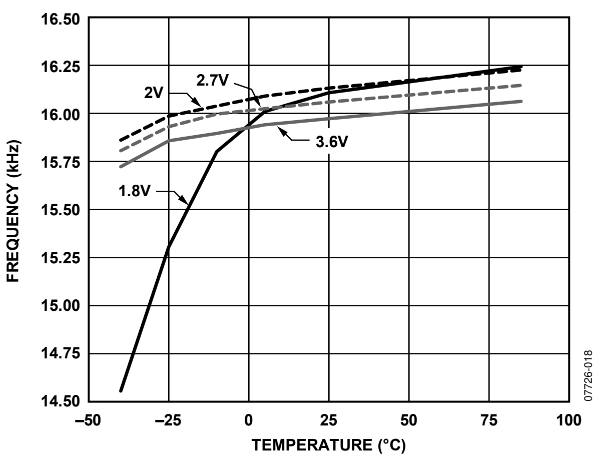


Figure 18. EXC Frequency Error vs. Temperature, V_{DD} = 1.8 V, 2 V, 2.7 V, and 3.6 V

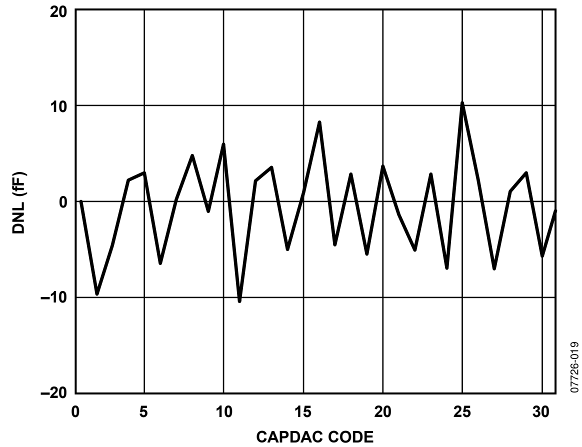


Figure 19. CAPDAC Differential Nonlinearity (DNL), V_{DD} = 1.8 V

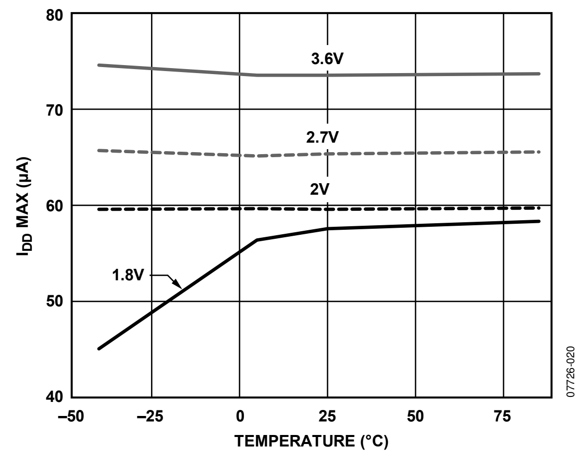


Figure 20. Current vs. Temperature, V_{DD} = 1.8 V, 2 V, 2.7 V, and 3.6 V

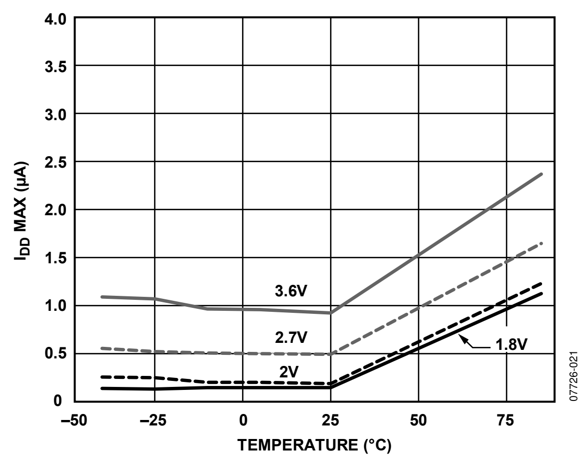


Figure 21. Power-Down Current vs. Temperature, V_{DD} = 1.8 V, 2 V, 2.7 V, and 3.6 V

THEORY OF OPERATION

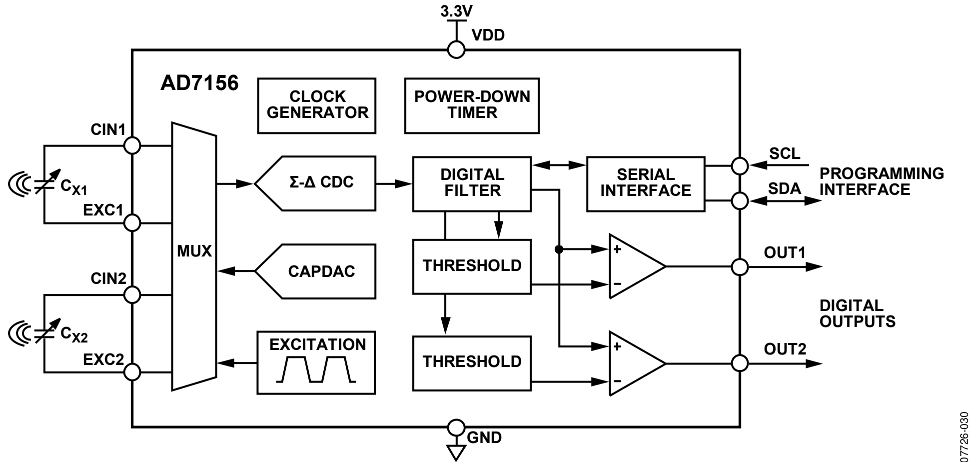


Figure 22. AD7156 Block Diagram

The AD7156 core is a high performance capacitance-to-digital converter (CDC) that allows the part to be interfaced directly to a capacitive sensor.

The comparators compare the CDC results with thresholds, either fixed or dynamically adjusted by the on-chip adaptive threshold algorithm engine. Thus, the outputs indicate a defined change in the input sensor capacitance.

The AD7156 also integrates an excitation source, CAPDAC for the capacitive inputs, an input multiplexer, a complete clock generator, a power-down timer, a power supply monitor, control logic, and an I²C®-compatible serial interface for configuring the part and accessing the internal CDC data and status, if required in the system (see Figure 22).

CAPACITANCE-TO-DIGITAL CONVERTER

Figure 23 shows the CDC simplified functional diagram. The converter consists of a second-order Σ-Δ charge balancing modulator and a third-order digital filter. The measured capacitance C_X is connected between an excitation source and the Σ-Δ modulator input. The excitation signal is applied on the C_X capacitor during the conversion, and the modulator continuously samples the charge going through the C_X. The digital filter processes the modulator output, which is a stream of 0s and 1s containing the information in 0 and 1 density. The data is processed by the adaptive threshold engine and output comparators; the data can also be read through the serial interface.

The AD7156 is designed for floating capacitive sensors. Therefore, both C_X plates have to be isolated from ground or any other fixed potential node in the system.

The AD7156 features slew rate limiting on the excitation voltage output, which decreases the energy of higher harmonics on the excitation signal and dramatically improves the system electromagnetic compatibility (EMC).

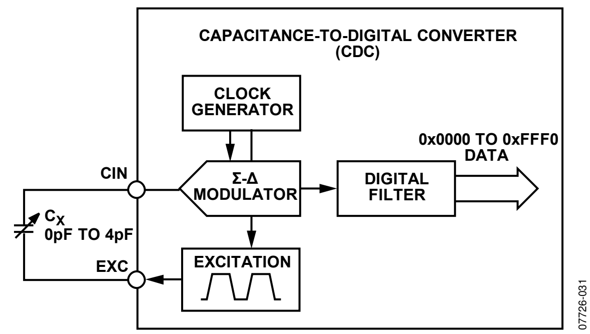


Figure 23. CDC Simplified Block Diagram

CAPDAC

The AD7156 CDC core maximum full-scale input range is 0 pF to 4 pF. However, the part can accept a higher input capacitance, caused, for example, by a nonchanging offset capacitance of up to 10 pF. This offset capacitance can be compensated for by using the programmable on-chip CAPDAC.

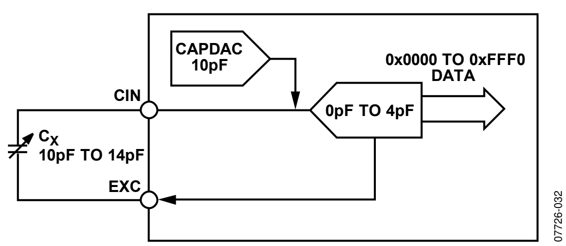


Figure 24. Using a CAPDAC

The CAPDAC can be understood as a negative capacitance connected internally to a CIN pin. The CAPDAC has a 6-bit resolution and a monotonic transfer function. Figure 24 shows how to use the CAPDAC to shift the CDC 0 pF to 4 pF input range to measure capacitance between 10 pF and 14 pF.

COMPARATOR AND THRESHOLD MODES

The AD7156 comparators and their thresholds can be programmed to operate in two modes: fixed and adaptive threshold modes. In an adaptive mode, the threshold is dynamically adjusted and the comparator output indicates fast changes and ignores slow changes in the input (sensor) capacitance. Alternatively, the threshold can be programmed as a constant (fixed) value, and the output then indicates any change in the input capacitance that crosses the defined fixed threshold.

The AD7156 logic output (active high) indicates either a positive or a negative change in the input capacitance, in both adaptive and fixed threshold modes (see Figure 25 and Figure 26).

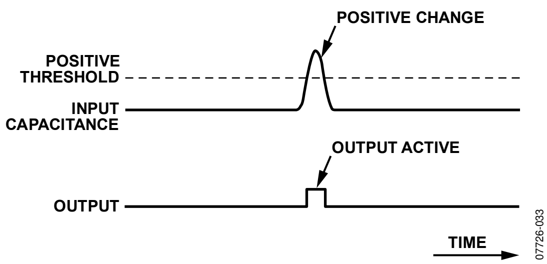


Figure 25. Positive Threshold Mode Indicates Positive Change in Input Capacitance

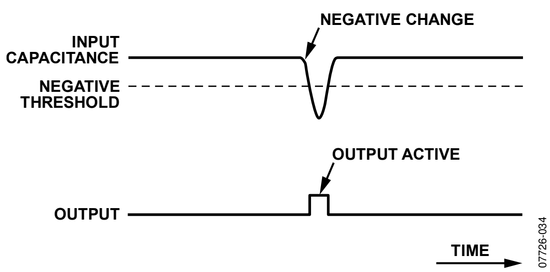


Figure 26. Negative Threshold Mode Indicates Negative Change in Input Capacitance

Additionally, for the adaptive mode only, the comparators can work as window comparators, indicating input either inside or outside a selected sensitivity band (see Figure 27 and Figure 28).

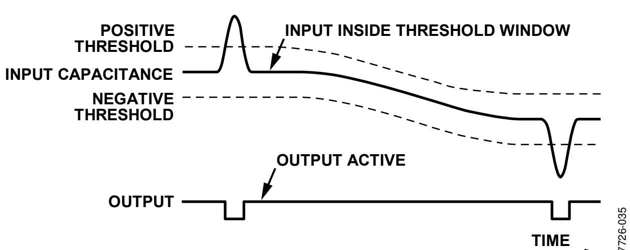


Figure 27. In-Window (Adaptive) Threshold Mode

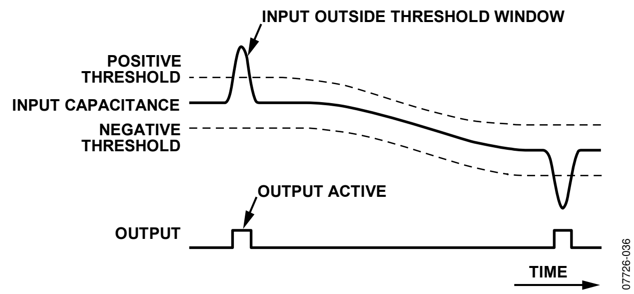


Figure 28. Out-Window (Adaptive) Threshold Mode

ADAPTIVE THRESHOLD

In an adaptive mode, the thresholds are dynamically adjusted, ensuring indication of fast changes (for example, an object moving close to a capacitive proximity sensor) and eliminating slow changes in the input (sensor) capacitance, usually caused by environment changes such as humidity or temperature or changes in the sensor dielectric material over time (see Figure 29).

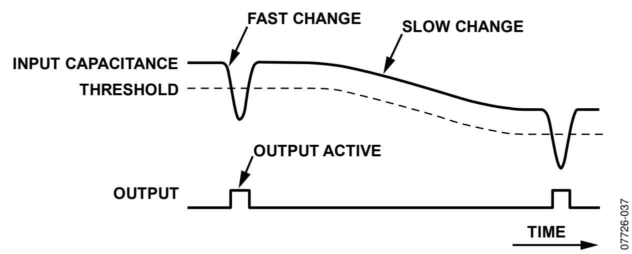


Figure 29. Adaptive Threshold Indicates Fast Changes and Eliminates Slow Changes in Input Capacitance

SENSITIVITY

In adaptive threshold mode, the output comparator threshold is set as a defined distance (sensitivity) above the data average, below the data average, or both, depending on the selected threshold mode of operation (see Figure 30). The sensitivity value is programmable in the range of 0 LSB to 255 LSB of the 12-bit CDC converter (see the Register Descriptions section).

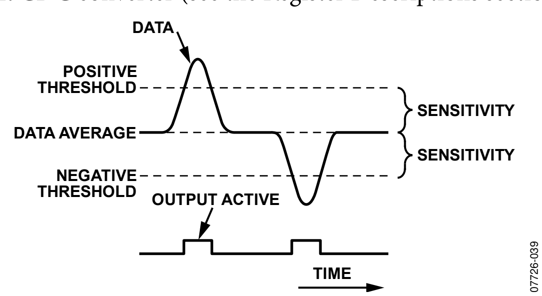


Figure 30. Threshold Sensitivity

DATA AVERAGE

The adaptive threshold algorithm is based on an average calculated from the previous CDC output data, using the following equation:

$$Average(N) = Average(N-1) + \frac{Data(N) - Average(N-1)}{2^{ThrSettling\ +\ 1}}$$

where:
Average(*N*) is the new average value.
Average(*N* – *1*) is the average value from the previous cycle.
Data(N) is the latest complete CDC conversion result.
ThrSettling is a parameter, programmable in the setup registers.

A more specific case of the input capacitance waveform is a step change. The response of the average to an input capacitance step change (more exactly, response to a step change in the CDC output data) is an exponential settling curve, which can be characterized by the following equation:

$$Average(N) = Average(0) + Change(1 - e^{N / TimeConst})$$

where:
Average(*N*) is the value of average N complete CDC conversion cycles after a step change on the input.
Average(0) is the value before the step change.
$TimeConst = 2^{(ThrSettling + 1)}$
ThrSettling is a parameter, programmable in the setup registers.

See Figure 31 and the Register Descriptions section for further information.

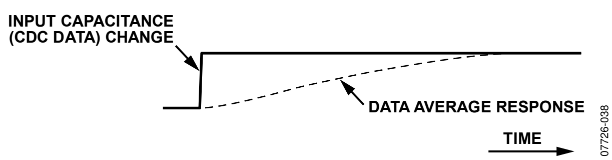


Figure 31. Data Average Response to Data Step Change

HYSTERESIS

In adaptive threshold mode, the comparator features hysteresis. The hysteresis is fixed to ¼ of the threshold sensitivity and can be programmed on or off. The comparator does not have hysteresis in the fixed threshold mode.

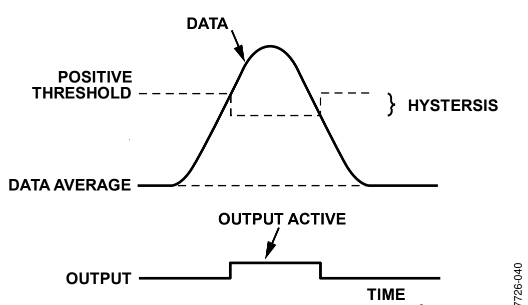


Figure 32. Threshold Hysteresis

TIMEOUT

In the case of a large, long change in the capacitive input, when the data average adapting to a new condition takes too long, a timeout can be set.

The timeout becomes active (counting) when the CDC data goes outside the band of data average ± sensitivity. When the timeout elapses (a defined number of CDC conversions is counted), the data average (and thus the thresholds), is forced to follow the new CDC data value immediately (see Figure 33).

The timeout can be set independently for approaching (for change in data toward the threshold) and for receding (for change in data away from the threshold). See Figure 34, Figure 35, and the Register Descriptions section for further information.

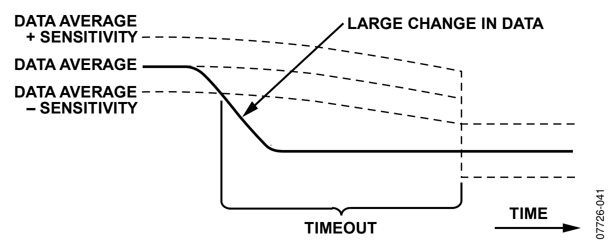


Figure 33. Threshold Timeout After a Large Change in CDC Data

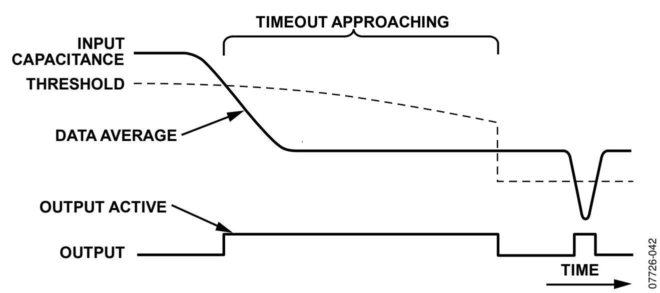


Figure 34. Approaching Timeout in Negative Threshold Mode Shortens False Output Trigger

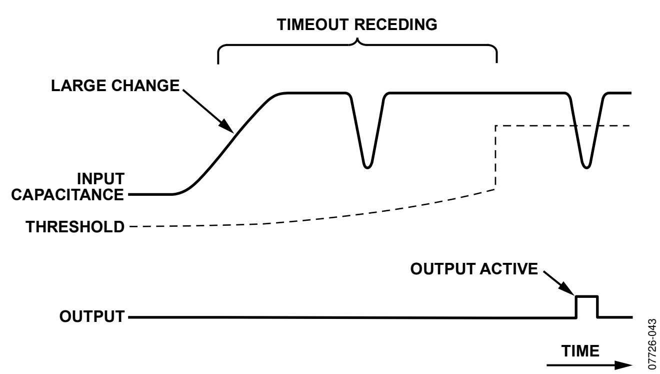


Figure 35. Positive Timeout in Negative Threshold Mode Shortens Period of Missing Output Trigger

AUTO-DAC ADJUSTMENT

In adaptive threshold mode, the part can dynamically adjust the CAPDAC to keep the CDC in an optimal operating capacitive range. When the auto-DAC function is enabled, the CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range (average > 0xA800), and the CAPDAC value is decremented when the data average goes below ¼ of the CDC full range (average < 0x5800). The auto-DAC increment or decrement step depends on the selected CDC capacitive input range (see the Setup Registers section).

When the CAPDAC value reaches 0, the ¼ threshold for further decrementing is ignored. Similarly, when the CAPDAC value reaches its full range, the ¾ threshold is ignored. The CDC and the rest of the algorithm are continuously working, and they are functional down to a capacitance input of 0 pF or as high as the capacitance input of (CAPDAC full range + CDC full range), respectively.

POWER-DOWN TIMER

In power sensitive applications, the AD7156 can be set to automatically enter power-down mode after a programmed period of time in which the outputs have not been activated. The AD7156 can then be returned to a normal operational mode either via the serial interface or by the power supply off/on sequence.

REGISTER DESCRIPTIONS

Table 5. Register Summary[1]

	Addr Pointer										
Register	**Dec**	**Hex**	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Status	0	0x00	R	PwrDown (0)	$\overline{\text{DacStep2}}$ (1)	OUT2 (0)	$\overline{\text{DacStep1}}$ (1)	OUT1 (0)	C1/C2 (0)	$\overline{\text{RDY2}}$ (1)	$\overline{\text{RDY1}}$ (1)
Ch 1 Data High	1	0x01	R	0x00							
Ch 1 Data Low	2	0x02	R	0x00							
Ch 2 Data High	3	0x03	R	0x00							
Ch 2 Data Low	4	0x04	R	0x00							
Ch 1 Average High	5	0x05	R	0x00							
Ch 1 Average Low	6	0x06	R	0x00							
Ch 2 Average High	7	0x07	R	0x00							
Ch 2 Average Low	8	0x08	R	0x00							
Ch 1 Sensitivity/ Ch 1 Threshold High	9	0x09	R/W	Ch 1 sensitivity (in adaptive threshold mode)/Ch 1 threshold high byte (in fixed threshold mode) 0x08							
Ch 1 Timeout/ Ch 1 Threshold Low	10	0x0A	R/W	Ch 1 timeout (in adaptive threshold mode)/CH 1threshold low byte (in fixed threshold mode) 0x86							
Ch 1 Setup	11	0x0B	R/W	RngH1 (0)	RngL1 (0)	(0)	$\overline{\text{Hyst1}}$ (0)	ThrSettling1 (4-bit value) (0x0B)			
Ch 2 Sensitivity/ Ch 2 Threshold High	12	0x0C	R/W	Ch 2 sensitivity (in adaptive threshold mode)/Ch 2 threshold high byte (in fixed threshold mode) 0x08							
Ch 2 Timeout/ Ch 2 Threshold Low	13	0x0D	R/W	Ch 2 timeout (in adaptive threshold mode)/Ch 2 threshold low byte (in fixed threshold mode) 0x86							
Ch 2 Setup	14	0x0E	R/W	RngH2 (0)	RngL2 (0)	(0)	$\overline{\text{Hyst2}}$ (0)	ThrSettling2 (4-bit value) (0x0B)			
Configuration	15	0x0F	R/W	ThrFixed (0)	ThrMD1 (0)	ThrMD0 (0)	EnCh1 (1)	EnCh2 (1)	MD2 (0)	MD1 (0)	MD0 (1)
Power-Down Timer	16	0x10	R/W	(0)	(1)	Power-down timeout (6-bit value) (0x00)					
Ch 1 CAPDAC	17	0x11	R/W	DacEn1 (1)	DacAuto1 (1)	DacValue1 (6-bit value) (0x00)					
Ch 2 CAPDAC	18	0x12	R/W	DacEn2 (1)	DacAuto2 (1)	DacValue2 (6-bit value) (0x00)					
Serial Number 3	19	0x13	R	Serial number—Byte 3 (MSB)							
Serial Number 2	20	0x14	R	Serial number—Byte 2							
Serial Number 1	21	0x15	R	Serial number—Byte 1							
Serial Number 0	22	0x16	R	Serial number—Byte 0 (LSB)							
Chip ID	23	0x17	R	Chip identification code							

[1] The default values are given in parentheses.

STATUS REGISTER

Address Pointer 0x00
8 Bits, Read Only
Default Value 0x53 Before Conversion, 0x54 After Conversion

The status register indicates the status of the part. The register can be read via the 2-wire serial interface to query the status of the outputs, check the CDC finished conversion, and check whether the CAPDAC has been changed by the auto-DAC function.

Table 6. Status Register Bit Map[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PwrDown	$\overline{\text{DacStep2}}$	OUT2	$\overline{\text{DacStep1}}$	OUT1	C1/C2	$\overline{\text{RDY2}}$	$\overline{\text{RDY1}}$
(0)	(1)	(0)	(1)	(0)	(0)	(1)	(1)

[1] The default values are given in parentheses.

Table 7. Status Register Bit Descriptions

Bit	Mnemonic	Description
7	PwrDown	PwrDown = 1 indicates that the part is in a power-down.
6	$\overline{\text{DacStep2}}$	$\overline{\text{DacStep2}}$ = 0 indicates that the Channel 2 CAPDAC value was changed after the last CDC conversion as part of the auto-DAC function. The bit value is updated after each finished CDC conversion on this channel.
5	OUT2	OUT2 = 1 indicates that the Channel 2 data (CIN2 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
4	$\overline{\text{DacStep1}}$	$\overline{\text{DacStep1}}$ = 0 indicates that the Channel 1 CAPDAC value was changed during the last conversion as part of the auto-DAC function. The bit value is updated after each finished CDC conversion on this channel.
3	OUT1	OUT1 = 1 indicates that the Channel 1 data (CIN1 capacitance) crossed the threshold, according to the selected comparator mode of operation. The bit value is updated after each finished CDC conversion on this channel.
2	C1/C2	C1/C2 = 0 indicates that the last finished CDC conversion was on Channel 1. C1/C2 = 1 indicates that the last finished CDC conversion was on Channel 2.
1	$\overline{\text{RDY2}}$	$\overline{\text{RDY2}}$ = 0 indicates a finished CDC conversion on Channel 2. The bit is reset back to 1 when the Channel 2 data register is read via the serial interface or after a part reset or power-up.
0	$\overline{\text{RDY1}}$	$\overline{\text{RDY1}}$ = 0 indicates a finished CDC conversion on Channel 1. The bit is reset back to 1 when the Channel 1 data register is read via serial interface or after a part reset or power-up.

DATA REGISTERS

Ch 1 Address Pointer 0x01, Address Pointer 0x02
Ch 2 Address Pointer 0x03, Address Pointer 0x04
16 Bits, Read Only
Default Value 0x0000

Data from the last complete capacitance-to-digital conversion reflects the capacitance on the input. Only the 12 MSBs of the data registers are used for the CDC result. The 4 LSBs are always 0, as shown in Figure 36.

The data register is updated after a finished conversion on the capacitive channel, with one exception: when the serial interface read operation from the data register is in progress, the data register is not updated and the new capacitance conversion result is lost.

The stop condition on the serial interface is considered to be the end of the read operation. Therefore, to prevent incorrect data reading through the serial interface, the two bytes of a data register should be read sequentially using the register address pointer autoincrement feature of the serial interface.

The nominal AD7156 CDC transfer function (an ideal transfer function excluding offset and/or gain error) maps the input capacitance between zero scale and full scale to output data codes between 0x3000 and 0xD000 only (see Table 8).

For an ideal part, linear, with no offset error and no gain error, the input capacitance can be calculated from the output data using the following equation:

$$C\ (\text{pF}) = \frac{Data - 12{,}288}{40{,}960} \times Input\_Range\ (\text{pF})$$

where *Input_Range* = 4 pF, 2 pF, 1 pF, or 0.5 pF.

The following is the same equation written with hexadecimal numbers:

$$C\ (\text{pF}) = \frac{Data - \text{0x3000}}{\text{0xA000}} \times Input\_Range\ (\text{pF})$$

With offset error and gain error included, the equation is:

$$C\ (\text{pF}) = \frac{Data - 12{,}288}{40{,}960} \times Input\_Range\ (\text{pF}) \times \left(1 + \frac{Gain\_Error(\%)}{100\%}\right) + Offset\_Error\ (\text{pF})$$

Or the same equation with hexadecimal numbers:

$$C\ (\text{pF}) = \frac{Data - \text{0x3000}}{\text{0xA000}} \times Input\_Range\ (\text{pF}) \times \left(1 + \frac{Gain\_Error(\%)}{100\%}\right) + Offset\_Error\ (\text{pF})$$

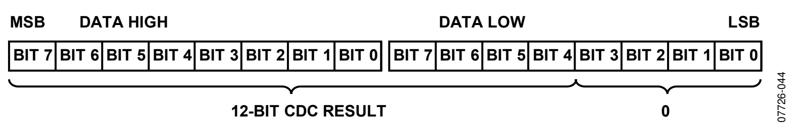


Figure 36. CDC Data Register

Table 8. AD7156 Capacitance-to-Data Mapping[1]

Data	Input Capacitance
0x0000	Under range (below 0 pF)
0x3000	Zero scale (0 pF)
0x5800	Quarter scale (+0.5 pF)—auto-DAC step down
0x8000	Midscale (+1 pF)
0xA800	Three-quarter scale (+1.5 pF)—auto-DAC step up
0xD000	Full scale (+2 pF)
0xFFF0	Over range (above +2 pF)

[1] An ideal part with no offset and gain error, values shown in picofarad for 2 pF capacitance input range.

AVERAGE REGISTERS

Ch 1 Address Pointer 0x05, Address Pointer 0x06
Ch 2 Address Pointer 0x07, Address Pointer 0x08
16 Bits, Read Only
Default Value 0x0000

These registers show the average calculated from the previous CDC data. The 12-bit CDC result corresponds to the 12 MSBs of the average register.

The settling time of the average can be set by programming the ThrSettling bits in the setup registers. The average register is overwritten directly with the CDC output data, that is, the history is erased if the timeout is enabled and elapses.

FIXED THRESHOLD REGISTERS

Ch 1 Address Pointer 0x09, Address Pointer 0x0A
Ch 2 Address Pointer 0x0C, Address Pointer 0x0D
16 Bits, Read/Write, Factory Preset 0x0886

A constant threshold for the output comparator in the fixed threshold mode can be set using these registers. The 12-bit CDC result corresponds to the 12 MSBs of the threshold register. The fixed threshold registers share the address pointer and location on chip with the sensitivity and timeout registers. The fixed threshold registers are not accessible in the adaptive threshold mode.

SENSITIVITY REGISTERS

Ch 1 Address Pointer 0x09
Ch 2 Address Pointer 0x0C
8 Bits, Read/Write, Factory Preset 0x08

Sensitivity registers set the distance of the positive threshold above the data average, and the distance of the negative threshold below the data average, in the adaptive threshold mode.

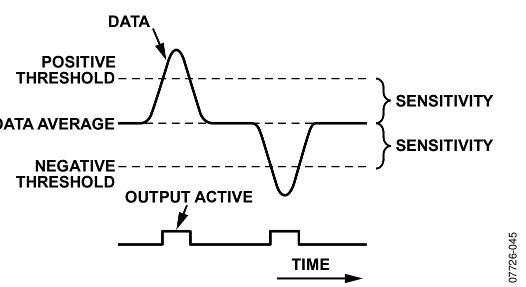


Figure 37. Threshold Sensitivity

The sensitivity is an 8-bit value and is mapped to the lower eight bits of the 12-bit CDC data, that is, it corresponds to the 16-bit data register as shown in Figure 38.

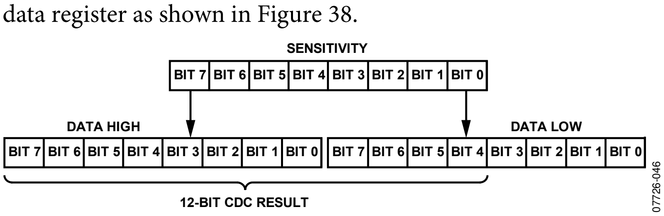


Figure 38. Relation Between Sensitivity Register and CDC Data Register

For an ideal part with no gain error, the sensitivity can be calculated using the following equation:

$$Sensitivity\,(\text{pF}) = \frac{Sens\_Reg}{2560} \times Input\_Range\,(\text{pF})$$

Or the same equation with hexadecimal numbers

$$Sensitivity\,(\text{pF}) = \frac{Sens\_Reg}{0\text{xA}00} \times Input\_Range\,(\text{pF})$$

With gain error included, the sensitivity can be calculated using the following equation:

$$Sensitivity\,(\text{pF}) = \frac{Sense\_Reg}{2560} \times Input\_Range\,(\text{pF}) \times \left(1 + \frac{Gain\_Error\,(\%)}{100\%}\right)$$

Or the same equation with hexadecimal numbers

$$Sensitivity\,(\text{pF}) = \frac{Sense\_Reg}{0\text{xA}00} \times Input\_Range\,(\text{pF}) \times \left(1 + \frac{Gain\_Error\,(\%)}{100\%}\right)$$

TIMEOUT REGISTERS

Ch 1 Address Pointer 0x0A
Ch 2 Address Pointer 0x0D
8 Bits, Read/Write, Factory Preset 0x86

Table 9. Timeout Register Bit Map

Bit	Mnemonic	Default
[7:4]	TimeOutApr	0x08
[3:0]	TimeOutRec	0x06

These registers set timeouts for the adaptive threshold mode.

The approaching timeout starts when the CDC data crosses the data average ± sensitivity band toward the threshold, according to the selected positive, negative, or window threshold mode. The approaching timeout elapses after the number of conversion cycles equals $2^{TimeOutApr}$, where TimeOutApr is the value of the four most significant bits of the timeout register.

The receding timeout starts when the CDC data crosses the data average ± sensitivity band away from the threshold, according to the selected positive or negative threshold mode. The receding timeout is not used in the window threshold mode. The receding timeout elapses after the number of conversion cycles equals $2^{TimeOutRec}$, where TimeOutRec is the value of the four least significant bits of the timeout register.

When either the approaching or receding timeout elapses (that is, after the defined number of CDC conversions is counted), the data average (and thus the thresholds) is forced to follow the new CDC data value immediately.

When the timeout register equals 0, timeouts are disabled.

SETUP REGISTERS

Ch 1 Address Pointer 0x0B
Ch 2 Address Pointer 0x0E
8 Bits, Read/Write, Factory Preset 0x0B

Table 10. Setup Registers Bit Map[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RngH	RngL		$\overline{\text{Hyst}}$	ThrSettling (4-Bit Value)			
(0)	(0)	(0)	(0)	(0x0B)			

[1] The default values are given in parentheses.

Table 11. Setup Registers Bit Descriptions

Bit	Mnemonic	Description			
7 6	RngH RngL	Range bits set the CDC input range and determine the step for the auto-DAC function.			
		RngH	**RngL**	**Capacitive Input Range (pF)**	**Auto-DAC Step (CAPDAC LSB)**
		0	0	2	4
		0	1	0.5	1
		1	0	1	2
		1	1	4	8
5		This bit should be 0 for the specified operation.			
4	$\overline{\text{Hyst}}$	$\overline{\text{Hyst}}$ = 1 disables hysteresis in adaptive threshold mode. This bit has no effect in fixed threshold mode; hysteresis is always disabled in the fixed threshold mode.			
[3:0]	ThrSettling	Determines dynamic behavior of the data average and thus the settling time of the adaptive thresholds. Data average is calculated from the previous CDC output data, using equation: $Average(N) = Average(N-1) + \frac{Data(N) - Average(N-1)}{2^{ThrSettling + 1}}$ where: *Average*(*N*) is the new average value. *Average*(*N* – *1*) is the average value from the previous cycle. *Data(N)* is the latest complete CDC conversion result. *ThrSettling* is the programmable parameter. The response of the average to an input capacitance step change (that is, response to the change in the CDC output data) is an exponential settling curve characterized by the following equation: $Average(N) = Average(0) + Change(1 - e^{N/TimeConst})$ where: *Average(N)* is the value of average N complete CDC conversion cycles after a step change on the input. *Average*(0) is the value before the step change. *TimeConst* can be selected in the range between 2 and 65,536 conversion cycle multiples, in steps of power of 2, by programming the ThrSettling bits. $TimeConst = 2^{(ThrSettling + 1)}$			

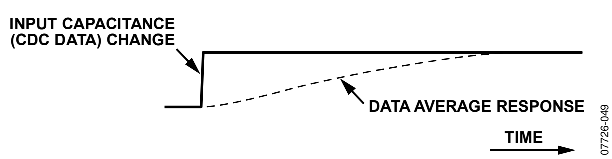


Figure 39. Data Average Response to Data Step Change

CONFIGURATION REGISTER

Address Pointer 0x0F

8 Bits, Read/Write, Factory Preset 0x19

Table 12. Configuration Register Bit Map[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ThrFixed (0)	ThrMD1 (0)	ThrMD0 (0)	EnCh1 (1)	EnCh2 (1)	MD2 (0)	MD1 (0)	MD0 (1)

[1] The default values are given in parentheses.

Table 13.Configuration Register Bit Descriptions

<table>
<tr><th>Bit</th><th>Mnemonic</th><th>Description</th></tr>
<tr><td>7</td><td>ThrFixed</td><td>ThrFixed = 1 sets the fixed threshold mode; the outputs reflect the comparison of data and a fixed (constant) value of the threshold registers.
ThrFixed = 0 sets the adaptive threshold mode; the outputs reflect the comparison of data to the adaptive thresholds. The adaptive threshold is set dynamically, based on the history of the previous data.</td></tr>
<tr><td>6
5</td><td>ThrMD1
ThrMD0</td><td>These bits set the output comparators mode
<table>
<tr><th rowspan="2">ThrMD1</th><th rowspan="2">ThrMD0</th><th rowspan="2">Threshold Mode</th><th colspan="2">Output Active When</th></tr>
<tr><th>Adaptive Threshold Mode</th><th>Fixed Threshold Mode</th></tr>
<tr><td>0</td><td>0</td><td>Negative</td><td>Data < average – sensitivity</td><td>Data < threshold</td></tr>
<tr><td>0</td><td>1</td><td>Positive</td><td>Data > average + sensitivity</td><td>Data > threshold</td></tr>
<tr><td>1</td><td>0</td><td>In-window</td><td>Data > average – sensitivity
and
Data < average + sensitivity</td><td></td></tr>
<tr><td>1</td><td>1</td><td>Out-window</td><td>Data < average – sensitivity
or
Data > average + sensitivity</td><td></td></tr>
</table></td></tr>
<tr><td>4</td><td>EnCh1</td><td>Enables conversion on Channel 1</td></tr>
<tr><td>3</td><td>EnCh2</td><td>Enables conversion on Channel 2</td></tr>
<tr><td>2
1
0</td><td>MD2
MD1
MD0</td><td>Converter mode of operation setup
<table>
<tr><th>MD2</th><th>MD1</th><th>MD0</th><th>Mode</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Idle</td><td>The part is fully powered up, but performing no conversion.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Continuous Conversion</td><td>The part is repeatedly performing conversions on the enabled channel(s); if two channels are enabled, the part is sequentially switching between them.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Single conversion</td><td>The part performs a single conversion on the enabled channel; if two channels are enabled, the part performs two conversions, one on each channel. After finishing the conversion(s), the part goes to the idle mode.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Power-down</td><td>The part powers down the on-chip circuits, except the digital interface.</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Reserved</td><td>Do not use these modes.</td></tr>
</table></td></tr>
</table>

POWER-DOWN TIMER REGISTER

Address Pointer 0x10
8 Bits, Read/Write, Factory Preset 0x40

Table 14. Power-Down Timer Register Bit Map[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Power-down timeout (6-bit value)					
(0)	(1)	(0x00)					

[1] The default values are given in parentheses.

Table 15.Power-Down Timer Register Bit Descriptions

Bit	Mnemonic	Description
7		This bit must be 0 for proper operation.
6		This bit must be 1 for proper operation.
[5:0]	Power-down timeout	This bit defines the period duration of the power-down timeout. If the comparator outputs have not been activated during the programmed period, the part enters power-down mode automatically. The part can be then returned to a normal operational mode either via the serial interface or by the power supply off/on sequence. The period is programmable in steps of 4 hours. For example, setting the value to 0x06 sets the duration to 24 hours. The maximum value of 0x3F corresponds to approximately 10.5 days. The value of 0x00 disables the power-down timeout, and the part does not enter power-down mode automatically.

CAPDAC REGISTERS

Ch 1 Address Pointer 0x11
Ch 2 Address Pointer 0x12
8 Bits, Read/Write, Factory Preset 0xC0

Table 16. CAPDAC Registers Bit Map[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DacEn	DacAuto	DacValue (6-bit value)					
(1)	(1)	(0x00)					

[1] The default values are given in parentheses.

Table 17. CAPDAC Registers Bit Descriptions

Bit	Mnemonic	Description
7	DacEn	DacEn = 1 enables capacitive the DAC.
6	DacAuto	DacAuto = 1 enables the auto-DAC function in the adaptive threshold mode. When the auto-DAC function is enabled, the part dynamically adjusts the CAPDAC to keep the CDC in an optimal operating capacitive range. The CAPDAC value is automatically incremented when the data average exceeds ¾ of the CDC full range, and the CAPDAC value is decremented when the data average goes below ¼ of the CDC full range. The auto-DAC increment or decrement step depends on the selected CDC capacitive input range. This bit has no effect in fixed threshold mode; the auto-DAC function is always disabled in the fixed threshold mode.
[5:0]	DacValue	CAPDAC value, Code 0x00 ≈ 0 pF, Code 0x3F ≈ CAPDAC full range.

SERIAL NUMBER REGISTER

Address Pointer 0x13, Address Pointer 0x14, Address Pointer 0x15, Address Pointer 0x16
32 Bits, Read Only, Factory Preset 0xXXXX

This register holds a serial number, unique for each individual part.

CHIP ID REGISTER

Address Pointer 0x17
8 Bits, Read Only, Factory Preset 0xXX

This register holds the chip identification code, used in factory manufacturing and testing.

SERIAL INTERFACE

The AD7156 supports an I²C-compatible, 2-wire serial interface. The two wires on the serial bus (interface) are called SCL (clock) and SDA (data). These two wires carry all addressing, control, and data information one bit at a time over the bus to all connected peripheral devices. The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the data transfer. The devices on the bus are classified as either master or slave devices. A device that initiates a data transfer message is called a master, whereas a device that responds to this message is called a slave.

To control the AD7156 device on the bus, the following protocol must be utilized. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that the start byte follows. This 8-bit start byte is made up of a 7-bit address plus an R/W bit indicator.

All peripherals connected to the bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The bits arrive MSB first. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. An exception to this is the general call address, which is described in the General Call section. In the idle condition, the device monitors the SDA and SCL lines waiting for the start condition and the correct address byte.

The R/W bit determines the direction of the data transfer. A Logic 0 LSB in the start byte means that the master writes information to the addressed peripheral. In this case, the AD7156 becomes a slave receiver. A Logic 1 LSB in the start byte means that the master reads information from the addressed peripheral. In this case, the AD7156 becomes a slave transmitter. In all instances, the AD7156 acts as a standard slave device on the serial bus.

The start byte address for the AD7156 is 0x90 for a write and 0x91 for a read.

READ OPERATION

When a read is selected in the start byte, the register that is currently addressed by the address pointer is transmitted to the SDA line by the AD7156. This is then clocked out by the master device, and the AD7156 awaits an acknowledge from the master.

If an acknowledge is received from the master, the address autoincrementer automatically increments the address pointer register and outputs the next addressed register content to the SDA line for transmission to the master. If no acknowledge is received, the AD7156 returns to the idle state and the address pointer is not incremented. The address pointers' autoincrementer allows block data to be written to or read from the starting address and subsequent incremental addresses.

In continuous conversion mode, the address pointers' autoincrementer should be used for reading a conversion result. This means that the two data bytes should be read using one multibyte read transaction rather than two separate single byte transactions. The single byte data read transaction may result in the data bytes from two different results being mixed. The same applies for four data bytes if both capacitive channels are enabled.

The user can also access any unique register (address) on a one-to-one basis without having to update all the registers. The address pointer register contents cannot be read.

If an incorrect address pointer location is accessed or if the user allows the autoincrementer to exceed the required register address, the following applies:

- In read mode, the AD7156 continues to output various internal register contents until the master device issues a no acknowledge, start, or stop condition. The address pointers' autoincrementer contents are reset to point to the status register at the 0x00 address when a stop condition is received at the end of a read operation. This allows the status register to be read (polled) continually without having to constantly write to the address pointer.
- In write mode, the data for the invalid address is not loaded into the AD7156 registers, but an acknowledge is issued by the AD7156.

WRITE OPERATION

When a write is selected, the byte following the start byte is always the register address pointer (subaddress) byte, which points to one of the internal registers on the AD7156. The address pointer byte is automatically loaded into the address pointer register and acknowledged by the AD7156. After the address pointer byte acknowledge, a stop condition, a repeated start condition, or another data byte can follow from the master. A stop condition is defined by a low-to-high transition on SDA while SCL remains high. If a stop condition is encountered by the AD7156, it returns to its idle condition and the address pointer is reset to 0x00.

If a data byte is transmitted after the register address pointer byte, the AD7156 loads this byte into the register that is currently addressed by the address pointer register and sends an acknowledge, and the address pointer autoincrementer automatically increments the address pointer register to the next internal register address. Thus, subsequent transmitted data bytes are loaded into sequentially incremented addresses.

If a repeated start condition is encountered after the address pointer byte, all peripherals connected to the bus respond exactly as outlined previously for a start condition; that is, a repeated start condition is treated the same as a start condition. When a master device issues a stop condition, it relinquishes control of the bus, allowing another master device to take control of the bus. Therefore, a master wanting to retain control of the bus issues successive start conditions known as repeated start conditions.

AD7156 RESET

To reset the AD7156 without having to reset the entire serial bus, an explicit reset command is provided. This uses a particular address pointer word as a command word to reset the part and upload all default settings. The AD7156 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The reset command address word is 0xBF.

GENERAL CALL

When a master issues a slave address consisting of seven 0s with the eighth bit (R/W) set to 0, this is known as the general call address. The general call address is for addressing every device connected to the serial bus. The AD7156 acknowledges this address and reads in the following data byte.

If the second byte is 0x06, the AD7156 is reset, completely uploading all default values. The AD7156 does not respond to the serial bus commands (do not acknowledge) during the default values upload for approximately 2 ms.

The AD7156 does not acknowledge any other general call commands.

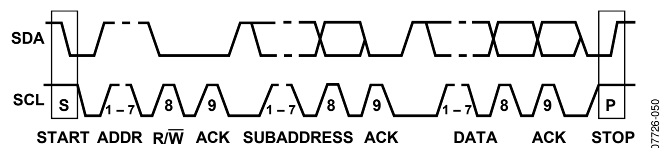


Figure 40. Bus Data Transfer

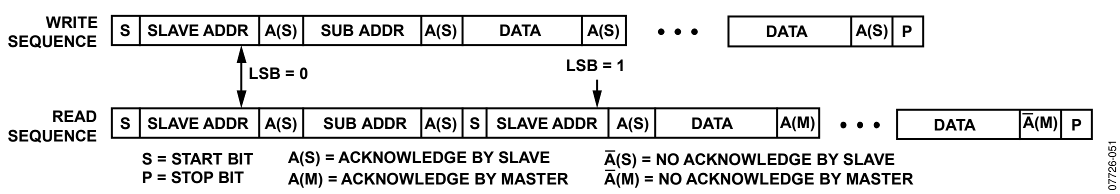


Figure 41. Write and Read Sequences

HARDWARE DESIGN CONSIDERATIONS

OVERVIEW

The AD7156 is an interface to capacitive sensors.

On the input side, Sensor C_X can be connected directly between the AD7156 EXC and CIN pins. The way it is connected and the electrical parameters of the sensor connection, such as parasitic resistance or capacitance, can affect the system performance. Therefore, any circuit with additional components in the capacitive front end, such as overvoltage protection, has to be carefully designed, considering the AD7156 specified limits and information provided in this section.

On the output side, the AD7156 can work as a standalone device, using the power-up default register settings and flagging the result on the digital outputs. Alternatively, the AD7156 can be interfaced to a microcontroller via the 2-wire serial interface, offering flexibility by overwriting the AD7156 register values from the host with a user-specific setup.

PARASITIC CAPACITANCE TO GROUND

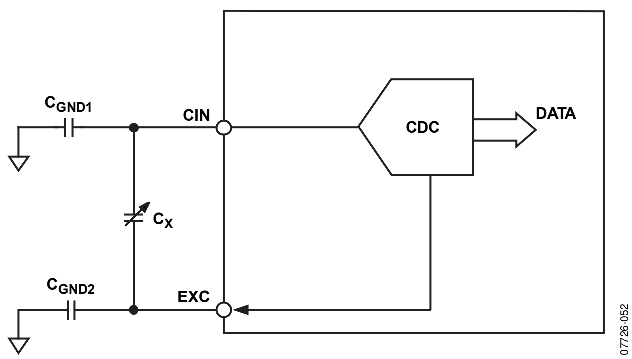


Figure 42. Parasitic Capacitance to Ground

The CDC architecture used in the AD7156 measures the capacitance, C_X, connected between the EXC pins and the CIN pins. In theory, any capacitance, C_{GND}, to ground should not affect the CDC result (see Figure 42).

The practical implementation of the circuitry in the chip implies certain limits, and the result is gradually affected by capacitance to ground (for information about the allowed capacitance to GND for CIN and information about excitation see Table 1 and Figure 4 to Figure 9).

PARASITIC RESISTANCE TO GROUND

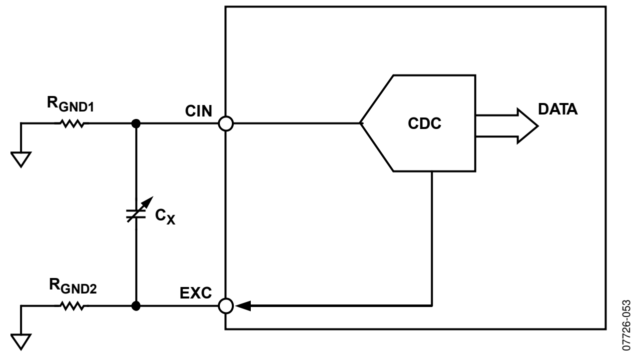


Figure 43. Parasitic Resistance to Ground

The AD7156 CDC result is affected by a leakage current from C_X to ground; therefore, C_X should be isolated from the ground. The equivalent resistance between C_X and ground should be maximized (see Figure 43). For more information, see Figure 10 to Figure 13.

PARASITIC PARALLEL RESISTANCE

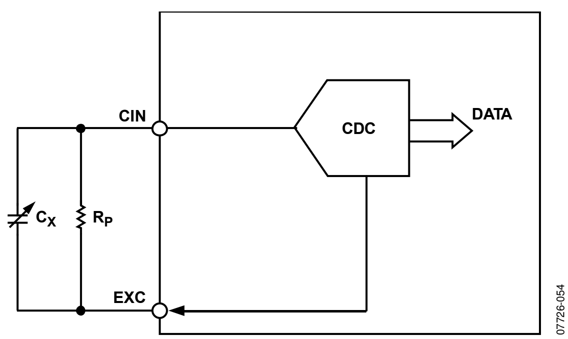


Figure 44. Parasitic Parallel Resistance

The AD7156 CDC measures the charge transfer between the EXC and CIN pins. Any resistance connected in parallel to the measured capacitance, C_X (see Figure 44), such as the parasitic resistance of the sensor, also transfers charge. Therefore, the parallel resistor is seen as an additional capacitance in the output data. The equivalent parallel capacitance (or error caused by the parallel resistance) can be approximately calculated as

$$C_P = \frac{1}{R_P \times f_{EXC} \times 4}$$

where:
R_P is the parallel resistance.
f_{EXC} is the excitation frequency.

For additional information, see Figure 15.

PARASITIC SERIAL RESISTANCE

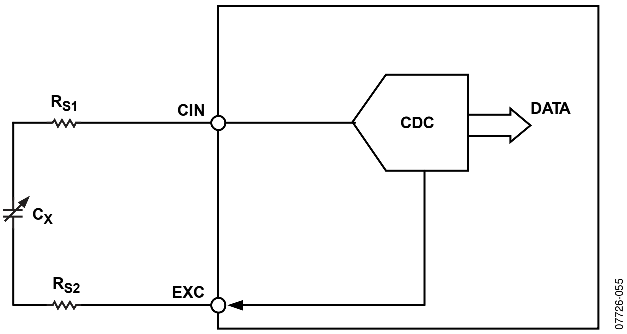


Figure 45. Parasitic Serial Resistance

The AD7156 CDC result is affected by a resistance in series with the measured capacitance.

The total serial resistance (R_{S1} + R_{S2} in Figure 45) should be in the order of hundreds of Ω (see Figure 14).

INPUT OVERVOLTAGE PROTECTION

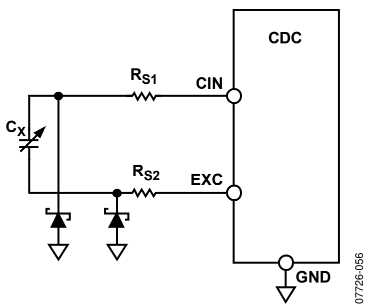


Figure 46. AD7156 CIN Overvoltage Protection

The AD7156 capacitive input has an internal ESD protection. However, some applications may require an additional over-voltage protection, depending on the application-specific requirements. Any additional circuit in the capacitive front end must be carefully designed, especially with respect to the limits recommended for maximum capacitance to ground, maximum serial resistance, maximum leakage, and so on.

INPUT EMC PROTECTION

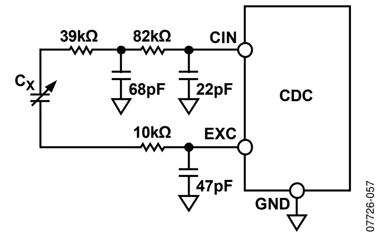


Figure 47. AD7156 CIN EMC Protection

Some applications may require an additional input filter for improving EMC. Any input filter must be carefully designed, considering the balance between the system capacitance performance and system electromagnetic immunity.

Figure 47 shows one of the possible input circuit configurations for significantly improving the system immunity against high frequency noise while only slightly affecting the AD7156 performance in terms of additional gain and offset error.

POWER SUPPLY DECOUPLING AND FILTERING

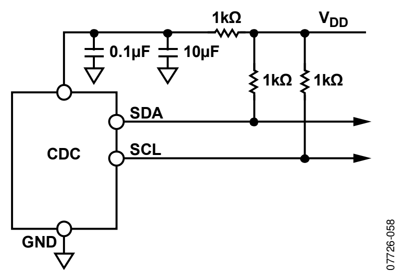


Figure 48. AD7156 V_{DD} Decoupling and Filtering

The AD7156 has good dc and low frequency power supply rejection but may be sensitive to higher frequency ripple and noise, specifically around the excitation frequency and its harmonics. Figure 48 shows a possible circuit configuration for improving the system immunity against ripple and noise coupled to the AD7156 via the power supply.

If the serial interface is connected to the other circuits in the system, it is better to connect the pull-up resistors on the other side of the V_{DD} filter than to connect to the AD7156. If the AD7156 is used in standalone mode and the serial interface is not used, it is better to connect the pull-up resistors directly to the AD7156 V_{DD}.

APPLICATION EXAMPLES

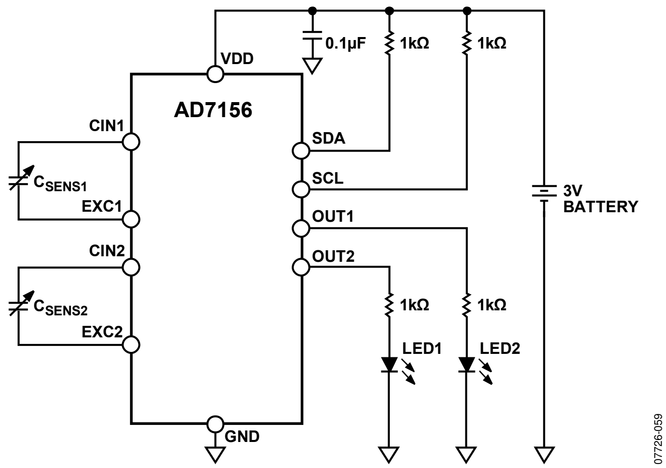


Figure 49. AD7156 Standalone Operation Application Diagram

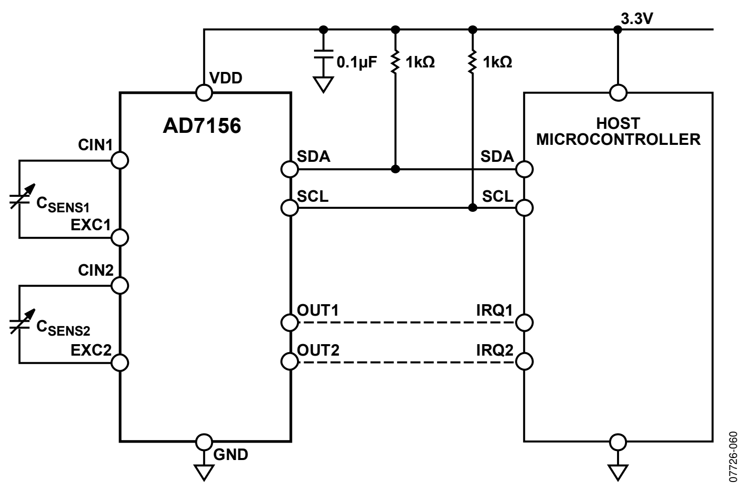


Figure 50. AD7156 Interfaced to a Host Microcontroller

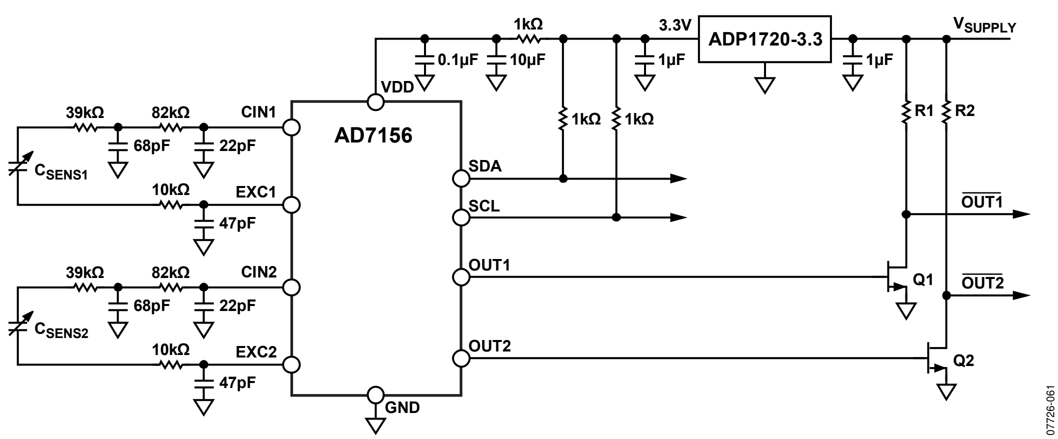


Figure 51. AD7156 Standalone Operation with EMC Protection

OUTLINE DIMENSIONS

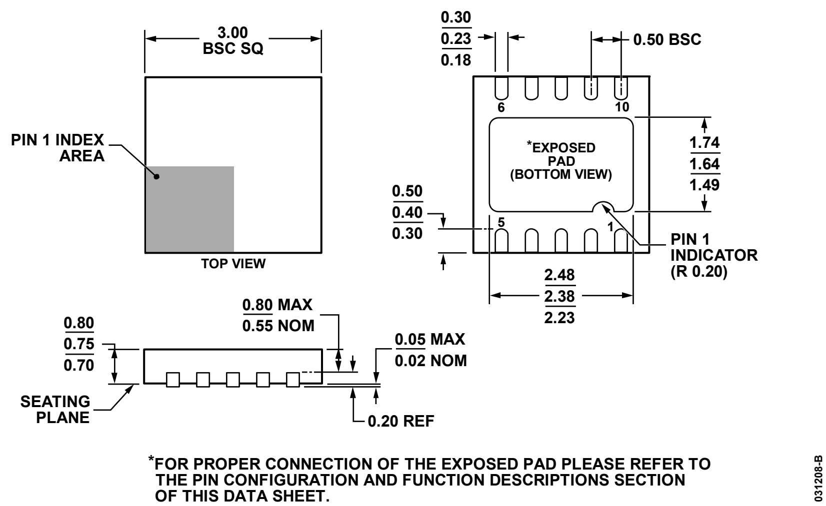


Figure 52. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD7156BCPZ-REEL[1]	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	C6L
AD7156BCPZ-REEL7[1]	−40°C to +85°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	C6L
EVAL-AD7156EBZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

D07726-0-10/08(0)

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