IVCR1401 35V 4A SiC and IGBT 8-Pin Driver with Integrated Negative Bias

1. Features

- Driver current capacity: 4A sink and source peak drive current
- Wide VCC range up to 35V
- Integrated 3.5V negative bias
- Designed for low side and suitable for bootstrap high-side power
- Programmable UVLO for positive and fixed UVLO for negative gate drive voltage
- Desaturation detection for short circuit protection with internal blanking time
- Fault output when UVLO or OCP detected
- 5V 10mA reference for external circuit, e.g. digital isolator
- TTL and CMOS compatible input
- SOIC-8 with optional exposed pad for high frequency and power applications
- Low propagation delay 45ns typical with build-in de-glitch filter

2. Applications

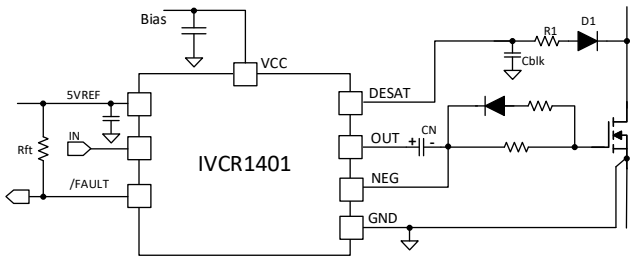
- EV On Board Chargers
- EV/HEV inverters and charging stations
- PV boosters and inverters
- UPS
- AC/DC and DC/DC converters

3. Description

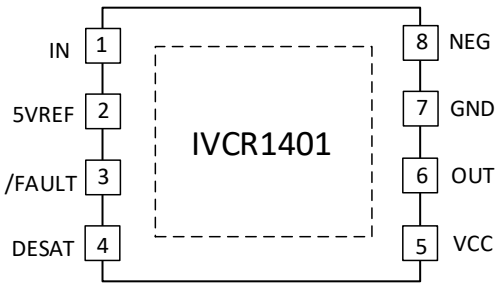
The IVCR1401 is a 4A single-channel, high-speed smart driver, capable of efficiently and safely driving SiC MOSFETs and IGBTs. Strong drive with a negative bias improves noise immunity against Miller effect at high dv/dt operation. Desaturation detection provides robust short circuit protection and reduces the risk of power device and system component damage. A fixed 200ns blanking time is inserted to prevent overcurrent protection from being prematurely trigged by switching edge current spike and noise. Programmable positive gate drive voltage UVLO and fixed negative bias UVLO protection ensures healthy gate operation voltages. An active low fault signal alerts system when UVLO or over current happens. Low propagation delay and mismatch with an optional exposed thermal pad enables SiC MOSFETs to switch at hundreds of kHz. Integrated negative voltage generation and 5V reference output minimize external component count. It is the first industrial SiC MOSFET and IGBT driver which includes negative voltage generation, desaturation and programmable UVLO in an 8-pin package. It is an ideal driver for a compact design.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCR1401DR	SOIC-8	Tape and Reel
IVCR1401D	SOIC-8	Tube
IVCR1401DPR	SOIC-8 (EP)	Tape and Reel
IVCR1401DP	SOIC-8 (EP)	Tube



Typical Application Diagram



Pin Layout (SOIC-8)

Table of Contents

4. Pin Configuration and Functions

PIN	NAME	I/O	DESCRIPTION
1	IN	I	Logic input
2	5VREF	O	5V/10mA output for external circuit
3	/FAULT	O	Open collector fault output, pulled to low when over current or UVLO is detected. External pull-up resistor can be used for UVLO threshold programming
4	DESAT	I	Desaturation detection input
5	VCC	P	Positive bias supply
6	OUT	O	Gate driver output
7	GND	G	Driver ground
8	NEG	O	Negative voltage output
	Exposed pad		Bottom exposed pad is often tied to GND on layout. SOIC-8 (EP) only

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Total supply voltage (reference to GND)	-0.3	35	V
V_{OUT}	Gate driver output voltage	-0.3	V_{CC}+0.3	V
I_{OUTH}	Gate driver output source current (at max pulse width 10us and 0.2% duty cycle)		6.6	A
I_{OUTL}	Gate driver output sink current (at max pulse width 10us and 0.2% duty cycle)		6.6	A
V_{IN}	IN signal voltage	-5.0	20	V
I_{5VREF}	5VREF output current		25	mA
V_{DESAT}	Voltage at DESAT	-0.3	V_{CC}+0.3	V
V_{NEG}	Voltage at NEG pin	OUT-5.0	V_{CC}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{CC}	Total supply voltage (reference to GND)	19	25	V
V_{IN}	Gate input voltage	0	15	V
V_{DESAT}	Voltage at DESAT	0	VCC	V
T_{AMB}	Ambient temperature	-40	125	°C

5.4 Thermal Information

		IVCR1401D	IVCR1401DP	UNIT
$R_{\theta JA}$	Junction-to-Ambient	112	39	°C/W
$R_{\theta JB}$	Junction-to-PCB	53	11	°C/W
$R_{\theta JP}$	Junction-to-exposed pad		5.1	°C/W

5.5 Electrical Specifications

Unless otherwise noted, V_{CC} = 25 V, TA = –40°C to 125°C, 1-µF bypass capacitance from V_{CC} to GND, f = 100 kHz. Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{CCq}	Quiescent current	IN=0V		1.44	3	mA
T_{st} (1)	Negative voltage build-up time	CN = 1uF, V_{CN} >2V V_{CN} =3.5V		10 28		us
UVLO						
V_{ON} V_{OFF}	Under voltage thresholds	Programming resistor Rft = 1.3kΩ (1)		18 17		V
		Programming resistor Rft = 6kΩ	13.8	15.8 14.8	16.8	
		Programming resistor Rft = 20kΩ (1)		13.9 13.1		
V_N	Negative voltage threshold			1.6		V
5VREF		source current 10mA	4.7	5.0	5.35	V
INPUT						
V_{INH}	IN rising threshold		1.6	1.86	2.1	V
V_{INL}	IN falling threshold		1.2	1.48	1.7	V
V_{INHYS}	IN hysteresis			0.4		V
V_{INNS}	IN negative voltage capability		-5			V
OUTPUTS (OUT and NEG)						
I_O (1)	Peak source and sink currents	C_{LOAD} =0.22uF, with external current limiting resistors, 1kHz switching frequency		4.0		A
V_{OH}	OUT high voltage	I_{OUTH} = -100mA	V_{DD}-0.3	V_{DD}-0.13		V
V_{OL}	OUT low voltage	I_{OUTL} = 100mA		0.08	0.2	V
R_{OH}	OUT pull-up resistance			1.3	3	Ω
R_{OL}	OUT pull-down resistance			0.8	2	Ω
V_{NEG}	NEG negative voltage	IN=0V	-4	-3.5		V
/FAULT						
I_{FAULT}	Fault sink current			10		mA
T_{FAULT}	Fault pulse width			10		us
DESAT						
I_{DESATL} I_{DESATH}	Sink current Source current			5.6 1.0		mA
V_{th}	DESAT threshold		8.8	9.54	10.6	V
T_{blk}	Blanking time		160	200	250	ns
Timing						
TD_{ff} TD_{rr}	Falling delay Rising delay	Cload = 1.8nF	30 30	45 45	80 80	ns
T_f T_r	Fall time Rise time	Cload = 1.8nF	6 6	13 13	20 20	ns

(1) Ensured by design and characterization, not 100% tested in production.

6 Typical Characteristics

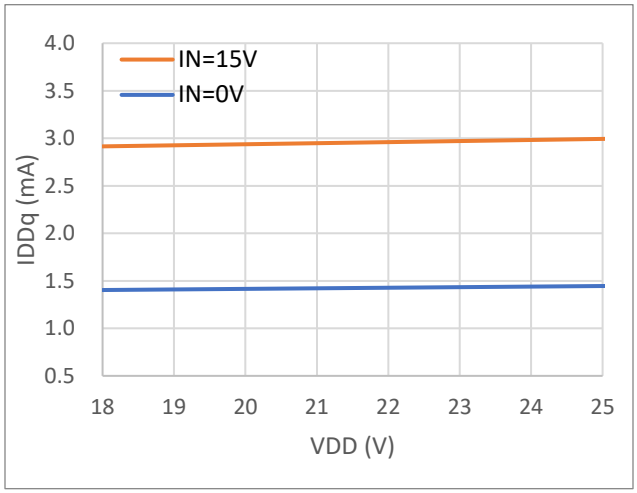


Figure 1. Quiescent Current IDDq vs VDD

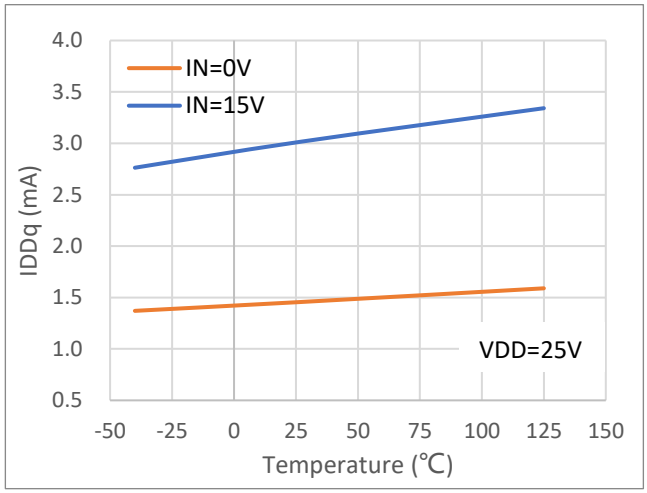


Figure 2. Quiescent Current IDDq vs Temperature

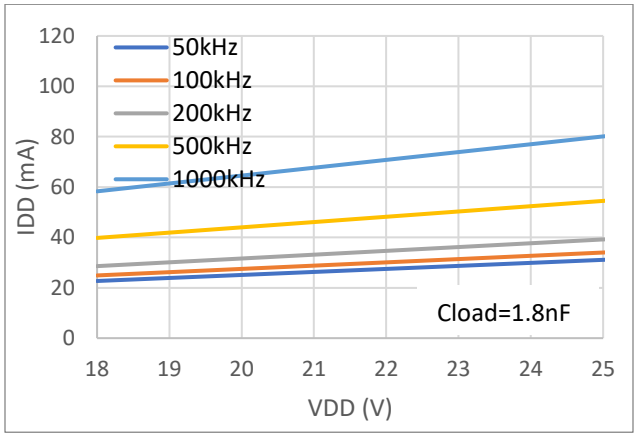


Figure 3. Operating Current IDD vs VDD

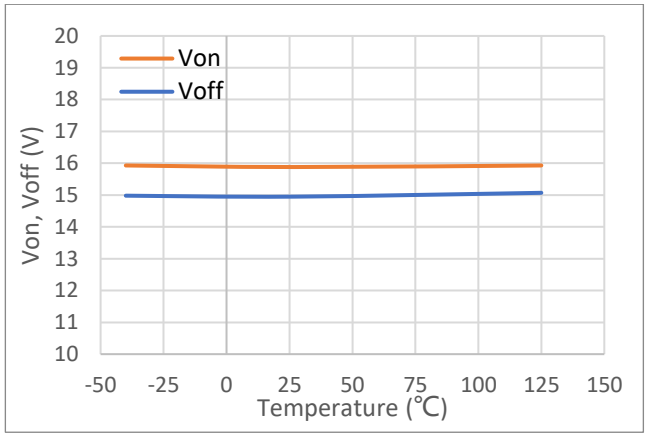


Figure 4. UVLO vs Temperature

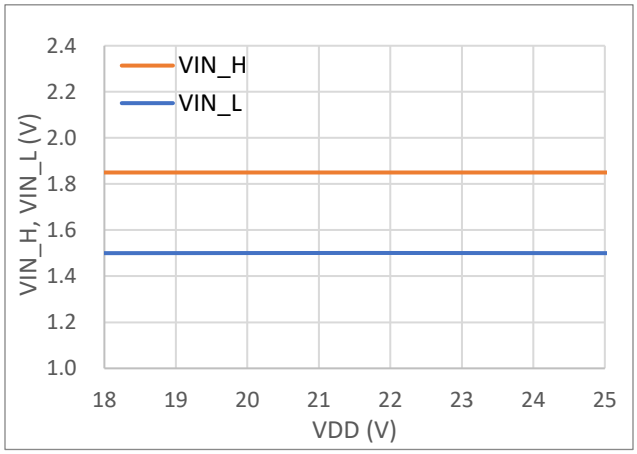


Figure 5. Input Threshold Voltage vs VDD

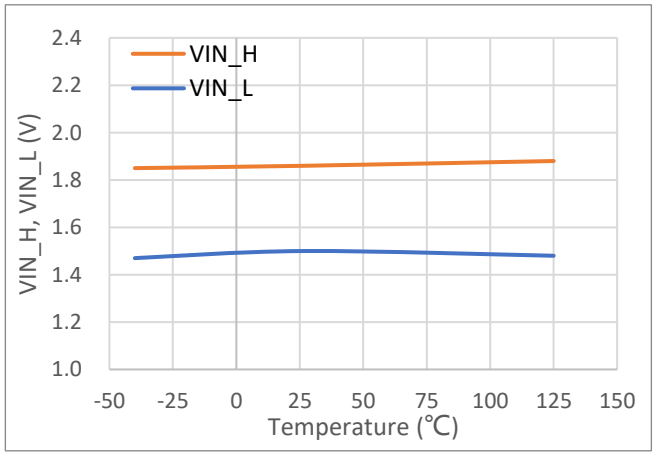


Figure 6. Input Threshold Voltage vs Temperature

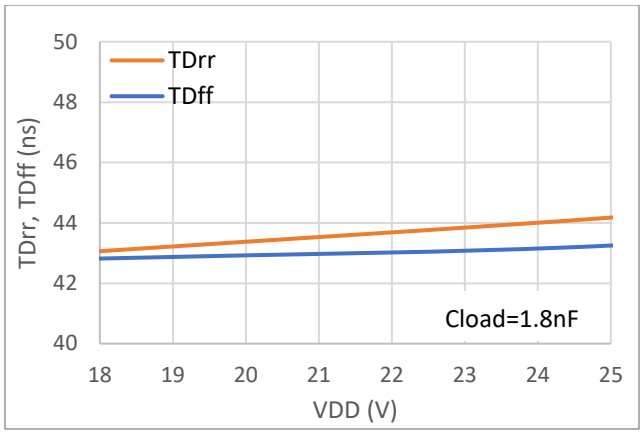


Figure 7. Propagation Delays vs VDD

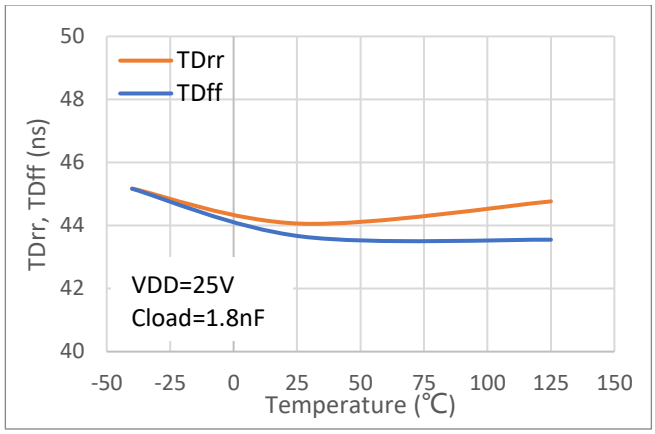


Figure 8. Propagation Delays vs Temperature

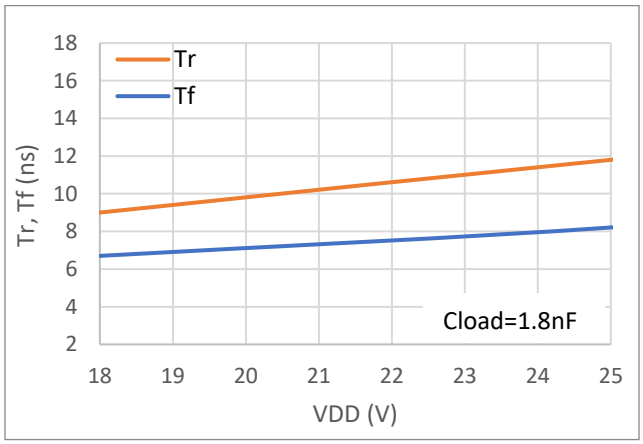


Figure 9. Rise Time and Fall time vs VDD

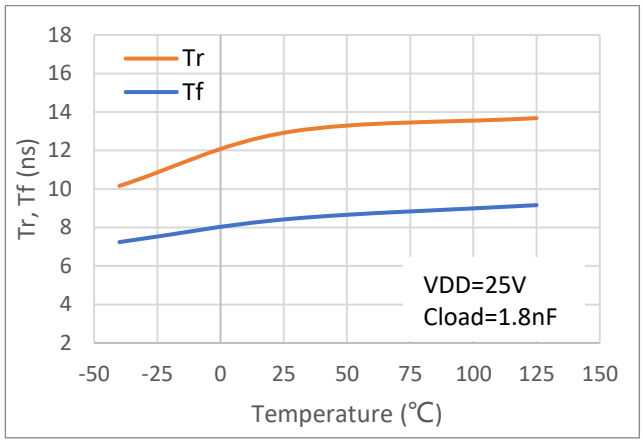
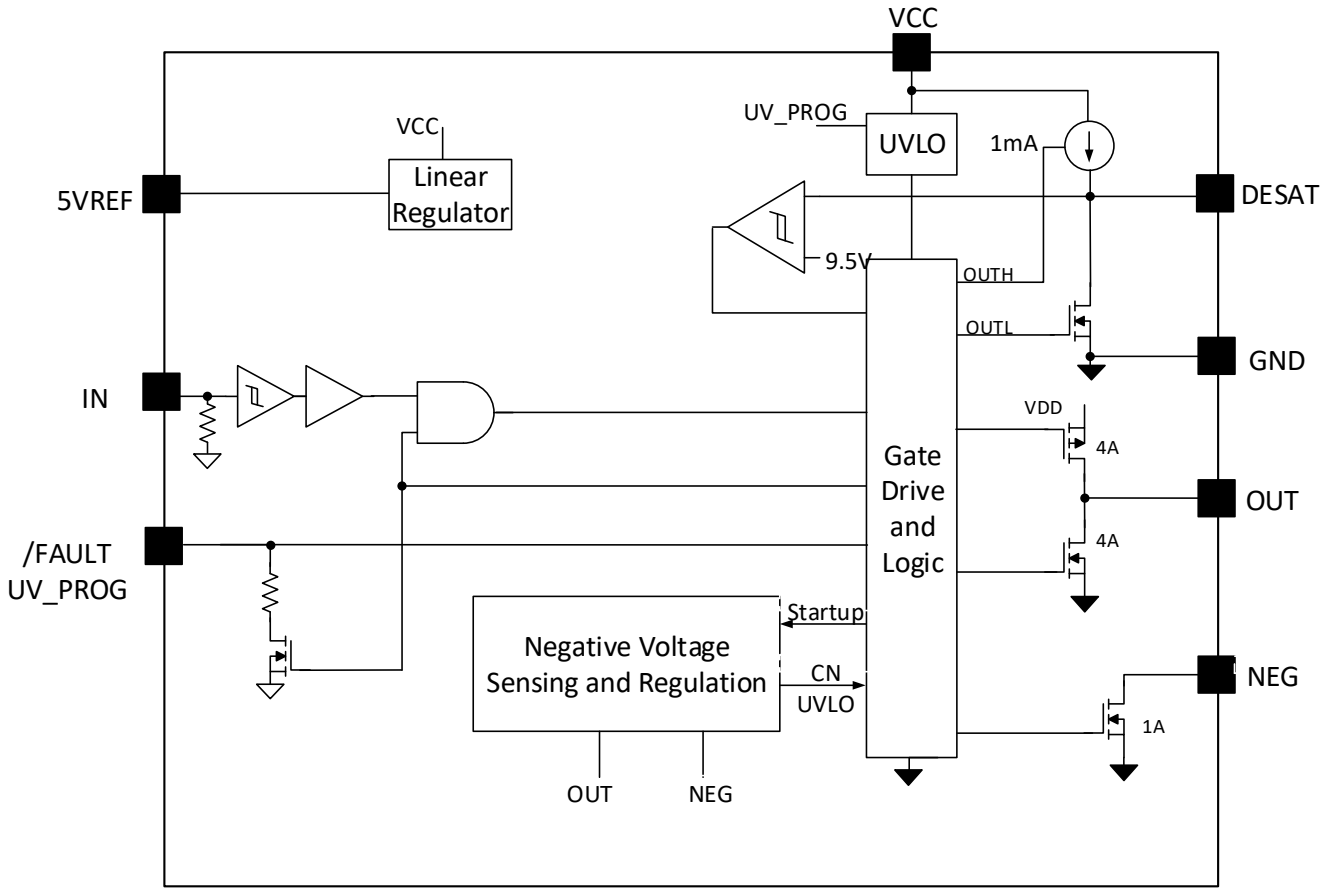


Figure 10. Rise Time and Fall time vs Temperature

7 Detail Description

IVCR1401 driver represents InventChip's cutting-edge single channel low-side high-speed gate driver technology development. It features built-in negative voltage generation, desaturation/short-circuit protection, programmable UVLO. This driver offers the best-in-class characteristics and the most compact and reliable SiC MOSFET gate driving control. It is the first industry driver equipped with all necessary SiC MOSFET gate driving features in a SOIC-8 package.

Function Block Diagram



7.1 Input

IN is a non-inverting logic gate driver input. The pin has a weak pulldown. The input is a TTL and CMOS compatible logic level with maximum 20V input tolerance.

7.2 Output

IVCR1401 features a 4A totem-pole output stage. It delivers high peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition. Strong sink capability results in a very low pull-down impedance in the driver output stage which improves immunity against parasitic Miller turn-on effect, especially where low gate-charge Si MOSFETs or emerging wide bandgap SiC MOSFETs are used.

7.3 Negative Voltage Generation

At startup, NEG output is pulled to GND and provides a high current path for a current source to charge the external negative-voltage capacitor C_N (1uF typical) through OUT pin. The capacitor can be charged to above 2.0V in less than 10us. Before the capacitor voltage, VCN, charged up, /FAULT stays low/active, disregarding IN's logic level. After the negative bias is ready, both NEG pin and /FAULT pin are released and OUT starts to follow input signal IN. A built-in negative voltage regulator regulates the negative voltage to -3.5V for normal operation, regardless of PWM frequency and duty cycle. The gate drive signal, NEG, then switches between V_{CC}-3.5V and -3.5V.

7.4 Under Voltage Protections and Programming

All internal and external biases of the driver are monitored to ensure a healthy operation condition. V_{CC} is monitored by a programmable under voltage detection circuit. The driver output is shut down (pulled low) or stays low if the voltage is below set limit. The external /FAULT pull-up resistor is utilized as a V_{CC} UVLO programming resistor for UVLO setting. The pull-up resistor is tied to 5VREF. At startup, the pull-up resistance can be sensed by internal circuit. Based on the resistance value, a corresponding UVLO level is selected. The Electrical Specifications table above gives the details of the settings. Note that the table gives VCC UVLO thresholds, which are 3.5V higher than gate voltages.

The negative voltage is also monitored. Its UVLO has a fix 1.5V negative-going threshold. Negative voltage capacitor defect could result in the capacitor voltage below the threshold. The UVLO protection will then pull MOSFET's gate to ground. The /FAULT is pulled low when UVLO is detected.

7.5 Desaturation Detection

When short circuit or over current happens, the power device's (SiC MOSFET or IGBT) drain or collector current can increase to such a high value that the devices get out of saturation state, and Vds/Vce of the devices will rise to a substantially high value. DESAT pin with a blanking capacitor Cblk, normally clamped to Id x Rds_on, now is able to charge up much higher by an internal 1mA constant current source. When the voltage reaches typical 9.5V threshold, OUT and /FAULT are both pulled low. A 200ns blank time is inserted at OUT rising edge to prevent DESAT protect circuit from being triggered prematurely due to Coss discharge. To minimize the loss of internal constant current source, the current source is turned off when the main switch is at off state. By selecting a different capacitance, turn-off delay time (external blanking time) can be programmed. The blanking time can be calculated with,

$$T_{eblk} = C_{blk} \cdot V_{th} / I_{DESAT}$$

For example, if C_{blk} is 47pF, T_{eblk} = 47pF ·9.5V / 1mA = 446ns.

Note T_{eblk} includes internal T_{blk} 200ns blanking time already.

For current limit setting, the following equation can be used,

$$I_{limit} = (V_{th} – R1* I_{DESAT} – V_{F\_D1})/ R_{ds\_on}$$

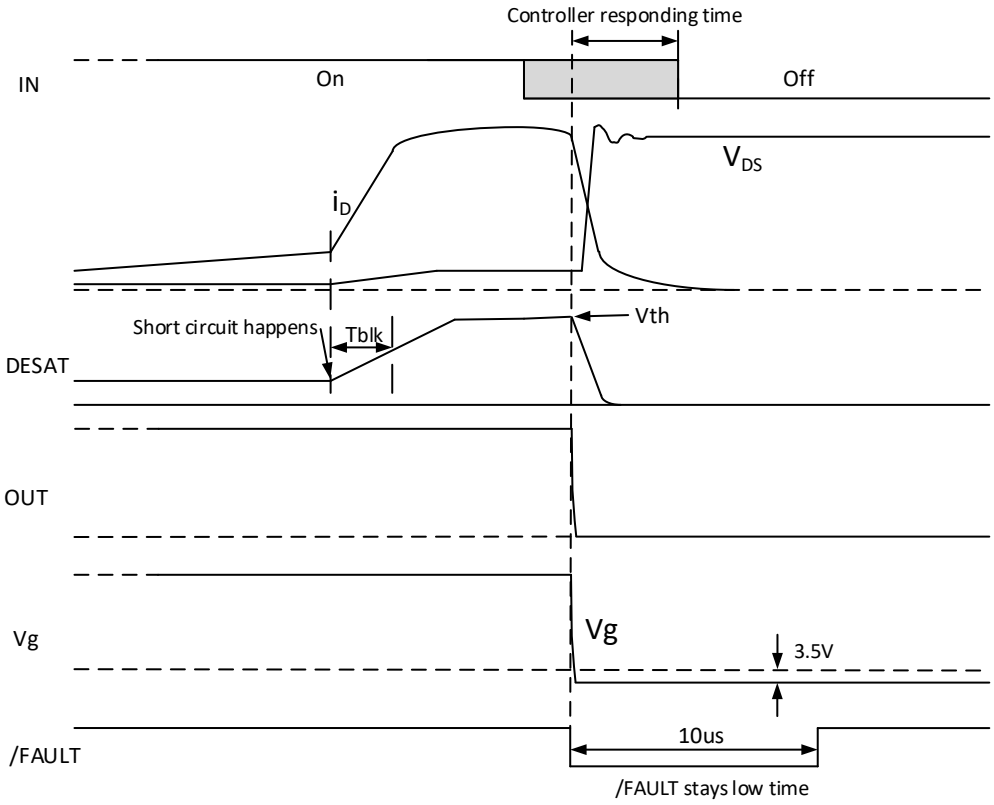
where R1 is a programming resistor, V_{F_D1} is high voltage diode forward voltage, R_{ds_on} is SiC MOSFET turn-on resistance at estimated junction temperature, such as 175C.

A different power system usually requires a different turn-off time. An optimized turn-off time can maximize the system short circuit capability while limiting Vds and bus voltage ringing.

7.6 Fault

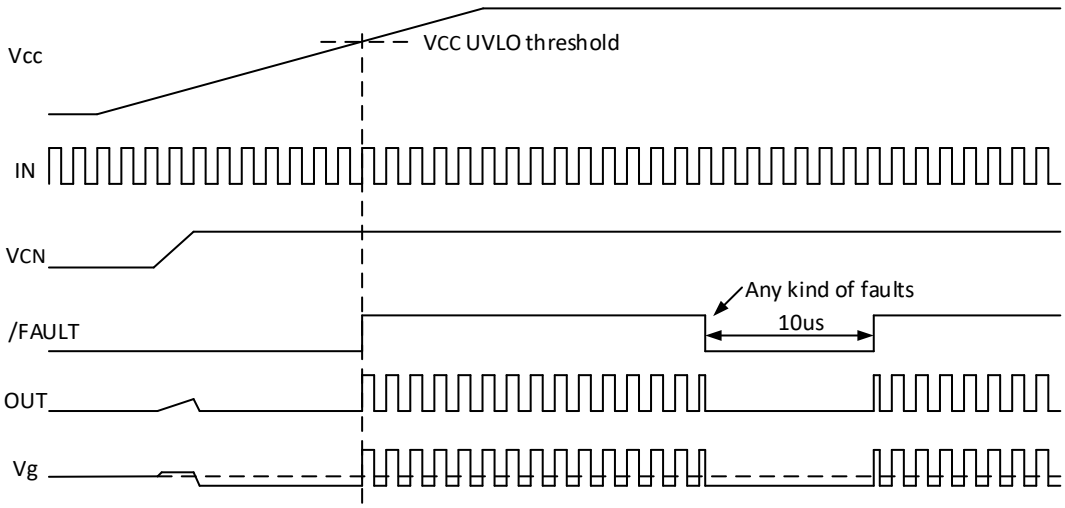
/FAULT is an open collector output with no internal pull-up resistance. When desaturation and under voltages are detected, the /FAULT pin and OUT are both pulled low. The /FAULT signal will stay at low for 10us after

the fault condition is removed. /FAULT is an auto recovery signal. System controller will need to decide how to respond the /FAULT signal. Following diagram shows the signal sequence.



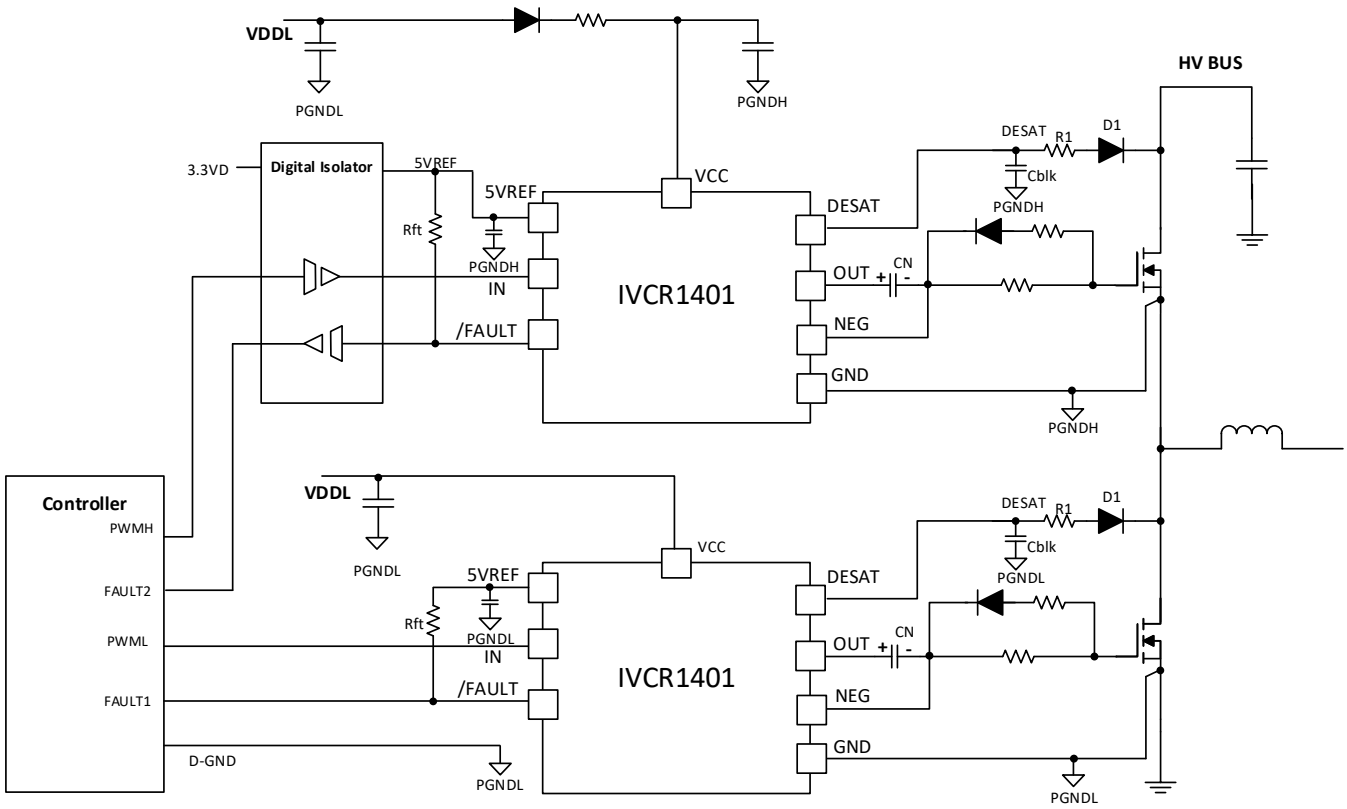
7.7 NEG

The external negative bias capacitor is quickly charged up when NEG goes low. It happens during power up and restart period right before 10us /FAULT low period expires after any fault is detected. During power up and restart period, the negative bias capacitor voltage V_{CN} is measured. As soon as the voltage is beyond VN UVLO threshold, NEG becomes high-impedance and OUT takes over gate drive control.



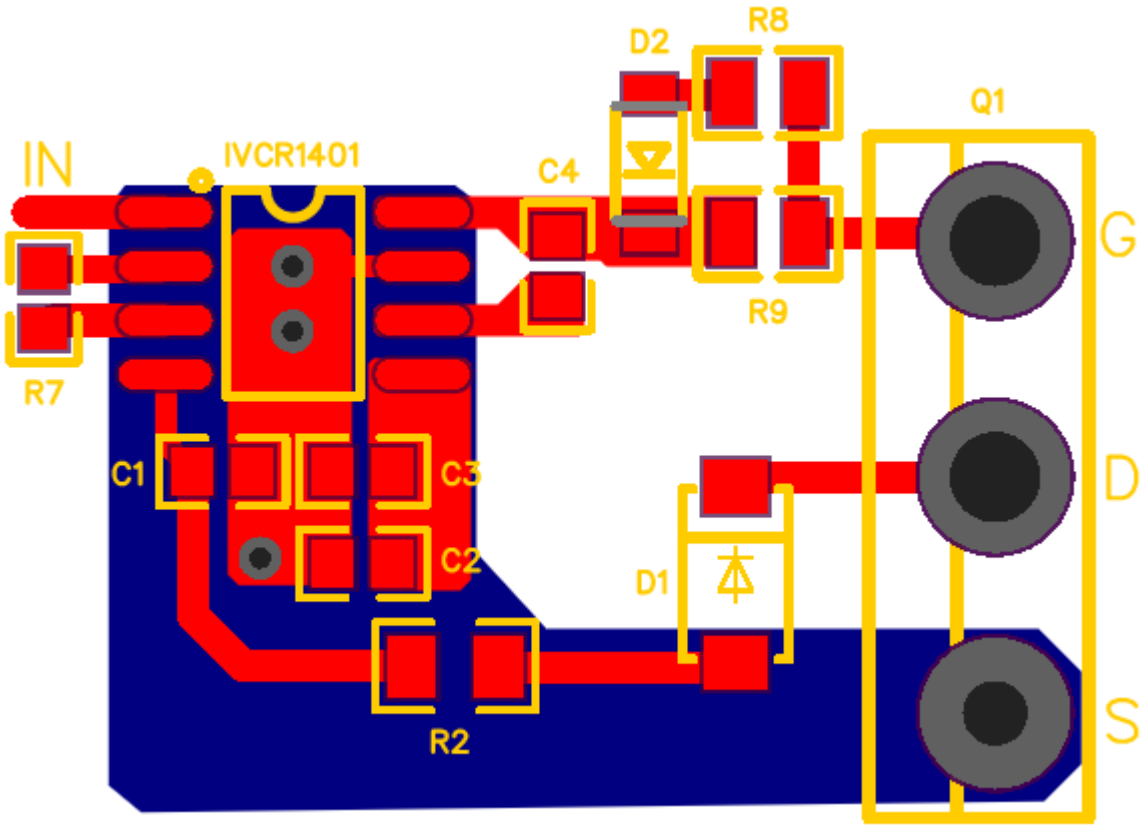
8 Applications and Implementation

IVCR1401 is an ideal driver for a compact design. It is a low-side driver. However, with a built-in negative voltage generator, the driver can be used as a high-side driver without using an isolated bias. A low-cost bootstrap can then be used instead. Following circuit diagram shows a typical half bridge driver application.



9 Layout

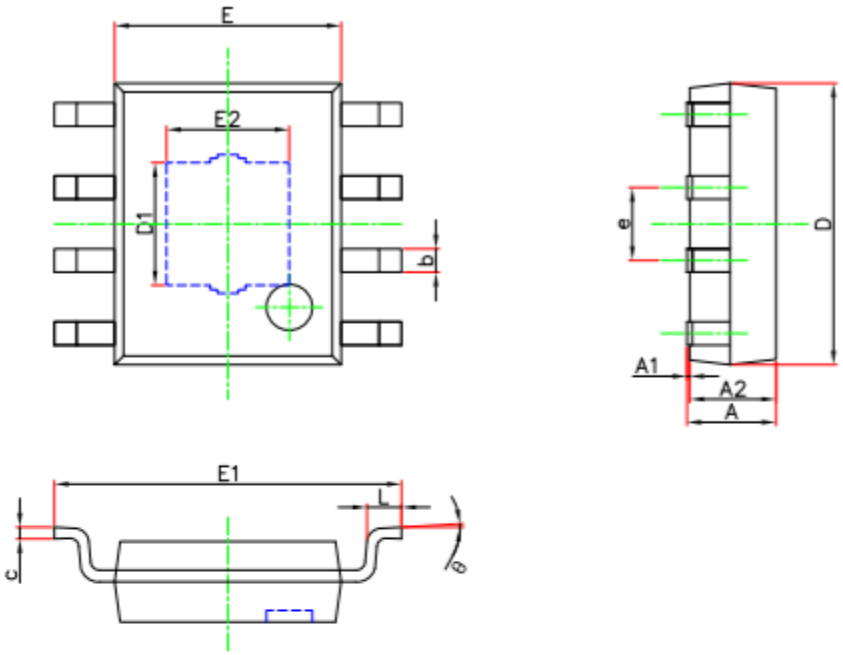
A good layout is a key step to achieve desired circuit performance. Solid ground is the first to start with. It is recommended to tie the exposed pad to the driver ground. It is a general rule that capacitors have a higher priority than resistors for location arrangement. A 1uF and a 0.1uF decoupling capacitors should be close to VCC pin and grounded to the driver ground plane. Negative voltage capacitor should locate near to OUT and NEG pins. Blanking capacitor should be close to the driver as well. A small filter (with10ns time constant) may be needed at the input of IN if the input signal traces have to pass through some noisy area. Following is a recommended layout.



Layout Example for IVCR1401

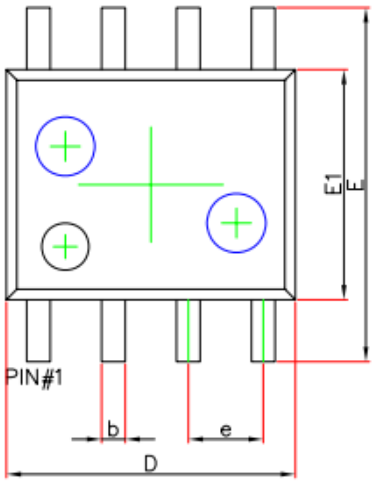
10 Packaging Information

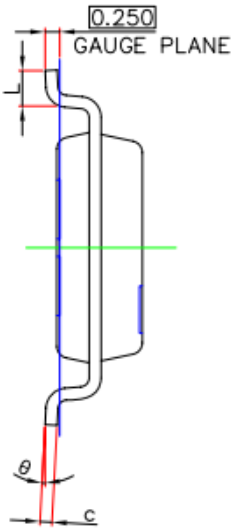
SOIC-8 (EP) Package Dimensions



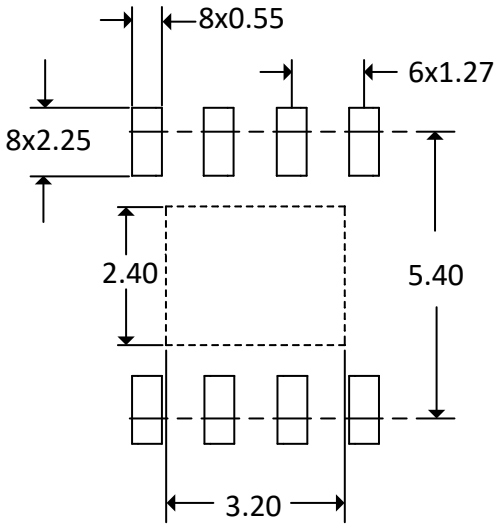
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	2.034	2.234	0.080	0.088
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.034	2.234	0.080	0.088
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOIC-8 Package Dimensions

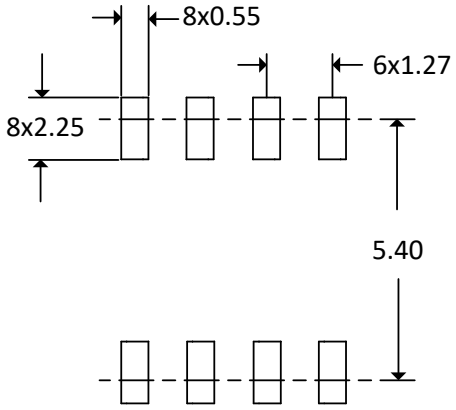




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



IVCR1401DP Recommended Soldering Dimensions



IVCR1401D Recommended Soldering Dimensions