RT9089AGQW DDR Termination Regulator Evaluation Board

Purpose

The RT9089A is a sink/source tracking termination regulator. This document explains the function and use of the RT9089A evaluation board (EVB), and provides information to enable operation, modification of the evaluation board and circuit to suit individual requirements.

Table of Contents

Introduction

General Product Information

The RT9089A is a sink/source tracking termination regulator. It is specifically designed for low-cost and lowexternal component count systems. The RT9089A possesses a high speed operating amplifier that provides fast load transient response and only requires a minimum 10μF ceramic output capacitor. The RT9089A supports remote sensing functions and all features required to power the DDRI/DDRII/DDRIII and Low Power DDRIII/DDRIV VTT bus termination according to the JEDEC specification. The RT9089A is available in the thermal efficient package, WDFN-10L 2x2.

Product Feature

- **VIN Input Voltage Range : 1.1V to 3.5V**
- **VCNTL Input Voltage Range : 2.9V to 5.5V**
- **Support Ceramic Capacitors**
- **10mA Source/Sink Reference Output**
- **Meet DDRI, DDRII JEDEC Spec**
- **Support DDRIII, Low Power DDRIII/DDRIV VTT Applications**
- **Soft-Start Function**
- **UVLO and OCP Protection**
- **Thermal Shutdown**

Applications

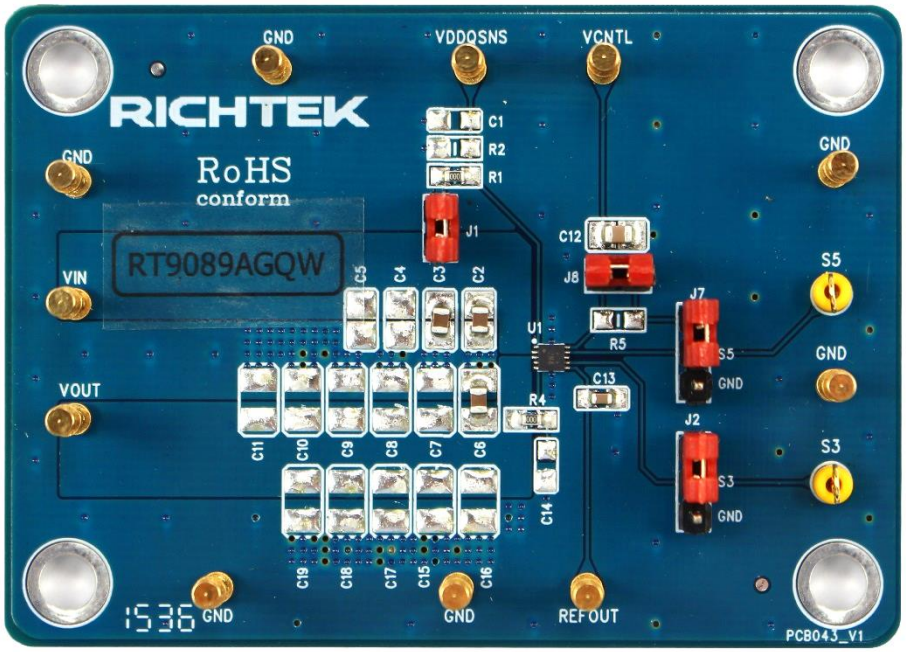
- **Notebook/Desktop/Server**
- **Telecom/Datacom, GSM Base Station, LCD-TV/PDPTV, Copier/Printer, Set-Top Box**

Key Performance Summary Table

Key Features	Evaluation Board Number : PCB043_V1
VIN Input Voltage Range	1.1V to 3.5V
VCNTL Input Voltage Range	2.9V to 5.5V
Max Output Current	2A
Default Output Voltage	Set by VDDQSNS pin voltage level (V_{OUT} = V_{DDQSNS} / 2)
Default Marking & Package Type	RT9089AGQW, WDFN-10L 2x2

Bench Test Setup Conditions

Headers Description and Placement



Please carefully inspect the EVB IC and external components, comparing them to the following Bill of Materials, to ensure that all components are installed and undamaged. If any components are missing or damaged during transportation, please contact the distributor or send e-mail to evb_service@richtek.com

Test Points

The EVB is provided with the test points and pin names listed in the table below.

Test point/ Pin name	Signal	Comment (expected waveforms or voltage levels on test points)
VIN	Input voltage	Power input of the regulator.
VOUT	Output voltage	Power output of the regulator.
VDDQSNS	Reference input	Reference input.
GND	Ground	Analog ground. Connect to negative terminal of the output capacitor. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
PGND	Power ground	Power ground of the regulator.
SENSE	Voltage sense input	Voltage sense input for the regulator. Connect to positive terminal of the output capacitor or the load.
REFOUT	Reference output	Reference output. Connect to GND through a 0.1µF ceramic capacitor.
S3	S3 signal input	S3 signal input.
S5	S5 signal input	S5 signal input.
VCNTL	Power good output test point	Control voltage input. Connect this pin to the 3.3V or 5V power supply. A ceramic decoupling capacitor with a value 4.7µF is required.

Power-up & Measurement Procedure

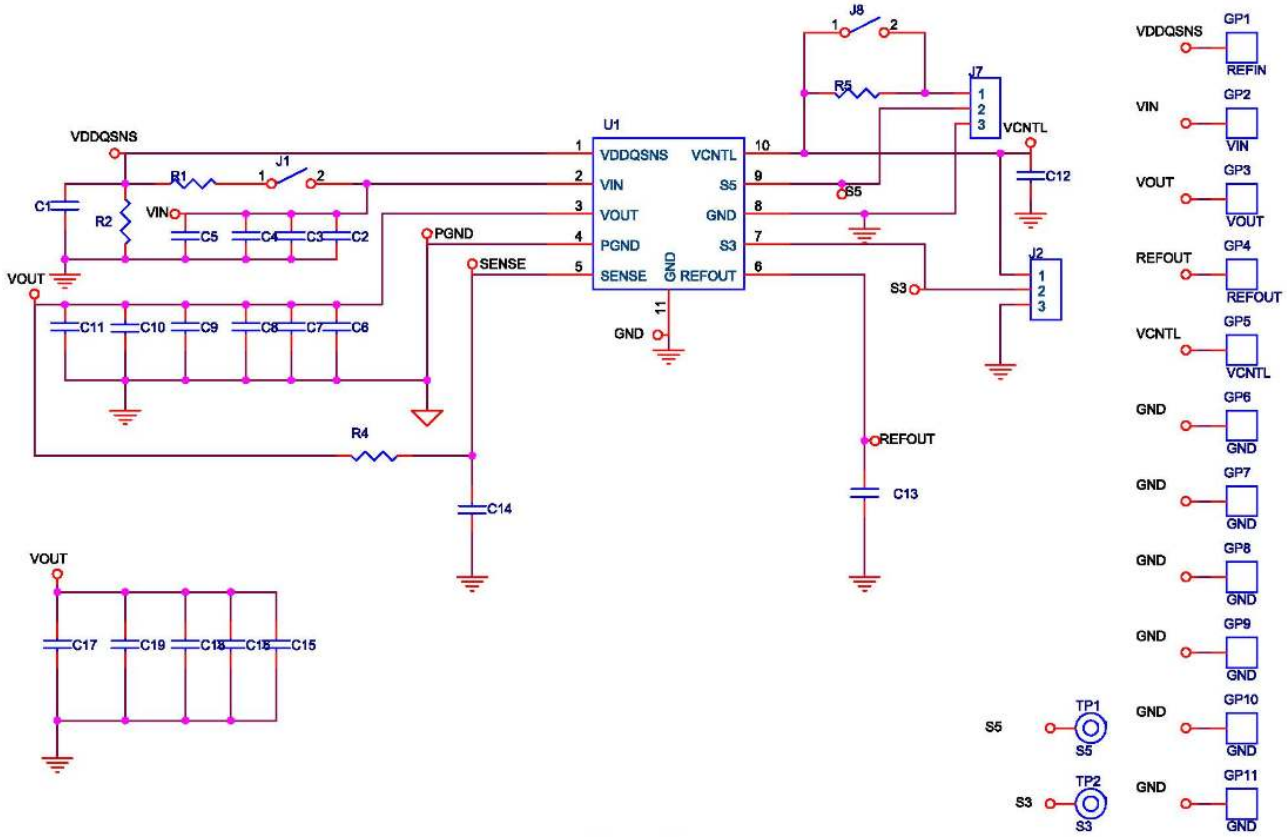
1. Short J1, J8, the (1, 2) pin of J2 and the (1, 2) pin of J7 by jumper respectively.
2. Provide input voltage (2.9V < V_{CNTL} < 5.5V) to VCNTL pin.
3. Connect input power (1.1V < V_{IN} < 3.5V) and input ground to VIN and GND pins respectively.
4. Connect positive end and negative end of load to VOUT and GND of output pins respectively.
5. The output voltage (V_{OUT}) can be set by the voltage level of VDDQSNS, since VDDQSNS is short with VIN :
   V_{OUT} = (V_{DDQSNS} / 2) = (V_{IN} / 2)

Specification

Parameter	Symbol	Min	Typ.	Max	Units
Control Input Voltage	V_{CNTL}	2.9		5.5	V
Supply Input Voltage	V_{IN}	1.1		3.5	V
VOUT Source Current Limit	$I_{LIM\_VOUT\_SR}$	2			A
VOUT Sink Current Limit	$I_{LIM\_VOUT\_SK}$	2			A

Schematic, Bill of Materials & Board Layout

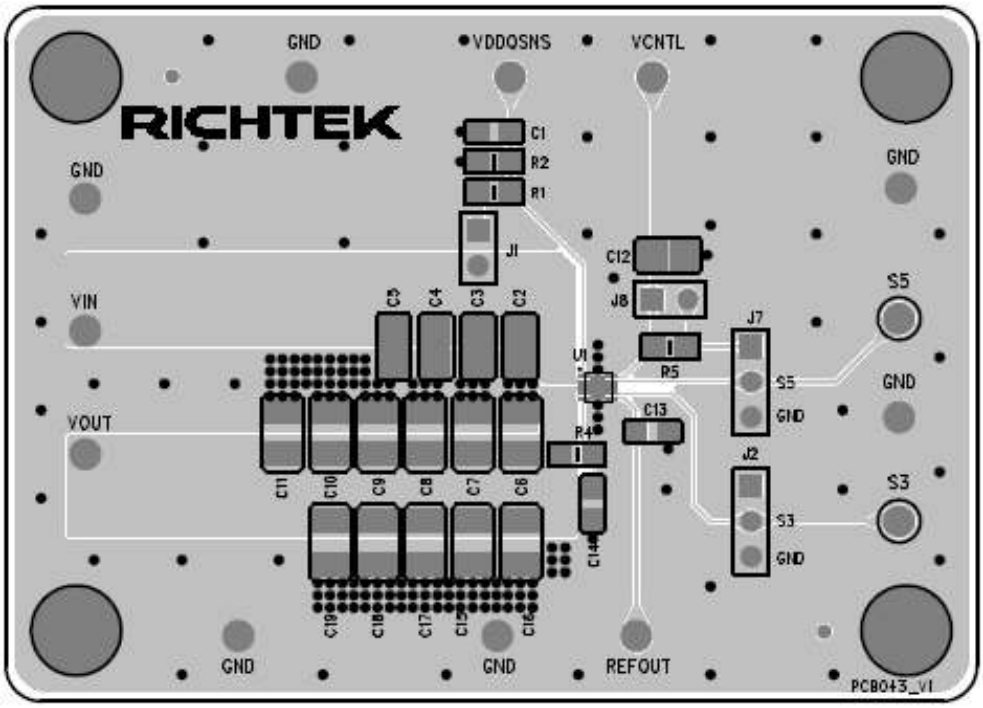
EVB Schematic Diagram



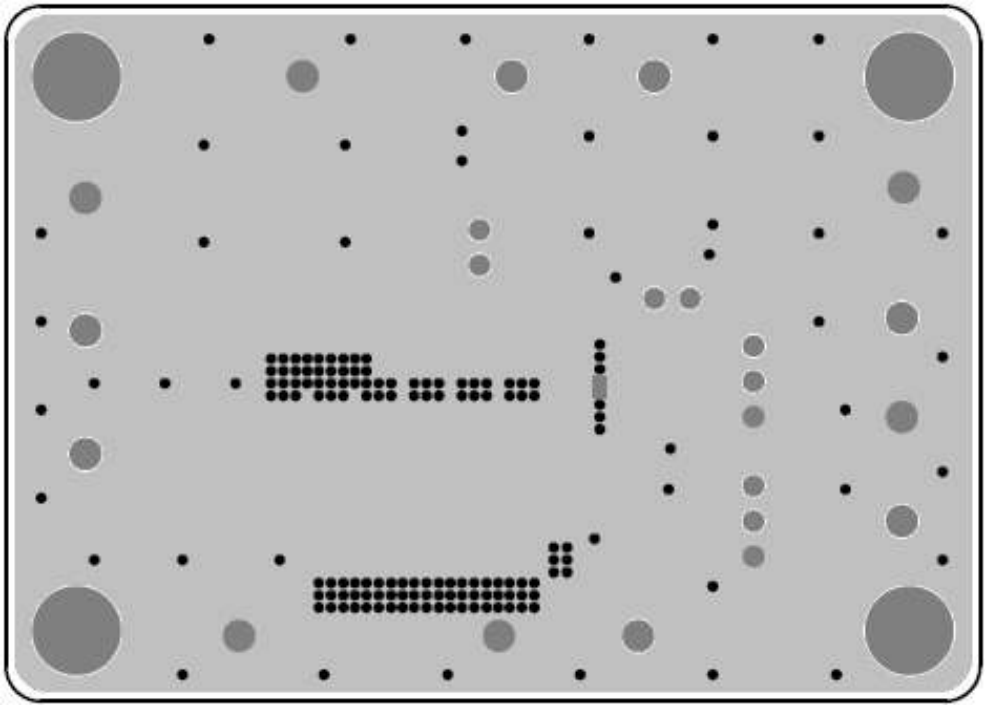
Bill of Materials

Reference	Qty	Part Number	Description	Package	Manufacture
U1	1	RT9089AGQW	DDR Termination Regulator	WDFN-10L 2x2	RICHTEK
C12	1	C2012X5R0J475KT00HW	4.7µF/6.3V/X5R	C-0805	TDK
C13	1	0805B104K500	0.1µF/50V/X7R	C-0805	WALSIN
C2, C3	2	C2012X5R1C106KT	10µF/16V/X5R	C-0805	TDK
C6	1	C2012X5R1C106KT	10µF/16V/X5R	C-0805	TDK
C1, C4, C5, C7, C8, C9, C10, C11, C14, C15, C16, C17, C18, C19, R2, R5	16		NC		
R1, R4	2		0Ω	R-0603	

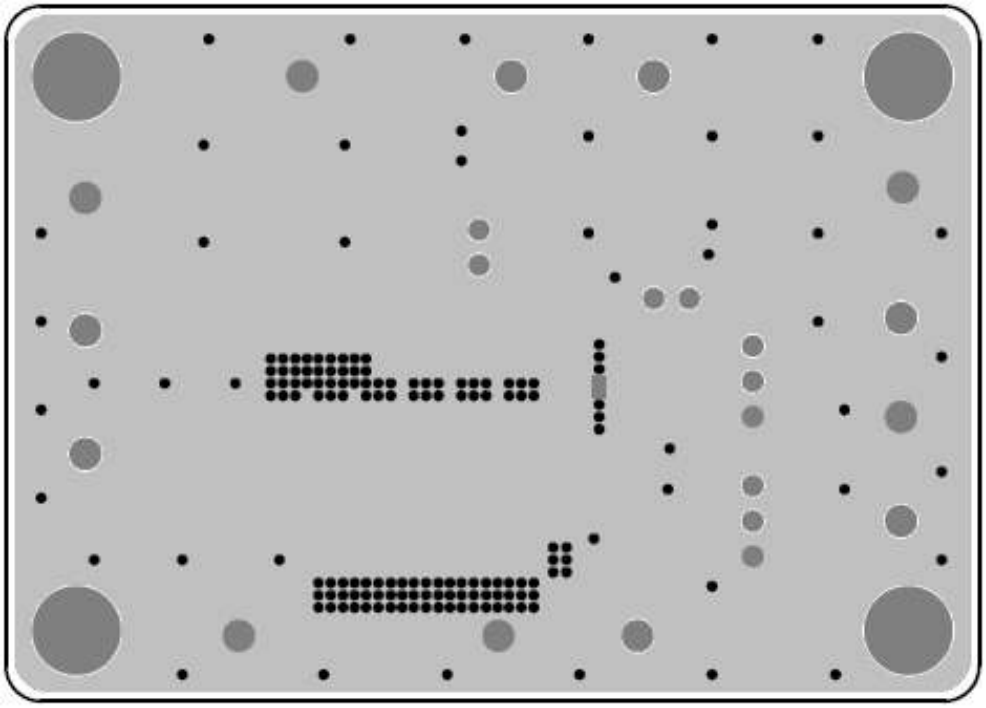
PCB Layout



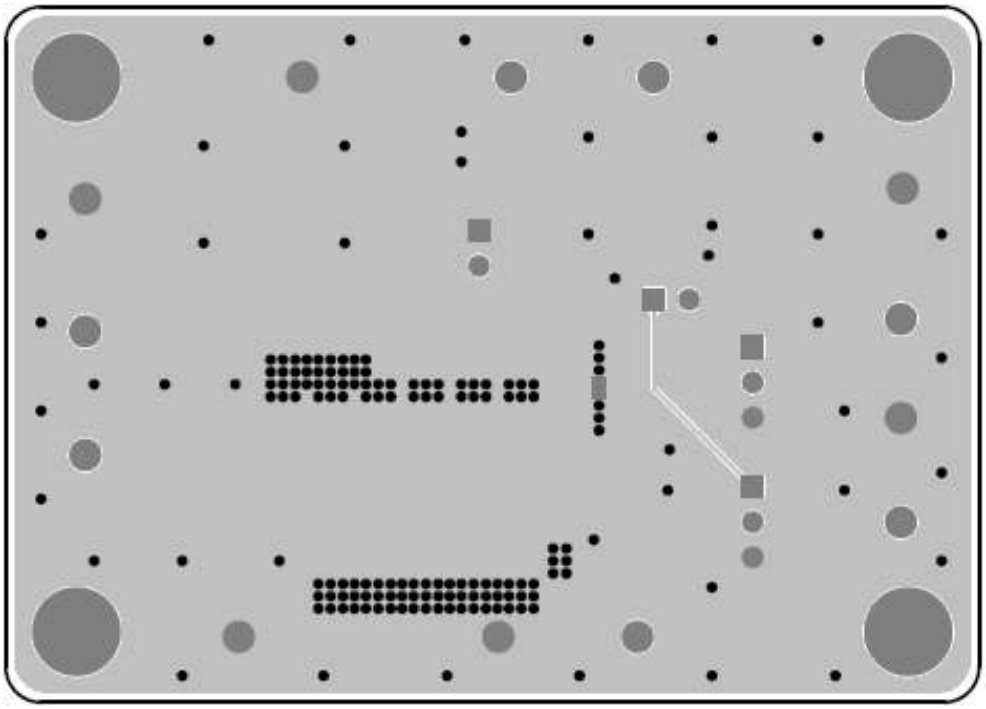
Top View (1st layer)



PCB Layout—Inner Side (2nd Layer)



PCB Layout—Inner Side (3rd Layer)



Bottom View (4th Layer)

More Information

For more information, please find the related datasheet or application notes from Richtek website http://www.richtek.com.

Important Notice for Richtek Evaluation Board