

## 100353 Low Power 8-Bit Register

### General Description

The 100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs ( $D_n$ ), true outputs ( $Q_n$ ), a clock input (CP), and a common clock enable pin ( $\overline{CEN}$ ). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the  $\overline{CEN}$  input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

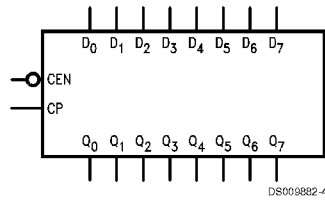
The 100353 output drivers are designed to drive 50 $\Omega$  termination to -2.0V. All inputs have 50 k $\Omega$  pull-down resistors.

### Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range

### Ordering Code:

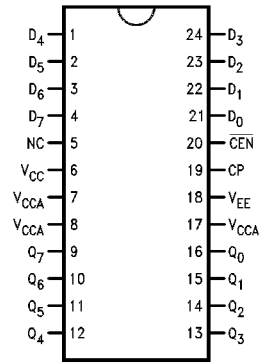
### Logic Symbol



Pin Names	Description
$D_0$ - $D_7$	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
$Q_0$ - $Q_7$	Data Outputs
NC	No Connect

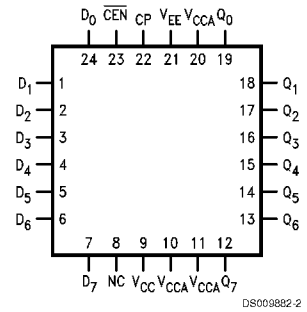
# Connection Diagrams

24-Pin DIP



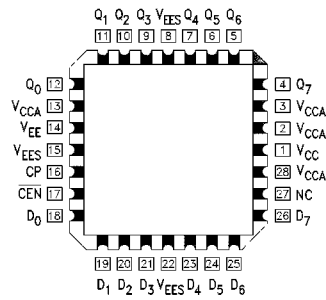
DS009882-1

24-Pin Quad Cerpak



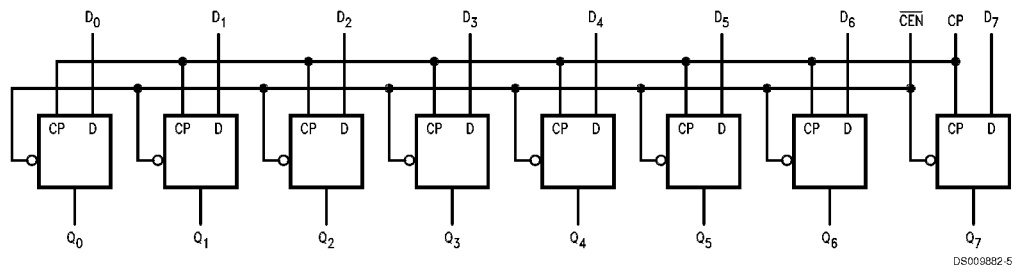
DS009882-2

28-Pin PCC



DS009882-3

## Logic Diagram



## Truth Table

Inputs			Outputs
D <sub>n</sub>	$\overline{\text{CEN}}$	CP	Q <sub>n</sub>
L	L	↗	L
H	L	↗	H
X	X	L	NC
X	X	H	NC
X	H	X	NC

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 NC = No Change  
 ↗ = LOW to HIGH Transition

## Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
Plastic	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to + 0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

## Commercial Version

### DC Electrical Characteristics (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) or $V_{IL}$ (Max)	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610	mV		
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for all Inputs	
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for all Inputs	
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current			240	μA	$V_{IN} = V_{IH}$ (Max)	
$I_{EE}$	Power Supply Current	-119		-61	mA	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	
		-122		-61			

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DIP AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	425		425		425		MHz	Figures 1, 2
$t_{PLH}$	Propagation Delay	1.40	3.00	1.40	3.00	1.50	3.10	ns	Figures 1, 2
$t_{PHL}$	CP to Output								(Note 4)
$t_{TLH}$	Transition Time	0.45	2.00	0.45	2.00	0.45	2.00	ns	Figures 1, 2
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time								
	$D_n$	1.10		1.10		1.10		ns	Figures 1, 3
	$\overline{CEN}$ (Disable Time)	0.40		0.40		0.40			
	$\overline{CEN}$ (Release Time)	1.10		1.10		1.10			
$t_h$	Hold Time							ns	Figures 1, 4
	$D_n$	0.10		0.10		0.10			
$t_{pw}(H)$	Pulse Width HIGH							ns	Figures 1, 2
	CP	2.00		2.00		2.00			

**Note 4:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## PCC and Cerpack AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	425		425		425		MHz	Figures 1, 2
$t_{PLH}$	Propagation Delay	1.40	2.80	1.40	2.80	1.50	2.90	ns	Figures 1, 2
$t_{PHL}$	CP to Output								(Note 6)
$t_{TLH}$	Transition Time	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 2
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time								
	$D_n$	1.00		1.00		1.00		ns	Figures 1, 3
	$\overline{CEN}$ (Disable Time)	0.30		0.30		0.30			
	$\overline{CEN}$ (Release Time)	1.00		1.00		1.00			
$t_h$	Hold Time $D_n$	0		0		0		ns	Figures 1, 4
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 2
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 5)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 5)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		260		260		260	ps	PCC Only (Note 5)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		280		280		280	ps	PCC Only (Note 5)

**Note 5:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ( $t_{OSHL}$ ), or LOW to HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

**Note 6:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Industrial Version PCC

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$  (Note 7)

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}$ (Max)	Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620	mV	or $V_{IL}$ (Min)	
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}$ (Min)	Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage		-1565		-1610	mV	or $V_{IL}$ (Max)	
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for all Inputs	
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for all Inputs	
$I_{IL}$	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL}$ (Min)	
$I_{IH}$	Input HIGH Current		240		240	μA	$V_{IN} = V_{IH}$ (Max)	
$I_{EE}$	Power Supply Current	-119	-61	-119	-61	mA	Inputs Open	
		-122	-61	-122	-61		$V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$	

**Note 7:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## PCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$f_{max}$	Toggle Frequency	425		425		425		MHz	Figures 1, 2
$t_{PLH}$	Propagation Delay	1.40	2.80	1.40	2.80	1.50	2.90	ns	Figures 1, 2
$t_{PHL}$	CP to Output								(Note 8)
$t_{TLH}$	Transition Time	0.40	2.50	0.45	1.90	0.45	1.90	ns	Figures 1, 2
$t_{THL}$	20% to 80%, 80% to 20%								
$t_s$	Setup Time								
	$D_n$	0.60		1.00		1.00		ns	Figures 1, 3
	$\overline{CEN}$ (Disable Time)	0.90		0.30		0.30			
$\overline{CEN}$ (Release Time)	1.40		1.00		1.00				
$t_h$	Hold Time $D_n$	0.30		0		0		ns	Figures 1, 4
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 2

**Note 8:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Military Version—Preliminary

### DC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Max) Loading with $50\Omega$ to $-2.0V$	(Notes 9, 10, 11)
		-1085	-870	mV	$-55^\circ C$		
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IL}$ (Min)	(Notes 9, 10, 11)
		-1830	-1555	mV	$-55^\circ C$		
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Min) Loading with $50\Omega$ to $-2.0V$	(Notes 9, 10, 11)
		-1085		mV	$-55^\circ C$		
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IL}$ (Max)	(Notes 9, 10, 11)
			-1555	mV	$-55^\circ C$		
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed HIGH Signal for all Inputs	(Notes 9, 10, 11, 12)
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^\circ C$ to $+125^\circ C$	Guaranteed LOW Signal for all Inputs	(Notes 9, 10, 11, 12)
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 9, 10, 11)
$I_{IH}$	Input HIGH Current		240	$\mu A$	$0^\circ C$ to $+125^\circ C$	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 9, 10, 11)
			340	$\mu A$	$-55^\circ C$		
$I_{EE}$	Power Supply Current	-125	-50	mA	$-55^\circ C$ to $+125^\circ C$	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$	(Notes 9, 10, 11)
		-130				$V_{EE} = -4.2V$ to $-5.7V$	

**Note 9:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 10:** Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.

**Note 11:** Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**Note 12:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$f_{max}$	Toggle Frequency	400		400		400		MHz	Figures 1, 2	(Note 16)
$t_{PLH}$	Propagation Delay	0.70	3.30	0.80	3.10	0.80	3.80	ns	Figures 1, 2	(Notes 13, 14, 15, 17)
$t_{PHL}$	CP to Output									
$t_{TLH}$	Transition Time	0.40	2.50	0.40	2.40	0.40	2.70	ns		
$t_{THL}$	20% to 80%, 80% to 20%									
$t_s$	Setup Time								Figures 1, 3	(Note 16)
	$D_n$	0.60		0.60		0.60		ns		
	$\overline{CEN}$ (Disable Time)	0.90		0.70		0.90				
	$\overline{CEN}$ (Release Time)	1.40		1.40		2.10				
$t_h$	Hold Time $D_n$	0.30		0.30		0.30		ns	Figures 1, 4	(Note 16)
$t_{pw(H)}$	Pulse Width HIGH CP	2.00		2.00		2.00		ns	Figures 1, 2	(Note 16)

**Note 13:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

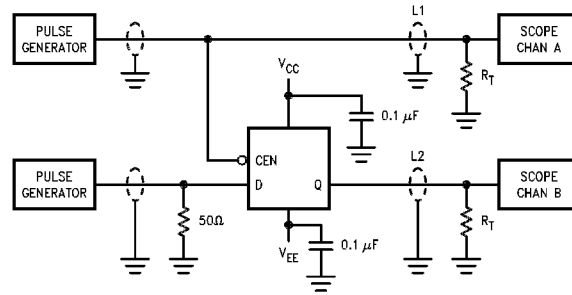
**Note 14:** Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.

**Note 15:** Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$ , temperatures, Subgroups A10 and A11.

**Note 16:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

**Note 17:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Test Circuitry



DS00982-6

### Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1  $\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with 50Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

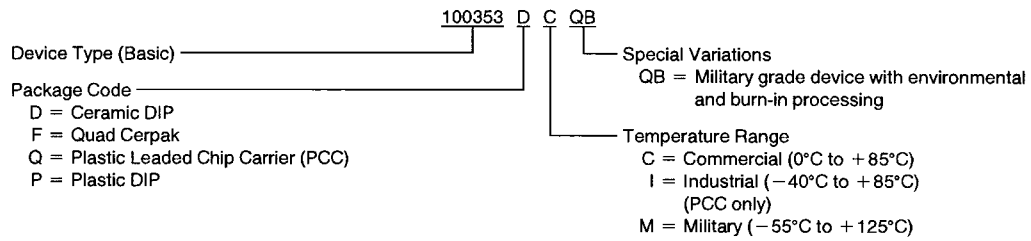
FIGURE 1. AC, Toggle Frequency Test Circuit





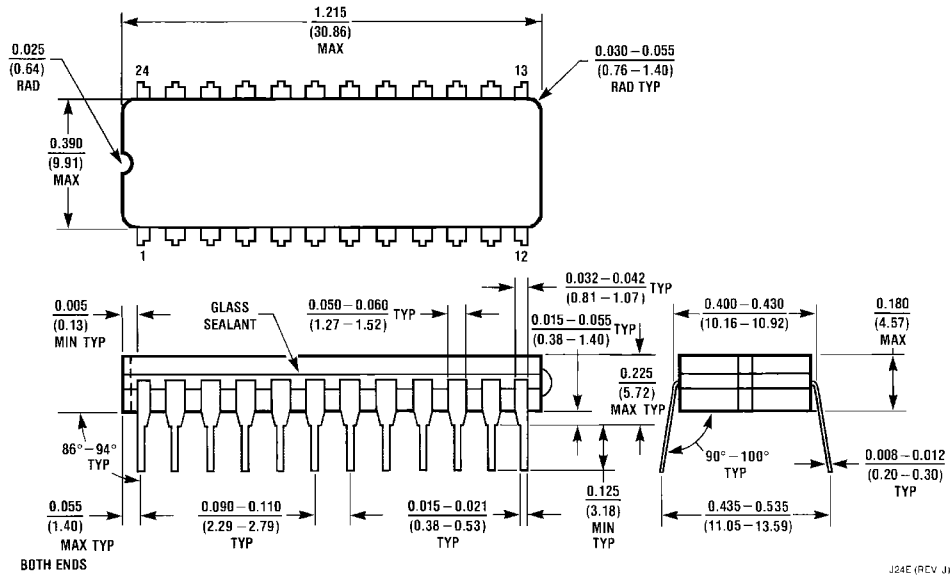
## Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

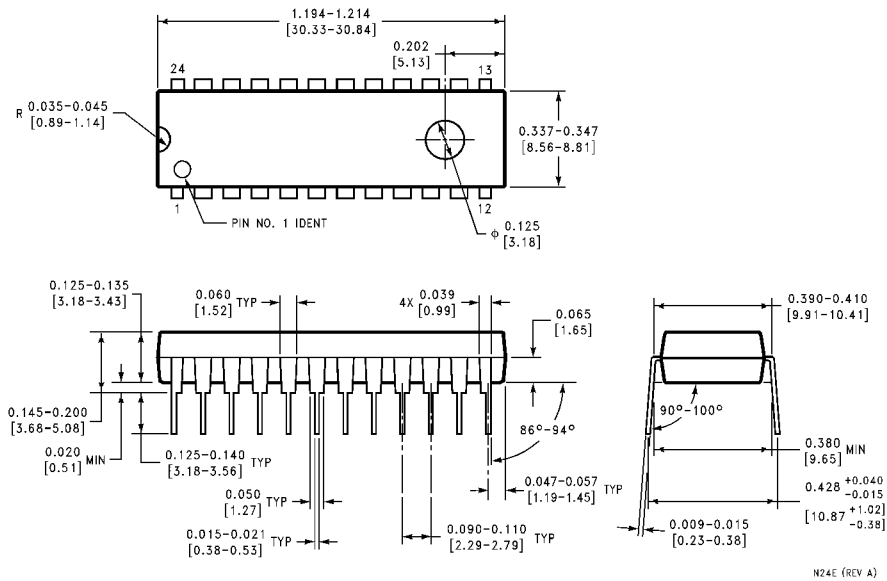


DS09882-11

**Physical Dimensions** inches (millimeters) unless otherwise noted

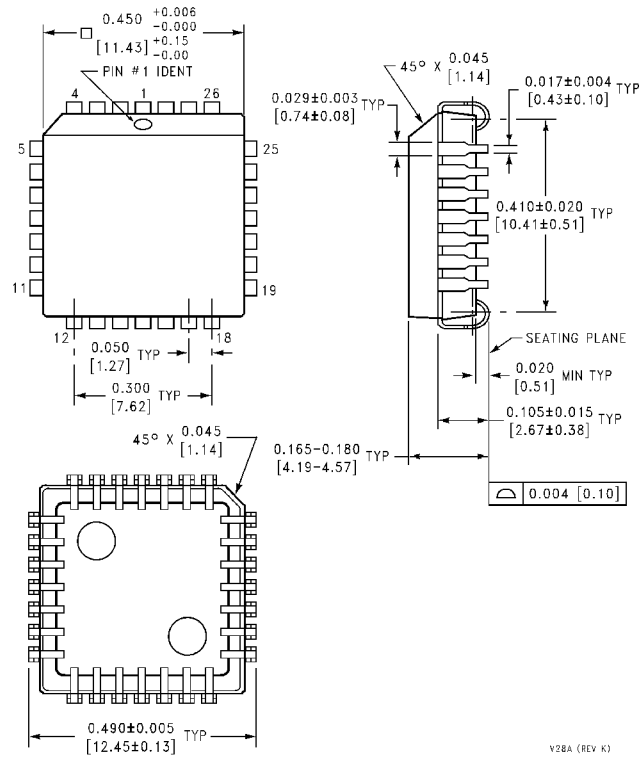


**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**  
Package Number J24E



**24-Lead Plastic Dual-In-Line Package (P)**  
Package Number N24E

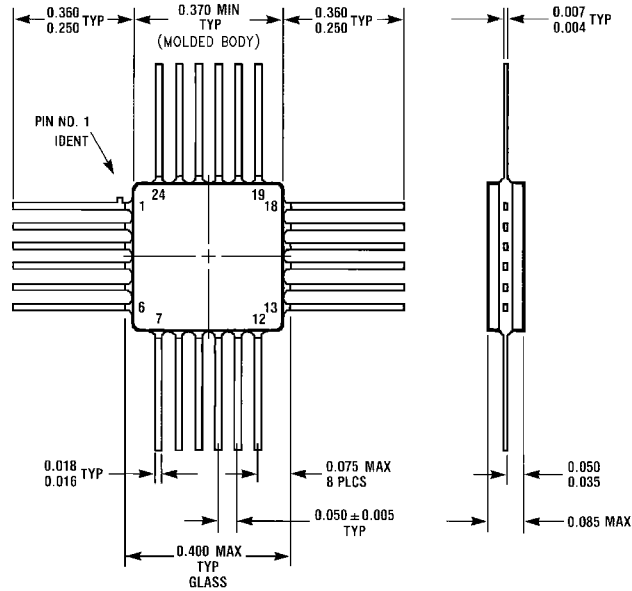
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Chip Carrier (Q)  
Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24 Lead Quad Cerpak (F)  
Package Number W24B**

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