TS12A12511 5-Ω Single-Channel SPDT Analog Switch With Negative Signaling Capability

1 Features

- ±2.7-V to ±6-V dual supply
- 2.7-V to 12-V single supply
- 5-Ω (typical) ON-state resistance
- 1.6-Ω (typical) ON-state resistance flatness
- 3.3-V, 5-V compatible digital control inputs
- Rail-to-rail analog signal handling
- Fast t_{ON}, t_{OFF} times
- Supports both digital and analog signal applications
- Tiny 8-lead SOT-23, 8-lead MSOP, and QFN-8 packages
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - ±2000-V Human Body Model (A114-B, Class II)
  - ±1000-V Charged-Device Model (C101)

2 Applications

- Automatic test equipment
- Power routing
- Communication systems
- Data acquisition systems
- Sample-and-hold systems
- Relay replacement
- Grid Infrastructure

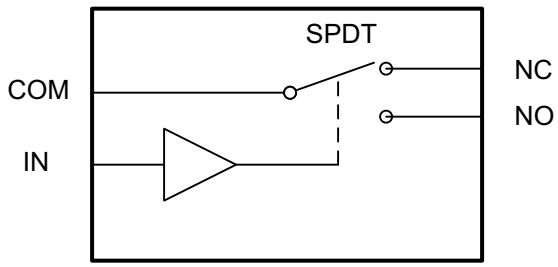
3 Description

The TS12A12511 is a bidirectional, single-channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or –6 V to 6 V. This switch conducts equally well in both directions when it is on. The device also offers a low ON-state resistance of 5 Ω (typical), which is matched to within 1 Ω between channels. The maximum current consumption is <1 µA and –3 dB bandwidth is >93 MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available packaged in an 8-lead VSSOP, 8-lead SOT-23, and a 8-pin WSON.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS12A12511	DCN (SOT-23, 8)	2.90 mm × 1.63 mm
	DGK (VSSOP, 8)	3.00 mm × 3.00 mm
	DRJ (WSON, 8)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2019) to Revision E (September 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Applications* section	1
• Updated the *Leakage Current vs I/O Voltage (Switch ON)* and *Leakage Current vs I/O Voltage (Switch OFF)* figures	8

Changes from Revision C (January 2015) to Revision D (January 2019)	Page
• Added Junction temperature to the *Absolute Maximum Ratings* table	4

Changes from Revision B (April 2011) to Revision C (January 2015)	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision A (May 2010) to Revision B (April 2011)	Page
• Deleted preview status from DGK and DCN packages	3

5 Pin Configuration and Functions

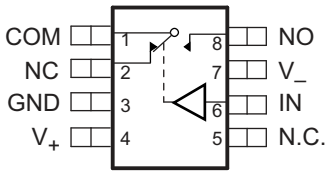


Figure 5-1. DGK Package, 8-Pin VSSOP (Top View)

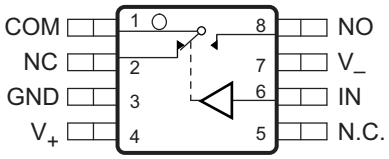
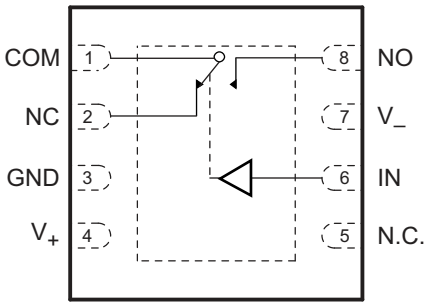


Figure 5-2. DCN Package, 8-Pin SOT-23 (Top View)



N.C. – Not internally connected NC – Normally closed NO – Normally open
The Exposed Thermal Pad must be electrically connected to V_ or left floating.

Figure 5-3. DRJ Package, 8-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COM	1	I/O	Common. Can be an input or output.
GND	3	—	Ground (0 V) reference
IN	6	I	Logic control input
NC	2	I/O	Normally closed. Can be an input or output.
N.C.	5	—	No connect. Not internally connected.
NO	8	I/O	Normally open. Can be an input or output.
V_{CC}	4	I	Most positive power supply
$-V_{CC}$	7	I	Most negative power supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
Thermal pad		—	The Exposed Thermal Pad must be electrically connected to V_ or left floating.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_{CC} to $-V_{CC}$			0	13	V
V_{CC} to GND			–0.3	13	V
$-V_{CC}$ to GND			–6.5	0.3	V
$V_{I/O}$	Analog inputs	NC, NO, or COM	$-V_{CC}$ – 0.5	V_{CC} + 0.5	V
I_{IN}	Digital inputs			±30	mA
$I_{I/O}$	Peak current	NC, NO, or COM		±100	mA
	Continuous current	NC, NO, or COM		±50	mA
T_A	Operating temperature		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{CC}	0	12	V
$-V_{CC}$	–6	0	V
$V_{I/O}$	$-V_{CC}$	V_{CC}	V
V_{IN}	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS12A12511			UNIT
		DCN	DGK	DRJ	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.4	184.5	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.9	71.0	48.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	144.4	104.5	24.2	
ψ_{JT}	Junction-to-top characterization parameter	7.8	11.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	141.7	103.3	24.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	9.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ±5-V Dual Supply

V_{CC} = 5 V ± 10%, $–V_{CC}$ = –5 V ± 10%, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					$-V_{CC}$		V_{CC}	V
R_{ON}	ON-state resistance	V_{NC} = -4.5 V to +4.5 V or V_{NO} = –4.5 V to 4.5 V, I_{COM} = –10 mA; see Figure 7-1		5			5	8	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V, I_{COM} = –10 mA		1	1.2			1.6	Ω
$R_{ON(flat)}$	ON-state resistance flatness	V_{NC} = -3.3 V to +3.3 V or V_{NO} = -3.3 V to +3.3 V, I_{COM} = –10 mA		1.6	2.2			2.2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V V_{COM} = -4.5 V to +4.5 V; see Figure 7-2	–1	±0.5	1	–50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = -4.5 V to +4.5 V or V_{NO} = -4.5 V to +4.5 V V_{COM} = open; see Figure 7-3	–1	±0.5	1	–50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					2.4		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		0.005		–1		1	µA
C_{IN}	Control input capacitance			2.5					pF
DYNAMIC(1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 7-5		80	95			115	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V		41	50			56	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 7-6		36		18			ns
Q_C	Charge injection	V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 7-7		26					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 7-8		–70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 7-9		–70					dB
BW	Bandwidth –3 dB	R_L = 50 Ω, C_L = 5 pF; see Figure 7-10		93					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15pF, VNO = 1V_{RMS}, f = 20 kHz; see Figure 7-11		0.004%					
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz; see Figure 7-4		14					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz; see Figure 7-4		60					pF
SUPPLY									
I_{CC}	Positive supply current			0.03				1	µA

(1) Specified by design, not subject to production test.

6.6 Electrical Characteristics: 12-V Single Supply

V_{CC} = 12 V ± 10%, -V_{CC} = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} =0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = –10 mA, see Figure 7-1		5			5	8	Ω
ΔR_{on}	ON-state resistance match between channels	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, I_{COM} = –10 mA		1.6	2.4			2.6	Ω
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} = 3.3 V to 7V or V_{NO} = 3.3 V to 7 V, I_{COM} = –10 mA		1.7			1.8	3.2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} = 0 V to 10.8 V or V_{NO} = 0 V to 10.8 V, V_{COM} = 0 V to 10.8 V; see Figure 7-2	–10	±0.5	10	–50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = 0 V to 10.8V or V_{NO} = 0 V to 10.8 V, V_{COM} = open; see Figure 7-3	–10	±0.5	10	–50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					5		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		±0.005		–0.1		0.1	µA
C_{IN}	Digital input capacitance			2.7					pF
DYNAMIC (1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 7-5		56	85			110	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 7-5		25	30			31	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 7-6		30		19			ns
Q_C	Charge injection	R_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 7-7		491					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 7-8		–70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 7-9		–70					dB
BW	Bandwidth –3 dB	R_L = 50 Ω, C_L = 5 pF, see Figure 7-10		200					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15pF, V_{NO} = 1 V_{RMS}, f = 20 kHz; see Figure 7-11		0.04%					
$C_{NC(OFF)}$, $CI_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz, see Figure 7-4		14					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $C_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz, see Figure 7-4		55					pF
SUPPLY									
I_{CC}	Positive supply current			0.07				1	µA

(1) Specified by design, not subject to production test.

6.7 Electrical Characteristics: 5-V Single Supply

V_{CC} = 5 V ± 10%, -V_{CC} = 0 V, GND = 0 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A= 25°C			T_A= –40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
	Analog signal range					0		V_{CC}	V
R_{on}	ON-state resistance	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA; see Figure 7-1		8	10			12.5	Ω
ΔR_{on}	ON-state resistance match between channels	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA		1	1.1			1.5	Ω
$R_{on(flat)}$	ON-state resistance flatness	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, I_{COM} = –10 mA		1.3			1.3	2	Ω
LEAKAGE CURRENTS									
$I_{NC(OFF)}$, $I_{NO(OFF)}$	OFF leakage current	V_{NC} =0 V to 4.5 V or V_{NO} = 0 V to 4.5 V, V_{COM} = 0 V to 4.5 V; see Figure 7-2	–1	±0.5	1	–50		50	nA
$I_{NC(ON)}$, $I_{NO(ON)}$	ON leakage current	V_{NC} = 0 V to 4.5V or V_{NO} = 0 V to 4.5 V, V_{COM} = open; see Figure 7-3	–1	±0.5	1	–50		50	nA
DIGITAL INPUTS									
V_{INH}	High-level input voltage					2.4		V_{CC}	V
V_{INL}	Low-level input voltage					0		0.8	V
I_{INL}, I_{INH}	Input current	V_{IN} = V_{INL} or V_{INH}		0.01		–0.1		0.1	µA
C_{IN}	Digital input capacitance			2.8					pF
DYNAMIC(1)									
t_{ON}	Turn-ON time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 7-5		119	145			178	ns
t_{OFF}	Turn-OFF time	R_L = 300 Ω, C_L = 35 pF, V_{COM} = 3.3 V; see Figure 7-5		38	47			95.2	ns
t_{BBM}	Break-before-make time delay	R_L = 300 Ω, C_L = 35 pF, V_{NC} = V_{NO} = 3.3 V; see Figure 7-6		79		44			ns
Q_C	Charge injection	V_{GEN} = V_{NC} = V_{NO} = 0 V, R_{GEN} = 0 Ω, C_L = 1 nF; see Figure 7-7		65					pC
O_{ISO}	OFF isolation	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 7-8		–70					dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 7-9		–70					dB
BW	Bandwidth –3 dB	R_L = 50 Ω, see Figure 7-10		152					MHz
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF, V_{NO} = 1 VRMS, f = 20 kHz; see Figure 7-11		0.04%					
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	f = 1 MHz, see Figure 7-4		15					pF
$C_{COM(ON)}$, $C_{NC(ON)}$, $I_{NO(ON)}$	COM, NC, NO ON capacitance	f = 1 MHz, see Figure 7-4		55					pF
POWER REQUIREMENTS									
I_{CC}	Positive supply current	V_{IN} = 0 V or V_{CC}		0.02				1	µA

(1) Specified by design, not subject to production test.

6.8 Typical Characteristics

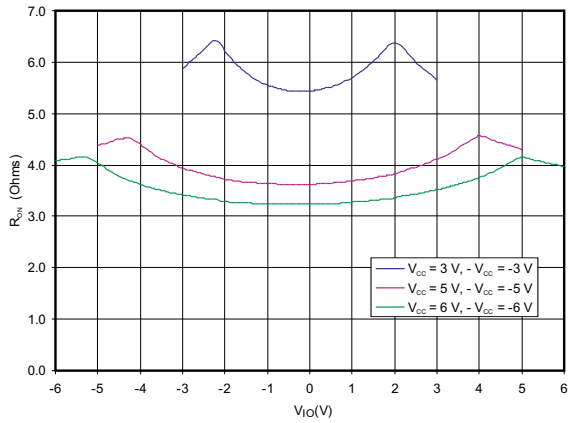


Figure 6-1. R_{ON} vs V_{IO}

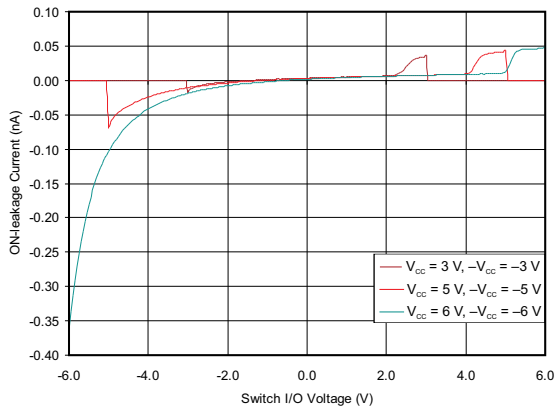


Figure 6-2. Leakage Current vs I/O Voltage (Switch ON)

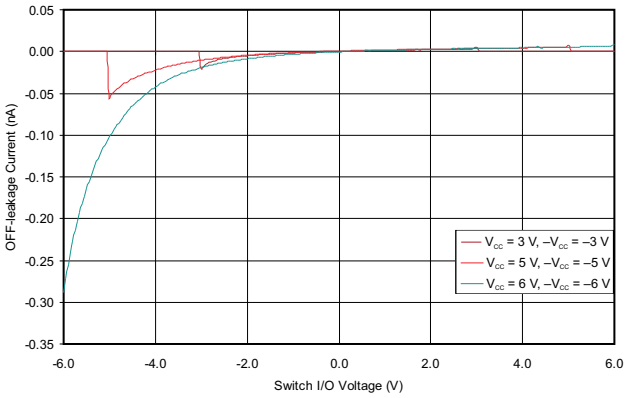


Figure 6-3. Leakage Current vs I/O Voltage (Switch OFF)

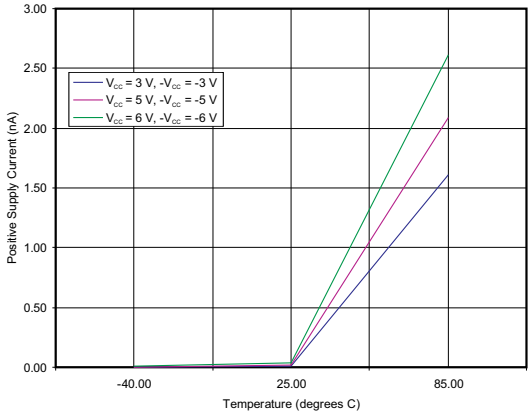


Figure 6-4. Positive Supply Current vs Temperature

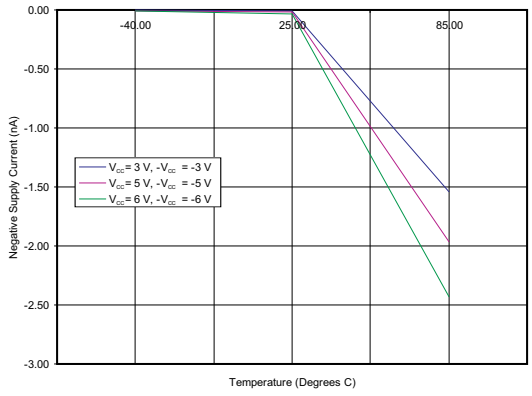


Figure 6-5. Negative Supply Current vs Temperature

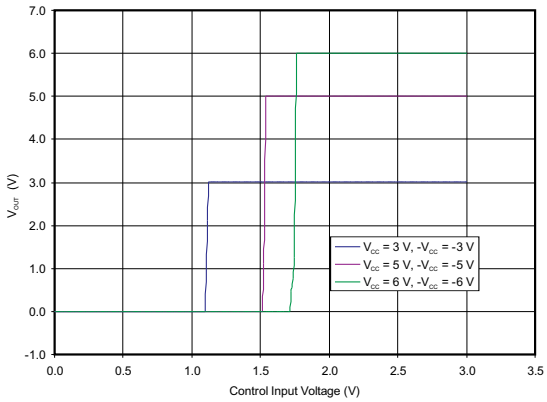


Figure 6-6. Control Input (IN) Threshold Voltage

6.8 Typical Characteristics (continued)

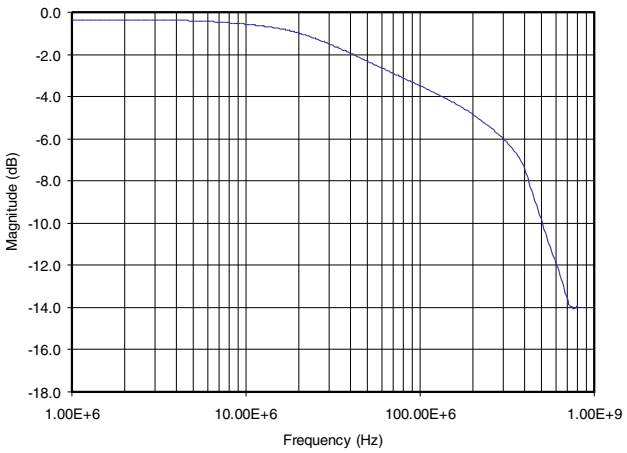


Figure 6-7. Bandwidth Dual Supply (±5 V)

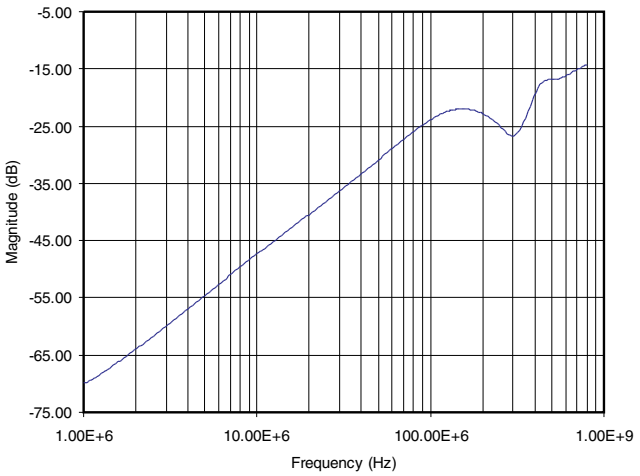


Figure 6-8. Off Isolation vs Frequency Dual Supply (±5 V)

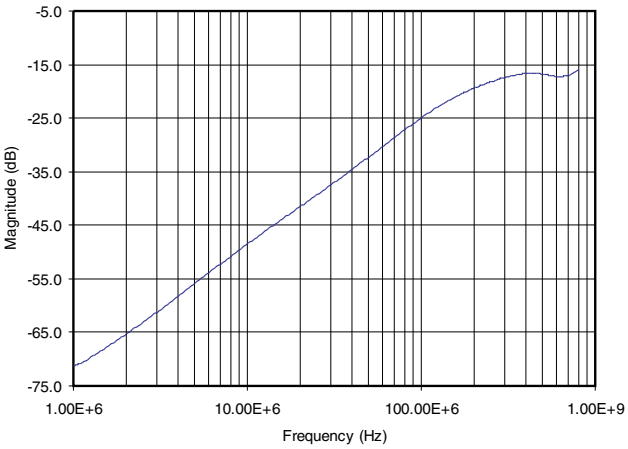


Figure 6-9. Crosstalk vs Frequency Dual Supply (±5 V)

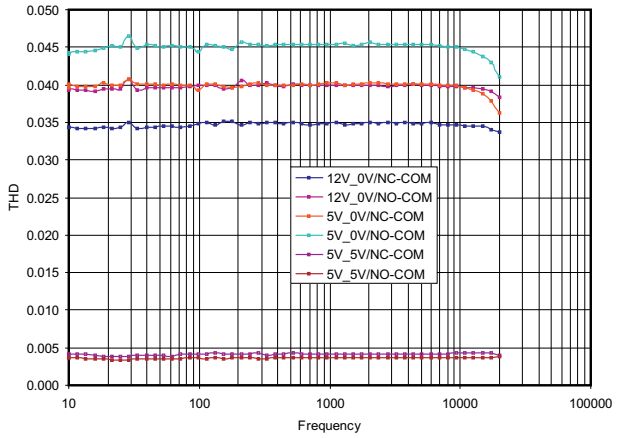


Figure 6-10. THD+N (%) vs Frequency

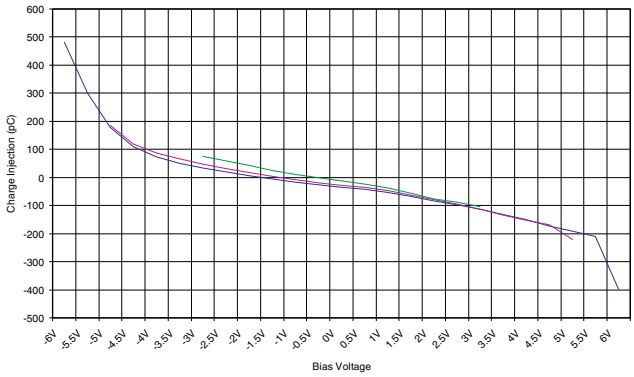
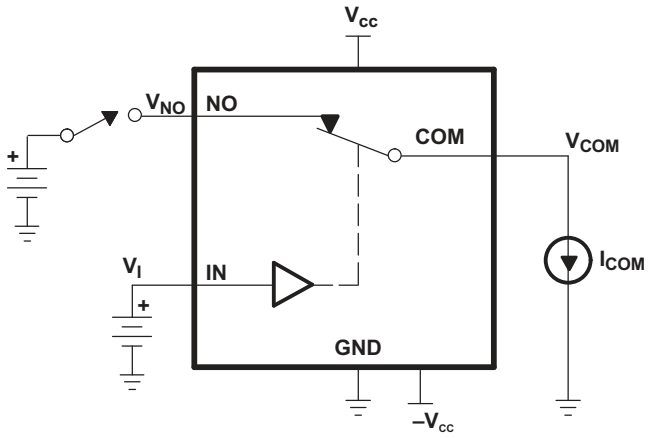


Figure 6-11. Charge Injection vs Bias Voltage

7 Parameter Measurement Information

7.1 Test Circuits

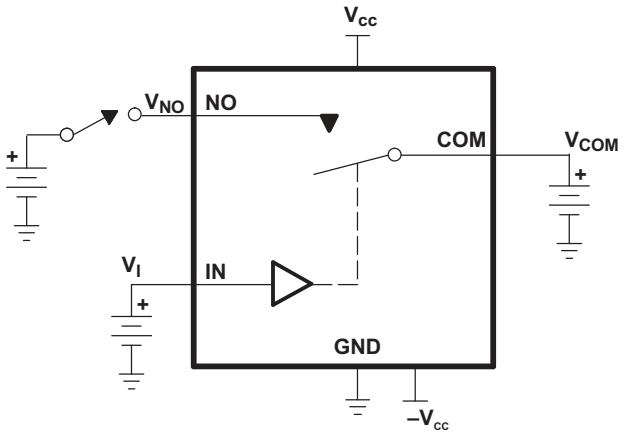


Channel ON

$R_{on} = \frac{V_{COM} - V_{NO}}{I_{COM}}$

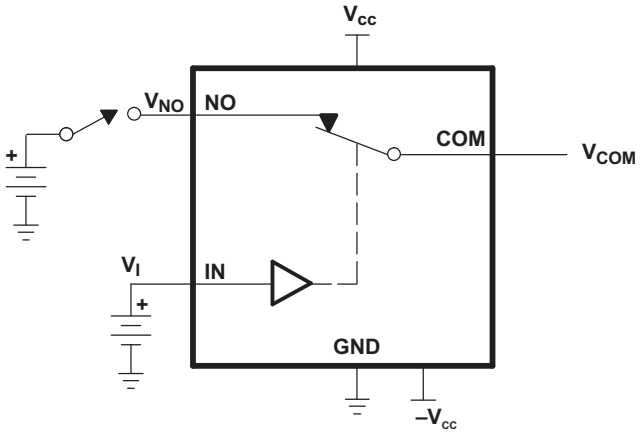
$V_I = V_{IH}$ or V_{IL}

Figure 7-1. ON-State Resistance



OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}

Figure 7-2. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$)



ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

Figure 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

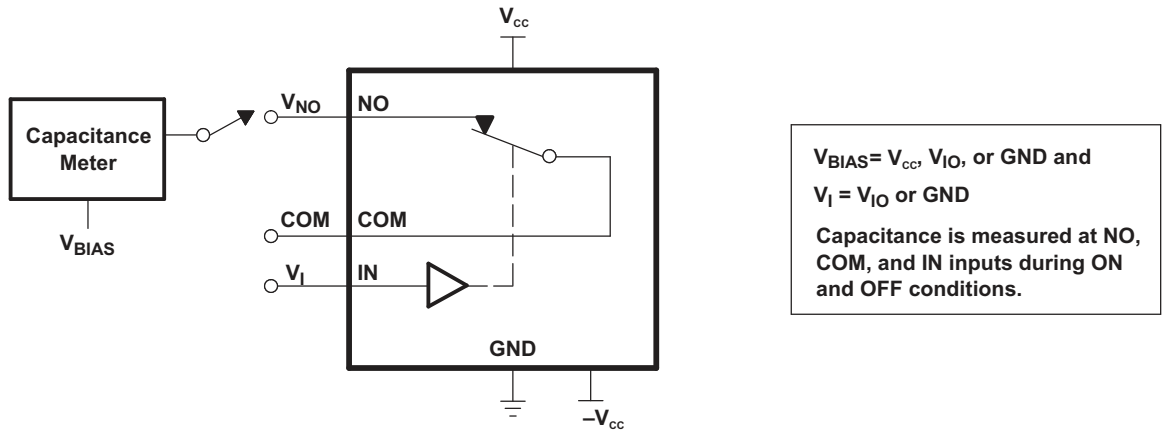
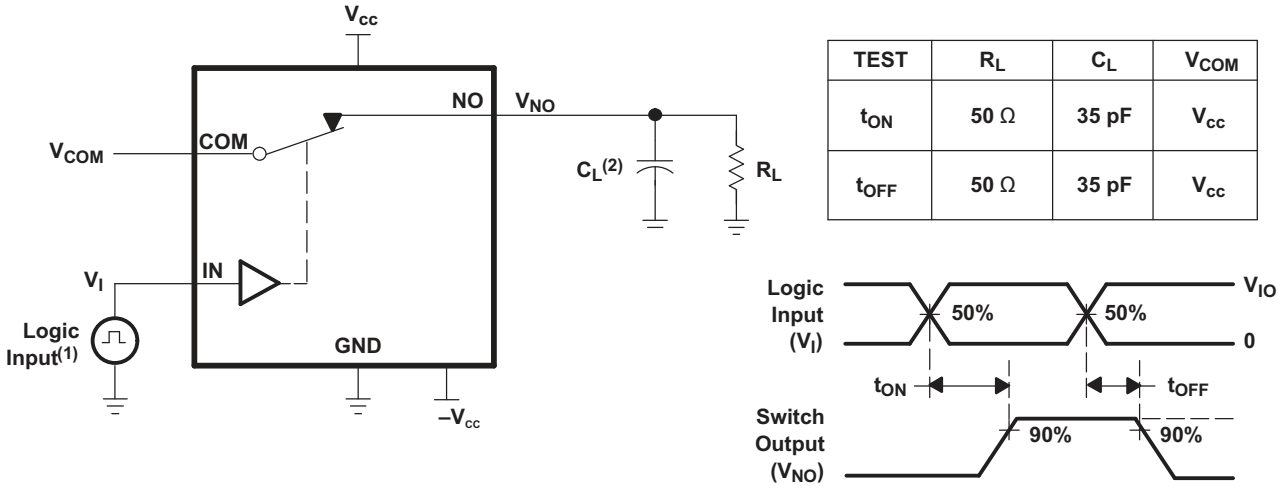


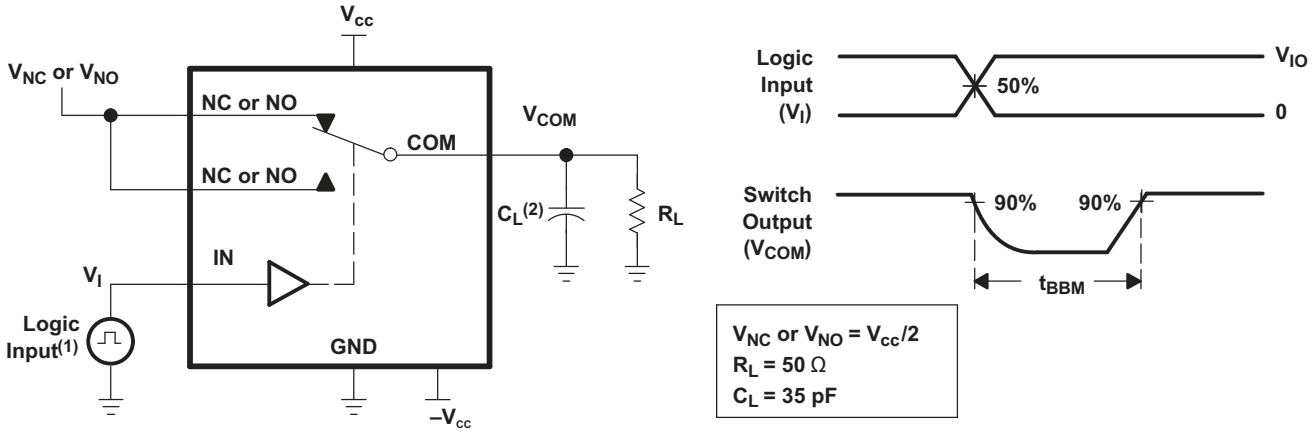
Figure 7-4. Capacitance ($C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{cc}
t_{OFF}	50 Ω	35 pF	V_{cc}

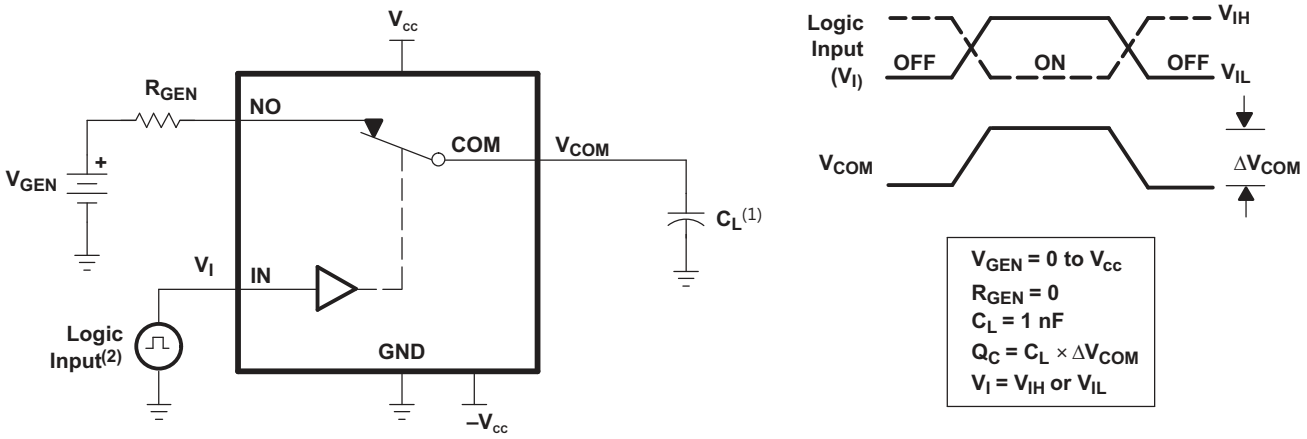
(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 7-5. Turn-ON (t_{ON}) and Turn-OFF Time (t_{OFF})



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 7-6. Break-Before-Make Time Delay (t_{BBM})



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 7-7. Charge Injection (Q_C)

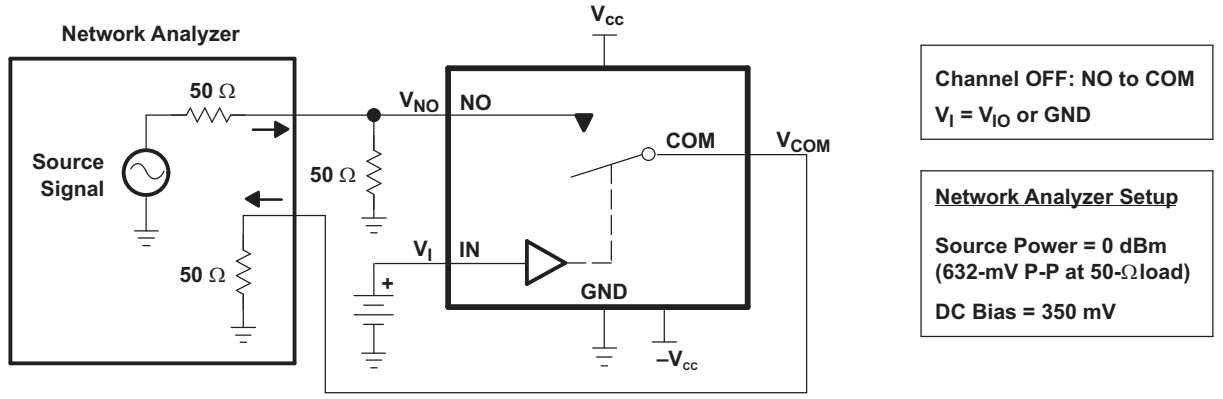


Figure 7-8. OFF Isolation (O_{ISO})

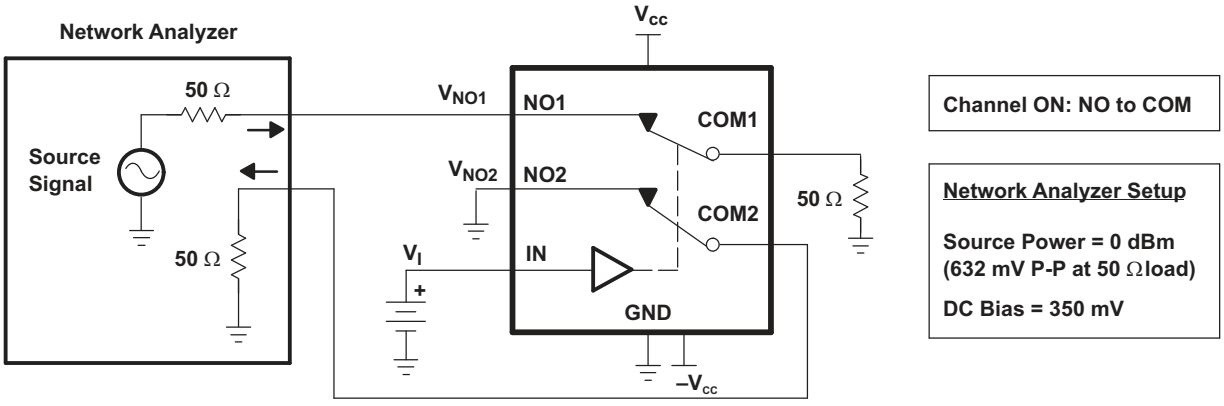


Figure 7-9. Channel-to-Channel Crosstalk (X_{TALK})

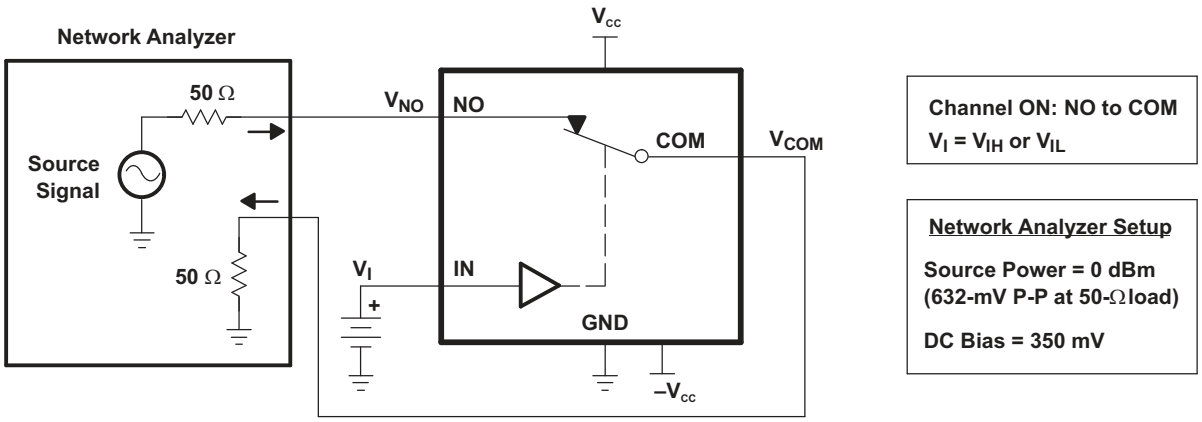
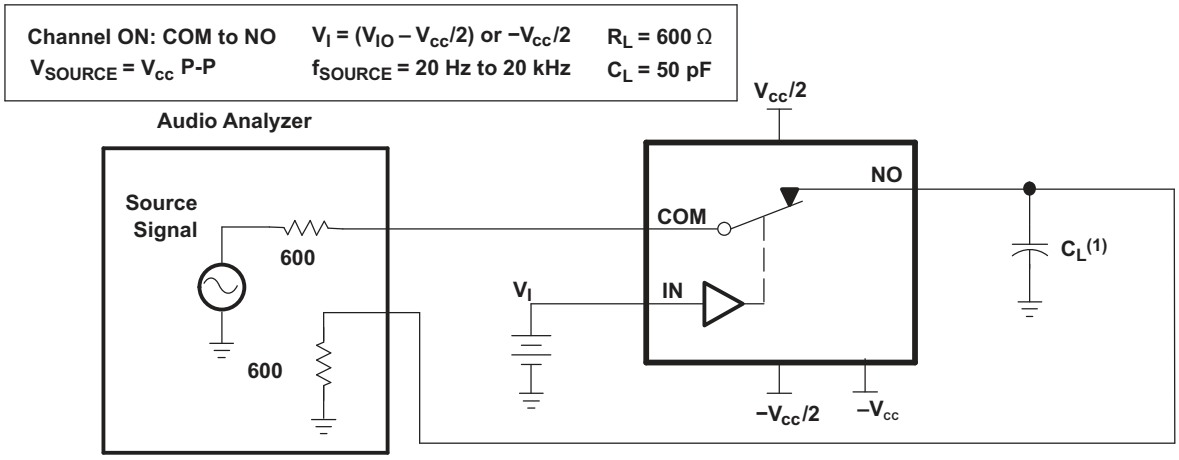


Figure 7-10. Bandwidth (BW)



(1) C_L includes probe and jig capacitance.

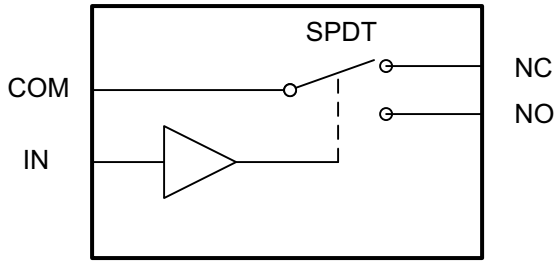
Figure 7-11. Total Harmonic Distortion

8 Detailed Description

8.1 Overview

The TS12A12511 is a bidirectional, single channel, single-pole double-throw (SPDT) analog switch that can pass signals with swings of 0 to 12 V or –6 V to 6 V. This switch conducts equally well in both directions when it is on. It also offers a low ON-state resistance of 5 Ω (typical), which is matched to within 1 Ω between channels. The maximum current consumption is < 1 µA and –3 dB bandwidth is > 93 MHz. The TS12A12511 exhibits break-before-make switching action, preventing momentary shorting when switching channels. This device is available in an 8-lead MSOP, 8-lead SOT-23, and 8-pin QFN package.

8.2 Functional Block Diagram



8.3 Feature Description

The TS12A12511 can pass signals with swings of 0 to 12 V or –6 V to 6. The device is great for applications where the AC signals do not have a common mode voltage since both the positive and negative swing of the signal can be passed through the device with little distortion.

8.4 Device Functional Modes

Table 8-1. Truth Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	On	Off
H	Off	On

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Analog signals that range over the entire supply voltage (V_{CC} to GND) or (V_{CC} to -V_{CC}) can be passed with very little change in ON-state resistance. The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

9.2 Typical Application

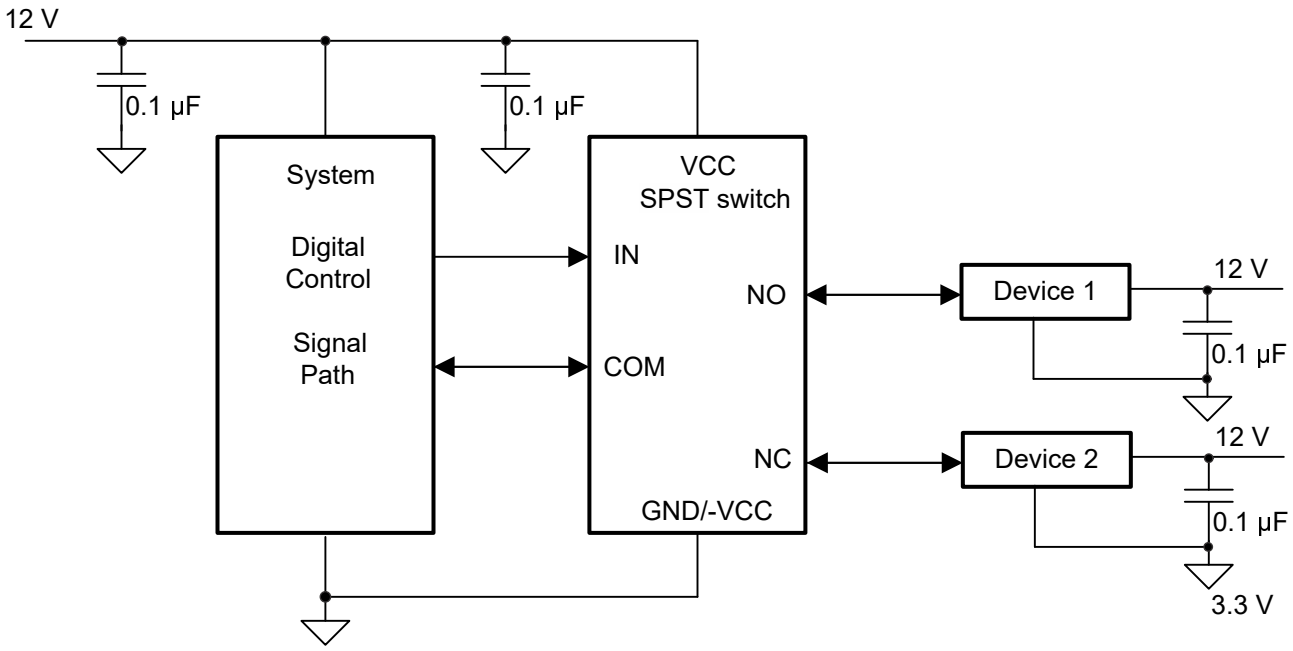


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

Pull the digitally controlled input select pin IN to VCC or GND to avoid unwanted switch states that could result if the logic control pin is left floating.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch since the TS12A12511 input or output signal swing of the device is dependant of the supply voltage V_{CC} and -V_{CC}.

9.2.3 Application Curve

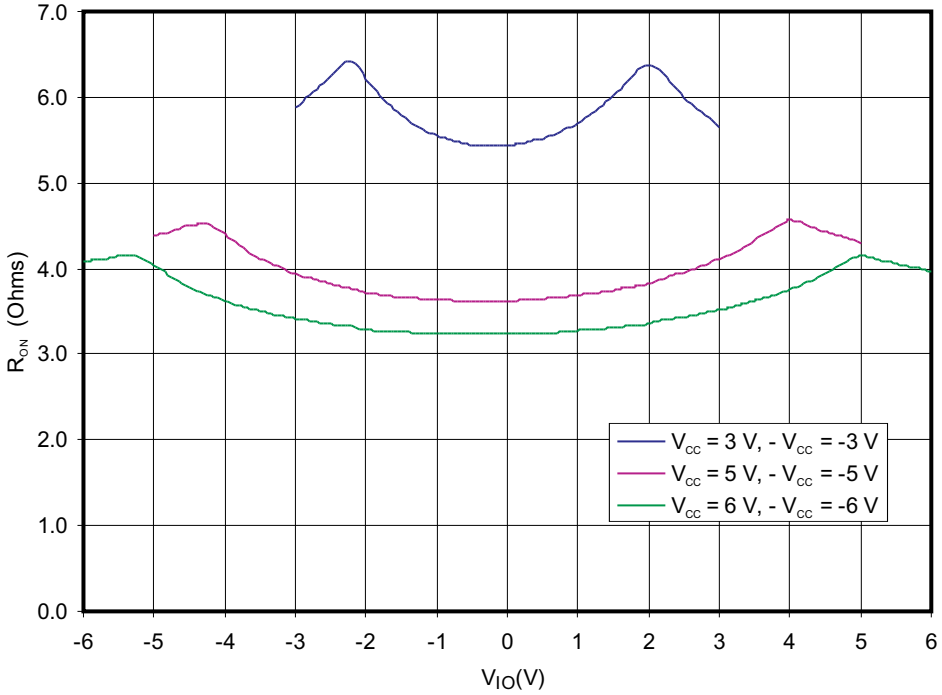


Figure 9-2. R_{ON} vs V_{IO}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC and -VCC on first, followed by NO, NC, or COM.

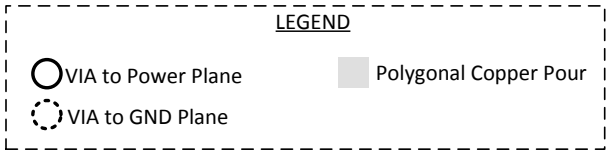
Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

It is recommended to place a bypass capacitor as close to the supply pins, VCC and -VCC, as possible to help smooth out lower frequency noise and provide better load regulation across the frequency spectrum. Minimize trace lengths and vias on the signal paths to preserve signal integrity.

11.2 Layout Example



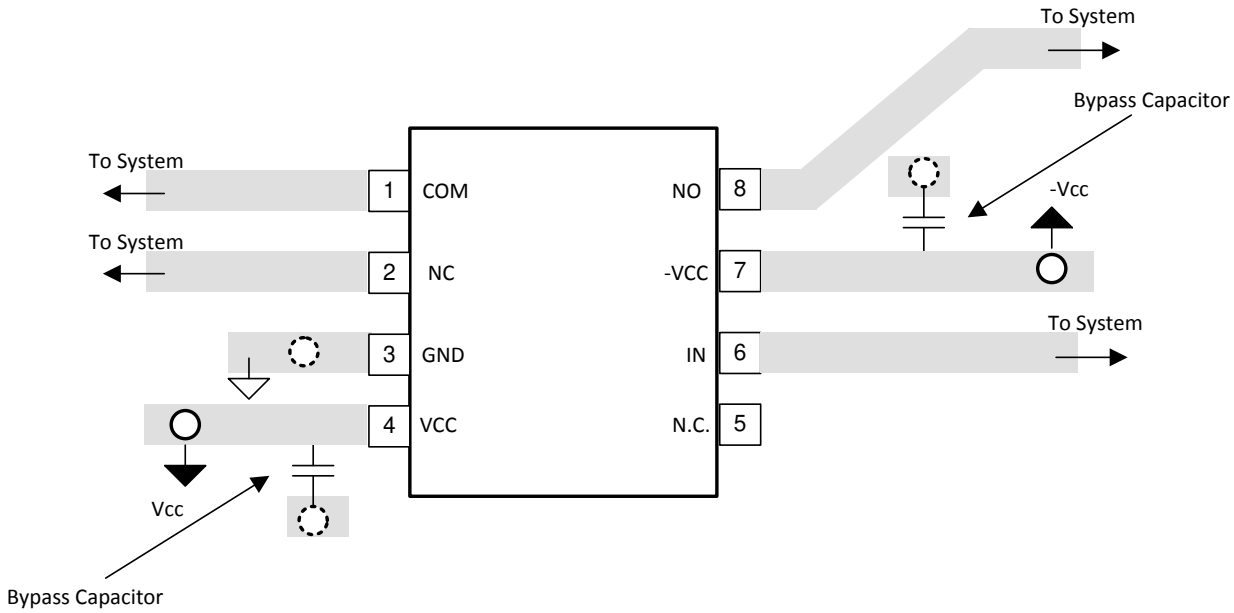


Figure 11-1. Layout Schematic

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS12A12511DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFHS NFHA	Samples
TS12A12511DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2US 2UA	Samples
TS12A12511DRJR	ACTIVE	SON	DRJ	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZVE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

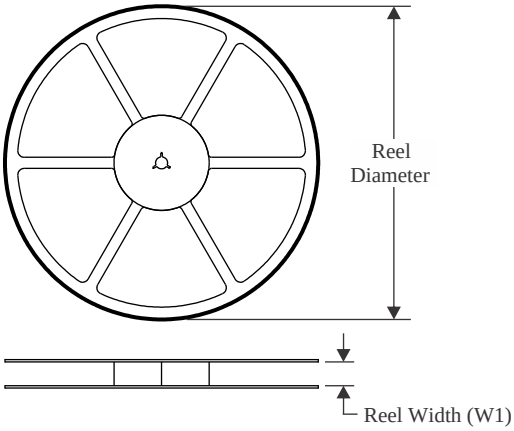
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

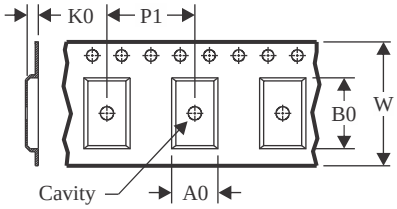
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

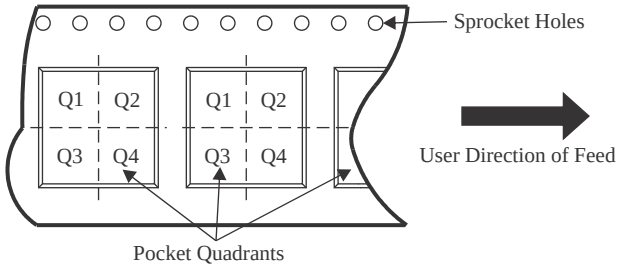


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

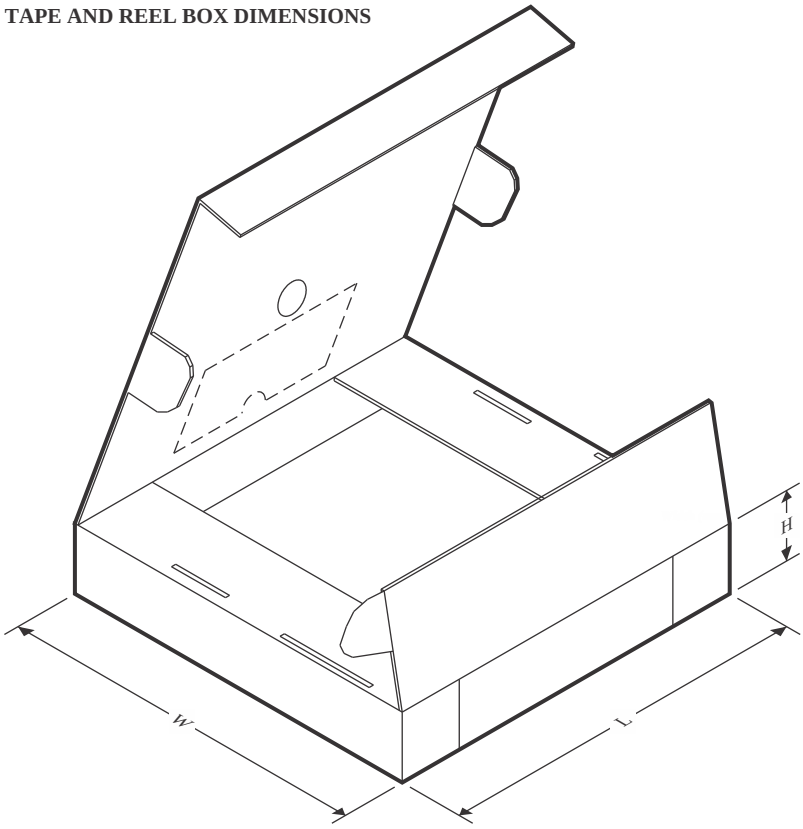
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS12A12511DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS12A12511DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS12A12511DRJR	SON	DRJ	8	1000	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

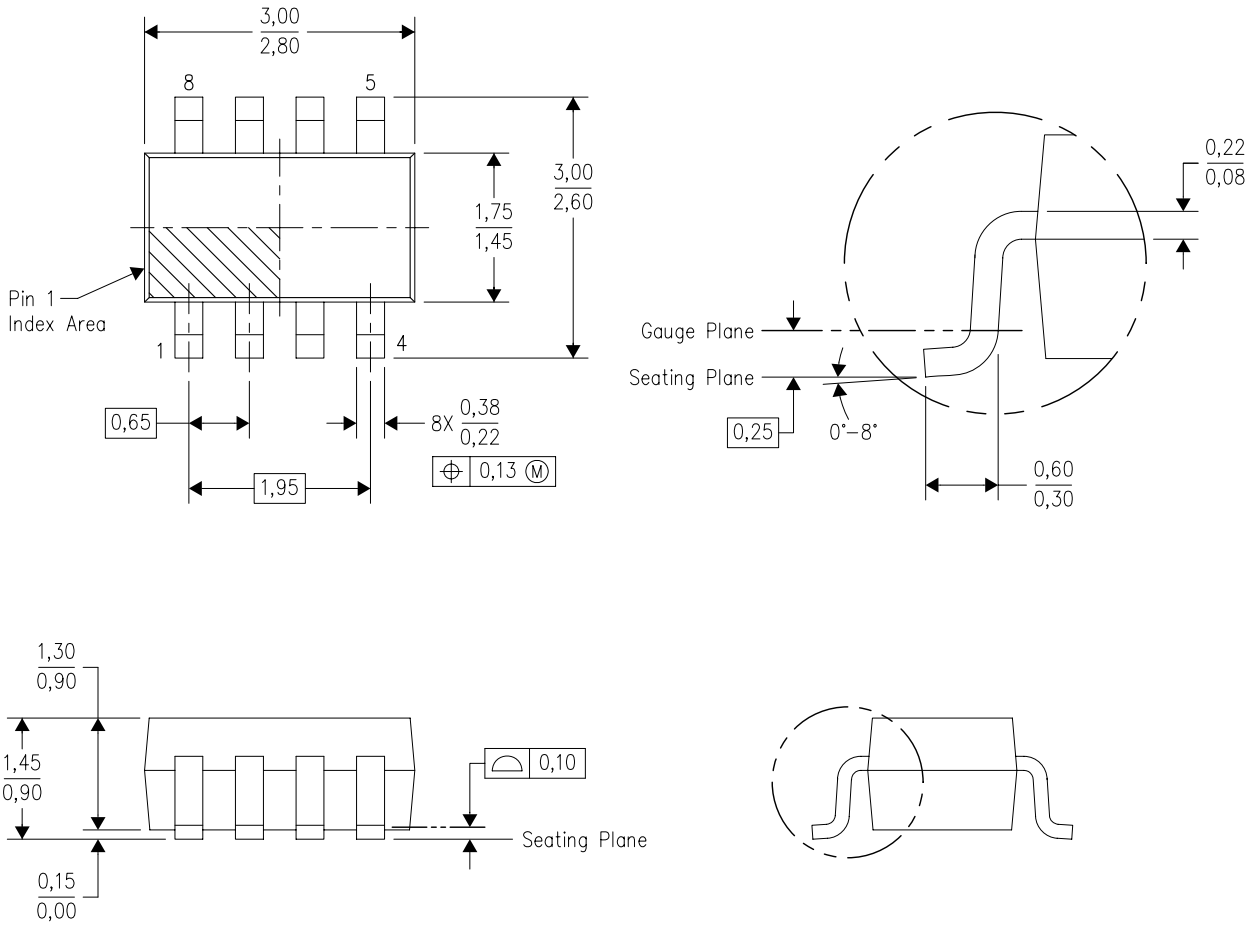
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

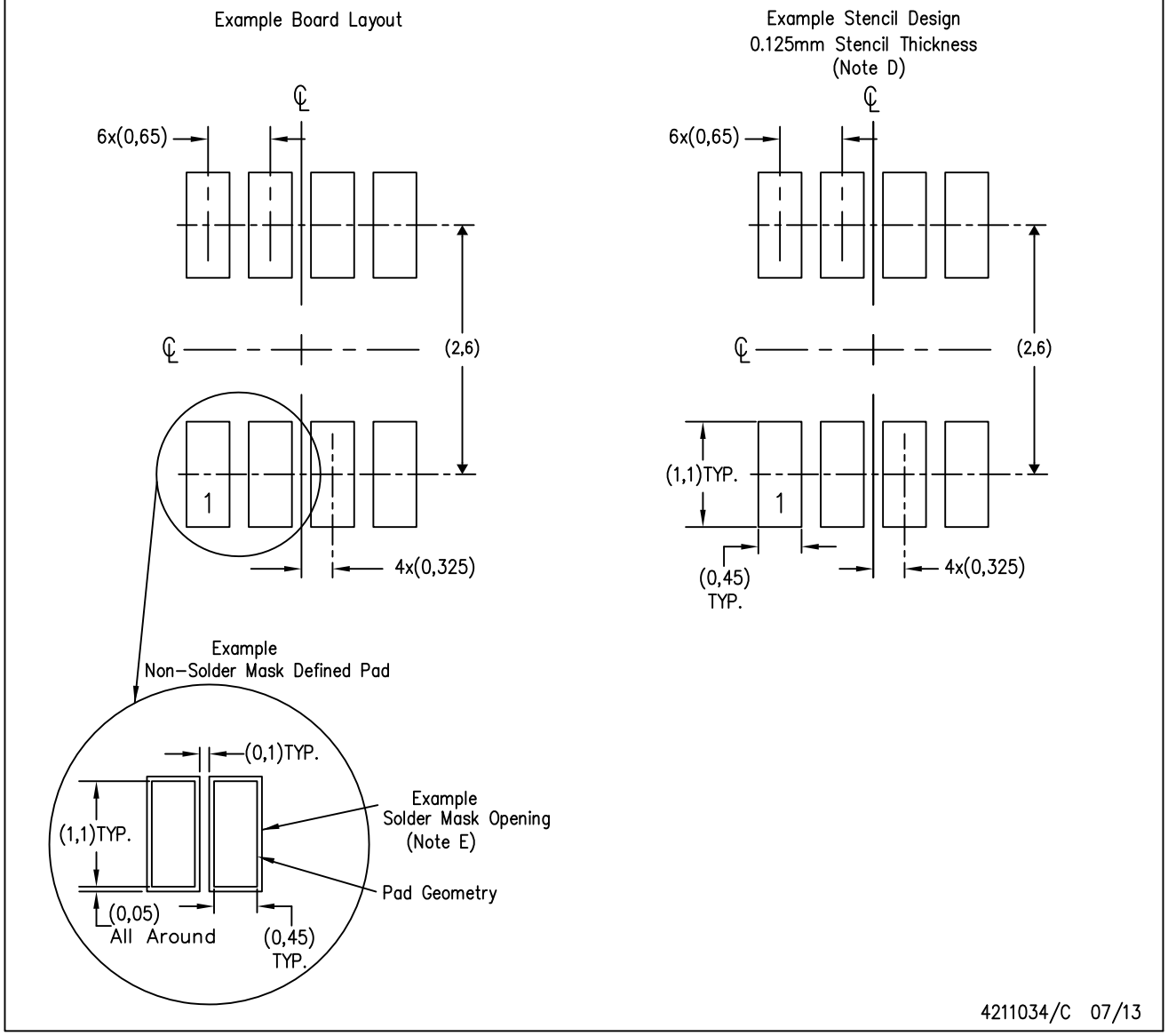
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS12A12511DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TS12A12511DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TS12A12511DRJR	SON	DRJ	8	1000	210.0	185.0	35.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



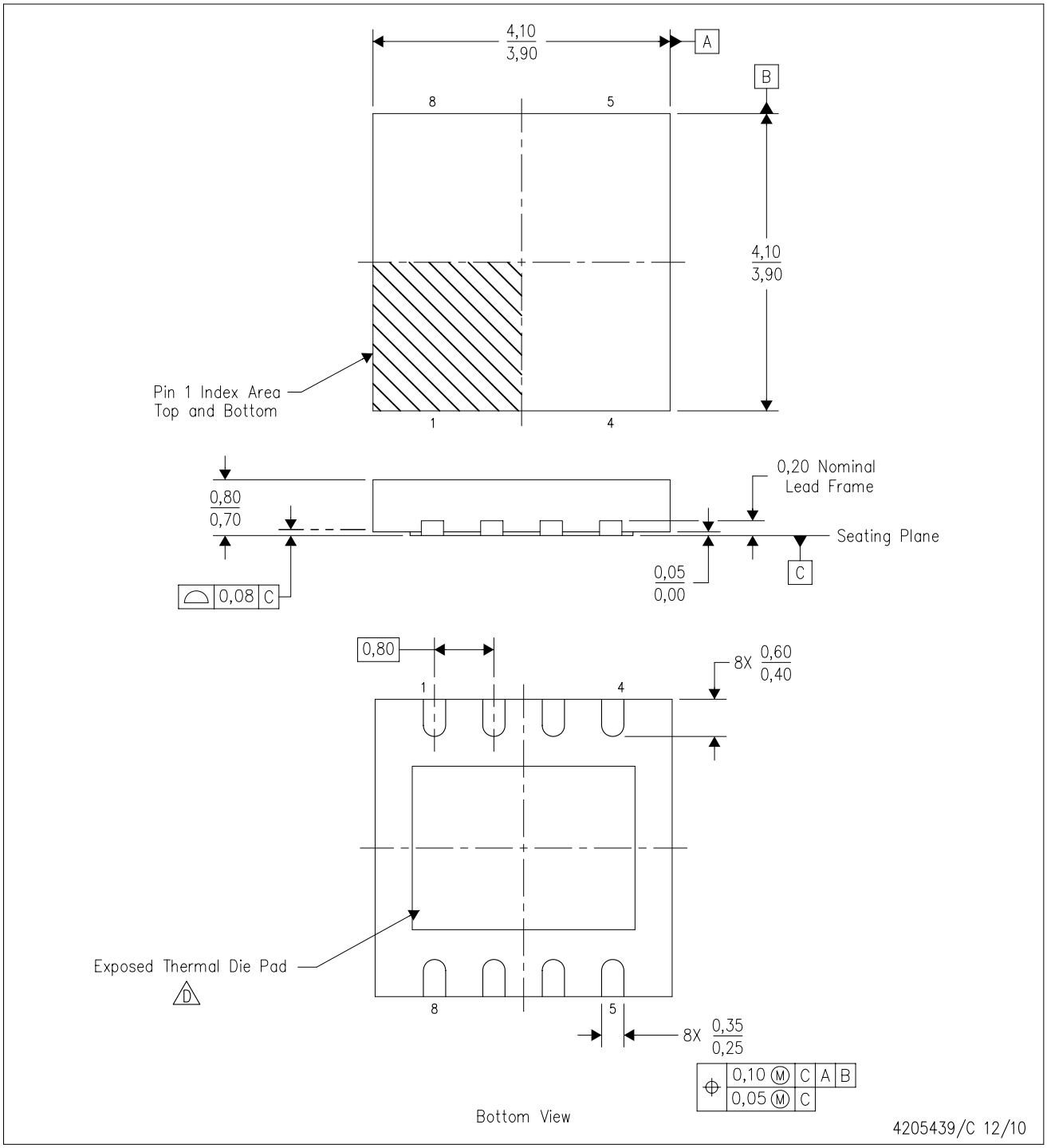
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–229 variation WGGB.

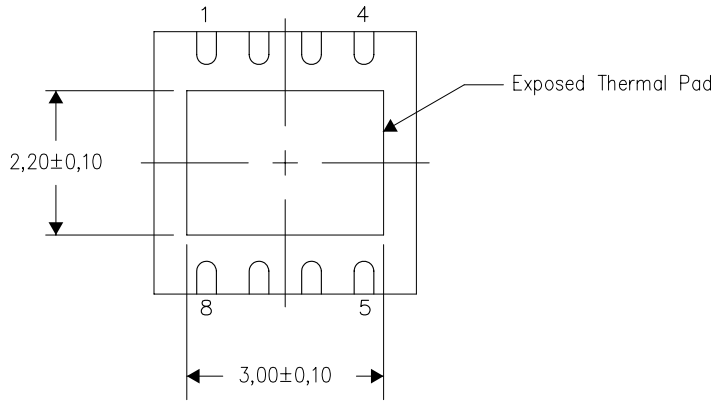
DRJ (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



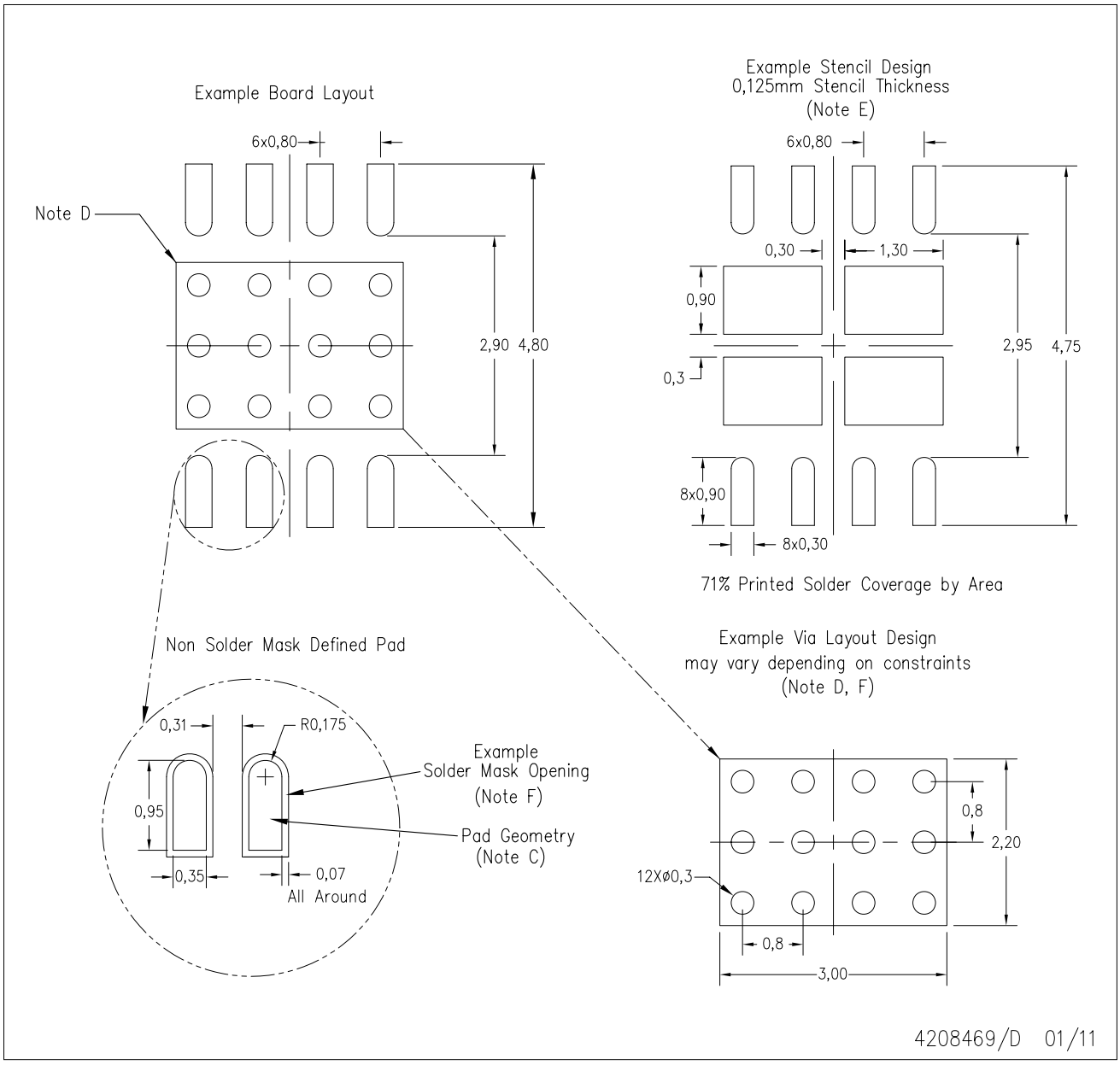
Bottom View

Exposed Thermal Pad Dimensions

4206882/F 01/11

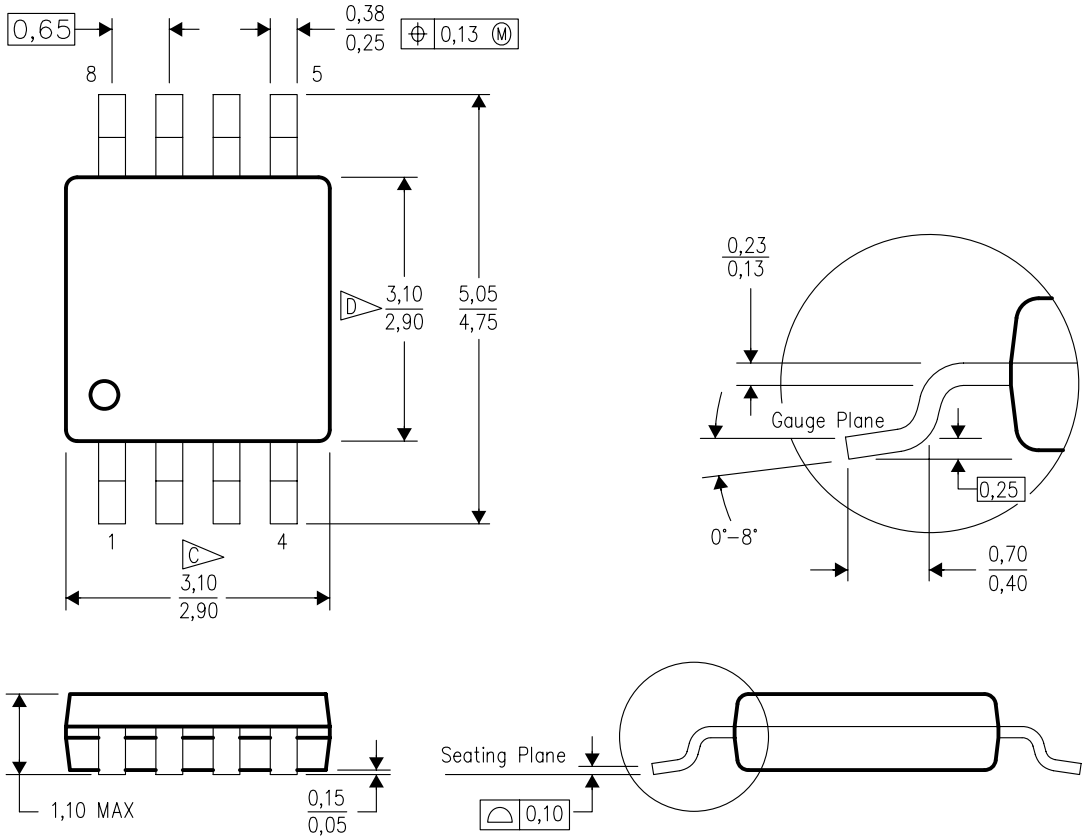
NOTE: All linear dimensions are in millimeters

DRJ (S–PWSON–N8) SMALL PACKAGE OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances and vias tenting recommendations for vias placed in the thermal pad.

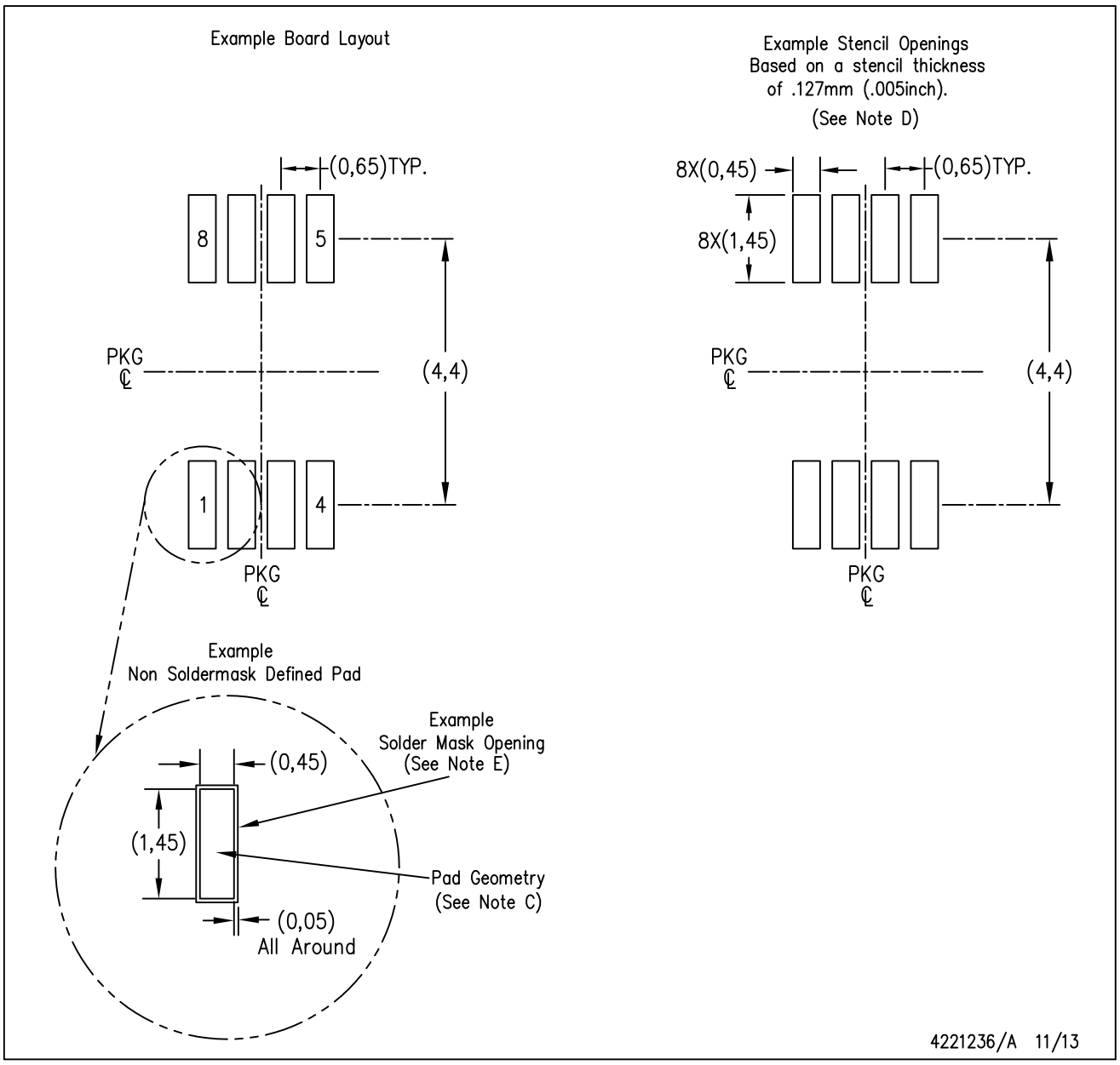
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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