

**FEATURES**

Fully certified DO-160G EMC protection on RS-485 bus pins:
Section 22 lightning protection Waveform 3, Waveform 4/
Waveform 1, and Waveform 5A pin injection, Level 4
protection

DO-160G Section 25 ESD protection: ± 15 kV air discharge
RS-485 A Pin and RS-485 B pin and HBM ESD protection:
 $> \pm 30$ kV

± 42 V ac/dc peak fault protection on RS-485 bus pins

TIA/EIA RS-485 compliant over full supply range
3.0 V to 5.5 V operating voltage range on V_{CC}
1.62 V to 5.5 V V_{IO} logic supply

Common-mode input range: -25 V to $+25$ V

2.5 Mbps data rate, maximum

Half duplex

Enhanced 2.1 V driver output strength at 4.5 V V_{CC}

Receiver short-circuit, open circuit, and floating input fail-safe

Supports 256 bus nodes (96 k Ω receiver input resistance)
 -55°C to $+125^{\circ}\text{C}$ temperature option

Glitch free power-up and power-down (hot swap)

16-lead, narrow body SOIC package

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications
(AQEC standard)

Military -55°C to $+125^{\circ}\text{C}$ operating temperature range

Controlled manufacturing baseline

1 assembly/test site

Enhanced product change notification

Qualification data available on request

APPLICATIONS

**Military and aerospace (MILA) avionics for sensors,
actuators, and engine control**

GENERAL DESCRIPTION

The ADM3095E-EP is a 3.0 V to 5.5 V, 2.5 Mbps, RS-485 transceiver that features up to ± 42 V ac/dc peak bus overvoltage fault protection on the RS-485 bus pins. This device is designed to withstand overvoltage faults, such as short circuits directly to power supplies, and overvoltage faults, such as ± 24 V ac supplies connected in error to the RS-485 A and B bus pins. The ADM3095E-EP integrates fully certified DO-160G electromagnetic capability (EMC) protection on the RS-485 bus pins, with Section 22 lightning protection. The ADM3095E-EP also provides Section 25 ± 15 kV electrostatic discharge (ESD) air discharge protection. For Section 22 lightning, the ADM3095E-EP provides protection for Waveform 3, Waveform 4/Waveform 1, and Waveform 5A to Level 4 connecting 33 Ω or 47 Ω current limiting resistors to GND.

This device has an extended common-mode input voltage (V_{CM}) range of ± 25 V to improve data communication reliability in noisy environments over long cable lengths where ground loop voltages are possible. The combination of extended common-mode input voltage range, overvoltage fault protection, and DO-160 EMC protection make the ADM3095E-EP a completely integrated EMC protected RS-485 transceiver.

The ADM3095E-EP also features a logic supply pin, V_{IO} , for a flexible digital interface, operational to voltages as low as 1.62 V. The ADM3095E-EP features a high driver differential output voltage, V_{OD} , of 2.1 V minimum at power supply voltages greater than 4.5 V. The device is fully characterized over extended operating temperature ranges, with options of -55°C to $+125^{\circ}\text{C}$, and is available in a 16-lead, narrow body SOIC package.

Additional information and technical information can be found in the [ADM3095E](#) data sheet.

TABLE OF CONTENTS

| | | | |
|---------------------------------|---|--|----|
| Features | 1 | ESD Caution..... | 6 |
| Enhanced Product Features | 1 | Pin Configuration and Function Descriptions..... | 7 |
| Applications..... | 1 | Typical Performance Characteristics | 8 |
| General Description | 1 | Test Circuits..... | 11 |
| Revision History | 2 | Theory of Operation | 12 |
| Functional Block Diagram | 3 | Certified DO-160G EMC Protection | 12 |
| Specifications..... | 4 | DO-160G ADM3095E-EP Test Details..... | 12 |
| Timing Specifications | 5 | Outline Dimensions | 14 |
| Timing Diagrams..... | 5 | Ordering Guide | 14 |
| Absolute Maximum Ratings..... | 6 | | |
| Thermal Resistance | 6 | | |

REVISION HISTORY

9/2017—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

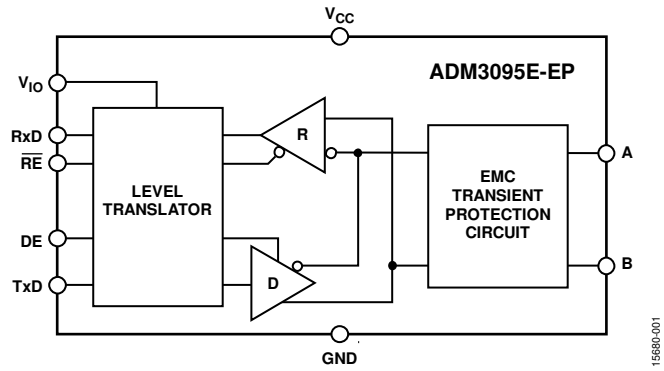


Figure 1. Functional Block Diagram

SPECIFICATIONS

$V_{CC} = 3.0\text{ V}$ to 5.5 V , $T_A = -55^\circ\text{C}$ (T_{MIN}) to 125°C (T_{MAX}), unless otherwise noted.

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|----------------|------|---------------|---------------|--|
| DRIVER | | | | | |
| Differential Output Voltage (V_{OD}) | 1.5 | | 5.0 | V | $V_{CC} \geq 3.0\text{ V}$, $R = 27\ \Omega$ or $50\ \Omega$; see Figure 25 |
| | 2.1 | | 5.0 | V | $V_{CC} \geq 4.5\text{ V}$, $R = 27\ \Omega$ or $50\ \Omega$; see Figure 25 |
| Differential Output Voltage over Common Mode Range [V_{OD3}] | 1.5 | | 5.0 | V | $V_{CC} \geq 3.0\text{ V}$, $V_{CM} = -25\text{ V}$ to $+25\text{ V}$; see Figure 26 |
| | 2.1 | | 5.0 | V | $V_{CC} \geq +4.5\text{ V}$, $V_{CM} = -25\text{ V}$ to $+25\text{ V}$; see Figure 26 |
| $\Delta V_{OD} $ for Complementary Output States | | | 0.2 | V | $R = 27\ \Omega$ or $50\ \Omega$; see Figure 25 |
| Common-Mode Output Voltage (V_{OC}) | | | 3 | V | $R = 27\ \Omega$ or $50\ \Omega$; see Figure 25 |
| $\Delta V_{OC} $ for Complementary Output States | | | 0.2 | V | $R = 27\ \Omega$ or $50\ \Omega$; see Figure 25 |
| Output Short-Circuit Current (V_{OUT}) | | | | | |
| High | -250 | | +250 | mA | $-42\text{ V} \leq V_{SC}^1 \leq +42\text{ V}$ |
| Low | -250 | | +250 | mA | $-42\text{ V} \leq V_{SC}^1 \leq +42\text{ V}$ |
| DRIVER INPUT LOGIC | | | | | |
| Input Logic Threshold Low | | | $0.33 V_{IO}$ | V | $1.62\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ |
| Input Logic Threshold High | $0.7 V_{IO}$ | | | V | $1.62\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ |
| Logic Input Current | | | ± 1 | μA | $0 \leq V_{IN} \leq V_{IO}$ |
| RECEIVER | | | | | |
| Differential Input Threshold Voltage (V_{TH}) | -200 | -125 | -30 | mV | $-25\text{ V} \leq V_{CM} \leq +25\text{ V}$ |
| Input Hysteresis (ΔV_{TH}) | | 30 | | mV | $-25\text{ V} \leq V_{CM} \leq +25\text{ V}$ |
| Input Resistance (A, B) | 96 | | | k Ω | $-25\text{ V} \leq V_{CM} \leq +25\text{ V}$ |
| Input Capacitance (A, B) | | 150 | | pF | $T_A = 25^\circ\text{C}$ |
| Input Current (A, B) | -1.0 | | +1.0 | mA | $DE = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or $+5\text{ V}$, $V_{IN} = \pm 25\text{ V}$ |
| | -1.0 | | +1.0 | mA | $DE = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or $+5\text{ V}$, $V_{IN} = \pm 42\text{ V}$ |
| CMOS Logic Input Current (\overline{RE}) | | | ± 1 | μA | |
| Output Voltage | | | | | |
| Low (V_{OL}) | | | 0.2 | V | $I_{OUT} = 300\ \mu\text{A}$ |
| High (V_{OH}) | $V_{IO} - 0.2$ | | | V | $V_{IO} \geq +1.62\text{ V}$, $I_{OUT} = -300\ \mu\text{A}$ |
| Output Short-Circuit Current | 4 | | 85 | mA | $V_{OUT} = \text{GND}$ or V_{IO} , $\overline{RE} = 0\text{ V}$, $V_{IO} \geq 3.0\text{ V}$ |
| | | | 85 | mA | $V_{OUT} = \text{GND}/V_{IO}$, $\overline{RE} = 0\text{ V}$, $V_{IO} < 3.0\text{ V}$ |
| Three-State Output Leakage Current | | | ± 2 | μA | $\overline{RE} = V_{IO}$, $RxD = 0\text{ V}$ or V_{IO} |
| POWER SUPPLY | | | | | |
| V_{IO} | 1.62 | | V_{CC} | V | |
| Supply Current (I_{CC}) | | | | | |
| | | | 8 | mA | No load, $DE = V_{CC} = V_{IO}$, $\overline{RE} = 0\text{ V}$ |
| TxD Data Rate = 2.5 Mbps | | | 50 | mA | No load, $DE = V_{CC} = V_{IO}$, $\overline{RE} = V_{CC} = V_{IO}$ |
| RxD Data Rate = 2.5 Mbps | | | 6 | mA | No load, $DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$ |
| TxD/RxD Data Rate = 2.5 Mbps | | | 90 | mA | No load, $DE = V_{CC} = V_{IO}$, $\overline{RE} = 0\text{ V}$ |
| TxD/RxD Data Rate = 2.5 Mbps | | | 130 | mA | $R_L = 54\ \Omega$, $DE = V_{CC} = V_{IO}$, $\overline{RE} = 0\text{ V}$ |
| | | | 90 | mA | $R_L = 54\ \Omega$, $DE = V_{CC} = V_{IO}$, $\overline{RE} = 0\text{ V}$, $V_{CC} = 5.5\text{ V}$ |
| | | | 45 | mA | $R_L = 54\ \Omega$, $DE = V_{CC} = V_{IO}$, $\overline{RE} = 0\text{ V}$, $V_{CC} = 3.0\text{ V}$ |
| Supply Current in Shutdown Mode | | | 5 | μA | $DE = 0\text{ V}$, $\overline{RE} = V_{CC} = V_{IO}$ |

¹ V_{SC} is the short-circuit voltage at the RS-485 A or B bus pin.

TIMING SPECIFICATIONS

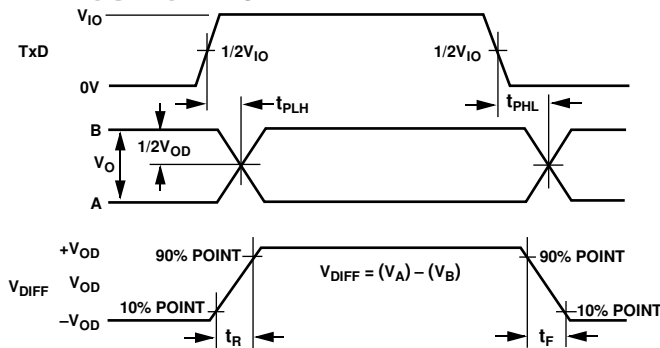
$V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{IO} = 1.62\text{ V to }V_{CC}$, $T_A = -55^\circ\text{C (T}_{MIN})\text{ to }125^\circ\text{C (T}_{MAX})$, unless otherwise noted.

Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------|------|------|---|
| DRIVER | | | | | |
| Data Rate | | | 2.5 | Mbps | |
| Propagation Delay (t_{PLH} , t_{PHL}) | | 35 | 500 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$; see Figure 2 and Figure 27 |
| Differential Skew (t_{SKEW}) | | 10 | 50 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$; see Figure 2 and Figure 27 |
| Rise/Fall Times (t_r , t_f) | | 40 | 130 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$; see Figure 2 and Figure 27 |
| Enable Time (t_{ZH} , t_{ZL}) | | 500 | 2500 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$; see Figure 4 and Figure 28 |
| Disable Time (t_{HZ} , t_{LZ}) | | 500 | 2500 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$; see Figure 4 and Figure 28 |
| Enable Time from Shutdown | | 4000 | 5500 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$; see Figure 4 and Figure 28 |
| RECEIVER | | | | | |
| Propagation Delay (t_{PLH} , t_{PHL}) | | 120 | 200 | ns | $C_L = +15\text{ pF}$, $V_{ID}^1 \geq \pm 1.5\text{ V}$; see Figure 3 and Figure 29 |
| | | 140 | 220 | ns | $C_L = +15\text{ pF}$, $V_{ID}^1 \geq \pm 600\text{ mV}$; see Figure 3 and Figure 29 |
| Skew (t_{SKEW}) | | 4 | 40 | ns | $C_L = +15\text{ pF}$, $V_{ID}^1 \geq \pm 1.5\text{ V}$; see Figure 3 and Figure 29 |
| Enable Time (t_{ZH} , t_{ZL}) | | 12 | 55 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$; see Figure 5 and Figure 30 |
| Disable Time (t_{HZ} , t_{LZ}) | | 12 | 55 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$; see Figure 5 and Figure 30 |
| Enable Time from Shutdown | | 3000 | 4500 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$; see Figure 5 and Figure 30 |
| Time to Shutdown | 50 | 330 | 3000 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$; see Figure 5 and Figure 30 |
| Rx, Pulse Width Distortion | | | 40 | ns | $C_L = +15\text{ pF}$, $V_{ID}^1 \geq \pm 1.5\text{ V}$; see Figure 3 and Figure 29 |

¹ V_{ID} is the input differential voltage to the RS-485 receiver.

TIMING DIAGRAMS



NOTES

- V_{OD} IS THE DIFFERENCE BETWEEN A AND B, WITH $+V_{OD}$ BEING THE MAXIMUM POINT OF V_{OD} , AND $-V_{OD}$ BEING THE MINIMUM POINT OF V_{OD} .

Figure 2. Driver Propagation Delay, Rise/Fall Timing Diagram

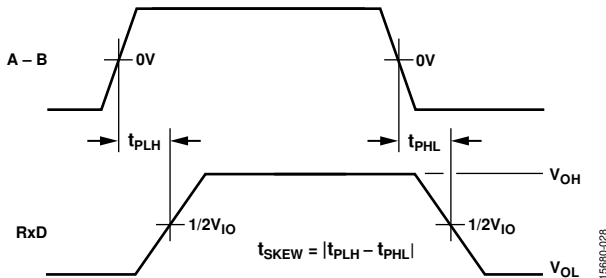


Figure 3. Receiver Propagation Delay Timing Diagram

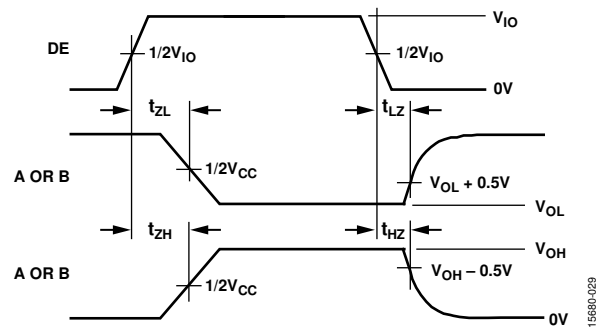


Figure 4. Driver Enable/Disable Timing Diagram

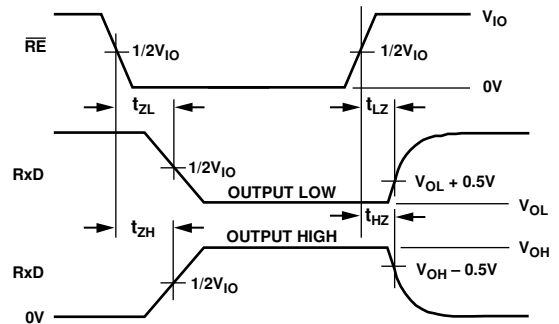


Figure 5. Receiver Enable/Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Rating |
|---|---|
| V_{CC} to GND | -0.5 V to +7 V |
| V_{IO} to GND | -0.5 V to +7 V |
| Digital Input/Output Voltage (DE, \overline{RE} , TxD, RxD) | -0.3 V to $V_{IO} + 0.3$ V |
| Driver Output/Receiver Input Voltage | ± 48 V |
| Military Operating Temperature Range | -55°C to $+125^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Maximum Junction Temperature | 150°C |
| Continuous Total Power Dissipation | 400 mW |
| Lead Temperature | |
| Soldering (10 sec) | 300°C |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD (A and B pins only) | |
| IEC 61000-4-2 Contact Discharge | ± 8 kV |
| IEC 61000-4-2 Air Discharge | ± 15 kV |
| Electrical Fast Transients (EFT) (A and B Pins Only) | |
| IEC 61000-4-4 Level 4 EFT | ± 2 kV |
| Surge (A and B pins only) | |
| IEC 61000-4-5 Level 4 Surge | ± 4 kV |
| Human Body Model (HBM) ESD Protection | |
| All Pins | ± 4 kV |
| A and B Pins Only | $> \pm 30$ kV |
| Field Induced Charged Device Model (FICDM) ESD | ± 1.25 kV |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

| Package Type | θ_{JA}^1 | θ_{JC}^1 | Unit |
|--------------|-----------------|-----------------|---------------------------|
| R-16 | 50.9 | 18.9 | $^\circ\text{C}/\text{W}$ |

¹ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias. See JEDEC JESD51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

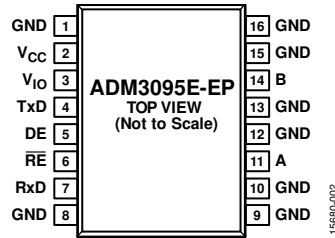


Figure 6. ADM3095E-EP Pin Configuration

Table 5. ADM3095E-EP Pin Descriptions

| Pin No. | Mnemonic | Description |
|-------------------------------|------------------------|---|
| 1, 8 to 10, 12, 13, 15, 16 | GND | Ground. |
| 2 | V _{CC} | 3.0 V to 5.5 V Power Supply. It is recommended that a 0.1 μ F decoupling capacitor is added between Pin V _{CC} and Pin GND. |
| 3 | V _{IO} | 1.62 V to 5.5 V V _{IO} Logic Supply. It is recommended that a 0.1 μ F decoupling capacitor is added between Pin V _{IO} and Pin GND. |
| 4 | TxD | Transmit Data Input. Data transmitted by the driver is applied to this input. |
| 5 | DE | Driver Output Enable. A high level on this pin enables the A and B driver differential outputs. A low level places them into a high impedance state. |
| 6 | $\overline{\text{RE}}$ | Receiver Enable Input. This is an active low input. Driving this input low enables the receiver and driving the input high disables the receiver. |
| 7 | RxD | Receiver Output Data. This output is high when $(A - B) > -30$ mV and low when $(A - B) < -200$ mV. |
| 11 | A | Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V _{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus. |
| 14 | B | Inverting Driver Output/Receiver Input. When the driver is disabled, or when V _{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus. |

TYPICAL PERFORMANCE CHARACTERISTICS

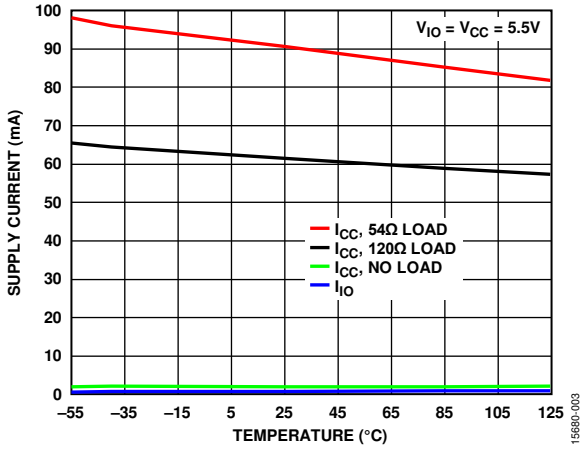


Figure 7. Supply Current vs. Temperature, Data Rate = 2.5 Mbps $V_{IO} = V_{CC} = 5.5V$

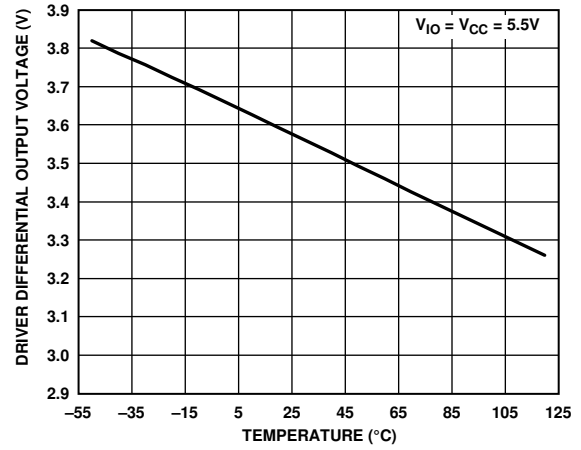


Figure 10. Driver Differential Output Voltage vs. Temperature

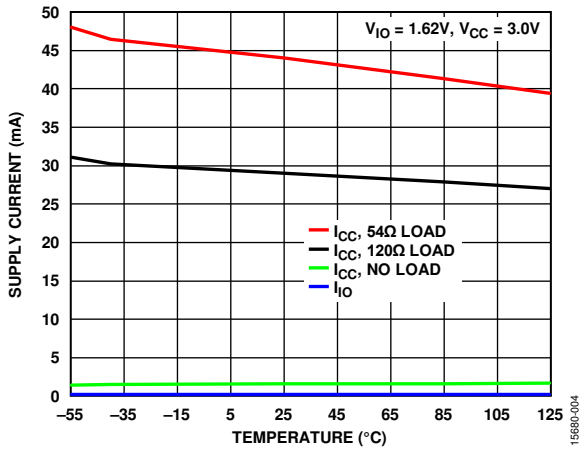


Figure 8. Supply Current vs. Temperature, Data Rate = 2.5 Mbps $V_{IO} = 1.62V, V_{CC} = 3.0V$

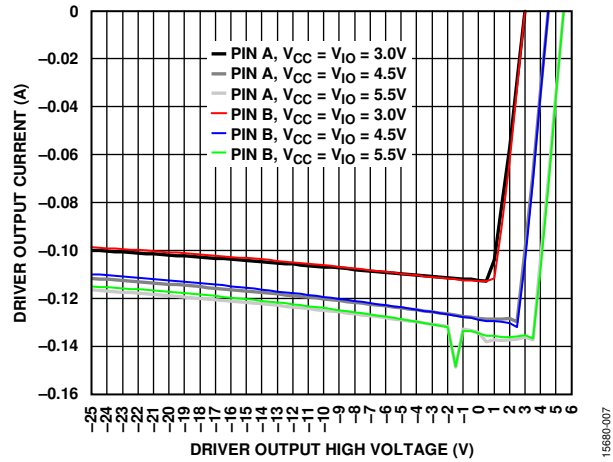


Figure 11. Driver Output Current vs. Driver Output High Voltage

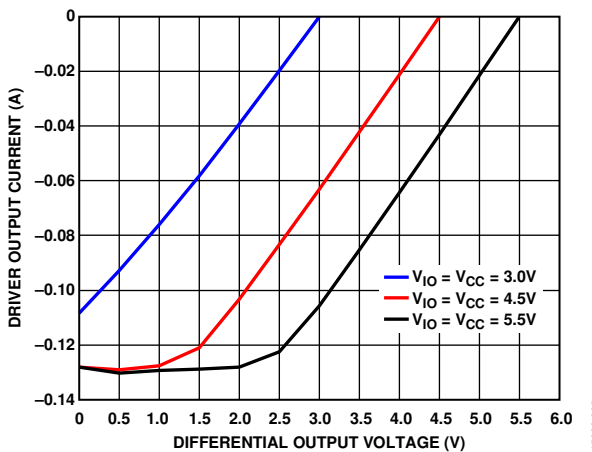


Figure 9. Driver Output Current vs. Differential Output Voltage

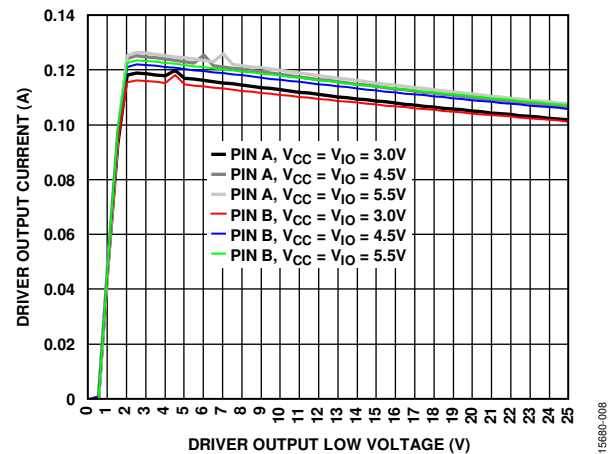


Figure 12. Driver Output Current vs. Driver Output Low Voltage

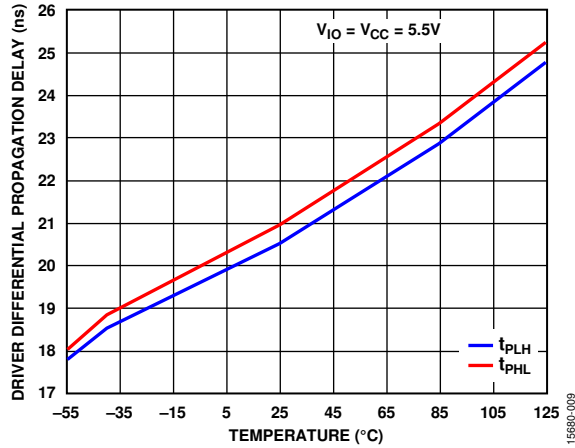


Figure 13. Driver Differential Propagation Delay vs. Temperature

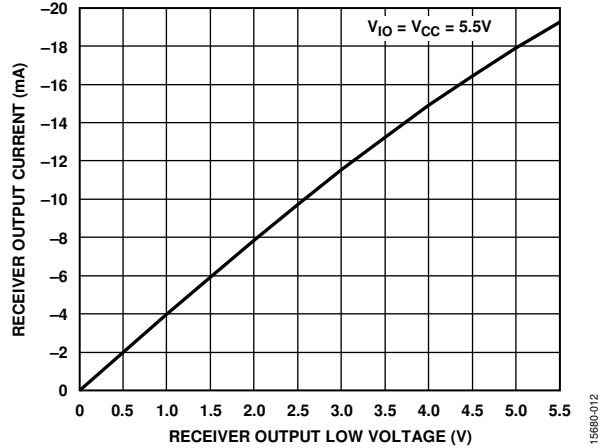


Figure 16. Receiver Output Current vs. Receiver Output Low Voltage

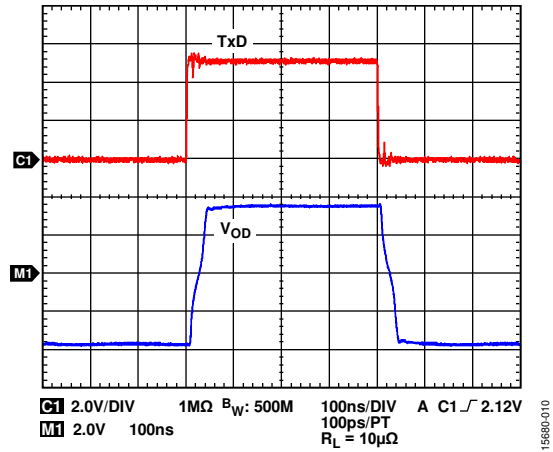


Figure 14. Driver Propagation Delay

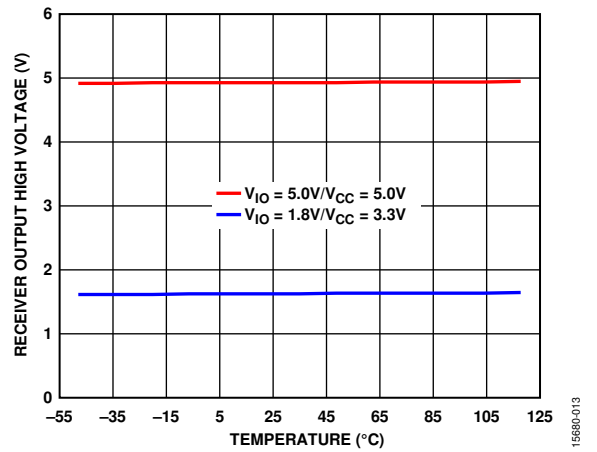


Figure 17. Receiver Output High Voltage vs. Temperature

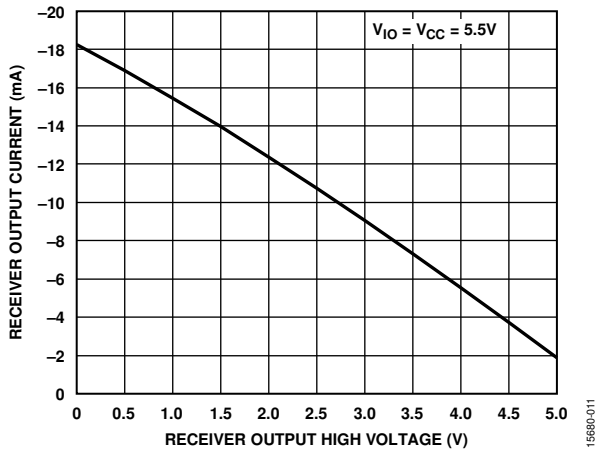


Figure 15. Receiver Output Current vs. Receiver Output High Voltage

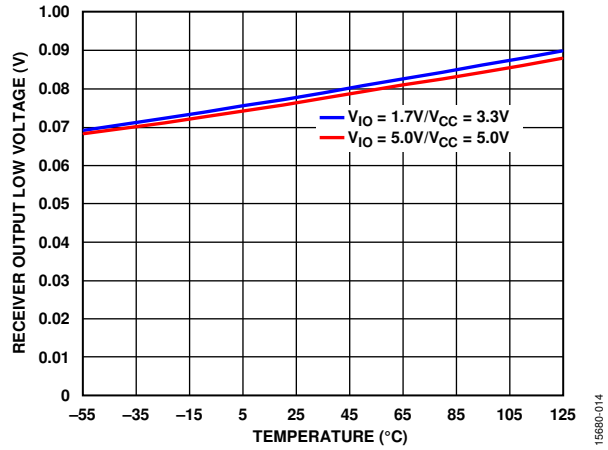


Figure 18. Receiver Output Low Voltage vs. Temperature

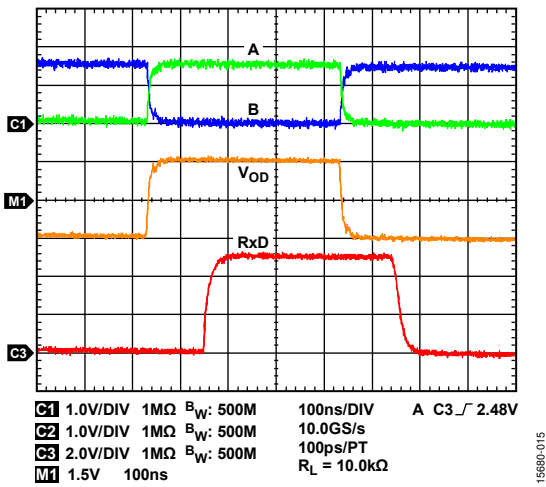


Figure 19. Receiver Propagation Delay

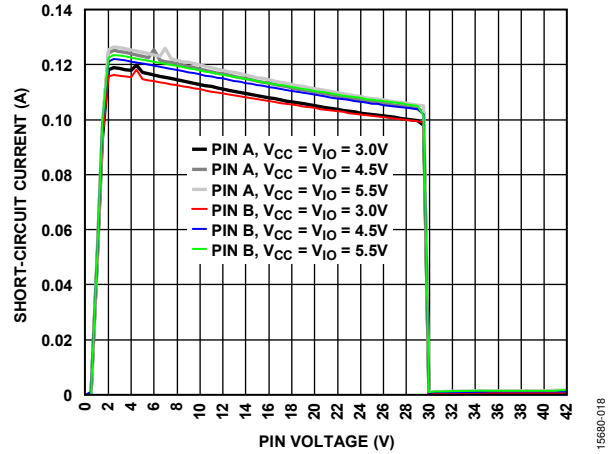


Figure 22. Short-Circuit Current vs. Pin Voltage

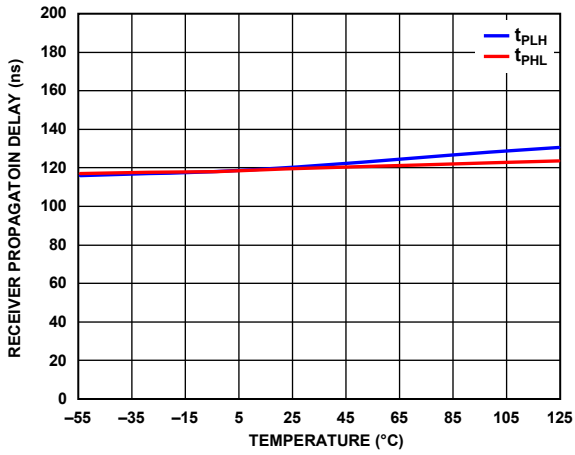


Figure 20. Receiver Propagation Delay vs. Temperature

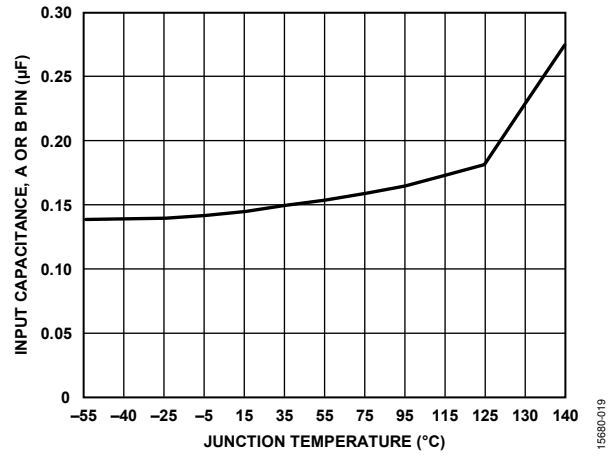


Figure 23. Input Capacitance, A or B Pin vs. Junction Temperature

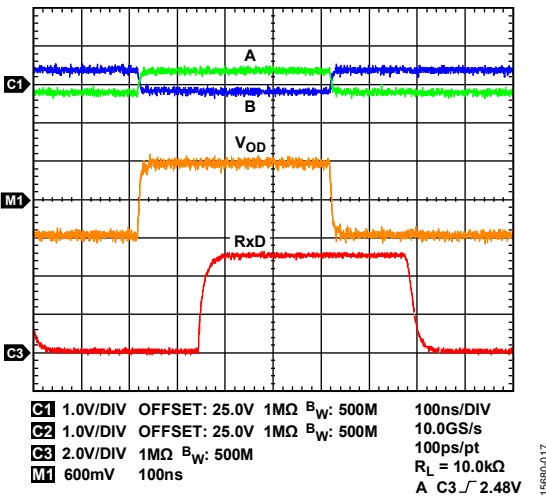


Figure 21. Receiver Performance with Input Common-Mode Voltage of 2.5V

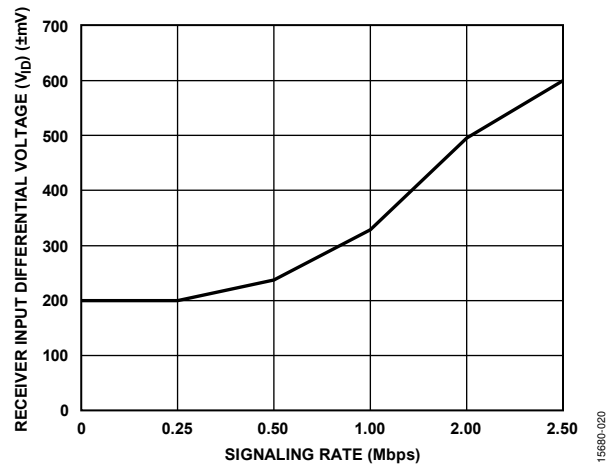


Figure 24. Receiver Input Differential Voltage (V_{ID}) vs. Signaling Rate

TEST CIRCUITS

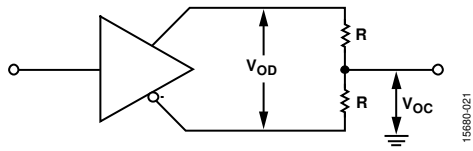


Figure 25. Driver Voltage Measurement

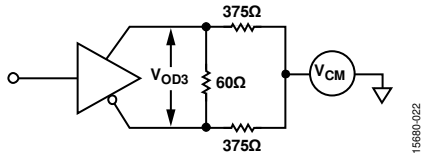


Figure 26. Driver Voltage Measurement over Common-Mode Voltage Range

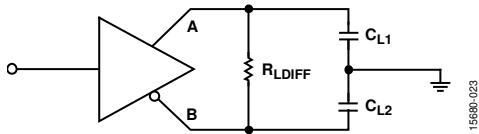


Figure 27. Driver Propagation Delay

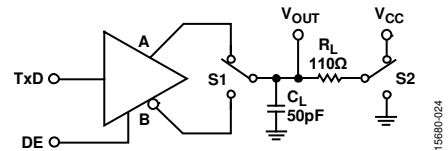


Figure 28. Driver Enable/Disable

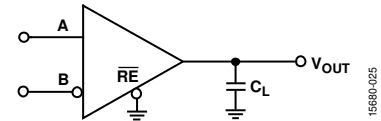


Figure 29. Receiver Propagation Delay

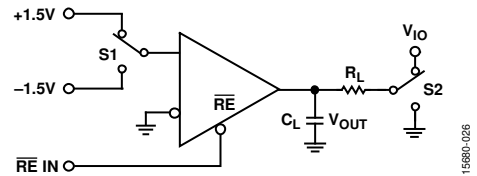


Figure 30. Receiver Enable/Disable

THEORY OF OPERATION

RS-485 WITH ADDED DO-160G EMC ROBUSTNESS

The ADM3095E-EP is a 3.0 V to 5.5 V RS-485 transceiver with added robustness that reduces system failures when operating in harsh application environments, such as MILA avionics for sensors, actuators, and engine control.

Lightning strikes to jet airliners are common—about once every 1000 flight hours. The DO-160G standard, *Environmental Conditions and Test Procedures for Airborne Equipment*, is a standard for the environmental testing of avionics hardware. Many airplane manufacturers specify DO-160G, Section 22, lightning induced transient susceptibility, as a requirement for critical systems, like guidance, radars, communications, engine controls, heat controls, and air controls. Aircraft radome, wing tips, fin tips, nacelles, and landing gear are areas most likely to be hit by lightning strikes.

The ADM3095E-EP integrates fully certified DO-160G EMC protection on RS-485 bus pins, with Section 22 lightning protection. The ADM3095E-EP also provides Section 25 ±15 kV ESD air discharge protection. For Section 22 lightning, the ADM3095E-EP provides protection against Waveform 3, Waveform 4/Waveform 1, and Waveform 5A to Level 4 using 33 Ω or 47 Ω current limiting resistors to GND.

CERTIFIED DO-160G EMC PROTECTION

Table 6 details the open circuit voltage (V_{OC}) and short-circuit current (I_{SC}) as specified in the DO-160G Section 22 lightning transient susceptibility standard for Waveform 3, Waveform 4/ Waveform 1, and Waveform 5A for pin injection testing. The peak currents for the DO-160G Level 4 tests are much greater than the standard industrial surge IEC 61000-4-5 peak currents.

The waveform shape with rise and decay times for the DO-160G standard are significantly longer than those specified by the IEC 61000-4-5 standard, as shown in Figure 31. Due to the high amounts of energy associated with the DO-160G Section 22 lightning standard, the ADM3095E-EP is tested using external 33 Ω or 47 Ω A pin and B pin bus current limiting resistors for testing to GND. These resistors are required in addition to the ADM3095E-EP integrated EMC protection circuitry.

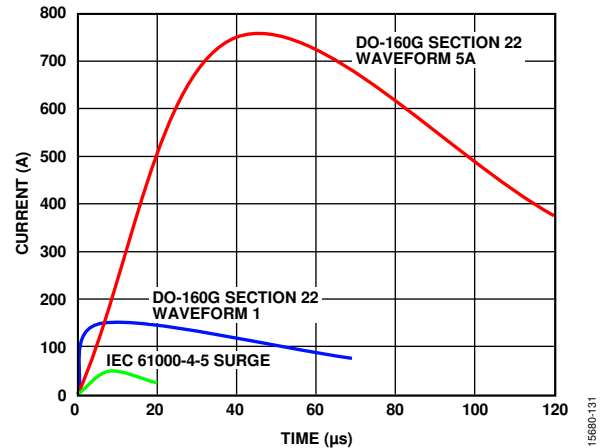


Figure 31. DO-160G Section 22 Waveform 1 and Waveform 5A, and IEC 61000-4-5 Surge Waveform

DO-160G ADM3095E-EP TEST DETAILS

Figure 32 and Figure 33 show the Waveform 3 test setup coupling and decoupling network (CDN), the Waveform 5A, and Waveform 4/Waveform 1 CDN. For testing to the RS-485 bus side, GND, an additional 33 Ω or 47 Ω current limiting resistance is added on the A and B bus pins. DO-160G Section 22 testing is performed on one pin at a time. The test is not performed in common mode. Table 7 and Table 8 show a summary of the ADM3095E-EP certified test results.

Table 6. DO-160G Section 22 Pin Injection Level 4 Compared to IEC 61000-4-5 Lightning Level 4

| Level | DO-160G Waveform 3 | DO-160G Waveform 4/Waveform 1 | DO-160G Waveform 5A | IEC 61000-4-5 |
|-------|--------------------|-------------------------------|---------------------|----------------|
| 4 | 1500 V, 60 A | 750 V, 150 A | 750 V, 750 A | 4000 V, 49 A |
| 3 | 600 V, 24 A | 300 V, 60 A | 300 V, 300 A | 2000 V, 24.5 A |

Table 7. DO-160G Section 22 Pin Injection Level 4 Certified Test Results

| Testing to | Current Limiting Resistor | DO-160 Waveform 3; 1500 V, 60 A | DO-160 Waveform 4/ Waveform 1; 750 V, 150 A | DO-160 Waveform 5A; 750 V, 750 A |
|------------|---------------------------|---------------------------------|---|----------------------------------|
| GND | 47 Ω or 33 Ω | Pass with 47 Ω | Pass with 33 Ω | Pass with 33 Ω |

Table 8. DO-160G Section 22 Pin Injection Level 3 Certified Test Results

| Testing to | Current Limiting Resistor | DO-160 Waveform 3; 600 V, 24 A | DO-160 Waveform 4/ Waveform 1; 300 V, 60 A | DO-160 Waveform 5A; 300 V, 300 A |
|------------|---------------------------|--------------------------------|--|----------------------------------|
| GND | 33 Ω | Pass | Pass | Pass |

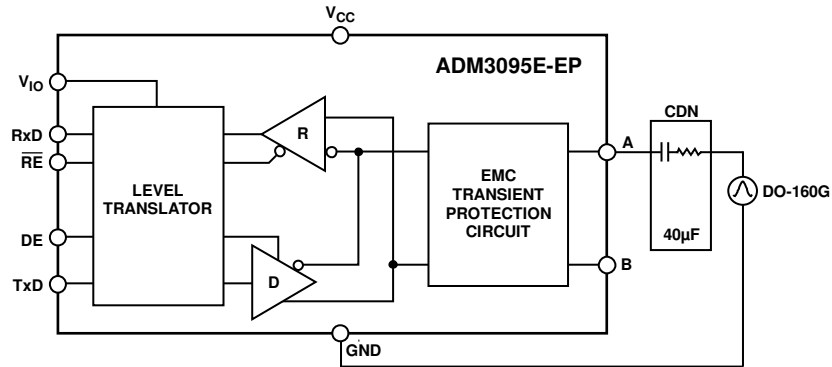


Figure 32. DO-160G Section 22 Waveform, 3 Test Setup and CDN Network

15680-132

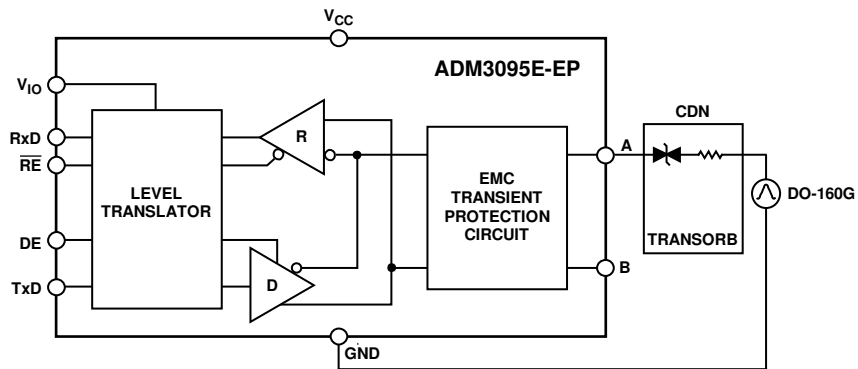
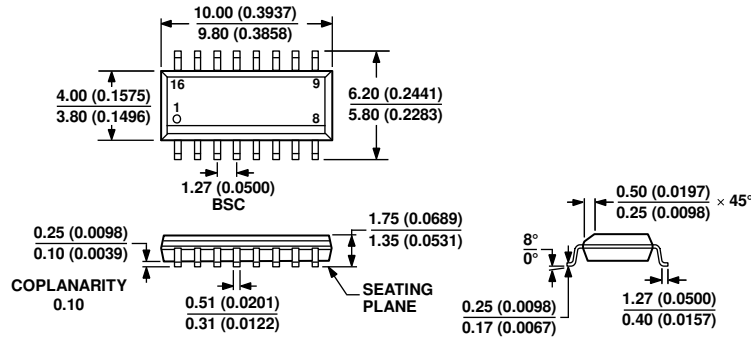


Figure 33. DO-160G Section 22 Waveform 5A and Waveform 4/Waveform 1 Test Setup and CDN Network

15680-133

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060604-A

Figure 34. 16-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-16)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADM3095ETRZ-EP | -55°C to +125°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| ADM3095ETRZ-EP-R7 | -55°C to +125°C | 16-Lead Standard Small Outline Package [SOIC_N] | R-16 |
| EVAL-ADM3095EEPZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.