MAX14616/MAX14616A

Micro-USB Interface Circuit Plus Intelligent Li+ Battery Chargers

General Description

The MAX14616/MAX14616A are a complete solution for interfacing to a micro-USB connector and include an advanced charger detection block, a linear battery charger, and a switch block capable of multiplexing USB, UART, audio, and composite video signals. The devices include an LED driver for battery charge status and battery present detection.

The MAX14616/MAX14616A support multiplexing USB 2.0 Hi-Speed, UART, and stereo audio signals with a single micro-USB connector. The USB channel features low 3Ω (typ) on-resistance and 7pF (typ) on capacitance to minimize USB signal degradation. The audio inputs feature negative rail signal operation down to -2V and 0.1Ω on-resistance flatness for low THD.

The MAX14616/MAX14616A charger detection block supports USB Battery Charger Detection Revision 1.1 requirements and also detects many common non-USB-defined power adapters. The SFOUT LDO provides a voltage-limited USB VBUS output for powering devices such as USB transceivers that cannot withstand high voltage. The MAX14616/MAX14616A include a composite video cable unplug detector capable of detecting the removal of a video termination resistor.

The MAX14616/MAX14616A battery charger adds a battery present detector to automatically disable the battery charger in case the battery is removed. They also include an open-drain LED driver to indicate the battery charger operation status.

The MAX14616/MAX14616A are available in a 25-bump (2mm x 2mm, 0.4mm pitch) WLP package and operates over the -40°C to +85°C extended temperature range.

Applications

- Media Players
- Cell Phones
- Digital Cameras
- eReaders
- Tablets

Benefits and Features

- High Level of Integration
  - Complete Solution for Micro-USB Connector Multiplexing
    - USB 2.0 Hi-Speed Switch with 3Ω (typ) On-Resistance
    - Negative-Rail Audio Inputs with Low THD
    - Detection Logic for Accessory Identification
    - Composite Video Load Removal Detection
- Internal Li+ Battery Charger with +28V (max) Input
- USB Battery Charger Detection
  - Supports USB BC1.1 with Advanced Features from USB BC1.2
  - Data Contact Detection (DCD) Support
  - USB DCP, SDP, and CDP Detection
  - Non-USB Defined Charger Detection Capability
- High-Voltage Protected LDO for USB Transceiver
- Charger Status LED Output Driver
- Battery Presence Monitor
- High-ESD Protection on COMN1, COMP2, and UID
  ±15kV for Human Body Model
  ±10kV for IEC 61000-4-2 Air Gap Discharge
  ±7kV for IEC 61000-4-2 Contact Discharge
- Saves Power in Portable Application
  - Low Supply Current
- Saves Space
  - 25-Bump, 2mm x 2mm, WLP Package

Ordering Information ***appears at end of data sheet.***

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Absolute Maximum Ratings

(All voltages referenced to GND.)
BAT, JIG, V_{IO}, $\overline{INT}$, THM ....-0.3V to +6V
LED...-0.3V to +6V
VB (Charger Mode) ....0.3V to +30V
VB (Microphone Mode) (Note 1) ....-0.3V to (V_{SWPOS} + 0.3V)
SFOUT–VB...+0.3V
CAP ....-0.3V to +4V
SDA, SCL ....-0.3V to (V_{BAT} + 0.3V)
SWITCH ENABLED or CPEn = 1 (Note 1)
SL1, SR2, COMN1, COMP2, UID, MIC,
IDB, DN1, DP2 ....-2.1V to (V_{SWPOS} + 0.3V)
UT1, UR2.....................................-0.3V to (V_{SWPOS} + 0.3V)
SWITCH DISABLED and CPEn = 0 (Note 2)
SL1, SR2, MIC, IDB, DN1, DP2,
UT1, UR2....................................... -0.3V to (V_{CCINT} + 0.3V)
COMN1, COMP2, UID ....-0.3V to +6V
Continuous Current into COMN1, COMP2 ....±200mA
Continuous Current into BAT, VB ....±1300mA
Continuous Current into All Other Bumps ....±100mA
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 19.2mW/°C above +70°C)...................1536mW
Operating Temperature Range.......................... -40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) (Note 3).........................+260°C

Note 1: V_{SWPOS} = min(V_{CCINT}, +3.3V)
Note 2: V_{CCINT} = max(V_{BAT}, min(V_{VB}, +4V))
Note 3: The WLP package is constructed using a unique set of package techniques that impose a limit on the thermal profile that the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 4)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....52°C/W

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{BAT}			2.8		5.5	V
	V_{VB}			3.5		28	
	V_{IO}			1.6		5.5	
Allowed VB Input-Voltage Range	V_{VB}			0		28	V
BAT Undervoltage Lockout Threshold	V_{UVLO}			0.4	2.0	2.65	V
BAT Supply Current	I_{BAT}	V_{BAT} = 3.6V, V_{VB} = 0V, no accessory attached	Low-power mode, LowPwr = 1, CPEn =0, ADCEn = 0		3	6	µA
			LowPwr = 0, CPEn = 0		28	50	
			LowPwr = 0, CPEn = 1		45	65	

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VB Supply Current	I_{VB}	V_{BAT} = 0V, I_{OUT} = 0mA, charger forced off	V_{VB} = 5V, CPEn = 0, MBCHOSTEN = 0, SFOUT is off, UID = open		350	500	µA
			V_{VB} = 5V, CPEn = 0, MBCHOSTEN= 0, SFOUT is on, UID = open		470	3000	
V_{IO} Supply Current	I_{IO}	LED = unconnected			0.1	1	µA
Internal VB Regulator Voltage	V_{PVB}			3.3	4	5.5	V
Internal Positive Regulator Voltage for Switches	V_{SWPOS}			3.3	3.4	3.5	V
Internal Negative Regulator Voltage for Switches	V_{SWNEG}			-2	-1.9	-1.8	V
CHARGER DETECTION							
VB-Detect-Threshold Voltage Rising	V_{VBDET}			3.2	3.4	3.6	V
VB-Detect-Threshold Voltage Hysteresis	V_{VBDET_HYST}				0.5		V
DP_SRC and DM_SRC Voltage	V_{DP_SRC}, V_{DM_SRC}	0µA ≤ I_{LOAD} ≤ 200µA		0.5	0.6	0.7	V
DAT_REF Voltage	V_{DAT_REF}			0.25	0.3	0.35	V
LGC Voltage	V_{LGC}			1.15	1.24	1.3	V
DP and DM Sink Current	I_{DP_SINK}, I_{DM_SINK}	0.15V ≤ V_{DP} = V_{DM} ≤ 3.6V		55	80	105	µA
DP Source Current	I_{DP_SRC}	0V ≤ V_{DP} ≤ 2.5V		5.5	8	10	µA
DP and DM Pulldown Resistance	R_{DP_DWN}, R_{DM_DWN}			17	20	23.3	kΩ
DP/DM Pulldown Current	I_{DP_PD}, I_{DM_PD}	V_{DM} = 0.15V or 3.6V		0.01	0.15	0.5	µA
COMN1 to VB Voltage Ratio	V_{BUS25}	V_{VB} = 5V		22.5	25	27.5	%
	V_{BUS47}			42.3	47	51.7	
	V_{BUS75}			70	75	80	
V_{IO} Reset Falling Threshold	$V_{IO\_RST\_TH}$			0.5	0.8	1.1	V
Battery Present Detect Threshold	V_{THM}	% of V_{SFOUT}	V_{THM} rising	18.0	18.5	19.0	%
			V_{THM} falling		18.3		
ACCESSORY DETECTION							
UID Low-Power Pullup Voltage	V_{UID_PU}	V_{BAT} = 3.6V, V_{VB} = 0V, LowPwr = 1			1.6		V
UID Low-Power Threshold Voltage	V_{UID_LP}	V_{BAT} = 3.6V, V_{VB} = 0V, LowPwr = 1		0.4	0.7	1	V
UID Low-Power Pullup Resistance	R_{UID_LP}			2	3.4		MΩ
ADC Low Threshold	R_{ADCLow}			32	40	49	Ω

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ID Pullup Current	I_{PUP}	V_{UID} = 2.55V and 0.9V	2.19	2.28	2.37	µA
		V_{UID} = 2.50V and 0.76V	5.756	6	6.24	
		V_{UID} = 2.35V and 0.70V	16.032	16.7	17.368	
		V_{UID} = 2.20V and 0.57V	45.214	47	48.786	
		V_{UID} = 2.12V and 0.05V	146.88	153	159.12	
		V_{UID} = 2.04V and 0.05V	2.235	2.5	2.735	mA
ADC Detection Resistors	R_{ADC}	GND	0		0.032	kΩ
		R_{VID}	0.049	0.075	0.472	
		1kΩ resistor	0.531	1	1.433	
		R1	1.722	2	2.112	
		R2	2.465	2.604	2.684	
		R3	3.091	3.208	3.35	
		R4	3.826	4.014	4.11	
		R5	4.67	4.82	5.05	
		R6	5.73	6.03	6.54	
		R7	7.39	8.03	8.43	
		R8	9.5	10.03	10.31	
		R9	11.6	12.03	12.69	
		R10	14.03	14.46	14.77	
		R11	16.76	17.26	17.61	
		R12	19.92	20.5	20.79	
		R13	23.49	24.07	24.63	
		R14	27.8	28.7	29.3	
		R15	33	34	34.7	
		R16	39	40.2	43	
		R17	49.6	49.9	53.4	
		R18	60.4	64.9	67.6	
		R19	76.3	80.07	84.9	
		R20	95.6	102	104	
		R21	117	121	129	
		R22	143	150	153	
		R23	173	200	212	
		R24	239	255	260	
		R25	293	301	312	
		R26	350	365	384	
		R27	425	442	450	
		R28	508	523	533	
		R29	601	619	655	
		R30	737	1000	1032	
		Open	1158			

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB ANALOG SWITCH (DN1, DP2)						
Analog Signal Range	V_{DN1}, V_{DP2}	RUID = open, LowPwr = 1 and CPEn = 0 (Note 2)	0		V_{CCINT}	V
		(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1 (Note 1)	0		V_{SWPOS}	
On-Resistance	R_{ONUSB}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.0V		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUSB}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, V_{COMN1}, V_{COMP2} = 400mV			0.5	Ω
On-Resistance Flatness	$R_{FLATUSB}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.3V		0.1	0.3	Ω
Off-Leakage Current	$I_{LUSB (OFF)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch open, V_{DN1}, V_{DP2} = 0.3V or 2.5V and V_{COMN1}, V_{COMP2} = 2.5V or 0.3V	-360		+360	nA
On-Leakage Current	$I_{USB(ON)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch closed, V_{DN1}, V_{DP2} = 0.3V or 2.5V	-360		+360	nA
UART ANALOG SWITCHES (UT1, UR2)						
Analog Signal Range	V_{UT1}, V_{UR2}	RUID = open, LowPwr = 1 and CPEn = 0 (Note 2)	0		V_{CCINT}	V
		(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1 (Note 1)	0		V_{SWPOS}	
On-Resistance	R_{ONUART}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.0V		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONUART}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, V_{COMN1}, V_{COMP2} = 1.5V			0.5	Ω
On-Resistance Flatness	$R_{FLATUART}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.0V		0.1	0.3	Ω
Off-Leakage Current	$I_{LUART(OFF)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch open, V_{UT1}, V_{UR2} = 0.3V or 2.5V and V_{COMN1}, V_{COMP2} = 2.5V or 0.3V	-360		+360	nA

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Leakage Current	$I_{LUART(ON)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch closed, V_{UT1}, V_{UR2} = 0.3V or 2.5V	-360		+360	nA
AUDIO ANALOG SWITCHES (SL1, SR2)						
Analog Signal Range	V_{AUDIO}	RUID = open, LowPwr = 1 and CPEn = 0 (Note 2)	0		V_{CCINT}	V
		(RUID < 1050kΩ or LowPwr=0) and CPEn = 1 (Note 1)	V_{SWNEG}		V_{SWPOS}	
On-Resistance	R_{ONA}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.0V		3	6	Ω
On-Resistance Match Between Channels	ΔR_{ONA}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, V_{COMN1}, V_{COMP2} = 1.5V			0.5	Ω
On-Resistance Flatness	R_{FLATA}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{COMN1}, I_{COMP2} = 10mA, 0V ≤ V_{COMN1}, V_{COMP2} ≤ 3.0V		0.1	0.3	Ω
Audio Off-Leakage Current	$I_{LA(OFF)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch open, V_{SL1}, V_{SR2} = 0.3V or 2.5V, V_{COMN1}, V_{COMP2} = 2.5V or 0.3V	-360		+360	nA
Audio On-Leakage Current	$I_{LA(ON)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch closed, V_{SL1}, V_{SR2} = 0.3V or 2.5V	-360		+360	nA
Shunt Resistor	R_{SHUNT}	I_{SHUNT} = 10mA	30	100	170	Ω
MIC ANALOG SWITCHES (MIC)						
Analog Signal Range	V_{MIC}	RUID = open, LowPwr = 1 and CPEn = 0 (Note 2)	0		V_{CCINT}	V
		(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1	0		2.5	
On-Resistance	R_{ONMIC}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{MIC} = 10mA, 0V ≤ V_{MIC} ≤ 3.0V		30	50	Ω
On-Resistance Flatness	$R_{FLATMIC}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{MIC} = 10mA, 0V ≤ V_{MIC} ≤ 3.0V		3	10	Ω
MIC Off-Leakage Current	$I_{LMIC(OFF)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch open, V_{MIC} = 0.3V or 2.5V, V_{VB} = 2.5V or 0.3V	-360		+360	nA

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MIC On-Leakage Current	$I_{LMIC(ON)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch closed, V_{MIC} = 0.3V or 2.5V		32	60	µA
ID BYPASS ANALOG SWITCH (IDB)						
Analog Signal Range	V_{IDB}	RUID = open, LowPwr = 1 and CPEn = 0 (Note 2)	0		V_{CCINT}	V
		(RUID < 1050kΩ or LowPwr = 0) and CPEn =1	V_{SWNEG}		V_{SWPOS}	
On-Resistance	R_{ONIDB}	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{IDB} = 10mA, 0V ≤ V_{IDB} ≤ 2.5V		3	6	Ω
On-Resistance Flatness	$R_{FLATIDB}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 3.0V, I_{IDB} = 10mA, 0V ≤ V_{IDB} ≤ 2.5V		0.1	0.3	Ω
IDB Off-Leakage Current	$I_{LIDB(OFF)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch open, V_{IDB} = 0.3V or 2.5V and V_{UID} = 2.5V or 0.3V	-360		+360	nA
IDB On-Leakage Current	$I_{LIDB(ON)}$	(RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, V_{BAT} = 4.2V, switch closed, V_{IDB} = 0.3V or 2.5V	-360		+360	nA
DIGITAL SIGNALS ($\overline{INT}$, SCL, SDA, JIG, BOOT, LED)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current	I_{INLEAK}		-250		+250	nA
Open-Drain Output-Voltage Low	V_{INTL}, V_{JIGL}, V_{LEDL}	I_{SINK} = 3mA			0.4	V
DYNAMIC PERFORMANCE						
Analog Switch Turn-On Time	t_{ON}	I²C STOP to switch on, R_L = 50Ω		0.2	0.5	ms
Analog Switch Turn-Off Time	t_{OFF}	I²C STOP to switch off, R_L = 50Ω		0.1	0.5	ms
Break-Before-Make Delay Time	t_{BBM}	R_L = 50Ω, T_A = +25°C (Note 6)	0			µs
MUIC Clock Period	t_{CK}			14.64		µs
USB Charger Detect Time	t_{DPSRC_ON}		40	46	60	ms
JIG Assertion Time		Resistor attached to ID until JIG assert (Note 7)		0.5		ms
Charger Detect Current Delay	t_{VDPSRC_HICRNT}		46		60	ms
VBUS Debounce Time	t_{MDEB}		20	30	40	ms
DCD Debounce Time			36	40	44	ms

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DCD Timeout		DCDCpl = 0		1.8	2	2.2	sec
		DCDCpl = 1				900	ms
Charger Detection Delay Timeout		CDDelay = 1			500		ms
COMN1, COMP2 On Capacitance	C_{ONCOM}	Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 240MHz, COMN1/COMP2 connected to DN1/DP2			7		pF
UID On Capacitance	C_{ONUID}	Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 1MHz, UID connected to MIC			7		pF
Off Capacitance	C_{OFF}	Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 1MHz	UT1, UR2		3		pF
			DN1, DP2		3		
			MIC		3		
			IDB		3		
Off-Isolation		R_L = 50Ω, f = 20kHz, V_{COMN1}, V_{COMP2} = $0.5V_{PP}$	UT1, UR2		-60		dB
MIC Isolation		BAT to MIC, MIC to UID switch enabled, R_L = 600Ω, 100Hz ≤ f ≤ 6kHz, V_{BAT} = 3.6V ± 0.5V			80		dB
BAT Supply PSRR		Noise from BAT to COMN1, COMP2 or MIC, R_L = 50Ω, f = 10kHz, V_{BAT} = 3.6V ± 0.2V			90		dB
Crosstalk		Any switch to any switch, R_L = 50Ω, f = 20kHz, V_{COMN1}, V_{COMP2} = $1V_{RMS}$			100		dB
MIC Total Harmonic Distortion	THD	MIC channel, 20Hz ≤ f ≤ 20kHz, V_{COMN1}, V_{COMP2} = $0.5V_{PP}$, R_L = 50Ω, DC bias = 0V, T_A = +25°C			0.05		%
BATTERY CHARGER (V_{VB} = 5V, V_{BAT} = 4V, T_A = -40°C to +85°C, unless otherwise specified)							
VBUS Charger Operating Range	V_{BUSOP}			4.0		V_{OVLO}	V
VBUSOK Trip Point	V_{BTP}	$V_{VB} – V_{BAT}$, rising		150	250	350	mV
		$V_{VB} – V_{BAT}$, falling		20	45	100	
		$V_{VB} – V_{BAT}$, hysteresis			205		
Input-Undervoltage Threshold	V_{BUVLO}	VB rising		3.8	3.9	4.0	V
Input-Undervoltage Threshold Hysteresis					600		mV
Input-Overvoltage Protection Threshold	V_{OVLO}	VB rising	OTPCGHCVS = 00	7.1	7.5	7.8	V
			OTPCGHCVS = 01		6.0		
			OTPCGHCVS = 10		6.5		
			OTPCGHCVS = 11		7.0		

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input-Overvoltage Threshold Hysteresis	V_{OVLO_HYS}				200		mV
SFOUT LDO Voltage	V_{SFOUT}	V_{VB} = 6.0V, I_{SFOUT} = 0mA		5.0	5.25	5.5	V
		V_{VB} = 5.0V, I_{SFOUT} = 15mA			4.9		
VB to BAT Input Resistance		V_{VB} = 4.1V, V_{BAT} = 4.0V			0.5		Ω
BAT Battery Regulation Voltage		I_{BAT} = 5mA, MBCCVWRC = 0000	T_A = +25°C	4.179	4.2	4.221	V
			T_A = -40°C to +85°C	4.158	4.2	4.242	
BAT Regulation Programmable Range	V_{BATREG}	I_{BAT} = 5mA (Note 8)	MBCCVWRC = 0001		4.0		V
			MBCCVWRC = 1111		4.35		
BAT Restart Fast-Charge Threshold	V_{BATRS}	From BAT regulation voltage, active only when AUTOSTOP is enabled			-150		mV
BAT Restart Fast-Charge Debounce					62		ms
Battery Fast-Charge Current	I_{BAT}	V_{BAT} = 3.5V	MBCICHWRCL = 0		90		mA
		V_{BAT} = 3.5V, MBCICHWRCL = 1	MBCICHWRCH = 0000		200		
			MBCICHWRCH = 0001		250		
			MBCICHWRCH = 0010		300		
			MBCICHWRCH = 0011		350		
			MBCICHWRCH = 0100		400		
			MBCICHWRCH = 0101	414	450	486	
			MBCICHWRCH = 0110		500		
			MBCICHWRCH = 0111		550		
			MBCICHWRCH = 1000		600		
			MBCICHWRCH = 1001		650		
			MBCICHWRCH = 1010		700		
			MBCICHWRCH = 1011		750		
			MBCICHWRCH = 1100		800		
			MBCICHWRCH = 1101		850		
			MBCICHWRCH = 1110		900		
			MBCICHWRCH = 1111		950		

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery End-of-Charge Threshold	I_{BAT_STOP}	I_{BAT} falling, battery is charged	EOCS = 0000		50		mA
			EOCS = 0001		60		
			EOCS = 0010		70		
			EOCS = 0011		80		
			EOCS = 0100		90		
			EOCS = 0101		100		
			EOCS = 0110		110		
			EOCS = 0111		120		
			EOCS = 1000		130		
			EOCS = 1001		140		
			EOCS = 1010		150		
			EOCS = 1011		160		
			EOCS = 1100		170		
			EOCS = 1101		180		
			EOCS = 1110		190		
			EOCS = 1111		200		
VB Prequalification Charge Current	I_{PRECHG}	V_{BAT} = 2V, V_{VB} = 5V			93		mA
Battery Charger Soft-Start Time		Ramp time from 93mA to fast-charge current			1.2		ms
Precharge Threshold	V_{PRECHG}				2.5		V
Precharge Threshold Hysteresis					170		mV
Precharge Watchdog Timeout					30		min
Fast-Charge Timer		TCHW = 000,001, 010, 101, or 110			5		Hour
		TCHW = 011			6		
		TCHW = 100			7		
Top-Off Timer					30		min
Die Temperature Thermal Limit	T_J	Die temperature rising (Note 9)			+105		°C

Electrical Characteristics (continued)

(V_{BAT} = 2.8V to 5.5V, V_{VB} = 3.5V to 5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{BAT} = 3.6V, V_{VB} = 5.0V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING SPECIFICATIONS (Figure 1)						
I²C Maximum Clock Frequency	f_{I2CCLK}			400		kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Repeated Start (SR) Condition Setup Time	$t_{SU:STA}$	90% to 90%	0.6			µs
START Condition Hold Time	$t_{HD:STA}$	10% of SDA to 90% of SCL	0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	0.6			µs
Clock Low Period	t_{LOW}	10% to 10%	1.3			µs
Clock High Period	t_{HIGH}	90% to 90%	0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Data setup time	100			ns
Data Setup Time to SCL Fall	$t_{HD:DAT}$	Data hold time	0			ns
ESD PROTECTION						
COMN1, COMP2, UID, BC		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap		±10		
		IEC61000-4-2 Contact		±7		
All Other Pins		Human Body Model		±2		kV

Note 5: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 6: Not production tested. Guaranteed by design.
Note 7: The JIG assertion time is a function of the ADC debounce time. Set the ADCDbSet bits in the CONTROL3 register to adjust this delay.
Note 8: Set the MBCCVWRC bits in the CHGCTRL3 register to adjust the battery regulation voltage, V_{BATREG}.
Note 9: The battery charge current is reduced when the die temperature reaches this limit.

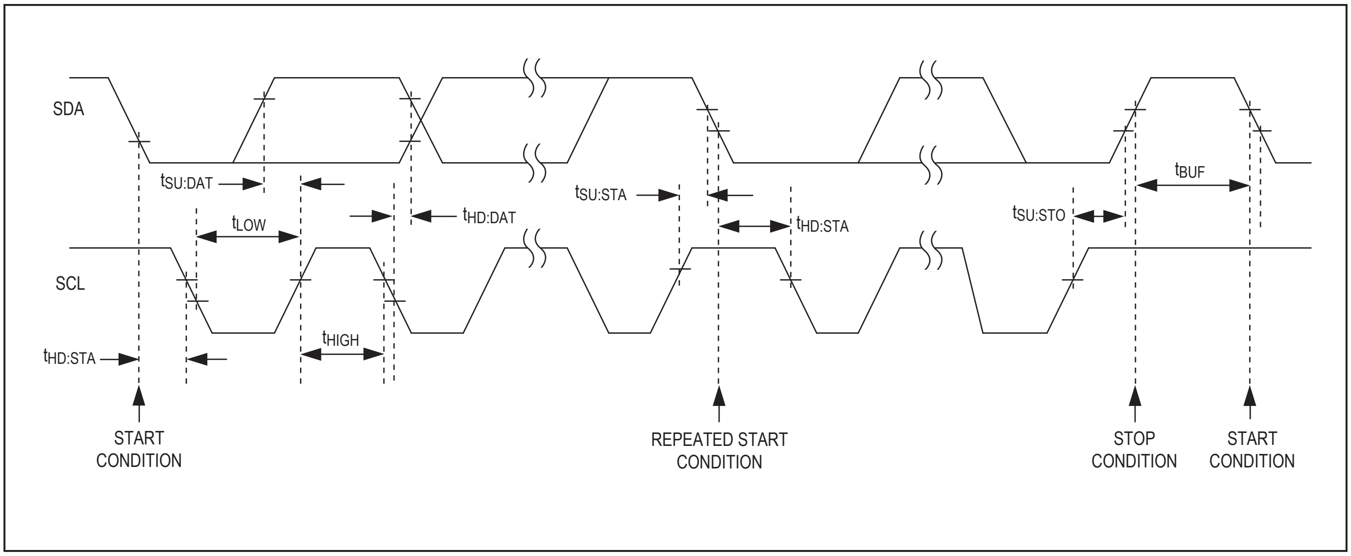
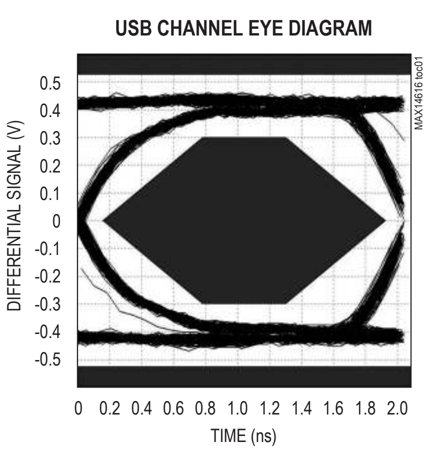
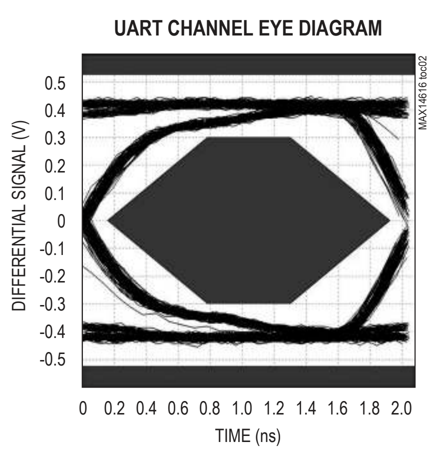


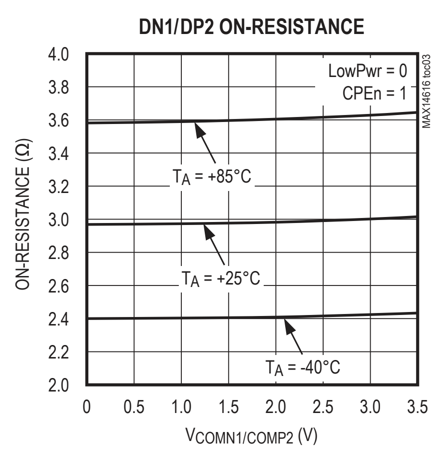
Figure 1. I²C Timing Diagram

Typical Operating Characteristics

(V_{BAT} = 4.0V, V_{VB} = 0V, T_A = +25°C, unless otherwise noted.)



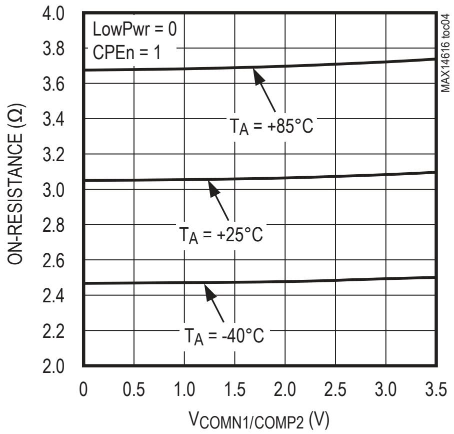




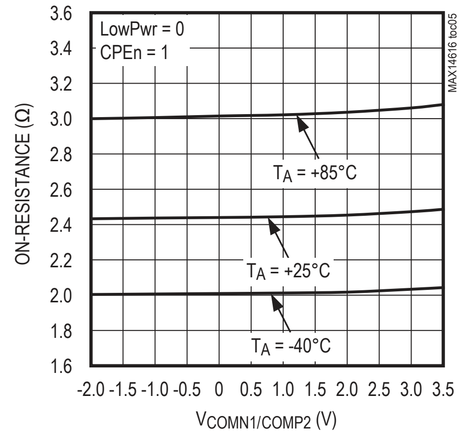
Typical Operating Characteristics (continued)

(V_{BAT} = 4.0V, V_{VB} = 0V, T_A = +25°C, unless otherwise noted.)

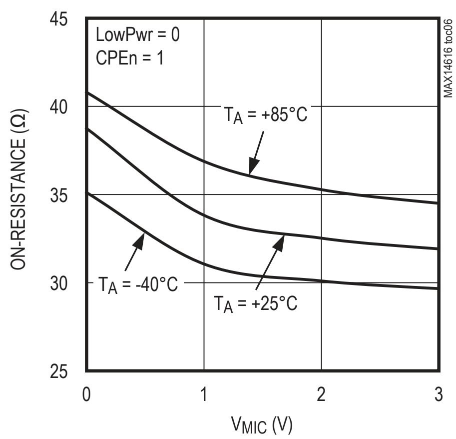
UT1/UR2 ON-RESISTANCE



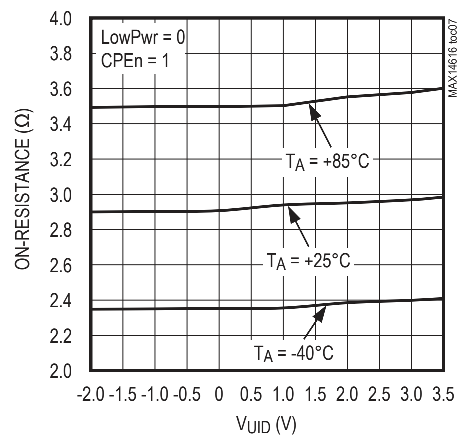
SL1/SR2 ON-RESISTANCE



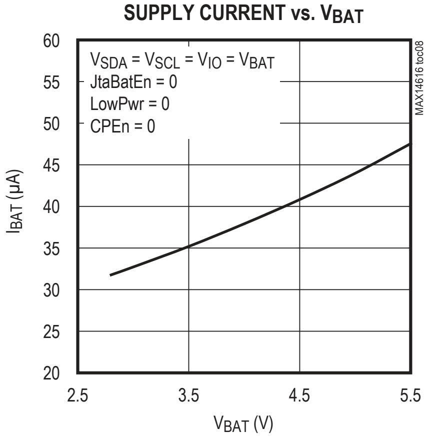
MIC ON-RESISTANCE



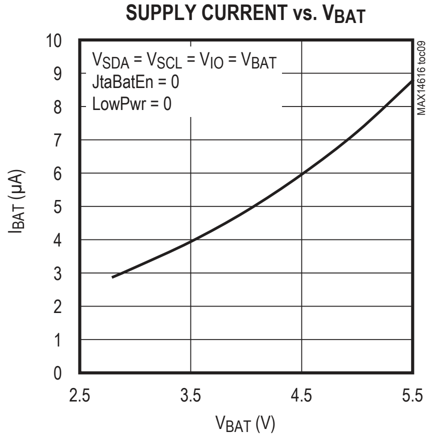
IDB ON-RESISTANCE



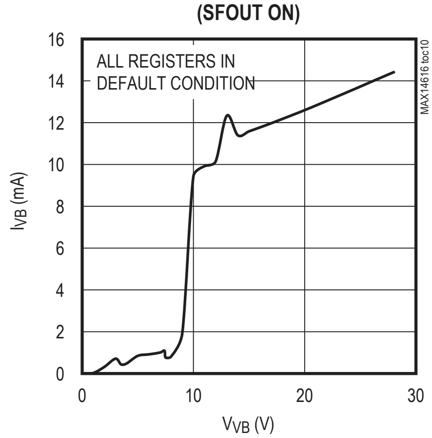
SUPPLY CURRENT vs. V_{BAT}



SUPPLY CURRENT vs. V_{BAT}



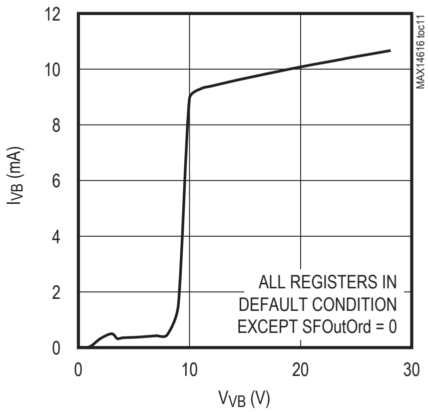
SUPPLY CURRENT vs. V_{VB} (SFOUT ON)



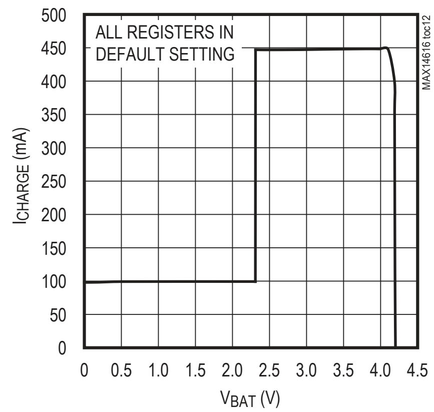
Typical Operating Characteristics (continued)

(V_{BAT} = 4.0V, V_{VB} = 0V, T_A = +25°C, unless otherwise noted.)

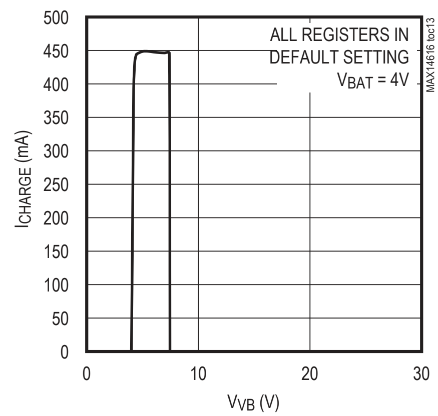
SUPPLY CURRENT vs. V_{VB} (SFOUT OFF)



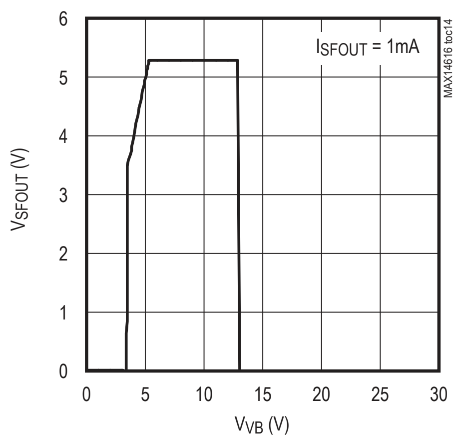
CHARGE CURRENT vs. V_{BAT} (V_{VB} = 5V)



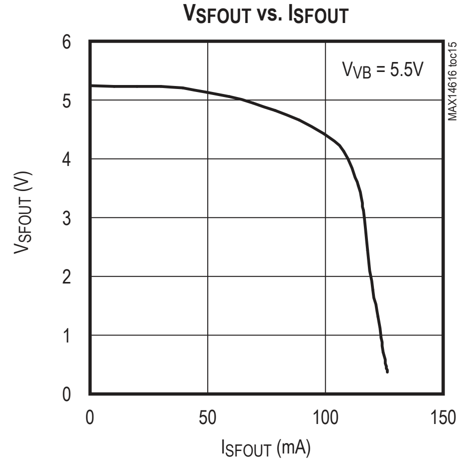
CHARGE CURRENT vs. V_{VB}



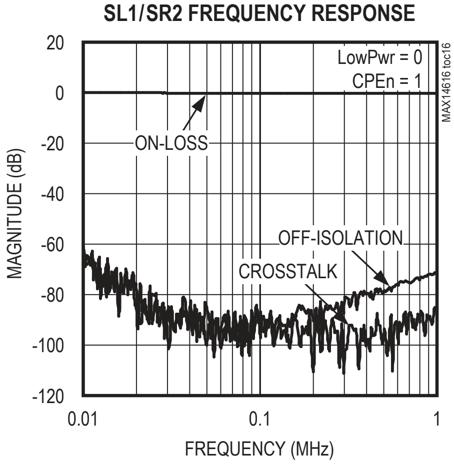
SFOUT VOLTAGE vs. VB VOLTAGE



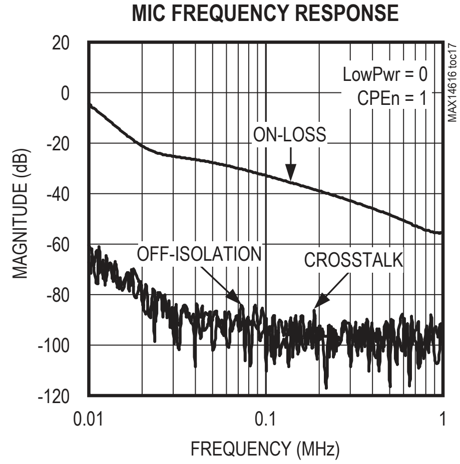
V_{SFOUT} vs. I_{SFOUT}



SL1/SR2 FREQUENCY RESPONSE

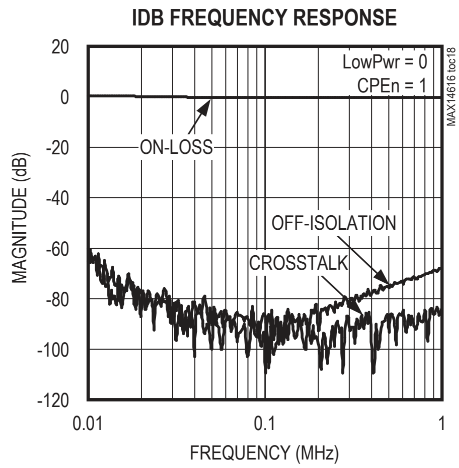


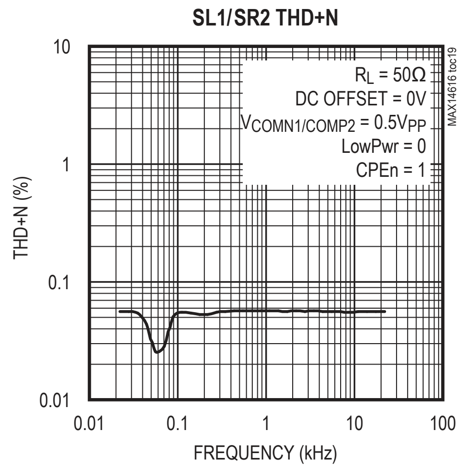
MIC FREQUENCY RESPONSE

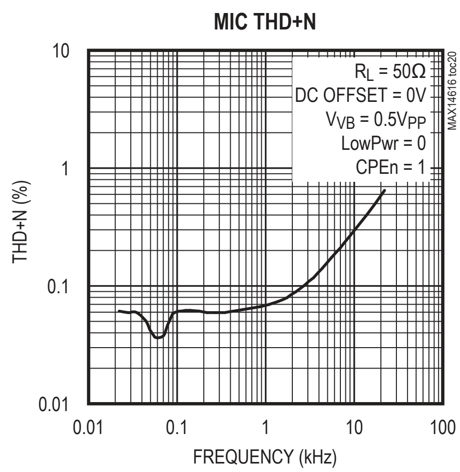


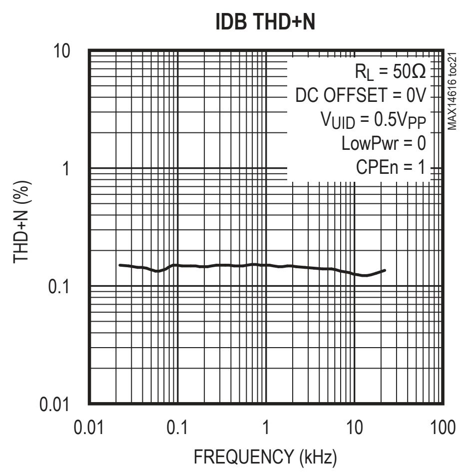
Typical Operating Characteristics (continued)

(V_{BAT} = 4.0V, V_{VB} = 0V, T_A = +25°C, unless otherwise noted.)





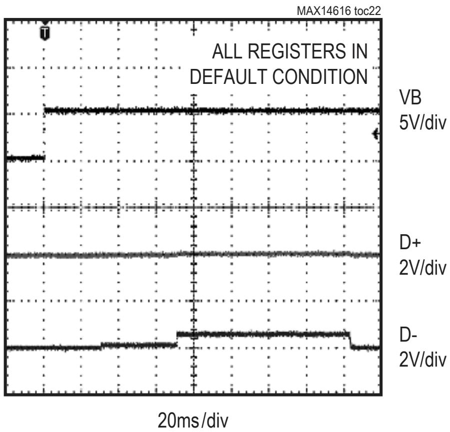




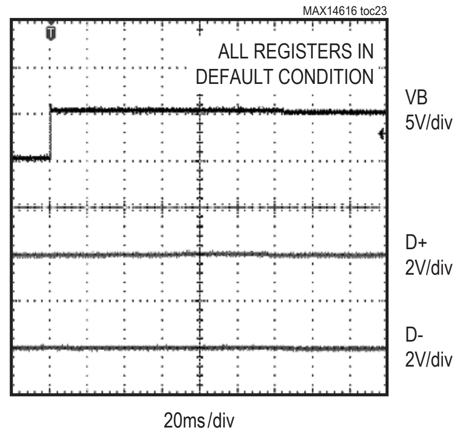
Typical Operating Characteristics (continued)

(V_{BAT} = 4.0V, V_{VB} = 0V, T_A = +25°C, unless otherwise noted.)

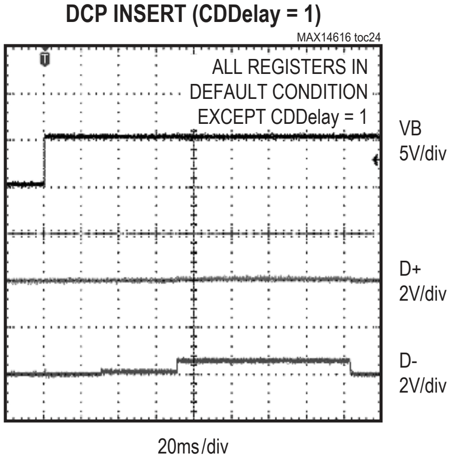
DCP INSERT



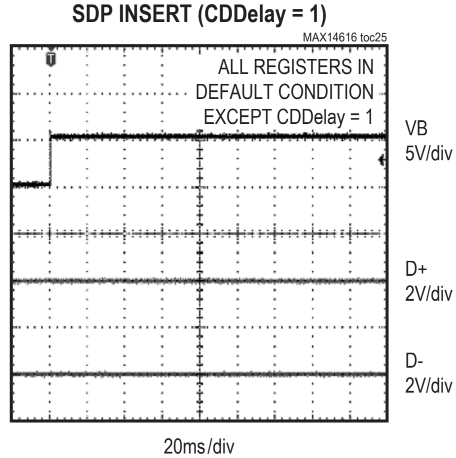
SDP INSERT



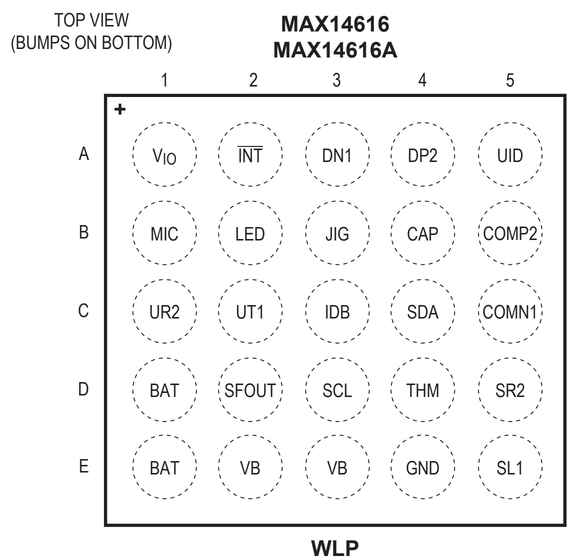
DCP INSERT (CDDelay = 1)



SDP INSERT (CDDelay = 1)



Bump Configuration



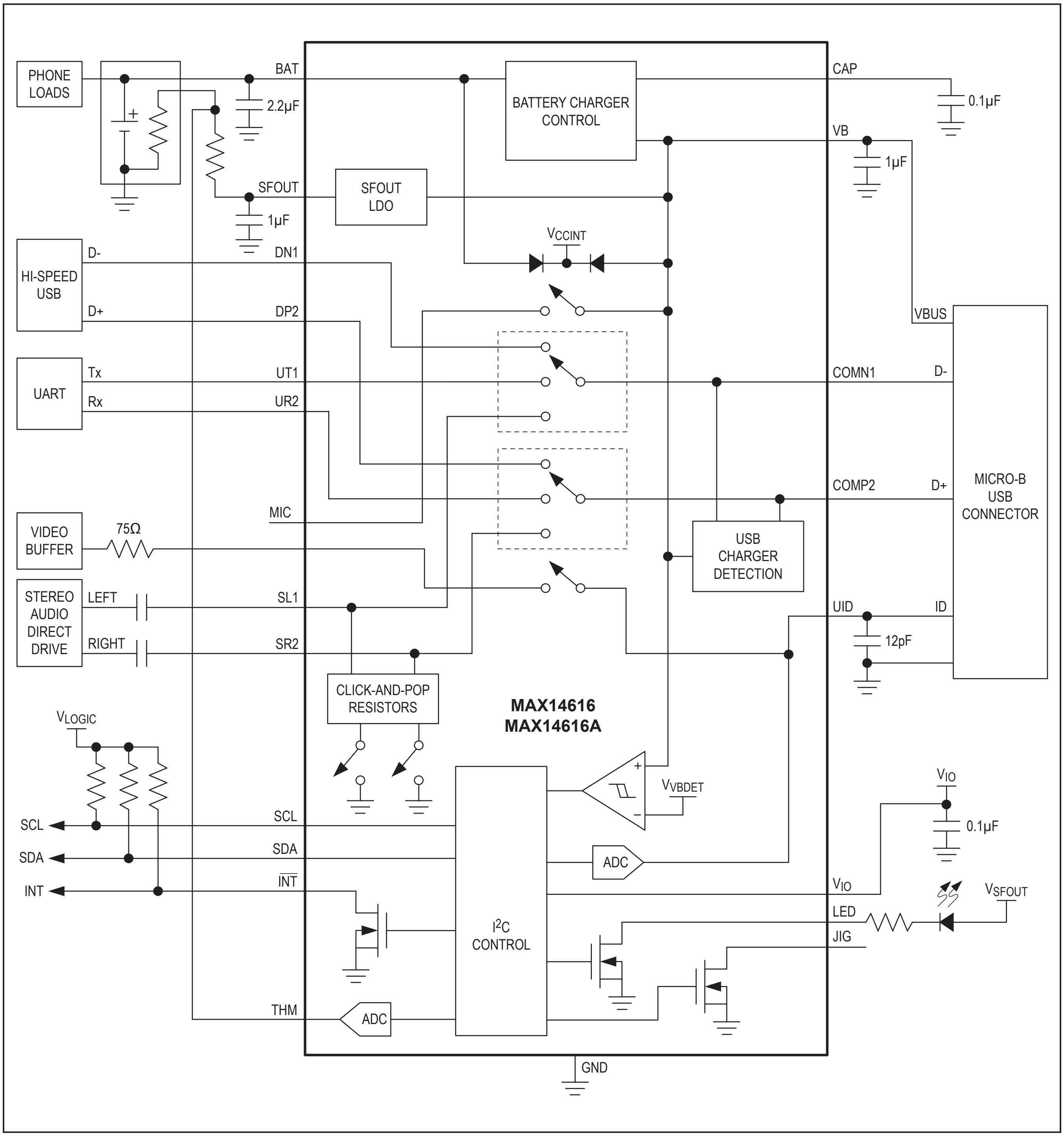
Bump Description

BUMP	NAME	FUNCTION
A1	V_{IO}	I^2C Reset Input. A falling edge on V_{IO} causes the I^2C registers to reset.
A2	$\overline{INT}$	Active-Low Open-Drain Interrupt Output. Connect $\overline{INT}$ to an external pullup resistor.
A3	DN1	USB D- Input/Output
A4	DP2	USB D+ Input/Output
A5	UID	USB ID Input. Connect UID to ID on micro-USB connector. Maximum capacitance allowed from UID to ground is 1nF.
B1	MIC	Microphone Output
B2	LED	Open-Drain LED Driver. LED is controlled by the battery charger status (Table 4) or the BTLDSet bits in the CONTROL3 register.
B3	JIG	Factory-Mode Open-Drain Output. JIG is controlled by the internal state machine or manually controlled by the JIGSet register bits.
B4	CAP	Internal LDO Bypass Output. Bypass CAP to GND with a 0.1µF (typ) ceramic capacitor for proper operation. Do not use CAP to drive an external load.
B5	COMP2	Common Input/Output 2. Connect COMP2 to D+ on the micro-USB connector.

Bump Description (continued)

BUMP	NAME	FUNCTION
C1	UR2	UART Receiver Input/Output
C2	UT1	UART Transmitter Input/Output
C3	IDB	USB ID Bypass. IDB is used to sense ID of the micro-USB connector for USB OTG transceivers and the pass composite video.
C4	SDA	I^2C Serial Data Input/Output. Connect SDA to external pullup resistor.
C5	COMN1	Common Input/Output 1. Connect COMN1 to D- on the micro-USB connector.
D1, E1	BAT	Battery Charger Output and Chip-Power Input. Bypass BAT to GND with a 2.2µF (min) ceramic capacitor.
D2	SFOUT	Overvoltage-Protected LDO Output. Internal LDO is powered from VB. Bypass SFOUT to GND with a 1µF (min) ceramic capacitor.
D3	SCL	I^2C Serial Clock Input. Connect SCL to an external pullup resistor.
D4	THM	Battery Presence Detection
D5	SR2	Stereo Audio Input/Output 2
E2, E3	VB	USB VBUS Input. VB provides power for internal circuitry when V_{BAT} is less than V_{VB}. VB is also the input source for the battery charger. Bypass VB to GND with a 1µF (min) ceramic capacitor.
E4	GND	Ground
E5	SL1	Stereo Audio Input/Output 1

Functional Diagram/Typical Application Circuit



Register Map

ADDRESS	NAME	b7	b6	b5	b4	b3	b2	b1	b0
0x00	**DEVICEID**	ChipID					DeviceID		
0x01	**INT1**	0	0	0	0	ADC1KI	ADCErrorI	ADCLowI	ADCI
0x02	**INT2**	0	0	VidRmI	VBVoltI	DXOVPI	DCDTmrI	ChgDetRunI	ChgTypI
0x03	**INT3**	0	0	BatDetI	ChgEnbldI	MBCCHGERRI	OVPI	CGMBCI	EOCI
0x04	**STATUS1**	ADC1K	ADCError	ADCLow	ADC				
0x05	**STATUS2**	VidRm	VBVolt	DXOVP	DCDTmr	ChgDetRun	ChgTyp		
0x06	**STATUS3**	0	BatDet		ChgEnbld	MBCCHGERR	OVP	CGMBC	EOC
0x07	**INTMASK1**	0	0	0	0	ADC1KM	ADCErrorM	ADCLowM	ADCM
0x08	**INTMASK2**	0	0	VidRmM	VBVoltM	DXOVPM	DCDTmrM	ChgDetRunM	ChgTypM
0x09	**INTMASK3**	0	0	BatDetM	ChgEnbldM	MBCCHGERRM	OVPM	CGMBCM	EOCM
0x0A	**CDETCTRL1**	CDPDet	0	DCDCpl	CDDelay	DCD2sCt	DCDEn	ChgTypMan	ChgDetEn
0x0B	**CDETCTRL2**	0	0	0	0	DxOVPEn	JtaBatEn	VidRmEn	FrcChg
0x0C	**CONTROL1**	IDBEn	MicEn	COMP2Sw			COMN1Sw		
0x0D	**CONTROL2**	RCPS	USBCpInt	AccDet	SFOutOrd	SFOutAsrt	CPEn	ADCEn	LowPwr
0x0E	**CONTROL3**	0	0	ADCDbSet		BTLDSet		JIGSet	
0x0F	**CHGCTRL1**	0	TCHW			0	1	0	0
0x10	**CHGCTRL2**	VCHGR_RC	MBCHOSTEN	0	1	0	1	0	0
0x11	**CHGCTRL3**	1	0	1	0	MBCCVWRC			
0x12	**CHGCTRL4**	0	0	0	MBCICHWRCL	MBCICHWRCH			
0x13	**CHGCTRL5**	0	0	1	0	EOCS			
0x14	**CHGCTRL6**	0	1	AUTOSTOP	1	0	0	0	1
0x15	**CHGCTRL7**	0	0	0	0	0	0	OTPCGHCVS	

Detailed Register Map

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
DEVICEID (0x00)				
ChipID (MAX14616)	Read Only	[7:3]	01110	**Chip Version**
ChipID (MAX14616A)	Read Only	[7:3]	10010	**Chip Version**
DeviceID	Read Only	[2:0]	101	**Device Identification**
INT1 (0x01) (All bits are cleared after a read) Bits in this register are set when associated bits in the STATUS1 register change. $\overline{\text{INT}}$ is asserted when any bit in the INT1 register is set, unless masked in the INTMASK1 register.				

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
RFU	Read Only	[7:4]	0000	Reserved
ADC1KI	Read Only	[3]	(Note 10)	**ADC 1K Detected or Removed Interrupt** 0 = No change 1 = ADC1K bit has changed
ADCErrorI	Read Only	[2]	(Note 10)	**ADC Error Interrupt** 0 = No change 1 = ADCError bit has changed
ADCLowI	Read Only	[1]	(Note 10)	**ADC Low-Bit Change Interrupt** 0 = No change 1 = ADCLow bit has changed
ADCI	Read Only	[0]	(Note 10)	**ADC Change Interrupt** 0 = No change 1 = ADC bits have changed
INT2 (0x02) (All bits are cleared after a read) Bits in this register are set when associated bits in the STATUS2 register change. $\overline{INT}$ is asserted when any bit in the INT2 register is set, unless masked in the INTMASK2 register.				
RFU	Read Only	[7:6]	00	Reserved
VidRmI	Read Only	[5]	(Note 10)	**Video Cable Removal Interrupt** 0 = No change 1 = VidRm bit has changed
VBVoltI	Read Only	[4]	(Note 10)	**VB Voltage Interrupt** 0 = No change 1 = VBVolt bit has changed
DXOVPI	Read Only	[3]	(Note 10)	**D+/D- OVP Interrupt** 0 = No change 1 = DXOVP bit has changed
DCDTmrI	Read Only	[2]	(Note 10)	**DCD Timer Interrupt** 0 = No change 1 = DCDTmr bit has changed
ChgDetRunI	Read Only	[1]	(Note 10)	**Charger Detection Running Status Interrupt** 0 = No change 1 = ChgDetRun bit has changed
ChgTypI	Read Only	[0]	(Note 10)	**Charger Type Interrupt** 0 = No change 1 = ChgTyp bits have changed
INT3 (0x03) (All bits are cleared after a read) Bits in this register are set when associated bits in the STATUS3 register change. $\overline{INT}$ is asserted when any bit in the INT3 register is set, unless masked in the INTMASK3 register.				

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
RFU	Read Only	[7:6]	00	Reserved
BatDetI	Read Only	[5]	(Note 10)	**Battery Presence Detect** 0 = No change 1 = BatDet bits have changed
ChgEnbldI	Read Only	[4]	(Note 10)	**Battery Charger Enable Interrupt** 0 = No change 1 = ChgEnbld bit has changed
MBCCHGERRI	Read Only	[3]	(Note 10)	**Battery Fast-Charge Timer Expire Interrupt** 0 = No change 1 = MBCCHGERR has changed
OVPI	Read Only	[2]	(Note 10)	**VB Overvoltage Protection Interrupt** 0 = No change 1 = OVP bit has changed
CGMBCI	Read Only	[1]	(Note 10)	**Charger Voltage OK Interrupt** 0 = No change 1 = CGMBC bit has changed
EOCI	Read Only	[0]	(Note 10)	**End-of-Charge Interrupt** 0 = No change 1 = EOC bit has changed
STATUS1 (0x04) Changes in bits in this register generate an interrupt in the INT1 register.				
ADC1K	Read Only	[7]	(Note 10)	**ADC 1KΩ Resistor Detection**. This bit is set when a 1kΩ or larger resistor to ground is detected on UID. 0 = No 1kΩ on UID 1 = 1kΩ detected on UID
ADCError	Read Only	[6]	(Note 10)	**ADC Error Detection**. This bit is set when the ADC cannot converge on a value due to noise or other interference. 0 = ADC Detection Error has not occurred 1 = ADC Detection Error has occurred
ADCLow	Read Only	[5]	(Note 10)	**ADCLow Bit**. This bit is cleared when UID is connected to GND. ADCLow is used to detect a 75Ω video cable; a video cable is present when ADCLow = 1 and ADC = 00000. See the *Accessory Detection* section for more information. 0 = UID resistance < 30Ω 1 = UID resistance ≥ 30Ω
ADC	Read Only	[4:0]	(Note 10)	**ADC Output**. Any change in the ADC bits triggers an interrupt in the INT1 register. See Table 4 in the *Accessory Detection* section.
STATUS2 (0x05) Changes in bits in this register generate an interrupt in the INT2 register.				

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
VidRm	Read Only	[7]	(Note 10)	**Video Cable Removal Detection Output**. VidRmEn must to be set to 1 and video amplifier is enabled and outputting a video signal for correct operation of VidRm function. The load removal can only be detected if the video amp is enabled and outputting a video signal. The video cable removal senses the change in the voltage drop across IDB and UID due to the presence of a video signal if a 75Ω monitor load is connected. 0 = Video load present 1 = Video cable load not present
VBVolt	Read Only	[6]	(Note 10)	**VB Detection Comparator Output**. This bit is set when the VBUS voltage rises above the VB detect threshold, V_{VBDET}. 0 = $V_{VB} < V_{VBDET}$ 1 = $V_{VB} \geq V_{VBDET}$
DXOVP	Read Only	[5]	(Note 10)	**D+/D- OVP Flag**. When DXOVP = 1, the charger detection state machine is forced off and CHGTYP = 000 to avoid reverse biasing from D+/D-. This flag can be asserted only when $V_{VB} \geq V_{VBDET}$. 0 = V_{COMN1} and $V_{COMP2} \leq V_{CCINT}$ 1 = V_{COMN1} or $V_{COMP2} > V_{CCINT}$
DCDTmr	Read Only	[4]	(Note 10)	**Data Contact Detection (DCD) Timer**. 0 = DCD timer is not running or is not expired 1 = DCD timer has been running for longer that 2 sec (min)
ChgDetRun	Read Only	[3]	(Note 10)	**Charger Detection State Machine Status**. 0 = Charger detection state machine is not running 1 = Charger detection state machine is running
ChgTyp	Read Only	[2:0]	(Note 10)	**USB Charger Detection Output**. 000 = Nothing attached 001 = USB cable attached 010 = Charging downstream port. Charger current depends on USB operating speed. 011 = Dedicated charger. The maximum charge current for the port is 1.5A. 100 = Apple 500mA charger. The maximum charge current for the port is 500mA. 101 = Apple 1A or 2A charger 110 = Special charger (bias on D+/D-) 111 = Reserved
STATUS3 (0x06) Changes in bits in this register generate an interrupt in the INT3 register.				

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
RFU	Read Only	[7]	0	Reserved
BatDet	Read Only	[6:5]	(Note 10)	**Battery Presence Monitor** 00 = Battery not present 01 = Reserved 10 = Battery present 11 = Reserved
ChgEnbld	Read Only	[4]	0	**Battery Charger Enable Status**. This bit only indicates the charger logic is enabled and does not indicate if the charger is passing current. See Tables 1 and 2. 0 = Charger is not enabled 1 = Charger is enabled
MBCCHGERR	Read Only	[3]	(Note 10)	**Battery Charger Error and Fast-Charging Timer Status**. Set the battery fast-charge timer in the CHGCTRL1 register (0x0F). 0 = Timer not expired 1 = Timer expired
OVP	Read Only	[2]	(Note 10)	**VB Overvoltage Protection Trip Level Status**. Set the VB overvoltage protection threshold in the CHGCTRL7 register (0x15). 0 = $V_{VB} \leq V_{OVLO}$ 1 = $V_{VB} > V_{OVLO}$
CGMBC	Read Only	[1]	(Note 10)	**Charger Power-OK Monitor**. This bit is set when the VB voltage is greater than the VBUSOK trip point voltage. 0 = $V_{VB} < V_{BTP}$ 1 = $V_{VB} \geq V_{BTP}$
EOC	Read Only	[0]	(Note 10)	**End-of-Charge Status**. This bit is set while charging a battery. 0 = Charger is in prequalification mode, fast-charge mode, disabled, or 30-minute top-off timer has expired (AUTOSTOP = 1) 1 = Charger is in top-off mode (AUTOSTOP = 1) or $I_{BAT} < I_{EOCS}$ (AUTOSTOP = 0).
INTMASK1 (0x07) Set the bits in the INTMASK1 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS1 and INT1 registers.				
RFU	Read Only	[7:4]	0000	Reserved
ADC1KM	Read/Write	[3]	0	**ADC 1K Detection Interrupt Mask** 0 = Mask 1 = Not masked
ADCErrorM	Read/Write	[2]	0	**ADC Error Interrupt Mask** 0 = Mask 1 = Not masked
ADCLowM	Read/Write	[1]	0	**ADC Low-Bit Change Interrupt Mask** 0 = Mask 1 = Not masked
ADCM	Read/Write	[0]	0	**ADC Change Interrupt Mask** 0 = Mask 1 = Not masked

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
INTMASK2 (0x08) Set the bits in the INTMASK2 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS2 and INT2 registers.				
RFU	Read Only	[7:6]	00	Reserved
VidRmM	Read/Write	[5]	0	**Video Cable Removal Interrupt Mask** 0 = Mask 1 = Not masked
VBVoltM	Read/Write	[4]	0	**VB Voltage Interrupt Mask** 0 = Mask 1 = Not masked
DXOVPM	Read/Write	[3]	0	**D+/D- OVPInterrupt Mask** 0 = Mask 1 = Not masked
DCDTmrM	Read/Write	[2]	0	**DCD Timer Interrupt Mask** 0 = Mask 1 = Not masked
ChgDetRunM	Read/Write	[1]	0	**Charger Detection Running Status Interrupt Mask** 0 = Mask 1 = Not masked
ChgTypM	Read/Write	[0]	0	**Charger Type Interrupt Mask** 0 = Mask 1 = Not masked
INTMASK3 (0x09) Set the bits in the INTMASK3 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS3 and INT3 registers.				
RFU	Read Only	[7:6]	00	Reserved
BatDetM	Read/Write	[5]	0	**Battery Detection Interrupt Mask** 0 = Mask 1 = Not masked
ChgEnbldM	Read/Write	[4]	0	**Battery Charger Enable Interrupt Mask** 0 = Mask 1 = Not masked
MBCCHGERRM	Read/Write	[3]	0	**Battery Fast-Charge Timer Interrupt Mask** 0 = Mask 1 = Not masked
OVPM	Read/Write	[2]	0	**VB Overvoltage Protection Interrupt Mask** 0 = Mask 1 = Not masked
CGMBCM	Read/Write	[1]	0	**Charger Voltage Power-OK Interrupt Mask** 0 = Mask 1 = Not masked
EOCM	Read/Write	[0]	0	**End-of-Charge Interrupt Mask** 0 = Mask 1 = Not masked

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CDETCTRL1 (0x0A)				
CDPDet	Read/Write	[7]	0	**USB-Charger Downstream-Port-Detection Method Selection** 0 = Use V_{DP_SRC} to drive D-. This is the reverse of the D+/D- short test. 1 = Use weak pullup method to detect USB CDP charger
RFU	Read/Write	[6]	0	Reserved
DCDCpl	Read/Write	[5]	1	**Data Contact Detection (DCD) Timeout Compliance Enable** 0 = Timeout 2000ms (typ) 1 = Timeout 900ms (max) (DCD Timeout Compliant to USB Battery Charger Detection Revision 1.2)
CDDelay	Read/Write	[4]	0	**Time Delay Before Charger Detection Starts After VBUS Is Valid** 0 = 0ms 1 = 500ms (typ)
DCD2sCt	Read/Write	[3]	1	**Data Contact Detection (DCD) Interrupt Exit** Sets the device to automatically exit Data Contact Detection when 2s interrupt is set (DCDTmr bit in the INT2 register is set). 0 = Stay in DCD until normal exit 1 = Always exit DCD when 2s interrupt is set
DCDEn	Read/Write	[2]	1	**Data Contact Detection (DCD) State Machine Enable** This bit enables/disables the DCD state machine prior to performing the short circuit detection on D+ and D-. When enabled, DCD must pass before D+/D- is tested for a short. If the DCD state machine is stuck, the DCD timer is set after 2sec (typ) and DCDTmr = 1. DCD is skipped when DCDEn = 0 and D+/D- short detection begins. 0 = Disable the DCD state machine 1 = Enable the DCD state machine
ChgTypMan	Read/Write	[1]	0	**Charger Type Manual Detection** This bit allows the user to force manual charger detection. The COMN1/COMP2 switches are open during manual charger detection. 0 = Disabled 1 = Force a Manual Charge Detection. This bit is automatically cleared when the detection state machine is complete.
ChgDetEn	Read/Write	[0]	1	**Charger Detection Enable**. This bit enables the USB charger detection on a rising edge on VB. 0 = Disabled. USB charger detection does not occur when the VB voltage rises. 1 = Enabled. USB charger detection occurs when $V_{VB} \geq V_{VBDET}$

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CDETCTRL2 (0x0B)				
RFU	Read only	[7:4]	0000	Reserved
DxOVPEn	Read/Write	[3]	1	**D+/D- OVP Monitor Enable** 0 = Disabled 1 = Enabled
JtaBatEn	Read/Write	[2]	1	**Battery Detection Enable** 0 = Disabled 1 = Enabled
VidRmEn	Read/Write	[1]	0	**Video Cable Load Removal Detection Enable.** 0 = Disabled 1 = Enabled
FrcChg	Read/Write	[0]	0	**Force Charger On**. In case of charger detection disabled (ChgDetEn = 0) or USB SDP with USB compliance enabled (USBCpInt = 1), the charger is turned off when a valid USB is present. Set FrcChg bit to 1 to force the charger to turn on. FrcChg is reset to 0 when VBUS is removed. Other charger controls may turn the charger off even when FrcChg = 1 (VCHGR_RC, MBCHOSTEN, AUTOSTOP, OVP, MBCCHGERR, BatDet). 0 = Charger is controlled by automatic state machine 1 = Charger is forced on
CONTROL1 (0x0C)				
IDBEn	Read/Write	[7]	0	**USB ID Bypass Enable**. Set to connect IDB to UID. 0 = Switch is open 1 = IDB connected to UID
MicEn	Read/Write	[6]	0 (Note 11)	**Microphone Enable**. Set to connect MIC to VB. 0 = Switch is open 1 = MIC connected to VB
COMP2Sw	Read/Write	[5:3]	000 (Note 11)	**COMP2 Switches Control**. Set these bits to connect COMP2 to DP2, SR2, or UR2. 000 = Switch is open 001 = COMP2 connected to DP2 (USB) 010 = COMP2 connected to SR2 (Audio Right) 011 = COMP2 connected to UR2 (UART RX) 100 to 111 = Switch is open
COMN1Sw	Read/Write	[2:0]	000 (Note 11)	**COMN1 Switches Control**. Set these bits to connect COMN1 to DN1, SL1, or UT1. 000 = Switch is open 001 = COMN1 connected to DN1(USB) 010 = COMN1 connected to SL1 (Audio Left) 011 = COMN1 connected to UT1 (UART TX) 100 to 111 = Switch is open

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CONTROL2 (0x0D)				
RCPS	Read/Write	[7]	0	**Click-and-Pop Resistors Setting**. Set this bit to enable or disable the click and pop reduction resistors on SL1 and SR2. 0 = Disabled 1 = Enabed
USBCplnt	Read/Write	[6]	0	**USB 2.0 Compliant Setting**. Set this bit if the battery charger is USB 2.0 compliant. 0 = Not USB 2.0 compliant 1 = USB 2.0 compliant
AccDet	Read/Write	[5]	1	**Automatic Accessory Detection Setting**. This bit enables the factory accessory detection state machine. This bit must be 0 for manual accessory detection through firmware. 0 = Disable factory accessory detection state machine 1 = Enable factory accessory detection state machine
SFOutOrd	Read/Write	[4]	1	**SFOUT Override Control**. This bit enables/disables SFOUT. 0 = Force SFOUT to off. The internal LDO is disabled and V_{SFOUT} is 0V when this bit is 0. 1 = SFOUT is automatically controlled by the VB voltage present and the SFOutAsrt bit.
SFOutAsrt	Read/Write	[3]	0	**SFOUT Assertion Control**. Set this bit to control the period when SFOUT turns on. 0 = SFOUT turns on after a complete run of the charger detection state machine or after a correct detection of a factory cable. 1 = SFOUT turns on always after a valid VBUS voltage detection with no wait.
CPEn	Read/Write	[2]	0	**Charge-Pump Enable**. This bit controls the charge pump required for the analog switches operation. The factory accessory state machine will automatically set CPEn = 1 when the analog switches are configured. Firmware can change this bit at any time. 0 = Disabled 1 = Enabed
ADCEn	Read/Write	[1]	1	**ADC Enable**. This bit enables or disables the internal ADC for accessory detection. 0 = ADC disabled 1 = ADC enabled
LowPwr	Read/Write	[0]	1	**ADC Low-Power-Mode Setting**. This bit enables low-power pulse mode for the internal ADC. 0 = Disable low-power mode 1 = Enable low-power mode

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CONTROL3 (0x0E)				
RFU	Read/Write	[7:6]	00	Reserved
ADCDbSet	Read/Write	[5:4]	00	**ADC Debounce Time Setting**. Set these bits to control the ADC debounce time. 00 = 0.5ms 01 = 10ms 10 = 25ms 11 = 38.62ms
BTLDSet	Read/Write	[3:2]	00	**LED Output Setting**. Set these bits to manually control the LED output. (Note 12) 00 = LED is controlled by auto detection 01 = LED is output low 10 = LED is high impedance 11 = LED is high impedance
JIGSet	Read/Write	[1:0]	00	**Jig Output Setting**. Set these bits to manually control the JIG output. (Note 12) 00 = JIG is controlled by auto detection 01 = JIG is high impedance 10 to 11 = JIG is output low
CHGCTRL1 (0x0F)				
RFU	Read Only	[7]	0	Reserved
TCHW	Read/Write	[6:4]	010	**Battery Fast-Charge Timer**. Set these bits to select the timer for fast-charge mode. 010 = 5hr 011 = 6hr 100 = 7hr 111 = Disable the fast-charge timer. 000, 001, 101, 110 = 5hr
RFU	Read Only	[3:0]	0100	Reserved
CHGCTRL2 (0x10)				
VCHGR_RC	Read/Write	[7]	1	**Wall-Adapter Rapid Charge**. Set this bit to enable battery fast-charge. 0 = Fast-charge mode is disabled. Charger remains in prequalification charge mode. 1 = Enable wall adapter rapid charge.
MBCHOSTEN	Read/Write	[6]	1	**Battery Charger Host Enable**. Set this bit to enable or disable the charger. The battery charger is automatically enabled when MBCHOSTEN = 1 and when ChgDetRun = 0 and ChgTyp = 010, 011, 100, or 101. If USBCplnt = 0, the charger is automatically turned on when ChgTyp = 001. 0 = Disabled 1 = Enabled
RFU	Read Only	[5:0]	010100	Reserved

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION	
CHGCTRL3 (0x11)					
RFU	Read Only	[7:4]	1010	Reserved	
MBCCVWRC	Read/Write	[3:0]	0000	**Battery-Charger Constant Voltage (CV) Mode**. Set these bits to control the regulated battery voltage.	
				0000 = 4.20V 0001 = 4.00V 0010 = 4.02V 0011 = 4.04V 0100 = 4.06V 0101 = 4.08V 0110 = 4.10V 0111 = 4.12V	1000 = 4.14V 1001 = 4.16V 1010 = 4.18V 1011 = 4.22V 1100 = 4.24V 1101 = 4.26V 1110 = 4.28V 1111 = 4.35V
CHGCTRL4 (0x12)					
RFU	Read Only	[7:5]	000	Reserved	
MBCICHWRCL	Read/Write	[4]	1	**Fast Battery Charge Current-Low Bit**. Set this bit to select the fast-charge current limit for battery charging. When this bit is 1, the charge current is defined by MBCICHWRCH. 0 = 90mA 1 = 200mA to 950mA	
MBCICHWRCH	Read/Write	[3:0]	0101	**Fast Battery Charge Current-High Bits**. Set these bits to select the fast-charge current limit for battery charging.	
				0000 = 200mA 0001 = 250mA 0010 = 300mA 0011 = 350mA 0100 = 400mA 0101 = 450mA 0110 = 500mA 0111 = 550mA	1000 = 600mA 1001 = 650mA 1010 = 700mA 1011 = 750mA 1100 = 800mA 1101 = 850mA 1110 = 900mA 1111 = 950mA

Detailed Register Map (continued)

FIELD NAME	READ/WRITE	BITS	DEFAULT	DESCRIPTION
CHGCTRL5 (0x13)				
RFU	Read Only	[7:4]	0010	Reserved
EOCS	Read/Write	[3:0]	0000	**End-of-Charge Current Setting**. Set these bits to select the current threshold level that triggers the end-of-charge (EOC) interrupt. 0000 = 50mA 0001 = 60mA 0010 = 70mA 0011 = 80mA 0100 = 90mA 0101 = 100mA 0110 = 110mA 0111 = 120mA 1000 = 130mA 1001 = 140mA 1010 = 150mA 1011 = 160mA 1100 = 170mA 1101 = 180mA 1110 = 190mA 1111 = 200mA
CHGCTRL6 (0x14)				
RFU	Read Only	[7:6]	01	Reserved
AUTOSTOP	Read/Write	[5]	1	**Auto Charging Stop**. See Figure 5. 0 = Disable charging shutoff. 1 = Enable charging shutoff after 30 min timer.
RFU	Read Only	[4:0]	10001	Reserved
CHGCTRL7 (0x15)				
RFU	Read Only	[7:2]	000000	Reserved
OTPCGHCVS	Read/Write	[1:0]	00	**Overvoltage Protection Threshold**. Set these bits to select the overvoltage protection threshold on VB (V_{OVLO}). In an overvoltage condition, $\overline{INT}$ asserts and charging stops; however, the MBCHOSTEN bit is not changed. 00 = V_{OVLO} is 7.5V 01 = V_{OVLO} is 6.0V 10 = V_{OVLO} is 6.5V 11 = V_{OVLO} is 7.0V

Note 10: The initial power-up value of these bits is dependent of the state of the device at power-up.
Note 11: The values of these bits represent the current operating state of the part when AccDet = 1.
Note 12: The initial power-up value of the JIG output depends on the resistor present at UID.

Table 1. Charger Status and I^2C bits

BatDet	MBCHOSTEN	VBVolt	MBCCHGERR	FrcChg	ChgDetRun	ChgTyp	AUTOSTOP	USBCpInt	ChgEnbld	CHARGER STATUS
00	X	X	X	X	X	X	X	X	0	Off
10	0	X	X	X	X	X	X	X	0	Off
10	1	0	X	X	X	X	X	X	0	Off
10	1	1	1	X	X	X	X	X	0	Off
10	1	1	0	X	1	X	X	X	0	Off
10	1	1	0	0	0	X	0 or (1 and 30 min timer not expired)	0	1	On
10	1	1	0	0	0	X	1 and 30 min timer expired	0	0	Off
10	1	1	0	0	0	Not 001	0 or (1 and 30 min timer not expired)	1	1	On
10	1	1	0	0	0	Not 001	1 and 30 min timer expired	1	0	Off
10	1	1	0	0	0	000	X	X	0	Off
10	1	1	0	1	0	000	0 or (1 and 30 min timer not expired)	X	1	On
10	1	1	0	1	0	000	1 and 30 min timer expired	X	0	Off
10	1	1	0	0	0	001	X	1	0	Off
10	1	1	0	1	0	001	0 or (1 and 30 min timer not expired)	1	1	On
10	1	1	0	1	0	001	1 and 30 min timer expired	1	0	Off

X = Don't Care

Detailed Description

The MAX14616/MAX14616A contain a Li+ battery charger, charger type detection block, and multiplex USB 2.0 Hi-Speed, UART, stereo audio, and a microphone on a single micro-USB connector. This device features an internal detection resource for determining the device connected and are controlled through the I^2C interface. Audio inputs feature negative-rail signal operation down to -2V (typ). The MAX14616/MAX14616A support USB Charging Specification Revision 1.1 and include a complete Li+ battery charger with adjustable maximum current up to 950mA.

Input Sources and Routing

The typical micro-USB connector has five signal lines: USB power, two USB signal lines (D-, D+), ID line, and ground. The USB power on the micro-USB connector connects to VB on the MAX14616/MAX14616A. The two USB signal lines, D-/D+, connect to COMN1 and COMP2. The ID line connects to the UID input.

USB Switch (DN1, DP2)

The MAX14616/MAX14616A support Hi-Speed, full speed, and speed USB signal levels. The USB channel is bidirectional and has low 3Ω (typ) on-resistance. The low on-resistance is stable as the analog input signals are swept from ground to V_{SWPOS} for low signal distortion.

UART Switch (UT1, UR2)

The MAX14616/MAX14616A support standard single-supply UART signals. The UART channel can also be used for Hi-Speed USB signals. The UART channel is bidirectional and has low 3Ω (typ) on-resistance.

Stereo Audio (SL1, SR2) and Microphone (MIC)

The MAX14616/MAX14616A support a stereo audio amplifier with a mono microphone. Figure 2 shows a typical application for a cell phone headset with a push-button remote control (see the *Accessory Detection* section) through a micro-USB connector. The MAX14616/MAX14616A route the LEFT (SL1) and RIGHT (SR2) channel audio to the D- (COMN1) and D+ (COMP2) lines. SL1 and SR2 are negative-rail capable to V_{SWNEG}. Internal 100Ω (typ) switched shunt resistors on the LEFT and RIGHT channel speaker lines can be enabled through the RCPS bit in the CONTROL2 register to reduce pops and clicks heard when the audio amplifier is switched on (See *Click and Pop Reduction*). The microphone signal is routed through the VBUS line on the micro-USB connector. SL1 and SR2 can alternatively be used to route a USB high-speed signal.

Composite Video with Stereo Audio

Composite video is supported by a cable with stereo audio output on D+/D-, and composite video on ID. The video cable is a unique case because it can be either an ID resistor (365kΩ) for a cable that is not connected to a

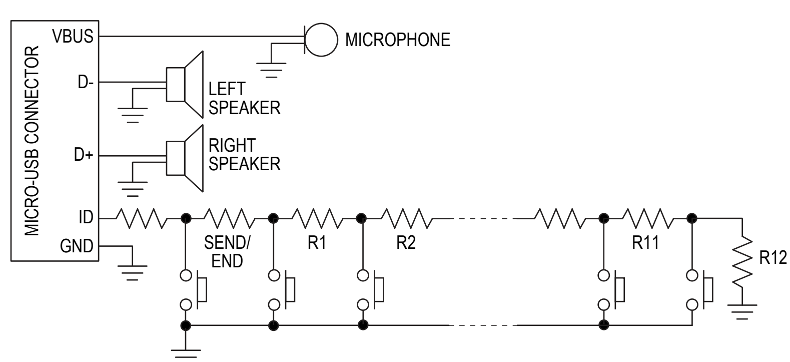


Figure 2. Headset with Remote Control

TV, or a 75Ω load to ground if the cable is connected to a TV. If the ADC reads a no-load video cable (365kΩ), then the system may choose to either ignore this condition and wait for 75Ω load, or indicate a GUI message to user to connect to video display. If an ADC reading of 0b00000 (ground) is found, the ADCLow bit is read to detect the difference between a 75Ω video load, and a ground ID pin for a USB OTG cable. After a 75Ω load is discovered, the video amplifier can be turned on and the IDB switch can be closed. Before enabling the video amplifier and closing the IDB switch, the ADC needs to be disabled (ADCEn = 0) to avoid interrupts from the video signal on the USB ID line. The removal of the video 75Ω load is detected using the video load removal circuit. Set VidRmEn = 1 and unmask the VidRm interrupt. After the removal is detected, open the IDB switch, disable the video removal detection (VidRmEn = 0) and enable the ADC. Note that if video removal detection is active, either turning off the video signal or removing the 75Ω load causes an interrupt to indicate video cable removal.

High-Impedance Mode for COMN1/COMP2

The MAX14616/MAX14616A allow COMN1 and COMP2 set to high-impedance (COMN1Sw and COMP2Sw = 100 to 111) to have a safe position when a headset is inserted. If COMN1 or COMP2 are left connected to one of the four inputs, there is a possibility of having a DC voltage present, causing a pop when a connection is made to a speaker.

Click-and-Pop Reduction

The MAX14616/MAX14616A support click-and-pop reduction through the RCPS bit in the CONTROL2 register. Set RCPS to 1 to connect 100Ω shunt resistors from the audio inputs (SL1 and SR2) to GND to remove any DC bias that results from AC-coupling capacitors prior to connecting them to COMN1 or COMP2.

Disable the click-and-pop shunt resistors prior to using the channel.

SFOUT LDO Output

The SFOUT LDO provides a 4.9V (typ) output, typically used to power a USB transceiver. SFOUT provides a voltage-limited supply that protects the USB transceiver from transient voltages up to 28V.

Factory Mode

Accessory detection is enabled at power-up (AccDet = 1 in the CONTROL2 register), enabling the Factory Detection State Machine (Figure 3). The MAX14616/MAX14616A detect accessories in the following order of priority:

1) Four factory-mode ID resistor values (see Table 2)
2) Audio headset. The accessory is detected as either a 1MΩ resistor, or any button press resistor value when VBUS is not present (see Table 3).
3) USB cable. A USB cable is detected when UID is unconnected and the ChgTyp bits in the STATUS2 register are ‘001’ or ‘010’. Charging may also be enabled automatically when ChgTyp = 001 if USBCpInt = 0.
4) Dedicated chargers. ChgTyp bits in the STATUS2 register are ‘011’, ‘100’, ‘101’, or ‘110’.

The MAX14616/MAX14161A factory detection state machine detects the external accessories and automatically configures the internal switches and JIG outputs (Table 2). Set the AccDet bit to 0 to disable automatic accessory detection. When automatic detection is disabled, the internal switch states must be manually controlled through the I^2C interface. It is recommended to always use software control instead of the automatic accessory detection after the host microprocessor boots.

Accessory Detection

The MAX14616/MAX14616A support multiple accessories by detecting unique characteristics including VB voltage, ID resistor, and USB charger detection. See Table 3 for more information.

Table 2. Factory-Mode Resistor Response (R_{ID})

R_{ID}	JIG	COMN1	COMP2
255kΩ	LOW	DN1	DP2
301kΩ	LOW	DN1	DP2
523kΩ	LOW	UT1	UR2
619kΩ	LOW	UT1	UR2
All other resistors	HIGH-Z	OPEN	OPEN

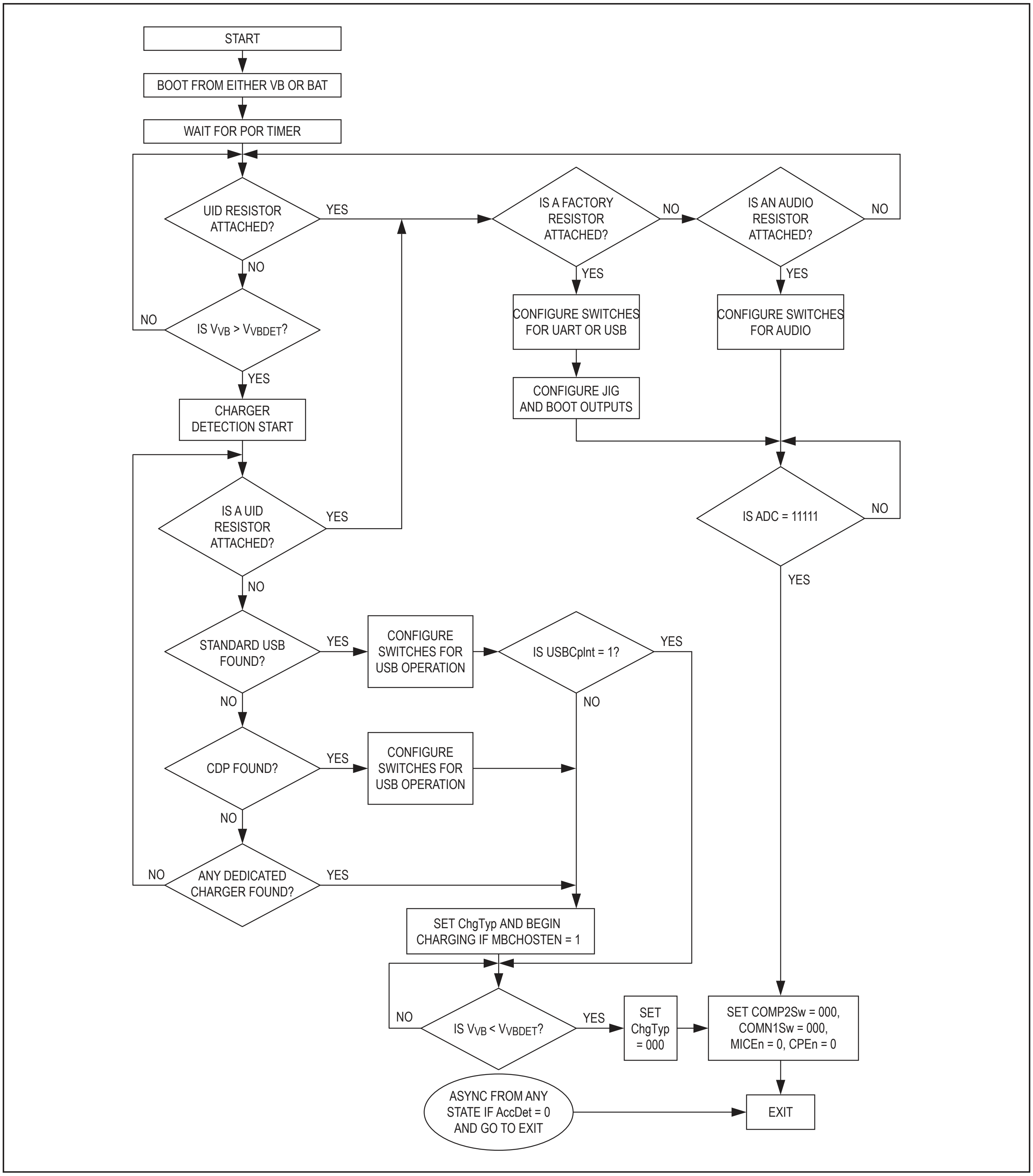


Figure 3. Factory Accessory Detection State Machine

Table 3. Accessory Detection Characteristics

ADC VALUE						ID RESISTOR	ADCLow	ADC1K	DESCRIPTION
HEX	4	3	2	1	0				
0x00	0	0	0	0	0	GND	0	0	USB OTG
						75Ω	1	0	Video Cable with Load
						1kΩ	1	1	1kΩ Resistor
0x01	0	0	0	0	1	2kΩ	1	0	SEND/END Button
0x02	0	0	0	1	0	2.604kΩ	1	0	Remote S1 Button
0x03	0	0	0	1	1	3.208kΩ	1	0	Remote S2 Button
0x04	0	0	1	0	0	4.014kΩ	1	0	Remote S3 Button
0x05	0	0	1	0	1	4.82kΩ	1	0	Remote S4 Button
0x06	0	0	1	1	0	6.03kΩ	1	0	Remote S5 Button
0x07	0	0	1	1	1	8.03kΩ	1	0	Remote S6 Button
0x08	0	1	0	0	0	10.03kΩ	1	0	Remote S7 Button
0x09	0	1	0	0	1	12.03kΩ	1	0	Remote S8 Button
0x0A	0	1	0	1	0	14.46kΩ	1	0	Remote S9 Button
0x0B	0	1	0	1	1	17.26kΩ	1	0	Remote S10 Button
0x0C	0	1	1	0	0	20.5kΩ	1	0	Remote S11 Button
0x0D	0	1	1	0	1	24.07kΩ	1	0	Remote S12 Button
0x0E	0	1	1	1	0	28.7kΩ	1	0	Reserved Accessory1
0x0F	0	1	1	1	1	34kΩ	1	0	Reserved Accessory2
0x10	1	0	0	0	0	40.2kΩ	1	0	Reserved Accessory3
0x11	1	0	0	0	1	49.9kΩ	1	0	Reserved Accessory4
0x12	1	0	0	1	0	64.9kΩ	1	0	Reserved Accessory5
0x13	1	0	0	1	1	80.07kΩ	1	0	CEA936 Audio Mode
0x14	1	0	1	0	0	102kΩ	1	0	Phone Powered Device
0x15	1	0	1	0	1	121kΩ	1	0	TTY Converter
0x16	1	0	1	1	0	150kΩ	1	0	UART Cable
0x17	1	0	1	1	1	200kΩ	1	0	CEA-936A Type 1 Charger
0x18	1	1	0	0	0	255kΩ	1	0	Factory-Mode USB
0x19	1	1	0	0	1	301kΩ	1	0	Factory-Mode USB
0x1A	1	1	0	1	0	365kΩ	1	0	Audio Video Cable with no Load
0x1B	1	1	0	1	1	442kΩ	1	0	CEA-936A Type 2 Charger
0x1C	1	1	1	0	0	523kΩ	1	0	Factory-Mode UART
0x1D	1	1	1	0	1	619kΩ	1	0	Factory-Mode UART
0x1E	1	1	1	1	0	1000kΩ	1	0	Audio Mode with Remote
0x1F	1	1	1	1	1	Open	1	0	USB, Dedicated Charger or Accessory Removal

Interrupts

The MAX14616/MAX14616A generate an interrupt in response to accessory insertion, removal, and to battery-charger status changes. The STATUS1 (0x04), STATUS2 (0x05), and STATUS3 (0x06) registers are the status bits for each interrupt source; changes of these bits set the associated interrupt bits in the INTx registers. The INTx registers are cleared after a read. See the *Detailed Register Map* for more information.

The INT1 (0x01), INT2 (0x02), and INT3 (0x03) registers contain the interrupt source bit. $\overline{\text{INT}}$ is asserted when any of these bits that are set unless masked in the INTMASKx registers. Read an INTx register to clear that register and deassert the $\overline{\text{INT}}$ output.

Each interrupt is independently maskable. Set any of the bits in the INTMASK1 (0x07), INTMASK2 (0x08), and INTMASK3 (0x09) registers to mask the associated interrupts. Bits in the INTx registers are set but $\overline{\text{INT}}$ is not asserted for masked interrupts. All interrupts are masked by default.

Detection Debounce

The MAX14616/MAX14616A include debounce timers to avoid generating multiple interrupts at the insertion of an accessory and for added noise and disturbance protection. The interrupt state must be maintained for the duration of the debounce delay before an interrupt at $\overline{\text{INT}}$ is generated.

The ADC debounce can be changed by the ADCDbSet bits in the CONTROL3 (0x0E) register to adjust the debounce delay during accessory insertion and removal.

Low-Power Modes

The MAX14616/MAX14616A contain multiple low-power modes. Set the appropriate bits (CPEn, ADCEn, or LowPwr) in the CONTROL2 register (0x0D) to enter low-power mode.

The CPEn bit controls the charge pump required for proper operation of the analog switches. Set CPEn to 0 to disable the charge pump. CPEn must be set to 1 anytime that a switch is enabled. Do not apply a negative-rail voltage to any switch when the charge pump is disabled. The MAX14616/MAX14616A turn on the charge pump automatically when AccDet = 1 when the switches are configured.

ADCEn controls the internal ADC. Set ADCEn to 0 to disable the ADC. In this mode, the ADC bits in the STATUS1 register are set to ‘11111,’ disabling all interrupt detection. Any pending interrupts due to a change in ADC value must still be cleared by reading the INT1 register.

Set the LowPwr bit to 1 to enable the ADC low-power mode. The MAX14616 enters the ADC low-power mode only if LowPwr = 1 and UID is not connected. The ADC will exit this mode and resume normal operation if any condition changes on UID.

USB Charger Detection

The MAX14616/MAX14616A detect battery charging sources as defined in USB Battery Charging rev1.1 (USB BC1.1) and are also able to detect charger types typically used by Apple devices. The MAX14616/MAX14616A also feature optional Data Contact Detection (DCD) as defined by USB BC1.2 with a configurable timeout.

The MAX14616/MAX14616A are capable of detecting multiple USB battery charging methods include Standard Downstream Ports (SDP), Charging Downstream Ports (CDP), Dedicated Charging Ports (DCP), Apple 500mA, 1000mA, and 2000mA chargers, and special charger (bias on D+/D-). Connecting a valid VBUS voltage to VB when ChgDetEn = 1 in the CDETCTRL1 register (0x0A) will enable automatic charger detection mode or set the ChgTypMan bit in the CDETCTRL1 register to 1 to force a manual charge detection. After the VB detection debounce delay, the MAX14616 opens the COMN1 and COMP2 (USB D- and D+) switches and initializes the internal state machine to detect the type of charging source connected. While in charger detection mode, checking for battery chargers in the following order:

1) Either VBUS rises above the VB detect threshold or ChgTypMan = 1. COMN1 and COMP2 switches are opened.
2) DCD (Data Contact Detection). The MAX14616/MAX14616A verify that the USB cable is fully inserted.
3) Apple charger detection, special charger detection, (including 5V bias on D+/D- (MAX14616A only)) and Dedicated Charging Ports (DCP) detection (Figure 4).
4) Standard Downstream Ports (SDP) and Charging Downstream Ports (CDP) detection.
5) In standard operating mode, AccDet = 0. COMN1 and COMP2 switches are returned to their previous state.

The ChgDetRun bit in the STATUS2 register (0x05) is 1 while the state machine is running. The output of the state machine is indicated by the ChgTyp bits in the STATUS2 register once the detection algorithm has been completed.

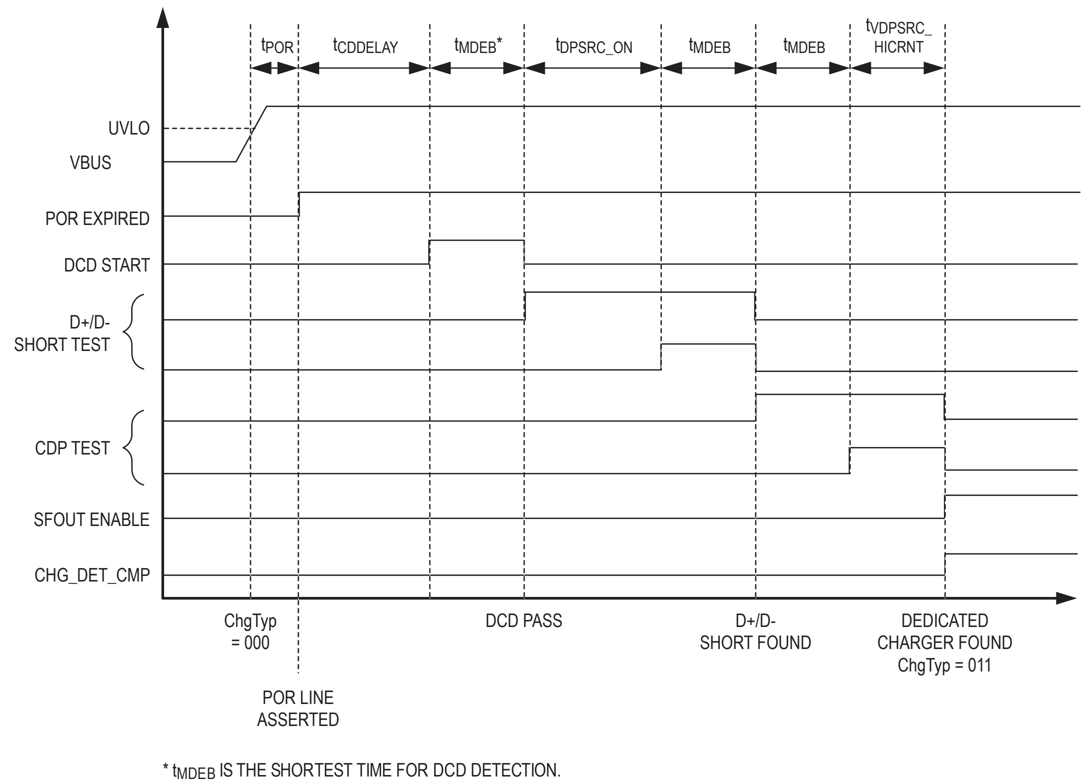


Figure 4. USB Dedicated Charger Detection Timing

BAT Battery Charger

The MAX14616/MAX14616A use voltage, current, and thermal control loops to charge a single Li+ cell and to protect the battery (Figure 5). Set the MBCHOSTEN bit in the CHGCTRL2 register (0x10) to enable the MAX14616 battery charger (Table 1).

Precharge Qualification

The MAX14616/MAX14616A feature precharge qualification for batteries with a cell voltage less than 2.5V (typ). When a battery with a cell voltage less than V_{PRECHG} is connected to the MAX14616/MAX14616A, the device charges the battery with a precharge current (I_{PRECHG}) of 90mA (typ). The prequalification state is complete when $V_{BAT} \geq V_{PRECHG}$.

Set the VCHGR_RC bit in the CHGCTRL2 register (0x10) to disable fast-charge mode and to continue to charge a battery with $V_{BAT} \geq V_{PRECHG}$ with the precharge current.

Soft-Start

The MAX14616/MAX14616A feature a soft-start when entering fast-charge mode to reduce inrush current on the input supply. After the prequalification state is complete ($V_{BAT} \geq V_{PRECHG}$), charging current ramps up in 1.2ms (typ) to the full charging current, I_{BAT}.

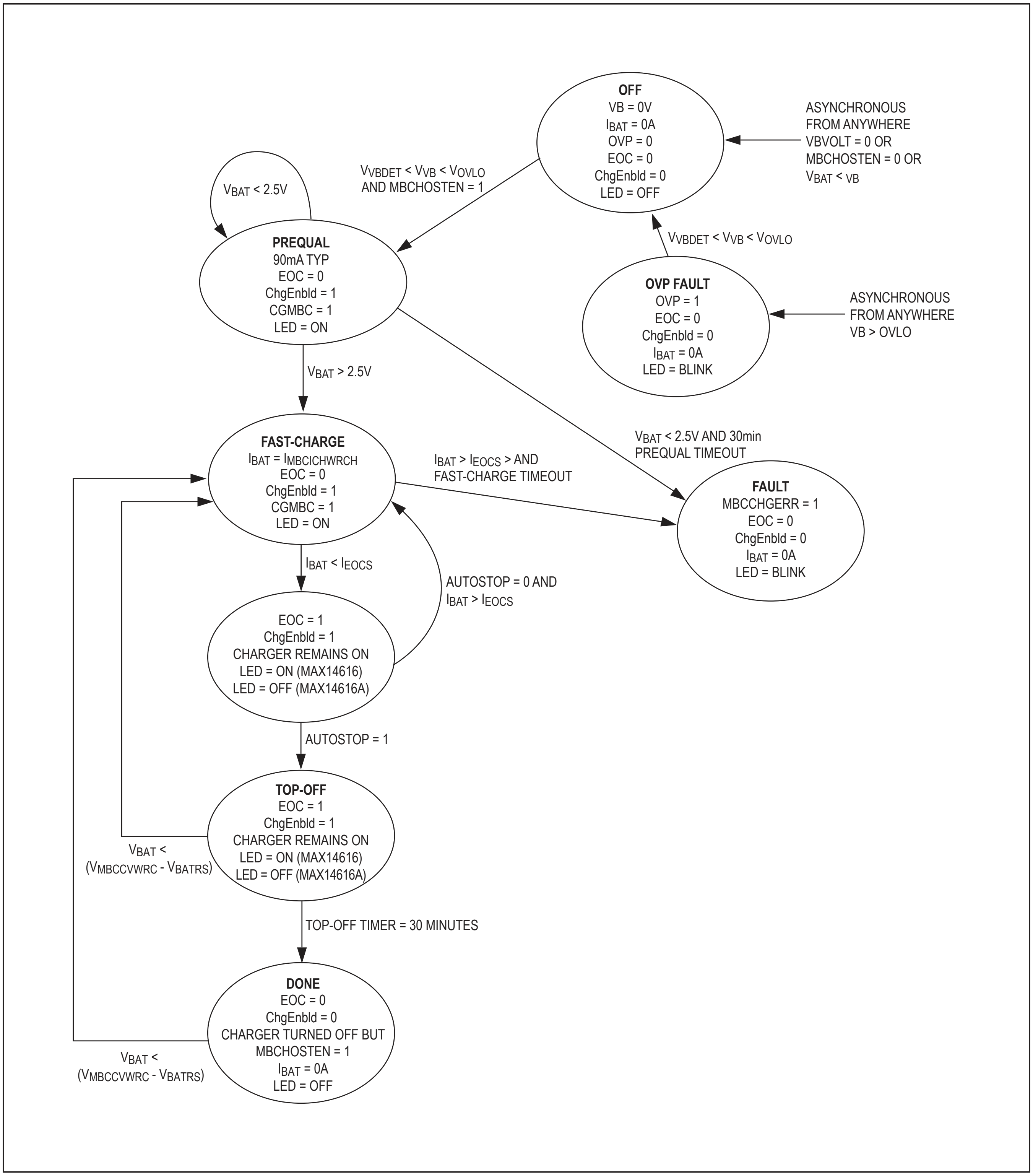


Figure 5. Battery Charger State Machine

Normal Battery Charging

When a battery ($V_{BAT} \geq V_{PRECHG}$) is connected and the VCHGR_RC bit in the CHGCTRL2 register (0x10) is 1, the MAX14616/MAX14616A enter the fast-charge state and charge the battery with a charge current, I_{BAT}. Set the MBCICHWRCL bit and the MBCICHWRCH bits in the CHGCTRL4 register (0x12) to set the fast I_{BAT} current from 90mA to 950mA. Charge current is reduced as the battery voltage approaches the battery regulation threshold, and the MAX14616/MAX14616A charger enters constant voltage regulation mode to maintain the battery at full charge. Set the MBCCVWRC bits in the CHGCTRL3 register (0x11) to set the battery regulation threshold.

The EOCI interrupt in the INT3 register (0x03) is set and $\overline{INT}$ asserts when the charge current falls below the battery end-of-charge threshold, indicating that the battery is fully charged. Set the end-of-charge threshold current by setting the EOCS bits in the CHGCTRL5 register (0x13). Note that the EOCI interrupt is set but $\overline{INT}$ does not assert if the battery charger enable interrupt mask bit (EOCM) in the INTMASK3 register (0x09) is set to 0.

When the battery is fully charged, depends on the AUTOSTOP setting, (AUTOSTOP = 0) the charger does not stop and an I^2C write to MBCHOSTEN is required to turn it off or (AUTOSTOP = 1) charging continues until the 30-minute (typ) top-off timer expires and then charging automatically stops. During the 30-minute top-off time, the MAX14616/MAX14616A continue to trickle charge the battery until the top-off timer runs out.

The MAX14616/MAX14616A continue to monitor the battery voltage at BAT and restarts the fast-charge battery mode if V_{BAT} falls 150mV (typ) below the battery regulation threshold for at least 62ms (typ).

Fast-Charge Timer

Set the TCHW bits in the CHGCTRL1 register (0x0F) to set the maximum time the charger will operate in fast-charge mode. The MAX14616/MAX14616A terminate fast-charge mode when the fast-charge timer has elapsed regardless of the V_{BAT} voltage. Set the TCHW bits to '111' to disable the fast-charge timer.

Thermal Regulation

The MAX14616/MAX14616A feature thermal regulation to limit the die temperature to 105°C (typ) during charging, allowing a higher charge current without risking damage to the device. When the MAX14616/MAX14616A temperature exceeds the thermal regulation limit, internal circuitry reduces the charge current, allowing the die to cool and protecting it from overheating.

Battery Charger Status LED Driver

The MAX14616/MAX14616A have a LED open-drain output that indicates the status of the battery charger (Table 4). After the fast charge, the MAX14616 and the MAX14616A have a different LED off operation. See Figure 5. The LED driver can be manually controlled by the BTLDSet control bits in CONTROL3 register (0x0E).

Battery Presence Detection

The MAX14616/MAX14616A feature battery presence detector. THM is connected to the pulldown resistor on the battery pack and a pullup resistor to SFOUT. The battery presence signal is used to control the LED indicator. The output of battery presence detector (BatDet) can be read in the STATUS3 register (0x06).

If no battery is present (BatDet = 00), the battery charger is disabled (Table 1).

Table 4. LED Output with Battery Charger Status

VBVolt	ChgEnbld	BatDet	MBCCHGERR	OVP	LED	EVENT
0	X	X	X	0	High-Z	No VBUS
1	1	10	0	0	Low	Charging
1	0	10	0	0	High-Z	Charging Done**
1	X	X	1	X	Blink*	Charging Error
1	X	X	X	1	Blink*	OVP
1	X	00	X	X	Blink*	No Battery

X = Don't Care

**Blink rate = 1Hz, 50% duty cycle*

***Either MBCHOSTEN = 0 or (AUTOSTOP = 1 and 30-minute top-off timer expired)*

I²C Serial Interface

Serial Addressing

The MAX14616/MAX14616A operate as a slave devices that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX14616/MAX14616A and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14616/MAX14616A 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition (Figure 1).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 6). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 7). The data on SDA must remain stable while SCL is high.

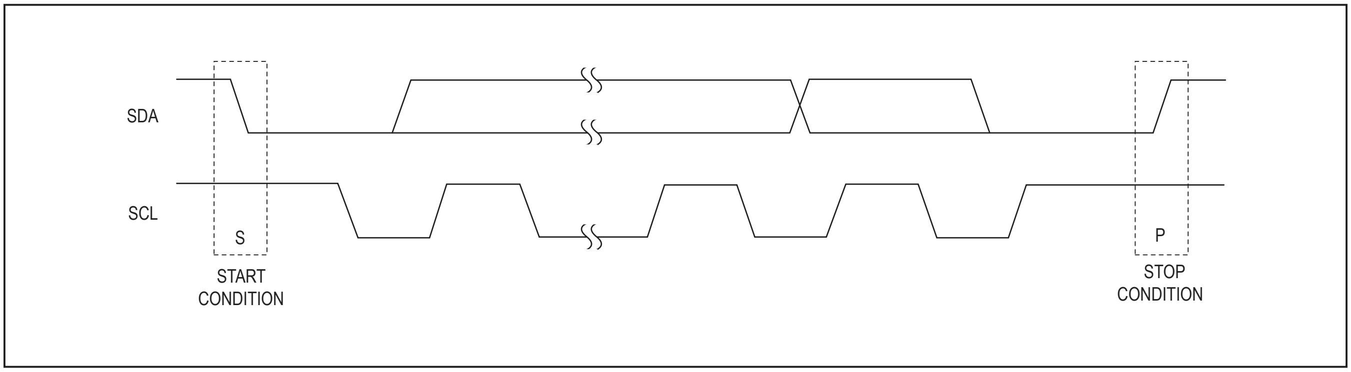


Figure 6. Start and Stop Conditions

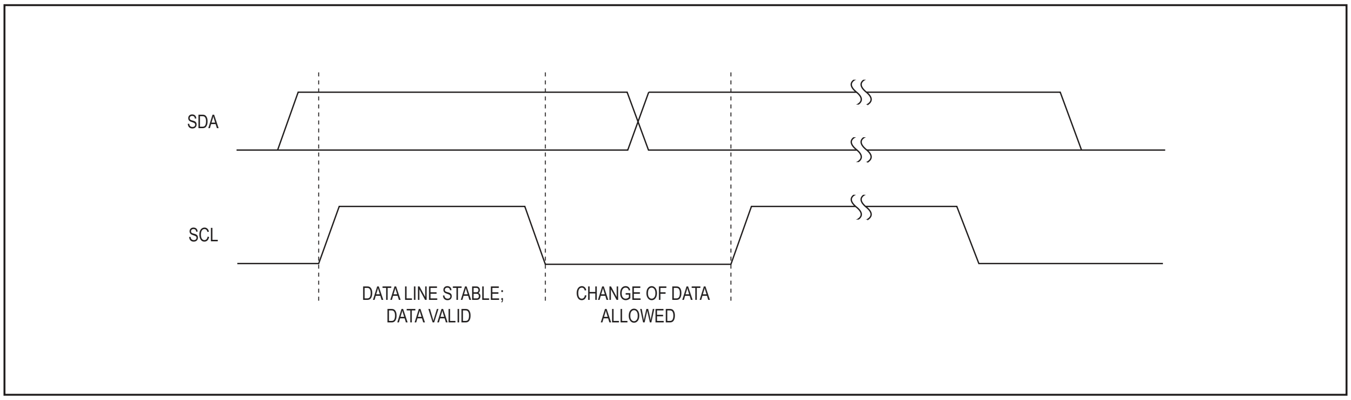


Figure 7. Bit Transfer

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 8), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires nine bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14616/MAX14616A, the master generates the acknowledge bit because the MAX14616/MAX14616A are recipients. When the MAX14616/MAX14616A are transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Address

The MAX14616/MAX14616A have a 7-bit long slave address. The bit following a 7-bit slave address is the $R\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the MAX14616/MAX14616A have 01001011 for read commands and 01001010 for write commands (Figure 9).

Bus Reset

The MAX14616/MAX14616A reset the bus with the I^2C start condition for reads. When the $R\overline{W}$ bit is set to 1, the MAX14616/MAX14616A transmit data to the master, thus the master is reading from the devices.

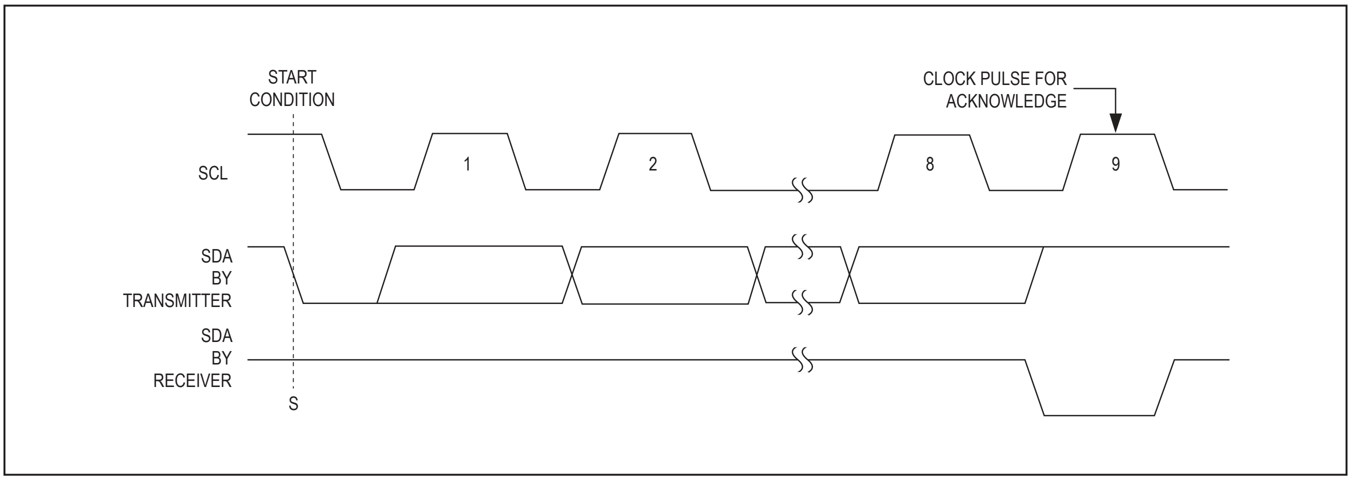


Figure 8. Acknowledge

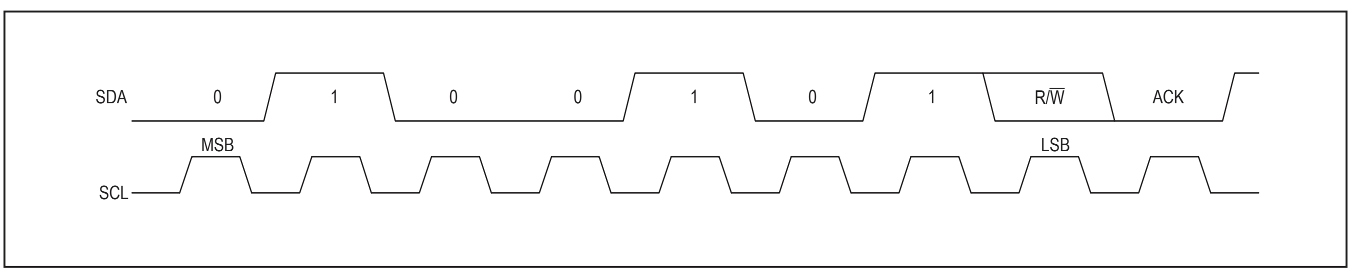


Figure 9. Slave Address

Format for Writing

A write to the MAX14616/MAX14616A comprise the transmission of the slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the MAX14616/MAX14616A are to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the MAX14616/MAX14616A take no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 10). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses auto-increments (Figure 11).

Format for Reading

The MAX14616/MAX14616A are read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 12). The master can now read consecutive bytes from the MAX14616/MAX14616A, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 13). Once the master sounds a NACK, the MAX14616/MAX14616A stop sending valid data.

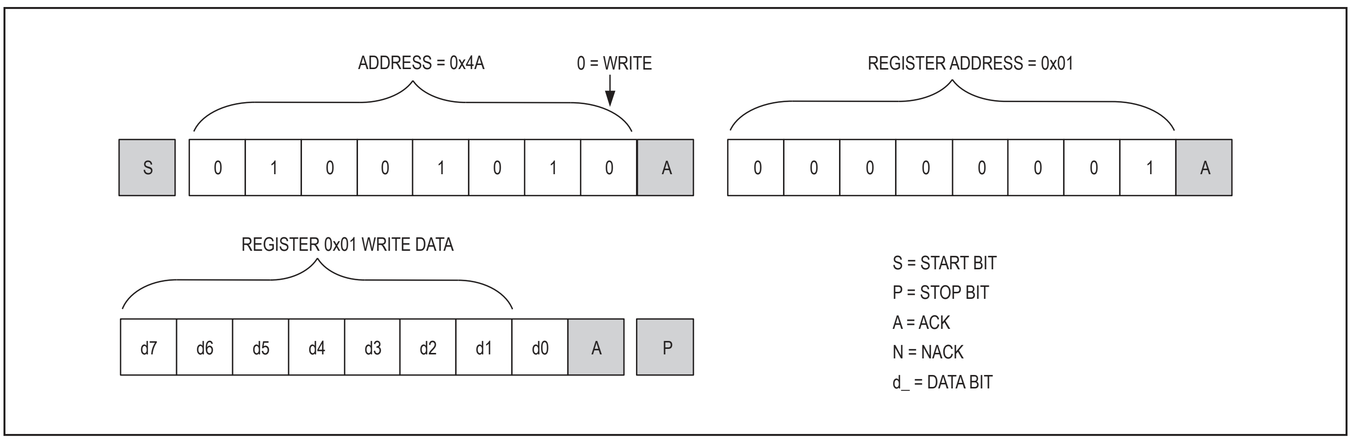


Figure 10. Format for I^2C Write

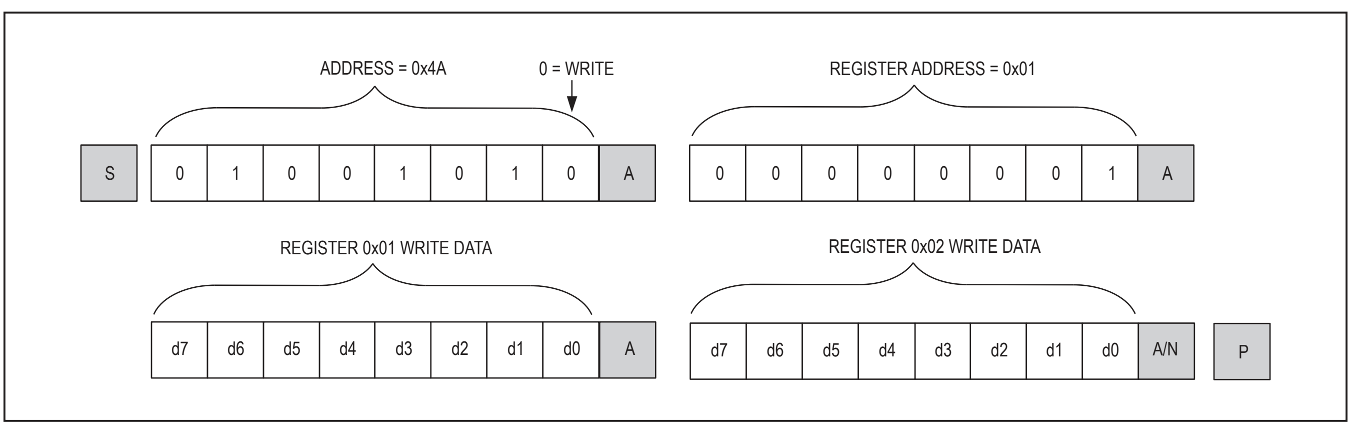


Figure 11. Format for Writing to Multiple Registers

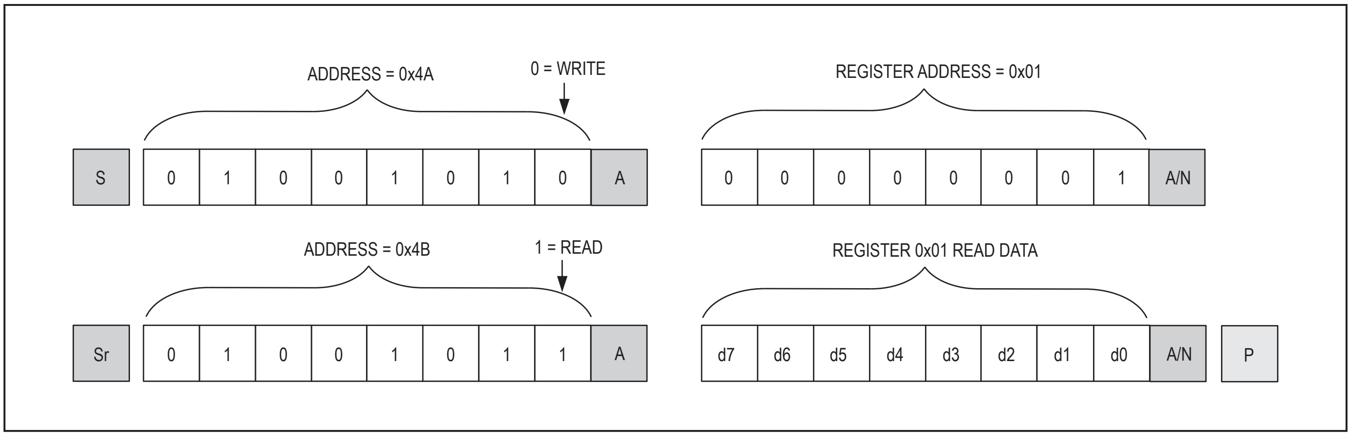


Figure 12. Format for Reads (Repeated Start)

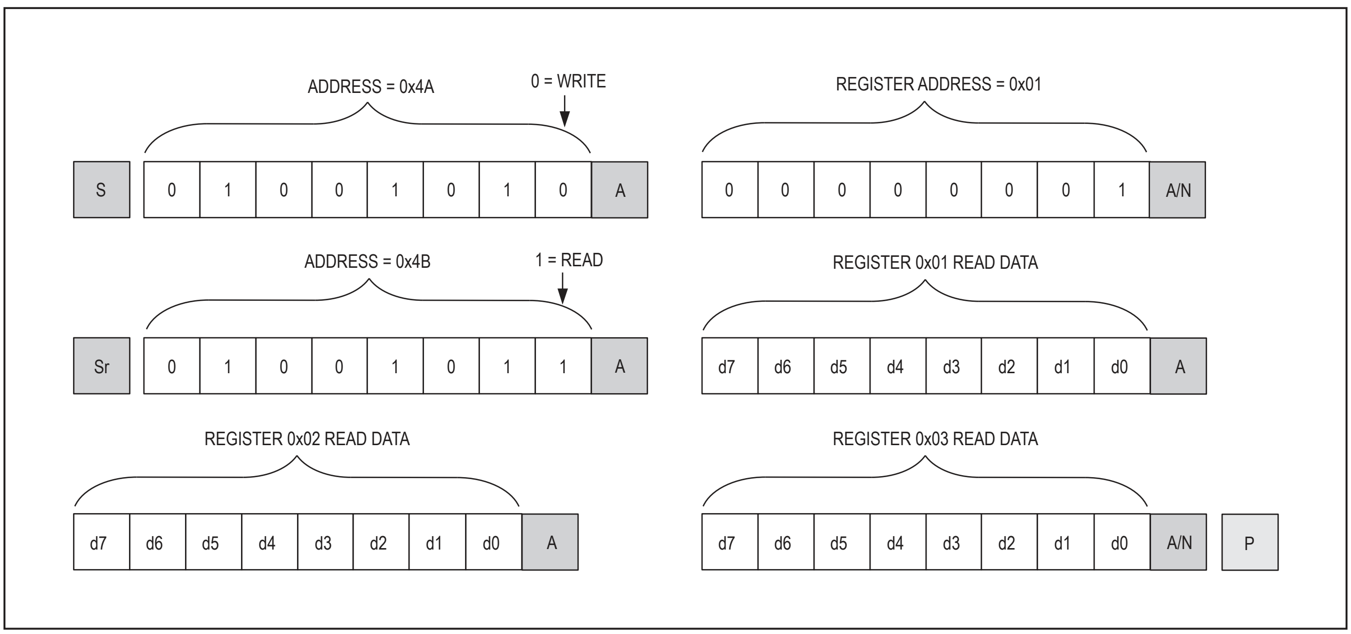


Figure 13. Format for Reading Multiple Registers

Applications Information

Hi-Speed USB

Hi-Speed USB requires careful PCB layout with 45Ω single-ended/90Ω differential controlled-impedance matched traces of equal lengths.

Power-Supply Bypassing

Bypass BAT to GND with a 2.2µF ceramic capacitor. Bypass V_{IO} to GND with a 0.1µF ceramic capacitor. Bypass VB to GND with a 1µF ceramic capacitor. Place all bypass capacitors as close as possible to the supply pins.

Choosing I²C Pullup Resistors

I^2C requires pullup resistors to provide a logic-high level to data and clock lines. There are tradeoffs between power dissipation and speed, and a compromise must be made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I^2C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for a clock frequency up to 400kHz (See the I^2C specifications for details).

In order to meet the rise time requirement, choose pullup resistors such that the rise time $t_R = 0.85 \times R_{PULLUP} \times C_{BUS} < 300ns$. If the transition time becomes too slow, the setup and hold times may not be met and waveforms may not be recognized.

PCB Layout

The MAX14616/MAX14616A dissipate a large amount of heat during battery charging from the internal battery charger. Proper PCB layout is critical to remove the heat from the die. As most of the heat is dissipated from the VB and BAT balls, connect these balls to large copper planes on the PCB. At least 2.5mm x 2.5mm of copper must be used for each VB and BAT (Figure 14).

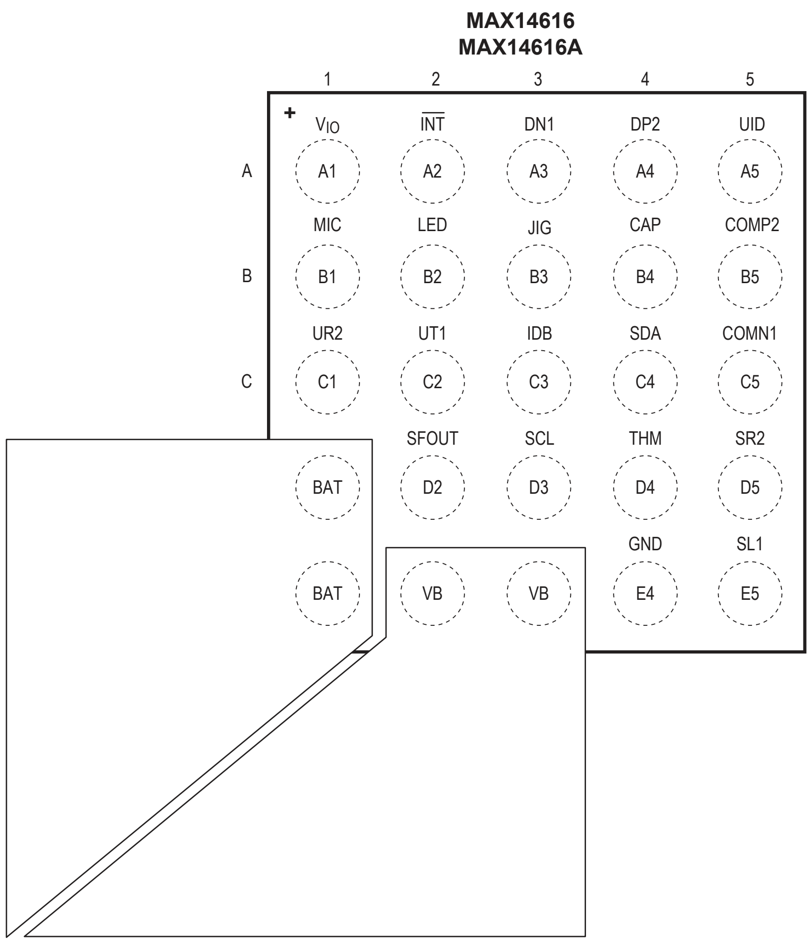


Figure 14. Recommended PCB Layout for BAT and VB

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. COMN1, COMP2, and UID are further protected against ESD up to ±15kV (HBM), ±10kV (Air Gap Discharge method described in IEC 61000-4-2) and ±7kV (Contact Discharge Method described in IEC 61000-4-2) without damage. The VB input withstands up to ±15kV (HBM) if bypassed with a 1µF ceramic capacitor close to the pin.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14616 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 15 shows the Human Body Model, and Figure 16 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 17 shows the IEC 61000-4-2 model, and Figure 18 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

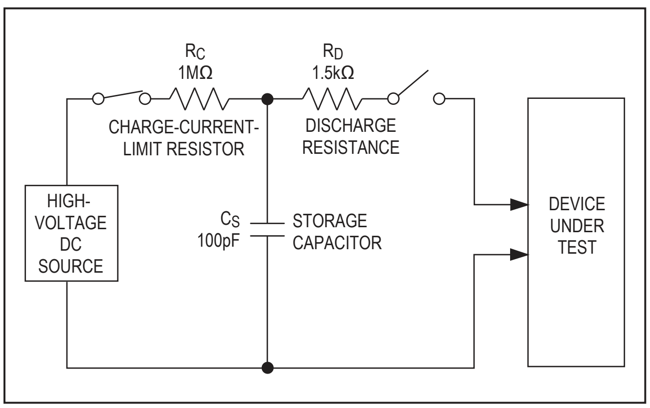


Figure 15. Human Body ESD Test Model

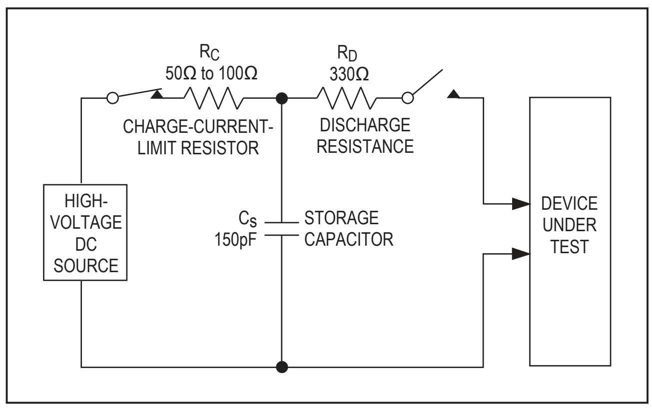


Figure 17. IEC 61000-4-2 ESD Test Model

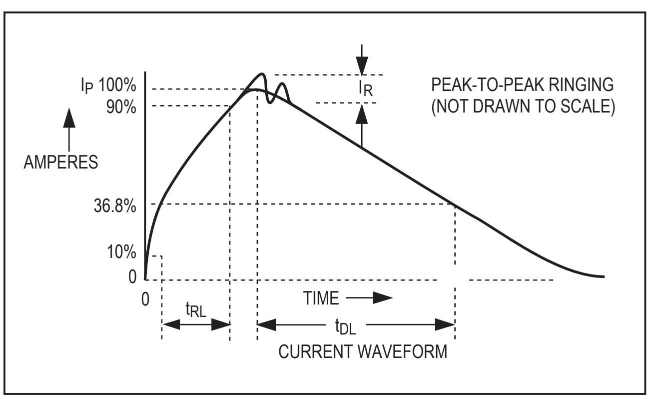


Figure 16. Human Body Current Waveform

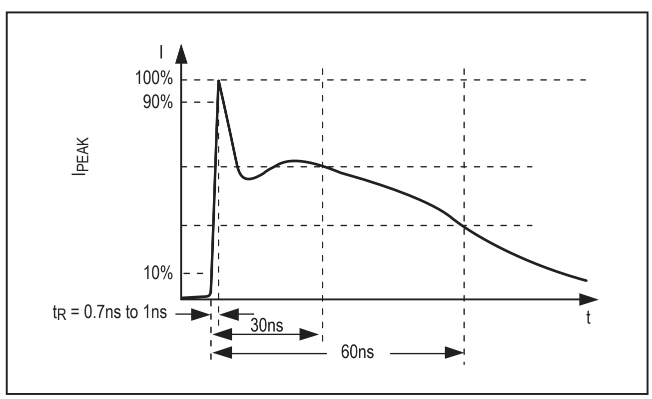


Figure 18. IEC 61000-4-2 ESD Generator Current Waveform

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14616EWA+T	-40°C to +85°C	25 WLP
MAX14616AEWA+T	-40°C to +85°C	25 WLP

+Denotes lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
25 WLP	W252B2+1	**21-0180**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—
1	6/12	Added the MAX14616A to the data sheet	1, 17, 19, 20, 24, 28, 29, 30, 31, 33, 34, 36, 37, 38, 39, 40, 41, 42, 43, 45, 47

