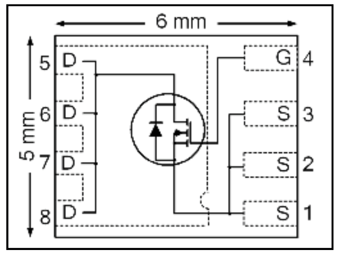
AUTOMOTIVE GRADE

AUIRFN8405

HEXFET® POWER MOSFET

V_{DSS}	**40V**
$R_{DS(on)}$ typ.	**1.6mΩ**
max	**2.0mΩ**
I_D (Silicon Limited)	**187A①**
I_D (Package Limited)	**95A**



PQFN 5X6 mm

G	D	S
Gate	Drain	Source

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this product an extremely efficient and reliable device for use in Automotive and wide variety of other applications.

Applications

- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Converter

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFN8405	PQFN 5mm x 6mm	Tape and Reel	4000	AUIRFN8405TR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	187①	A
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	132①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	95	
I_{DM}	Pulsed Drain Current ②	670⑩	
P_D @T_A = 25°C	Power Dissipation	3.3	W
P_D @$T_{C(Bottom)}$ = 25°C	Power Dissipation	136	
	Linear Derating Factor	0.022	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

Avalanche Characteristics

$E_{AS(Thermally\ Limited)}$	Single Pulse Avalanche Energy ③	190	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy	365	
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy②		mJ

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at http://www.irf.com/

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑨	——	1.1	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑨	——	30	
$R_{\theta JA}$	Junction-to-Ambient ⑧	——	44	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑧	——	28	

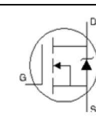
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	37	——	mV/°C	Reference to 25°C, I_D = 1.0mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	1.6	2.0	mΩ	V_{GS} = 10V, I_D = 50A
$V_{GS(th)}$	Gate Threshold Voltage	2.2	——	3.9	V	V_{DS} = V_{GS}, I_D = 100μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Internal Gate Resistance	——	2.4	——	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	145	——	——	S	V_{DS} = 10V, I_D = 50A
Q_g	Total Gate Charge	——	78	117	nC	I_D = 50A
Q_{gs}	Gate-to-Source Charge	——	21	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	25	——		V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	53	——		
$t_{d(on)}$	Turn-On Delay Time	——	9.5	——	ns	V_{DD} = 20V
t_r	Rise Time	——	30	——		I_D = 50A
$t_{d(off)}$	Turn-Off Delay Time	——	58	——		R_G = 2.7Ω
t_f	Fall Time	——	33	——		V_{GS} = 10V ⑤
C_{iss}	Input Capacitance	——	5142	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	758	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	501	——		f = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	900	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑦
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	1094	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	187①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	670⑩	A	
V_{SD}	Diode Forward Voltage	——	0.9	1.3	V	T_J = 25°C, I_S = 50A, V_{GS} = 0V ⑤
dv/dt	Peak Diode Recovery ④	——	5.2	——	V/ns	T_J = 175°C, I_S= 50A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	——	27	——	ns	T_J = 25°C; V_R = 34V,
		——	28	——		T_J = 125°C; I_F = 50A
Q_{rr}	Reverse Recovery Charge	——	16	——	nC	T_J = 25°C; di/dt = 100A/μs⑤
		——	18	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	0.92	——	A	T_J = 25°C

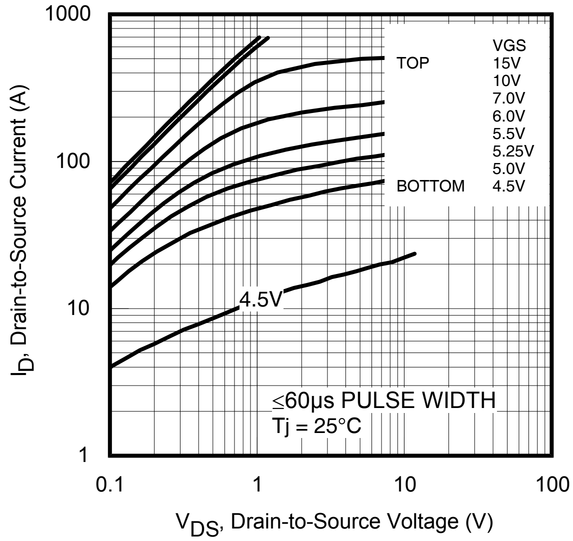


Fig. 1 Typical Output Characteristics

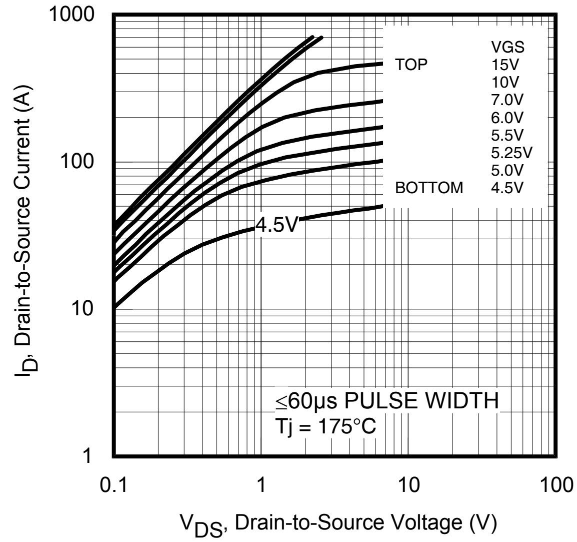


Fig. 2 Typical Output Characteristics

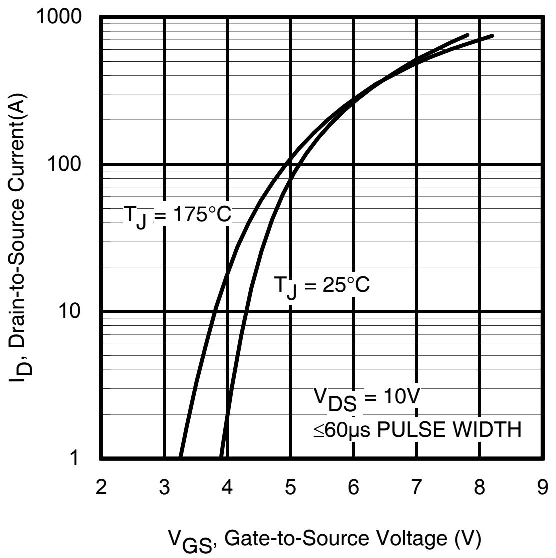


Fig. 3 Typical Transfer Characteristics

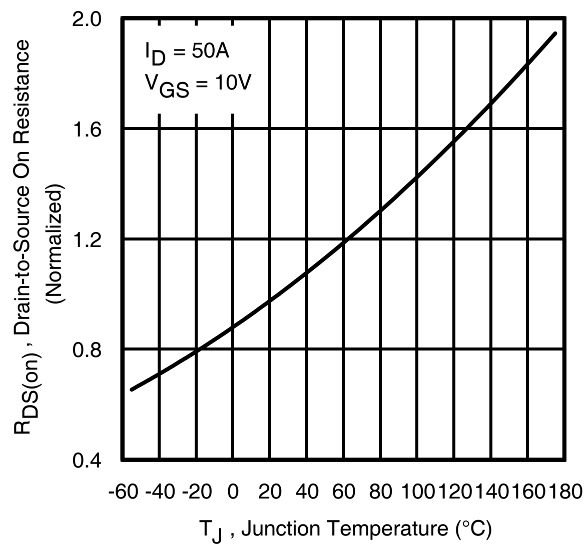


Fig. 4 Normalized On-Resistance vs. Temperature

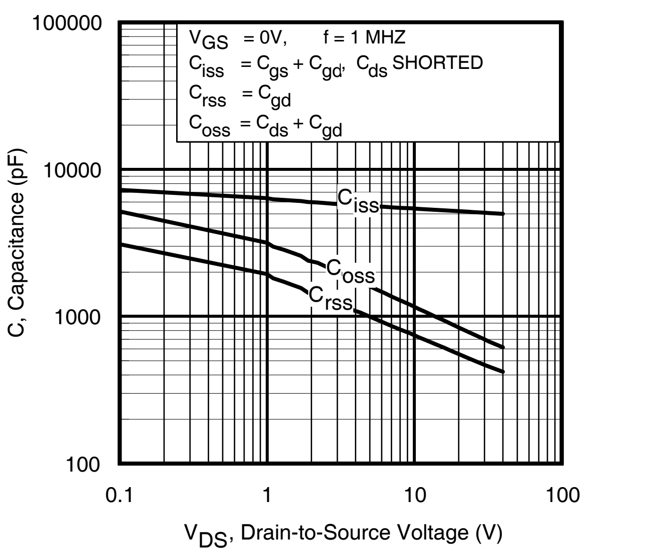


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

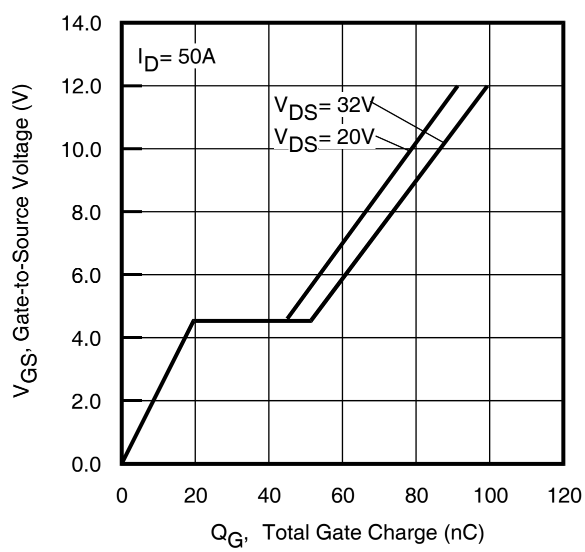


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

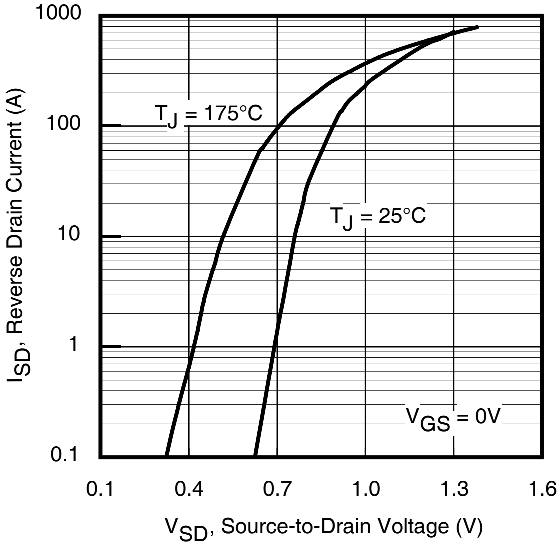


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

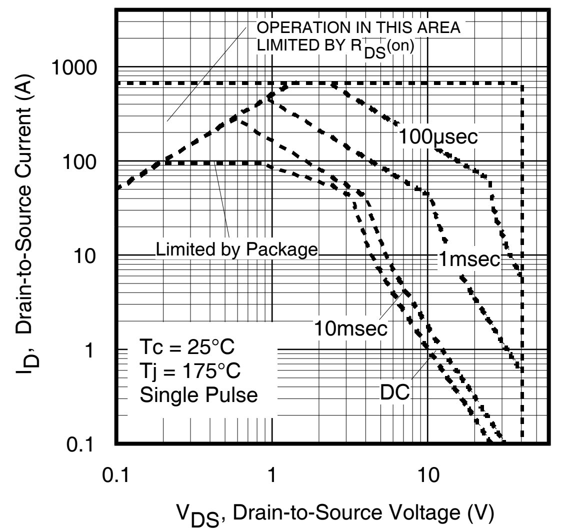


Fig 8. Maximum Safe Operating Area

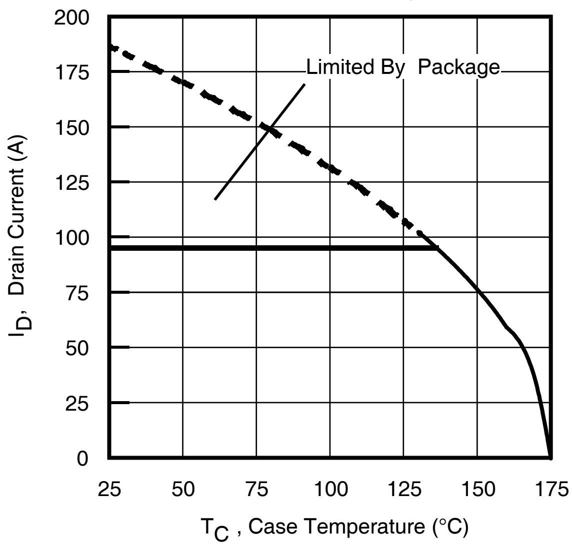


Fig 9. Maximum Drain Current vs. Case Temperature

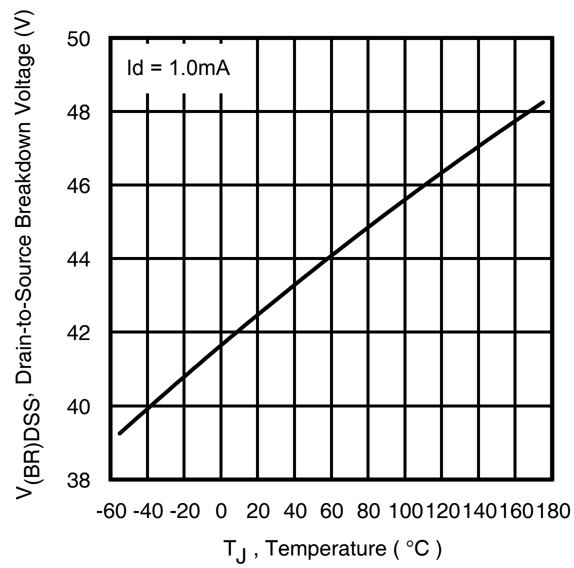


Fig 10. Drain-to-Source Breakdown Voltage

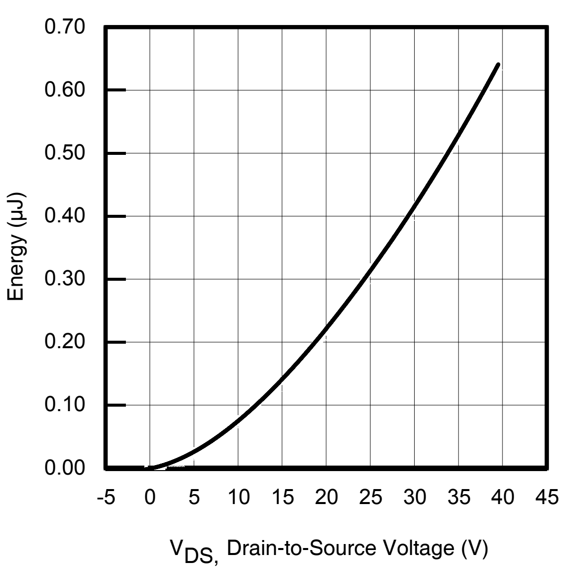


Fig 11. Typical Coss Stored Energy

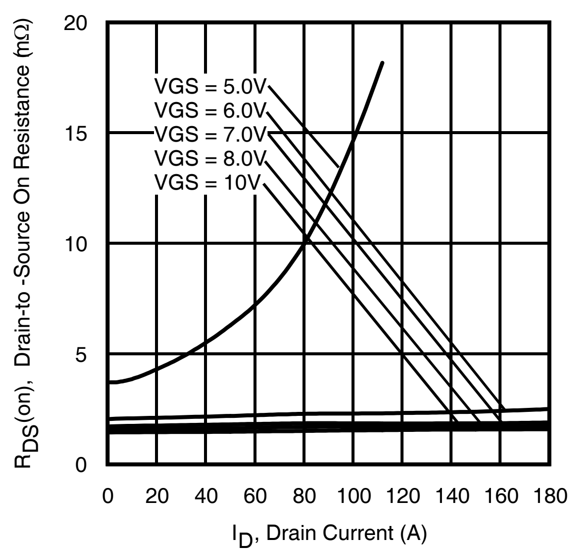


Fig 12. Typical On-Resistance vs. Drain Current

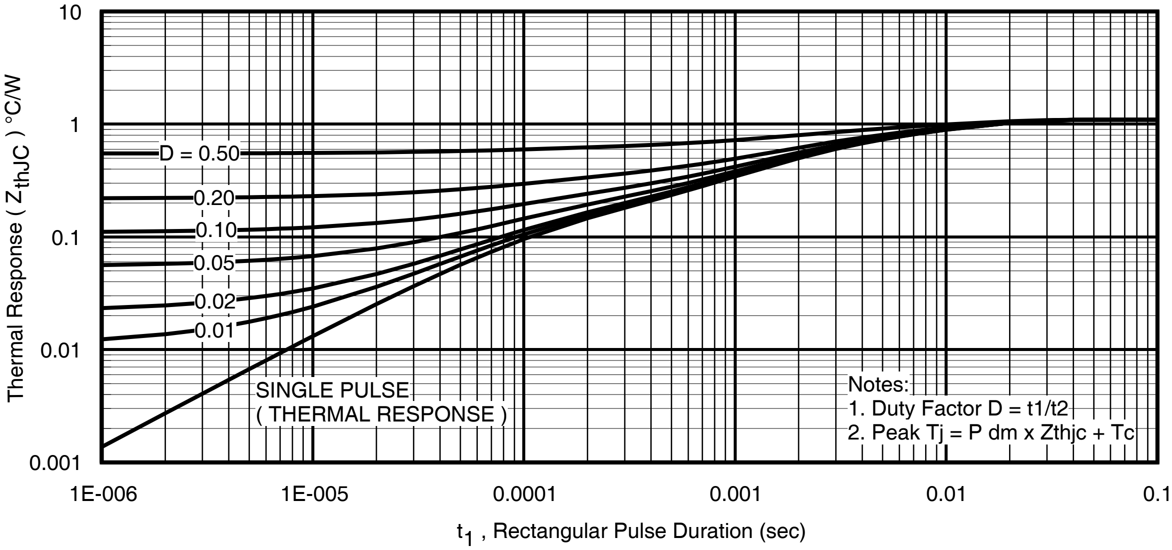


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

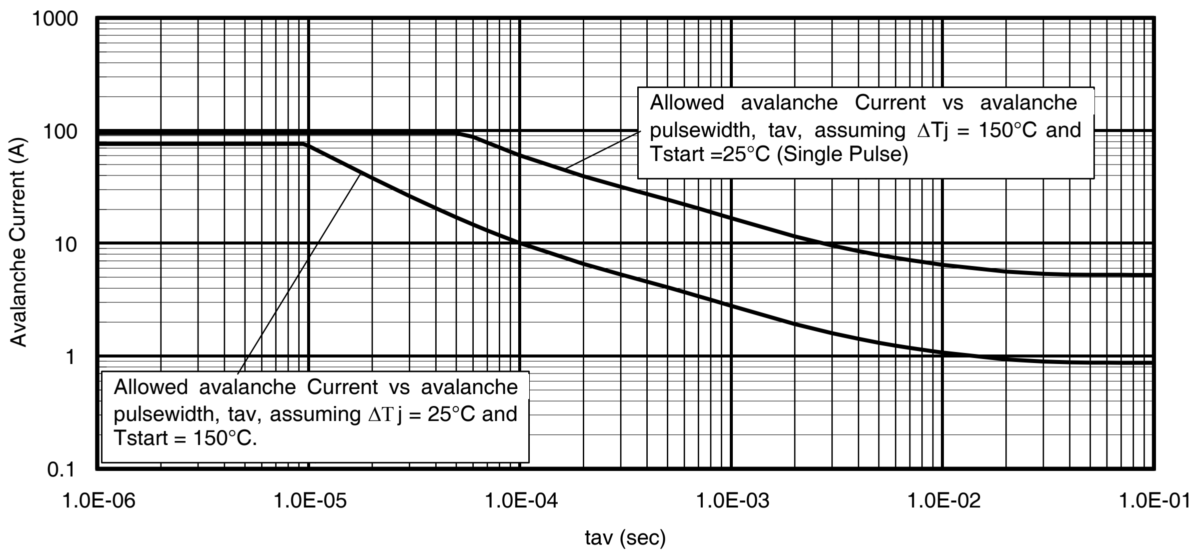


Fig 14. Typical Avalanche Current vs. Pulse Width

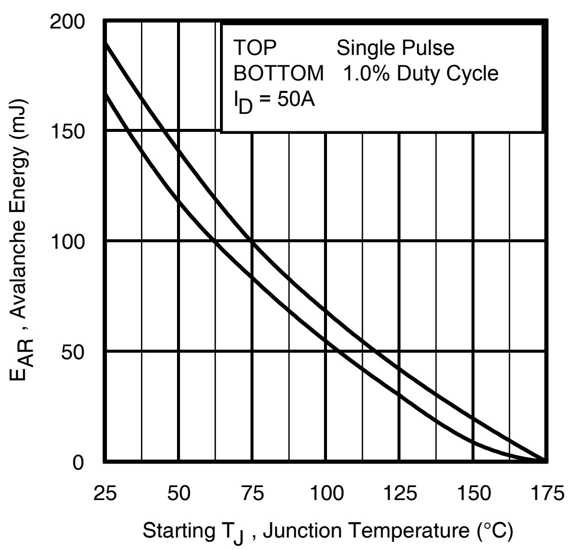


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

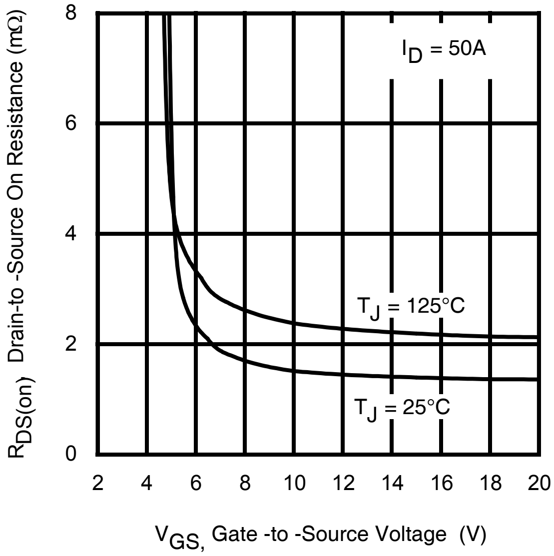


Fig 16. Typical On-Resistance vs. Gate Voltage

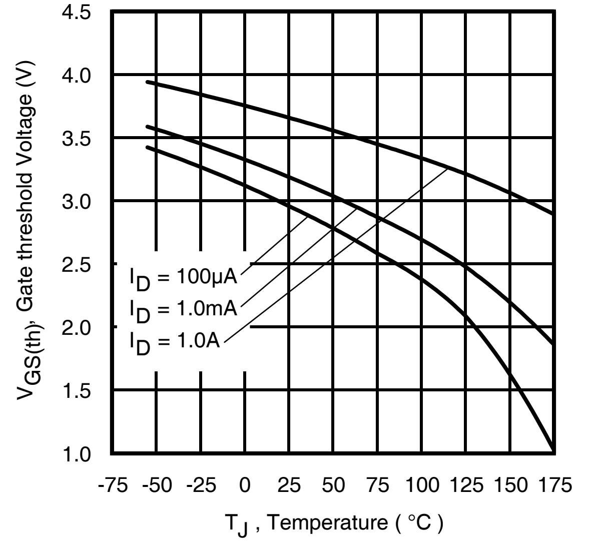


Fig 17. Threshold Voltage vs. Temperature

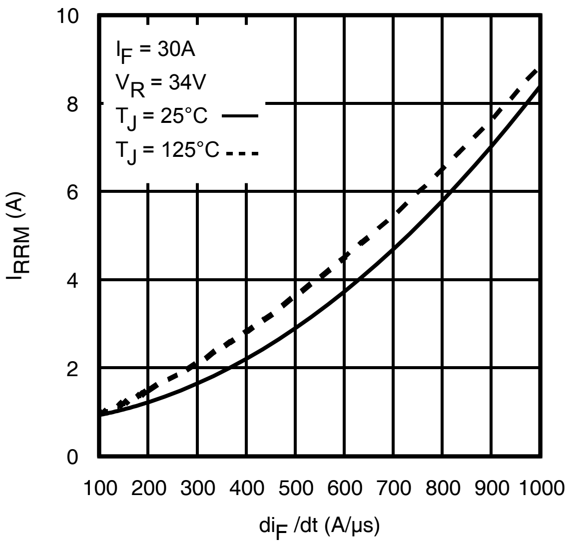


Fig. 18 - Typical Recovery Current vs. dif/dt

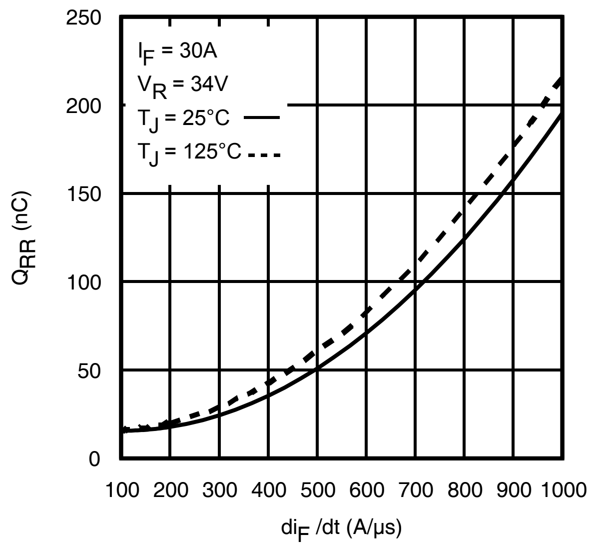


Fig. 19 - Typical Stored Charge vs. dif/dt

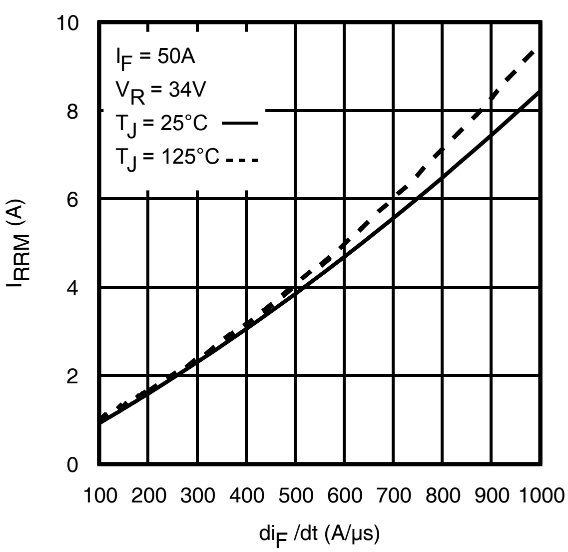


Fig. 20 - Typical Recovery Current vs. dif/dt

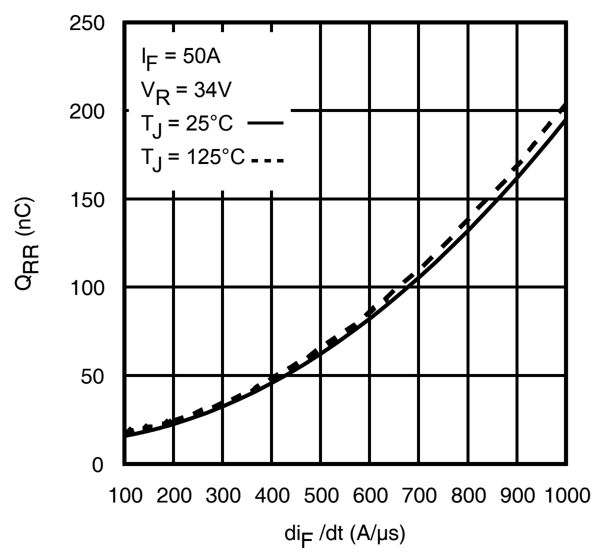


Fig. 21 - Typical Stored Charge vs. dif/dt

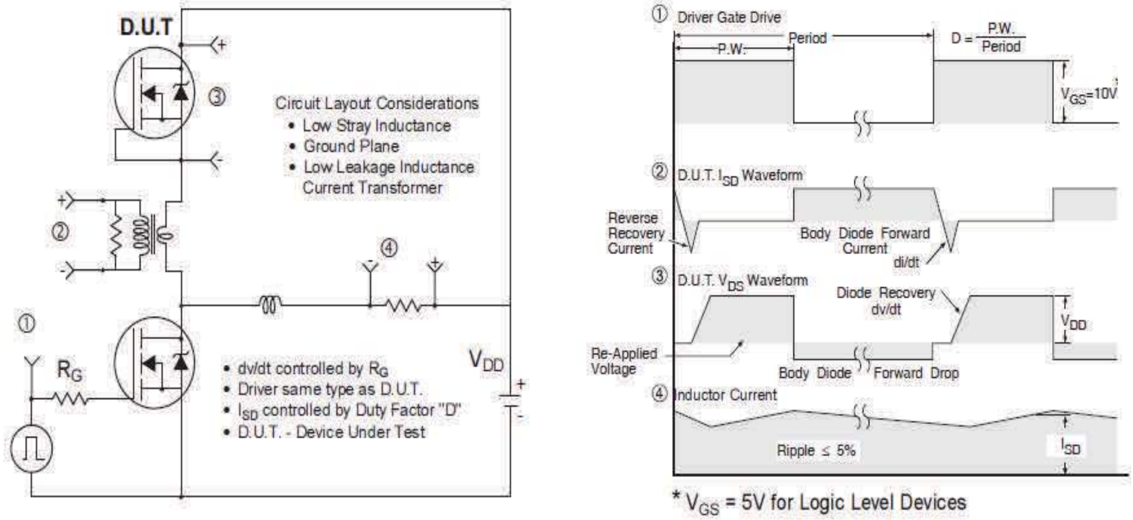


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

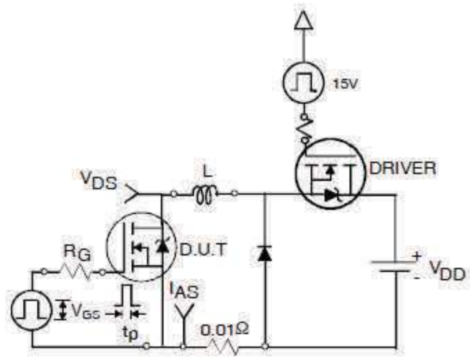


Fig 22a. Unclamped Inductive Test Circuit

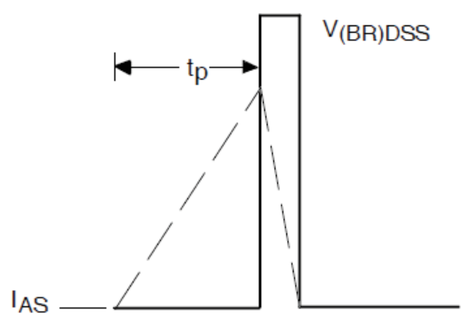


Fig 22b. Unclamped Inductive Waveforms

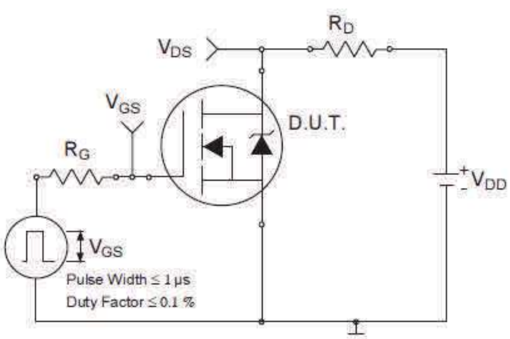


Fig 23a. Switching Time Test Circuit

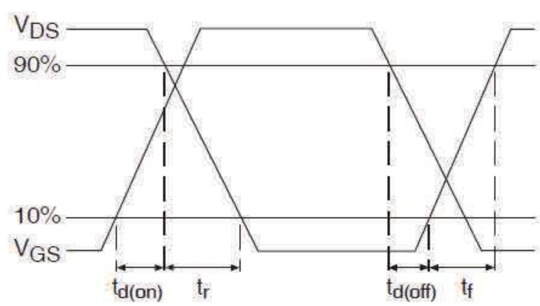


Fig 23b. Switching Time Waveforms

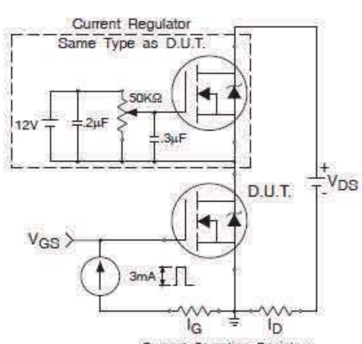


Fig 24a. Gate Charge Test Circuit

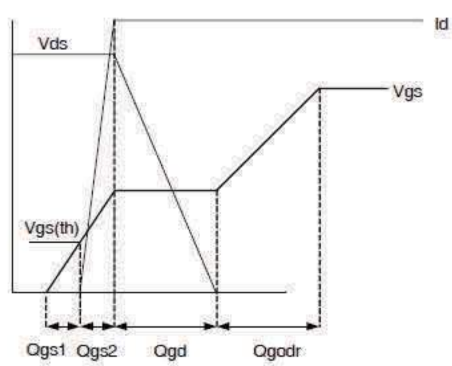
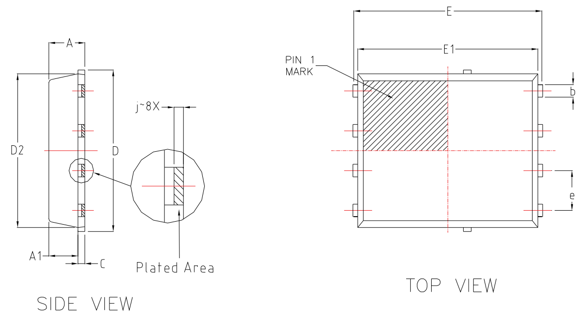
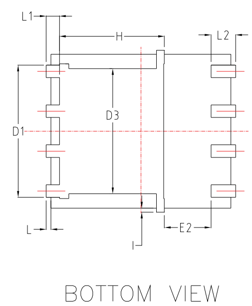


Fig 24b. Gate Charge Waveform

PQFN 5x6 Outline "E" Package Details

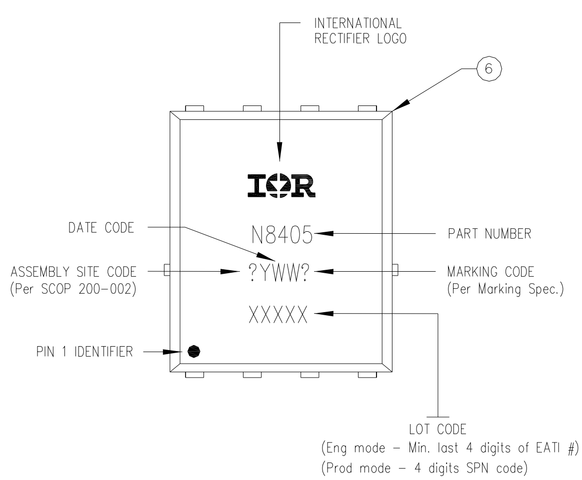


D I M	MM		
	MIN	NOM	MAX
A	0.90	1.10	1.17
A1	0.824	0.897	0.97
b	0.33	0.41	0.50
c	0.150	0.20	0.250
D	4.80	4.98	5.15
D1	3.91	4.22	4.36
D2	4.80	4.90	5.00
D3	3.85	4.00	4.15
E	5.90	6.05	6.15
E1	5.65	5.76	5.85
E2	1.10	/	/
e	1.27 BSC		
L	0.05	0.15	0.25
L1	0.38	0.425	0.50
L2	0.51	0.785	0.86
H	3.25	3.35	3.58
I	0	/	0.18
j	0.1015 BSC		



For footprint and stencil design recommendations, please refer to application note AN-1136 at
http://www.irf.com/technical-info/appnotes/an-1136.pdf
For visual inspection recommendations, please refer to application note AN-1154 at
http://www.irf.com/technical-info/appnotes/an-1154.pdf

PQFN 5x6 Outline "E" Part Marking

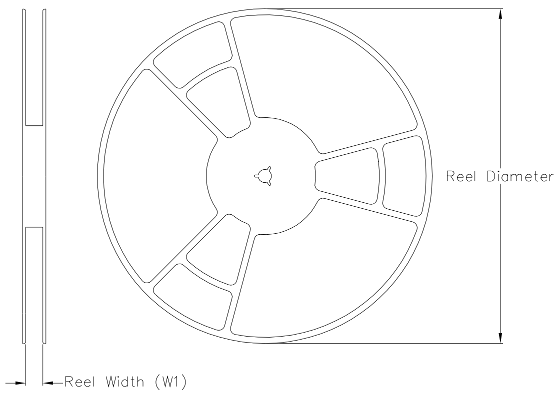


TOP MARKING (LASER)

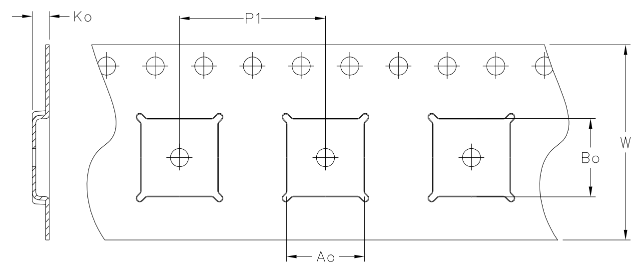
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

PQFN 5x6 Outline "E" Tape and Reel

REEL DIMENSIONS

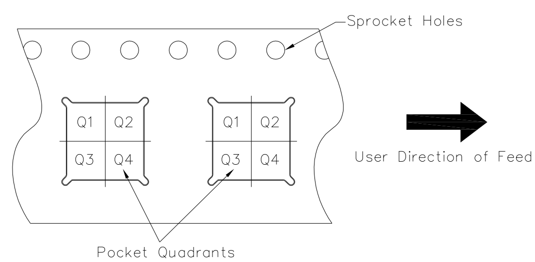


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		PQFN 5mm x 6mm	MSL1
ESD	Human Body Model	Class H1C (+/- 2000V)††	
		AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V)††	
		AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Highest passing voltage.

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 95A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by TJmax, starting TJ = 25°C, L = 0.152mH, R_G = 50Ω, I_{AS} = 50A, V_{GS} =10V.

④ $I_{SD} \le 50A$, di/dt ≤ 961A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175°C$.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 80%VDSS.

⑦ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while VDS is rising from 0 to 80% VDSS.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑨ R_θ is measured at TJ approximately 90°C.

⑩ Pulse drain current is limited at 380A by source bonding technology.

Revision History

Date	Comments
9/24/2018	• Updated datasheet with corporate template • Corrected typo on Gate-to-Source Leakage from “Ω” to “nA” on page 2

Published by
Infineon Technologies AG
81726 München, Germany

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