

IS32SE5120

24-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

July 2023

GENERAL DESCRIPTION

IS32SE5120 is an ultra-low-power, 24-channel capacitive touch controller. The controller allows sleep mode (under 10uA) and uses auto-detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration feature for the environment is to prevent false triggers.

A host MCU is required to communicate with IS32SE5120. An on-chip I²C slave controller with 400kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. The trigger event can be configured by setting the interrupt register. IS32SE5120 can support proximity sensing.

IS32SE5120 is available in the WQFN-32 package. It operates from 2.3V to 5.5V over the temperature range from -40°C to +125°C.

FEATURES

- 24-channel capacitive touch controller with

TYPICAL APPLICATION CIRCUIT (WQFN-32)

readable key value

- Touch-related threshold settings for individual key
- Optional multiple-key function
- GPIO toggle/invert function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Shield output shared with touch key channels
- Buzzer/Melody Generator shared with touch key channels
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C ~ +125°C
- Wettable flank WQFN-32
- ROHS & Halogen-Free compliant package
- AEC-Q100 qualification
- TSCA compliance

APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

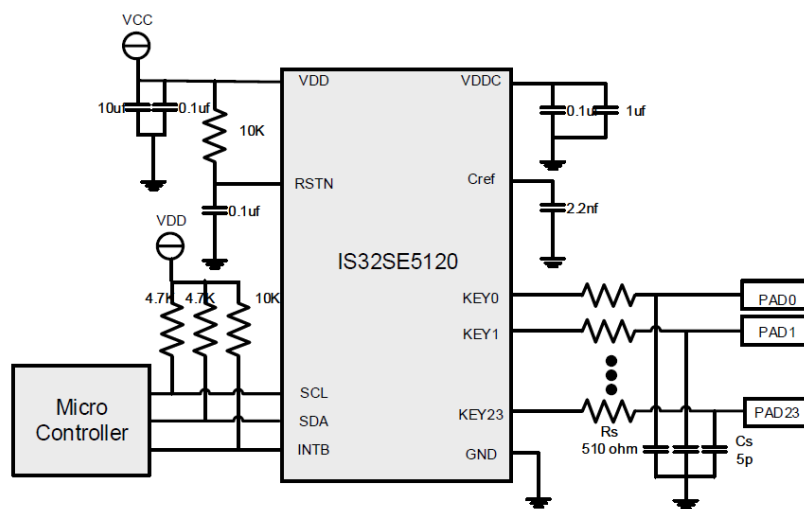


Figure 1 Typical Application Circuit (WQFN-32)

Note 1: The IC should be placed far away from the noise source to prevent EMS.

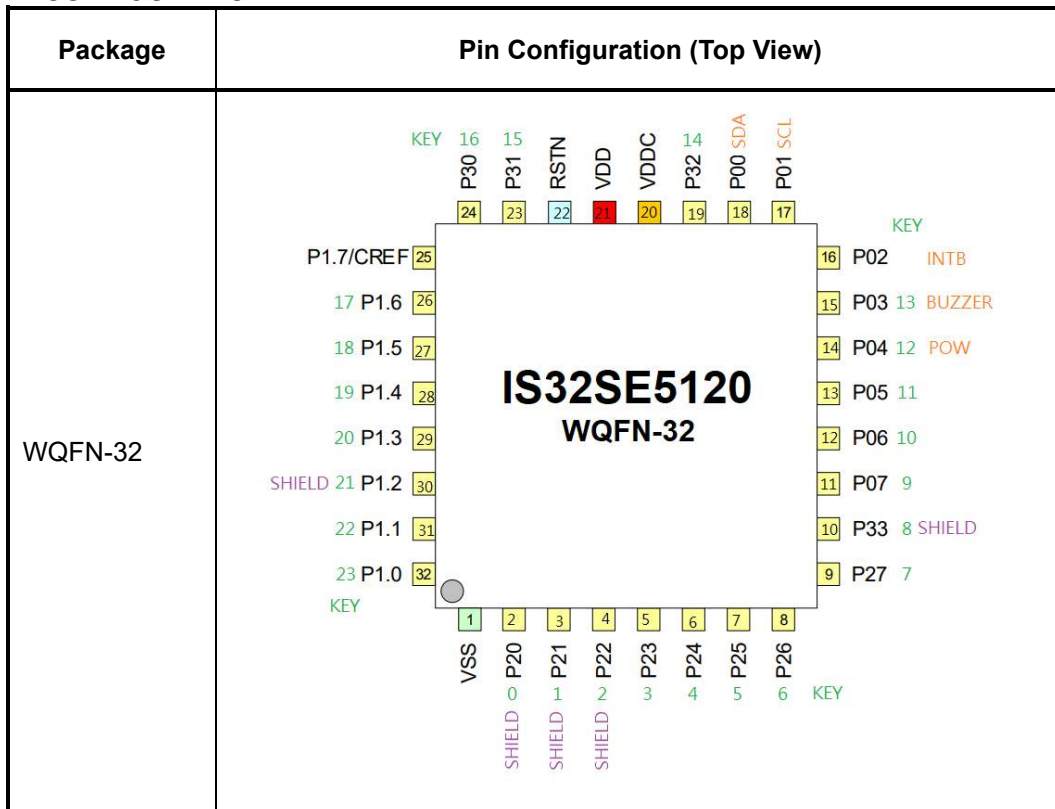
Note 2: The R_S and C_S should be placed as close to IC as possible to reduce EMI.

Note 3: The capacitors connected to VDD and VDDC should be as close to the chip as possible to reduce EMI.

Note 4: The capacitor 1uF connected to VDDC might need to be removed for quick VDD rising time application.

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PIN CONFIGURATION



PIN DESCRIPTION

No.	Pin	Description
1	VSS	Ground
2 - 4	KEY0 – KEY2/SHIELD	Multiple function pin. Can be configured to Input sense channels 0 – 2, or Shield output.
5 - 9	KEY3 – KEY7	Input sense channels 3 – 7
10	KEY8/SHIELD	Multiple function pin. Can be configured to Input sense channel 8, or Shield output.
11 - 13	KEY9 – KEY11	Input sense channels 9 – 11
14	KEY12/POW	Multiple function key. Can be configured to input sense channel 12, or Melody power control.
15	KEY13/Buzzer	Multiple function key. Can be configured to input sense channel 13, or Buzzer output.
16	INTB	Interrupt output (active low)
17	SCL	I2C serial clock
18	SDA	I2C serial data
19	KEY14	Input sense channel 14
20	VDDC	Internal 1.5V power supply. Typical decoupling capacitors of 0.1µF and 1µF should be added between VDDC and GND.
21	VDD	Power supply

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22	RSTN	Reset signal and Low Active
23 - 24	KEY15 – KEY16	Input sense channels 15 - 16
25	Cref	External reference Capacitor for touch sense
26 - 29	KEY17 – KEY20	Input sense channels 17 - 20
30	KEY21/SHIELD	Multiple function pin. Can be configured to Input sense channel 21, or Shield output.
31 - 32	KEY22 – KEY23	Input sense channels 22 - 23



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ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
IS32SE5120-QWLA3-TR	Wettable flank WQFN-32, Lead-free	2500/Reel

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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ $V_{DD}+0.3V$
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range T_A	-40°C ~ +125°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC 51-2A), $\theta_{JA}(WQFN-32)$	37.6°C/W
ESD (HBM)	±2kV
ESD (CDM)	±750V

Note 5: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{DD} = 2.3V \sim 5.5V$, unless otherwise noted. Typical values are $T_A = 25^\circ\text{C}$, $V_{DD} = 3.6V$.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Power Supply Current						
IDD Normal	Total IDD through VDD at 16MHz Peripherals off	-	3.5	-	mA	
IDD Normal	Total IDD through VDD at 1MHz Peripherals off	-	1.0	-	mA	
IDD versus Frequency	IDD Core Current versus Frequency	-	150	-	µA/ MHz	
IDD, Stop	IDD, stop mode	-	500	-	µA	Main regulator on
IDD, Sleep	IDD, sleep mode, 25°C	-	1.5	5	µA	Main regulator off
	IDD, sleep mode, 85°C	-	4	10	µA	Main regulator off
	IDD, sleep mode, 125°C	-	15	40	µA	Main regulator off
GPIO DC Characteristics						
VOH,4.5V	Output High Voltage 1 mA	-	-0.2	-0.5	V	Reference to VDD
VOL,4.5V	Output Low Voltage 8 mA	-	0.3	0.5	V	Reference to VSS
VOH,3.0V	Output High Voltage 1 mA	-	-0.3	-0.6	V	Reference to VDD
VOL,3.0V	Output Low Voltage 8 mA	-	0.3	0.6	V	Reference to VSS
I _{IOT}	Total IO Sink and Source Current	-80	-	80	mA	
VIH	Input High Voltage	$\frac{3}{4}V_D$	-	-	V	
VIL	Input Low Voltage	-	-	$\frac{1}{4}V_D$	V	
VIHYS	Input Hysteresis	-	1	-	-	
RPU	Equivalent Pull-Up resistance	-	25K	-	Ohm	
RPU,RSTN	RSTN Pull-Up resistance	-	5K	-	Ohm	
RPD	Equivalent Pull-Down Resistance	-	25K	-	Ohm	
REQAN1	Equivalent ANIO Switch Resistance @3.3V	-	110	-	Ohm	ANIO1 Switch
	Equivalent ANIO Switch Resistance @5V	-	100	-	Ohm	ANIO1 Switch

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SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
REQAN2	Equivalent ANIO Switch Resistance @3.3V	-	450	-	Ohm	ANIO2 Switch
	Equivalent ANIO Switch Resistance @5V	-	350	-	Ohm	ANIO2 Switch

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 6)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f _{SCL}	Serial-Clock frequency				400	kHz
t _{BUF}	Bus free time between a STOP and a START condition		1.3			μs
t _{HD, STA}	Hold time (repeated) START condition		0.6			μs
t _{SU, STA}	Repeated START condition setup time		0.6			μs
t _{SU, STO}	STOP condition setup time		0.6			μs
t _{HD, DAT}	Data hold time				0.9	μs
t _{SU, DAT}	Data setup time		100			ns
t _{LOW}	SCL clock low period		1.3			μs
t _{HIGH}	SCL clock high period		0.7			μs
t _R	Rise time of both SDA and SCL signals.	(Note 7)		20+0.1C _b	300	ns
t _F	Fall time of both SDA and SCL signals.	(Note 7)		20+0.1C _b	300	ns

Note 6: Guaranteed by design.

Note 7: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 × V_{DD} and 0.7 × V_{DD}.

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FUNCTION BLOCK DIAGRAM

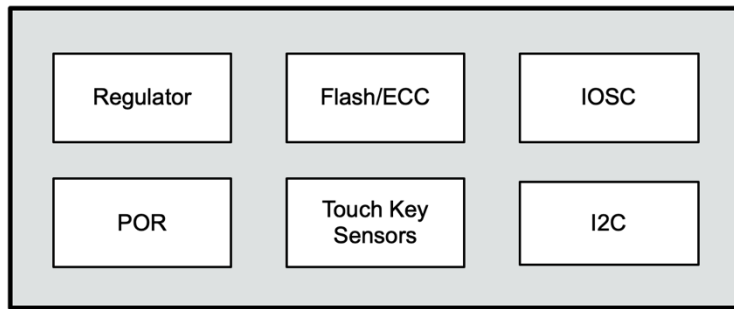


Figure 2: Function Block Diagram

Basic introduction for touch sense data process flow

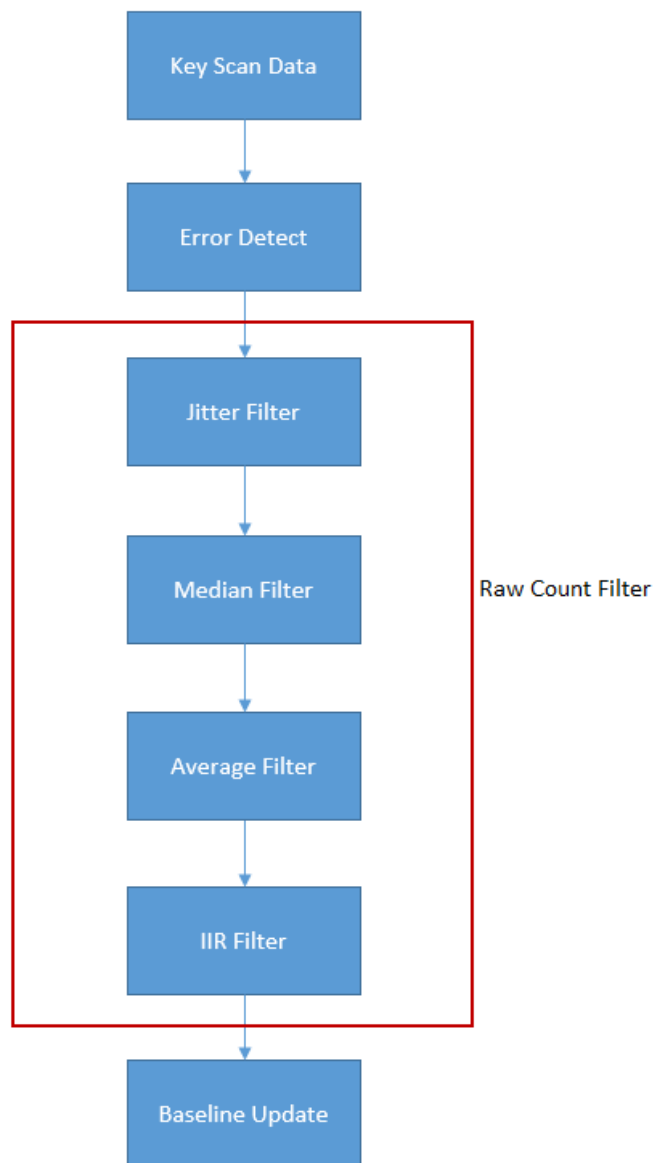


Figure 3: Touch Sense Data Process Flow

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Baseline process based on the difference between baseline and raw count

Baseline will be updated to the current raw count based on the below factors. For detailed information about baseline, please refer to Section 4.4.2 Key parameter in “IS31SE5120A Eval Board User’s Manual” application note.

Positive noise threshold

Baseline is updated if the difference count of baseline count and raw count is below the positive noise threshold.

Negative noise threshold

It is used with the low baseline reset count to reset baseline count to the current raw count. Please refer to the description of **Low baseline reset**.

Low baseline reset

Low baseline reset count of each key. A reset count increases one if the absolute $|raw\ count - baseline| > negative\ noise\ threshold$. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute $|raw\ count - baseline| \leq negative\ noise\ threshold$.

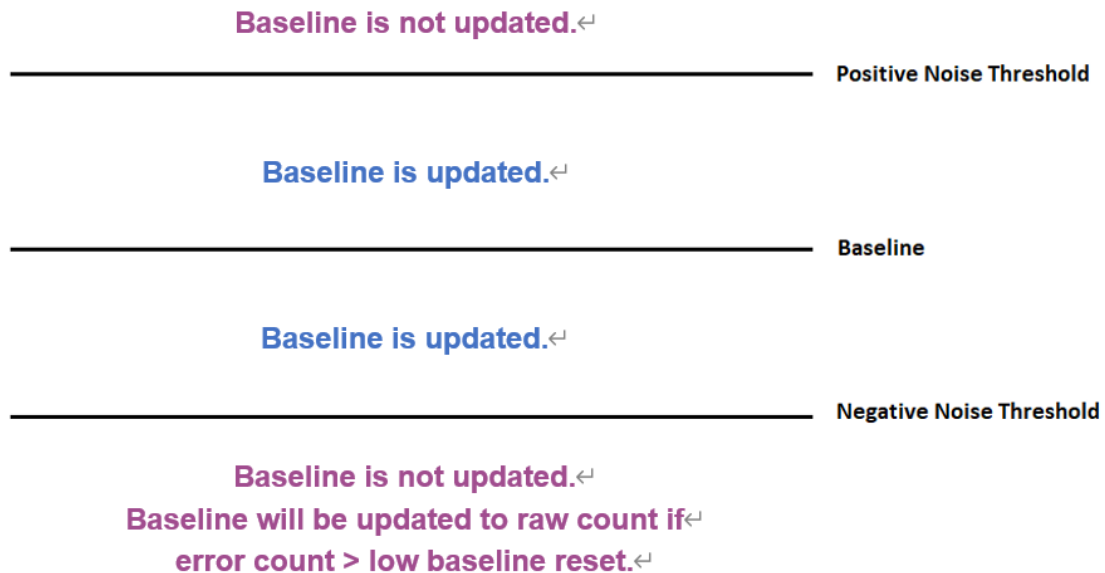


Figure 4: Baseline Process based on the difference between baseline and raw count

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Touch sense data identification

Ignore touch key scan if the signal exceeds the lock threshold.

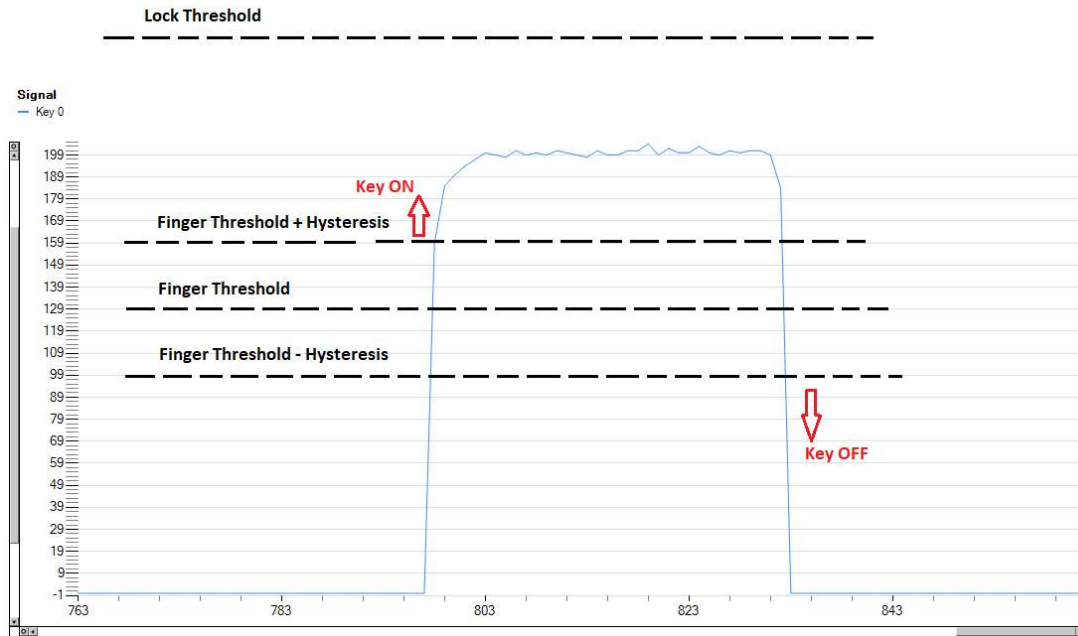


Figure 5: Touch Sense Data Identification

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DETAILED DESCRIPTION

I2C INTERFACE

S31SE5120 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. IS32SE5120 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command.

The complete slave address is:

Bit	A7:A1	A0
Value	0111100	1/0

The SCL line is uni directional. The SDA line is bi-directional (open collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. During communication, the microcontroller is the master and IS32SE5120 is the slave.

The timing diagram for the I2C is shown in Figure 6. The SDA is latched on to the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, and the most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the device address is sent, the master checks for "acknowledge" from IS32SE5120. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If IS32SE5120 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32SE5120, the register address byte is sent, and the most significant bit first. IS32SE5120 must generate another acknowledgment indicating that the registered address has been received.

Then 8-bit of data bytes are sent next, the most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS32SE5120 must generate another acknowledgment to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READ PORT REGISTERS

To read the device data, the bus master must first send the address of IS32SE5120 with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must send IS32SE5120 address with the R/W bit set to "1". Data from the register defined by the command byte is sent from IS32SE5120 to the master (Figure 9).

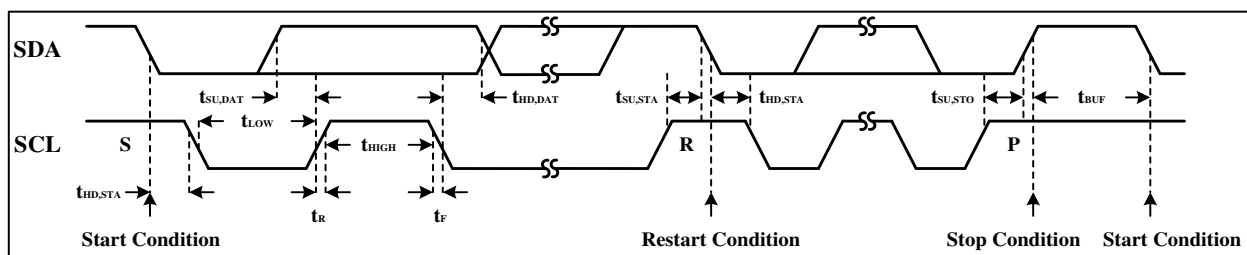


Figure 6: Interface Timing

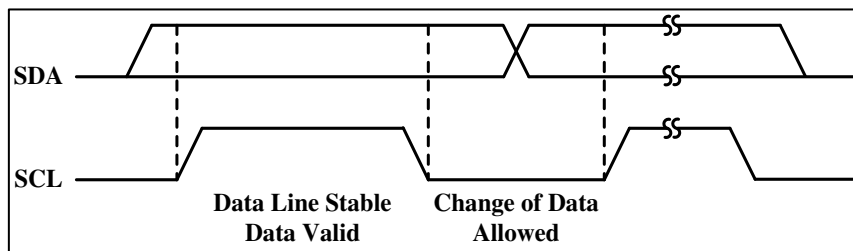


Figure 7: Bit Transfer

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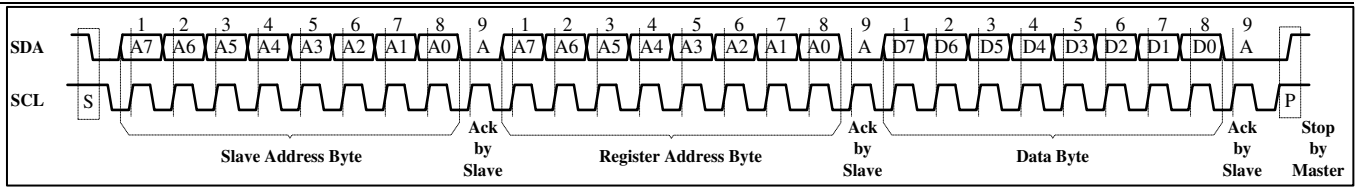


Figure 8: Writing to IS32SE5120

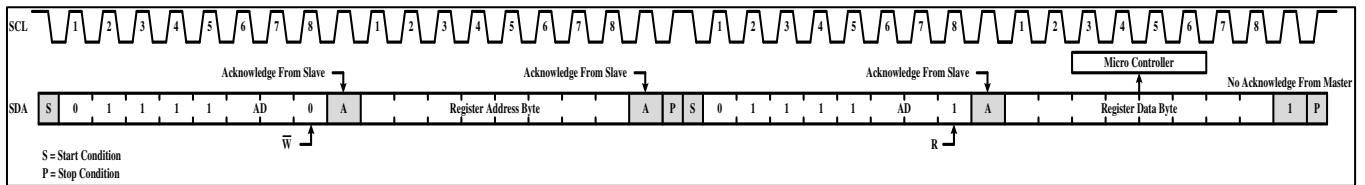


Figure 9: Reading from IS32SE5120

Note: Successive read or write protocol is supported.

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REGISTER DEFINITION

Page 0 Register list

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	20h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	20h
04h	Main Control	Management of system reset, power-saving, and parameters	W	00h
05h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
06h-08h	Key Status	Key 0-Key 23 status bits	R	00h
09h	BM	Buzzer data or stop command	W	-
09h	BM	Available buzzer buffer size	R	0Ah
0Ah-21h	Key Signal	Key 0-Key 23 signal value	R	00h
22h-51h	Key Raw Count	Key 0-Key 23 raw count value	R	0000h
52h-81h	Key Baseline	Key 0-Key 23 baseline value	R	0000h
82h-99h	Key Finger Threshold	Key 0-Key 23 finger threshold setting	R/W	50h or 28h
9Ah-B1h	Key Noise Threshold	Key 0-Key 23 noise threshold setting	R/W	28h or 14h
B2h-C9h	Key Negative Noise Threshold	Key 0-Key 23 negative noise threshold setting	R/W	28h or 14h
CAh-E1h	Key Low Baseline Reset	Key 0-Key 23 low baseline reset setting	R/W	1Eh
E2h-F9h	Key Hysteresis	Key 0-Key 23 hysteresis setting	R/W	08h or 04h
FAh-FFh	Slider 1-2 status	3 slider status registers for each slider	R/W	Addr FCh value: 80h, others value 00h

Page 1 Register list (extension memory)

Address	Name	Definition	R/W	Default
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0100h	Chip Part Number	Chip's part number	R	20h
0101h-0102h	Chip Version	Chip's version	R	-
0103h	Firmware Version	Firmware version	R	20h
0104h	Main Control	System reset, power-saving, and parameters management	W	00h
0105h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
0106h-0108h	Key Status	Key 0-Key 23 status bits	R	00h
0109h	BM	Buzzer data or stop command	W	-
0109h	BM	Available buzzer buffer size	R	0Ah
10Ah-121h	Key ON Debounce	Key 0-Key 23 debounce setting	R/W	03h
122h-124h	Key Interrupt Enable	Key 0-Key 23 enables Interrupts associated with capacitive touch sensor inputs	R/W	00h
125h	Raw Count Filter	Raw count filter setting	R/W	00h
126h	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
127h-128h	Lock Threshold	Lock threshold setting	R/W	03E8h
129h	Lock Scan Cycle	Lock scan cycle setting	R/W	08h
12Ah	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h
12Bh	Multiple Touch Key Configure	Multiple touch key function setting	R/W	03h
12Ch	Max Duration Time	Maximum duration time setting	R/W	1Ah
12Dh	Interrupt Configuration	Interrupt configuration	R/W	0Ah
12Eh	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
12Fh-131h	Key Pin Select	Select pins as Key0-Key23	R/W	000000h
132h-134h	Shield Pin Select	Select pin as a shield pin	R/W	000001h
135h-137h	INT Pin Select	Select pin as INT	R/W	000000h
138h-13Ah	Buzzer Pin Select	Select pin as a buzzer pin	R/W	002000h

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13Bh-13Dh	POW Pin Select	Select pin as buzzer power	R/W	00000h
13Eh-140h	GPIO Pin Select	Sets the GPIO enable KEY0~KEY23	R/W	01C000h
141h-143h	Slider 1 Pin Select	Max 8 keys	R/W	0000FCh
144h-146h	Slider 2 Pin Select	Max 8 keys	R/W	000000h
147h	TKIII Control register 1	Repeat sequence, initial setting delay, auto mode start delay, and low-frequency noise filter	R/W	13h
148h	TKIII Control register 2	Pseudo-random sequence setting	R/W	20h
149h	TKIII Control register 3	Multiple frequency scan/cycle count setting	R/W	03h
14Ah	TKIII CCHG	Internal charge capacitance setting	R/W	60h
14Bh	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
14Ch	System Clock Select	System clock setting	R/W	00h
14Dh	Spread Spectrum	Spread spectrum setting	R/W	0Ch
14Eh	Auto Sleep Mode	Auto enter sleep mode time setting	R/W	0Fh
14Fh	Sleep Mode Control	Sleep mode control setting	R/W	00h
150h-152h	Wake Up Key Select	Select Key0~Key23 to exit sleep mode	R/W	000000h
153h	Wake Up Threshold	Wake up threshold setting	R/W	08h
154h	TKIII Sleep Mode CCHG	Sleep mode internal charge capacitance setting	R/W	60h
155h	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
156h-157h	SLP_RAW	Sleep mode raw count value	R	0000h
158h-159h	SLP_Baseline	Sleep mode baseline value	R	0000h
15Ah-15Fh	Reserved	Reserved	-	-
160h	Slider 1 Mapping	Slider 1 Key position	R/W	07h
161h	Slider 1 Mapping	Slider 1 Key position	R/W	06h
162h	Slider 1 Mapping	Slider 1 Key position	R/W	05h
163h	Slider 1 Mapping	Slider 1 Key position	R/W	04h
164h	Slider 1 Mapping	Slider 1 Key position	R/W	03h

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165h	Slider 1 Mapping	Slider 1 Key position	R/W	02h
166h	Slider 1 Mapping	Slider 1 Key position	R/W	00h
167h	Slider 1 Mapping	Slider 1 Key position	R/W	00h
168h-16Fh	Slider 2 Mapping	Slider 2 Key position	R/W	00h
170h-17Fh	Reserved	Reserved	-	-
180h-182h	GPIO Value	Sensing the GPIO values for KEY0 – KEY23	R/W	01C000h
183h-185h	GPIO Enable	Enable KEY0 – KEY23 for GPIO	R/W	00001Ch
186h	GPIO Mapping 1	Key to GPIO mapping; see register for details	R/W	00h
187h	GPIO Mapping 2	Key to GPIO mapping; see register for details	R/W	00h
188h	GPIO Mapping 3	Key to GPIO mapping; see register for details	R/W	10h
189h	GPIO Mapping 4	Key to GPIO mapping; see register for details	R/W	0Fh
18Ah	GPIO Mapping 5	Key to GPIO mapping; see register for details	R/W	0Eh
18Bh-19Dh	GPIO Mapping 6-24	Key to GPIO mapping; see register for details	R/W	00h
19Eh-1A0h	GPIO Toggle EN	Enable GPIO Toggle mode for KEY0 – KEY23	R/W	100000h
1A1h	Key Scan Once	I2C control key scan	R/W	00h
1A2h	Table Ready Mark	Mark for flash data ready	R	00h

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Page 0 Registers

00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0010 0000

CPN Chip Part Number

Chip's part number 20h

01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2

CV1 & CV2 bytes contain chip revision. CV1 indicates the mask set version. CV2 indicates the minor version.

03h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	001	000	00

FV Firmware Version

Default version is 1.0.0

FV1[2:0] Major version

FV2[2:0] Minor version

FV3[1:0] Patch version

04h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset

1 System reset

RD Reset All Parameters to Manufacturer's Default Setting.

1 Reset all user-defined parameters to the

manufacturer's default setting.

SP Sleep Mode

1 Sleep mode

SS Save User Defined Parameters

1 Save current parameters into flash.

DW Deep Sleep Wake Up Reset Baseline

1 Reset touch key baseline after waking up from deep sleep mode.

DS Deep Sleep Mode

1 Keep sleep until waking up by I2C SDA falling edge.

Deep sleep mode will stop key scanning function and save more power consumption compared with the generic sleep mode.

05h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

06h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

07h Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

KSx Key8~Key15 Status

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If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.

- 0 Not detected.
- 1 Key is detected.

08h Key Status Register 3 (RO)

Bit	D7:D0
Name	KS[23:16]
Default	0000 0000

KSx Key16~Key23 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to “1”.

- 0 Not detected.
- 1 Key is detected.

09h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

BM Buzzer Register Write

Buzzer data or stop command

09h Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

BM Buzzer Register Read

It shows the available tone buffer size. IS32SE5120 has 10 built-in note buffers.

0Ah~21h KEY0~KEY23 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

KEYx_SIGNAL Key Signal Count

The difference between baseline and raw count. The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

22h, 24h..., 4Eh, 50h KEY0~KEY23 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

23h, 25h..., 4Fh, 51h KEY0~KEY23 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

KEYx_RAWCOUNT

Raw count of each key, provides an indication of the magnitude of the sensor's capacitance.

52h, 54h ..., 7Eh, 80h KEY0~KEY23 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

53h, 55h ..., 7Fh, 81h KEY0~KEY23 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

KEYx_Baseline

Baseline of each key

82h~99h KEY0~KEY23 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default Key0~Key16	0010 1000
Default Key17~Key23	0101 0000

KEYx_TH

Finger threshold of each key. It is used with hysteresis to determine the key state.

9Ah~B1h KEY0~KEY23 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default Key0~Key16	0001 0100
Default Key17~Key23	0010 1000

KEYx_NTH

Noise threshold of each key
Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

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B2h~C9h KEY0~KEY23 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default Key0~Key16	0001 0100
Default Key17~Key23	0010 1000

KEYx_NNTH

Negative noise threshold of each key.

CAh~E1h KEY0~KEY23 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

RCx Reset Count

Low baseline reset count of each key. A reset count increases one if the absolute |raw count – baseline| > absolute |negative noise threshold|. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute |raw count – baseline| ≤ absolute |negative noise threshold|.

E2h~F9h KEY0~KEY23 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default Key0~Key16	0000 0100
Default Key17~Key23	0000 1000

HYSTERESISx

Hysteresis of each key

FAh Slider1 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT Slider is active
 0 Disable slider
 1 Enable slider

INIP Initial position

FBh Slider1 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP

Default	0	0000000
---------	---	---------

DIR Direction of Slide1
 0 Rotate to left
 1 Rotate to right

ENDP End position of the slider

FCh Slider1 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	1	0000000

STA Status of Slider1
 0 Wheel
 1 Slider
 STA is the only bit for write.

DUR Duration
 The duration between the initial position to the end position. Every DUR bit increase presents 0.1s.

FDh Slider2 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT Slider2 is active
 0 Disable slider
 1 Enable slider

INIP Initial position

FEh Slider2 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

DIR Direction of Slide2
 0 Rotate to left
 1 Rotate to right

ENDP End position of the slider

FFh Slider2 Status Register 3 (RO)

Bit	D7	D6:D0
Name	STA	DUR
Default	0	0000000

STA Status of Slider2

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0 Wheel
1 Slider

DUR Duration

The duration between initial position to end position.
Every DUR bit increase presents 0.1s.

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Page 1 Registers (For Expand Memory)

100h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0010 0000

CPN Chip Part Number

Chip's part number 20h

101h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

102h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2

CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

103h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	001	000	00

FV Firmware Version

Default version is 1.0.0

FV1[2:0] Major version

FV2[2:0] Minor version

FV3[1:0] Patch version

104h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset

1 System reset

RD Reset All Parameters to Manufacturer's Default Setting.

1 Reset all user-defined parameters to the manufacturer's default setting.

SP Sleep Mode

1 Sleep mode

SS Save User Defined Parameters

1 Save current parameters into flash.

DW Deep Sleep Wake Up Reset Baseline

1 Reset touch key baseline after waking up from deep sleep mode.

DS Deep Sleep Mode

1 Keep sleep until waking up by I2C SDA falling edge.

Deep sleep mode will stop key scanning function and save more power consumption compared with the generic sleep mode.

105h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

106h Key Status Register 1 (RO)

Bit	D7:D0						
Name	KS[7:0]						
Default	0000 0000						

KSx Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

107h Key Status Register 2 (RO)

Bit	D7:D0							
Name	KS[15:8]							
Default	0000 0000							

KSx Key8~Key15 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

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1 Key is detected.

108h Key Status Register 3 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx Key16~Key23 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

109h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

BM Buzzer Register Write

Buzzer data or stop command

109h Buzzer Register (R)

	D7:D0
Name	BM[7:0]
Default	0000 1010

BM Buzzer Register Read

It shows the available tone buffer size. IS32SE5120 has 10 built-in note buffers.

10Ah~121h KEY0~KEY23 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0011

DEBOUNCEx

Debounce number of each key. When the acquired number > debounce setting value, then the key is granted as ON state.

122h~124h Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key causes the interrupt pin to be asserted when it is detected touched with the key's interrupt enable bit set.

INTEN Key Interrupt Enable

0 Disable

1 Enable

The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (12Dh) to "1", INTB pin will generate an interrupt signal.

125h Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

MF Median Filter

0 Disable

1 Enable

AF Average Filter

0 Disable

1 Enable

IIR IIR Filter

00 Disable

01 1/2

10 1/4

11 1/8

JF Jitter Filter

0 Disable

1 Enable

JD Jitter Delta

00 1

01 2

10 4

11 8

126h Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]
Default	0000 0001

RATIO

Range 1 ~ 255

127h Lock Threshold High Byte Register (RW)

Bit	D7:D0
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Name	LT[15:8]
Default	0000 0011

128h Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

LT Lock Threshold

129h Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

LSC Lock Scan Cycle

Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

12Ah Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

RCDL Raw Count Difference Limit

Ignore the key scan data if the difference between the previous raw count and the current raw count exceeds the limit.

12Bh Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	11

MTK Multiple Touch Key

- 00 Allow all keys to be triggered at one time.
- 01 Allow one key to be triggered at one time.
- 10 Allow two keys to be triggered at one time.
- 11 Allow three keys to be triggered at one time.

12Ch Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]-
Default	0	0	0	1	1010

MDEN Maximum Duration Time Enable

- 0 Disable

- 1 Enable

MDT Maximum Duration Time

- 0000 0.5s
- 0001 1s
- 0010 2s
- 0011 3s
- 0100 4s
- 0101 5s
- 0110 6s
- 0111 7s
- 1000 8s
- 1001 9s
- 1010 10s
- 1011 11s
- 1100 12s
- 1101 13s
- 1110 14s
- 1111 15s

MDT bits set the pressed time. When the key pressed duration exceeds the programmed time (MDT), the device will be forced to calibrate the pressed key. Set MDEN to “1” will enable this function.

12Dh Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

INE Interrupt Function Enable

- 0 Disable
- 1 Enable

ACEN Auto-Clear Interrupt Enable

- 0 Disable
- 1 Enable

ACT Auto-Clear Interrupt Time

- 000 10ms
- 001 20ms
- 010 30ms
- 011 40ms
- 100 50ms
- 101 100ms
- 110 150ms
- 111 200ms

When ACEN=0, the INT will keep low until the device’s 06h, 07h, and 08h registers are read, or the

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key is released. When ACEN=1, the INT will be released after the ACT setting time is expired even 06h, 07h, and 08h registers are not read, or the key is still pressed.

12Eh Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

INTRT Interrupt Repeat Time

0000	disable
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

After INTRT is set, a second interrupt will be generated after the interrupt repeat time is expired if there is a key keeping pressed.

12Fh~131h Key Pin Select Register (RW)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

Bit	D7:D0
Name	KS[23:16]
Default	0000 0000

KS Key Pin Selection Setting

0	Disable
1	Enable

132h~134h Shield Pin Select Register (RW)

Bit	D7:D0
Name	SHDE[7:0]
Default	0000 0001

Bit	D7:D0
Name	SHDE[15:8]
Default	0000 0000

Bit	D7:D0
Name	SHDE[23:16]
Default	0000 0000

SHDE Shield Enable (default for SHDE[14])

0	Disable shield driver
1	Enable shield driver

135h~137h INT Pin Select Register (RW)

Bit	D7:D0
Name	IPS1[7:0]
Default	0000 0000

Bit	D7:D0
Name	IPS1[15:8]
Default	0000 0000

Bit	D7:D0
Name	IPS1[23:16]
Default	0000 0000

IS32SE5120 interrupt Pin has been fixed at Pin 16 INTB and it doesn't work to set INT Pin Select Register 135h, 136h, and 137h.

138h~13Ah Buzzer Pin Select Register 1 (RW)

Bit	D7:D0
Name	BPS1[7:0]

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Default	-----
---------	-------

Bit	D7:D0
Name	BPS2[7:0]
Default	-- 1 - ----

Bit	D7:D0
Name	BPS3[7:0]
Default	-----

BPS1/2 Buzzer output Select 1/2

Enable BPS2[5] will set Pin15 as the Buzzer output pin.

BPS1[7:9] & BPS3[7:0] unused register bits.

13Bh Enable Buzzer Power Register 1 (RW)

Bit	D7:D0
Name	EBP1 [7:0]
Default	-----

13Ch Enable Buzzer Power Register 2 (RW)

Bit	D7:D0
Name	EBP2 [0]
Default	--- 1 ----

EBP1/2 Buzzer Power Select 1/2

EBP1[7:0] unused register bits.

EBP2[4] maps to KEY12. Writing 1 to EBP2[4] will enable KEY12 as the Buzzer Power. Setting other EBP2 bits doesn't work.

13Dh Enable Buzzer Power Register 3 (RW)

Bit	D7:D0
Name	EBP3 [7:0]
Default	-----

13Eh~140h GPIO Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	1100 0000

Bit	D7:D0
Name	GPIO[23:16]
Default	0000 0001

GPIO pin select will go with register 180h GPIO Value 1, register 181h GPIO Value 2, and register 182h GPIO Value 3 to have GPIO pin high or low.

141h~143h Slider1 Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	1111 1100

Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

Bit	D7:D0
Name	GPIO[23:16]
Default	0000 0000

144h~146h Slider2 Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

Bit	D7:D0
Name	GPIO[23:16]
Default	0000 0000

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147h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	LFNF
Default	00	01	00	11

RPT Repeat Sequence Count

00	No repeat
01	Repeat 4 times
10	Repeat 8 times
11	Repeat 16 times

INI Initial Setting Delay

INI[1-0] defines the number of TKCLK periods for the initial settling of pin Cref. The delay is (INI[1-0] + 1) * 4 * TKCLK.

ASTDLY Auto Mode Start Delay

ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] + 1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.

LFNF Low-Frequency Noise Filter Setting

Low-Frequency Noise Filter Setting

00 Disable LFNE

If the scan count with noise injection detection is larger than (LFNF [1-0] * 8), the scan result is ignored.

148h TKIII Control Register 2 (RW)

Bit	D3	D2:D1	D0
Name	-	-	-
Default	0	00	0

Bit	D7	D6	D5	D4
Name	-	-	PRS	-
Default	0	0	1	0

PRS Pseudo-Random Sequence

0	Disable PRS
1	Enable PRS

149h TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

MFEN Multiple Frequency Scan

0	Disable MF
1	Enable MF

CCNT Cycle Count of Each Conversion Sequence

000	1024
001	2048
010	4096
011	8192
100	12288
101	16384
110	32768
111	65536

14Ah TKIII CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select

000	10pF
001	20pF
010	30pF
011	40pF
100	50pF
101	60pF
110	70pF
111	80pF

14Bh TKIII PUD Register (RW)

Bit	D3:D0
Name	PUD [3:0]
Default	0000

Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	00	00

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we will try to maintain the raw count around half of CCNT for the case without key touch.

For DC current, PUD [3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD [3-0] enables 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable

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PUDREN Pull-up/Pull-down DC Resistor Enable

PUD Pull up DC Current

1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

PUD Pull up Resistor

1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

14Ch System Clock Select Register (RW)

Bit	D7:D4	D3	D2:D0
Name	-	CLKS	OSCD[2:0]
Default	0000	0	000

CLKS Clock Stretching (For I2C)

0	Disable stretching
1	Enable stretching

OSCD Oscillator Division

000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The default setting is 1 for 16MHz system clock.

14Dh Spread Spectrum Register (RW)

Bit	D7:D2		
Name	SSR[3:0]	SSA[1:0]	-
Default	0000	11	-

SS Spread Spectrum Setting

With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:

SSR [3:0] Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.

SSA [1:0] Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register.

SSA [1:0]=11	+/- 32
SSA [1:0]=10	+/- 16
SSA [1:0]=01	+/- 8
SSA [1:0]=00	+/- 4

14Eh Auto Sleep Mode Register (RW)

Bit	D3:D0		
Name	AST[3:0]-		
Default	1111		
Bit	D7	D6	D5:D4
Name	ASEN	-	BLMA[1:0]
Default	0	0	00

ASEN Auto-SLEEP Enable

0	Disable
1	Enable

BLMA Baseline moving average

The hardware baseline can be generated by the slow-moving average setting.

00	32 average
01	64 average
10	128 average
11	256 average

AST Auto Sleep Time

0000	0.5s
0001	1s
0010	1.5s
0011	2s
0100	2.5s
0101	3s
0110	3.5s
0111	4s
1000	4.5s
1001	5s
1010	6s
1011	7s
1100	8s
1101	9s
1110	10s

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14Fh Sleep Mode Control Register (RW)

Bit	D3:D2		D1:D0	
Name	T2[1:0]		T1[1:0]	
Default	00		00	
Bit	D7	D6	D5	D4
Name	-	PW	-	SC
Default	0	0	0	0

PW Proximity Wakeup
Disable: wake up>>scan key>>go to sleep again
Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected.

0 Disable
 1 Enable

SC Sleep Calibration

0 Disable
 1 Enable

T2 Wake Up Period with Key Disable
 The device will be woken up according to the T2 setting by polling the status of Key.

00 50ms
 01 100ms
 10 200ms
 11 300ms

T1 Wake Up Period with Key Enable
 The device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up the device.

00 2s
 01 4s
 10 8s
 11 16s

150h~152h Wake Up Key Select Register (RW)

Bit	D7:D0
Name	WK[7:0]
Default	0000 0000

Bit	D7:D0
Name	WK[15:8]

Default	0000 0000
---------	-----------

Bit	D7:D0
Name	WK[23:16]
Default	0000 0000

WK Wakeup Key Select Setting

0 Disable
 1 Enable

153h Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

Wake up threshold range from 0 to 255

154h TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D0
Name	CCHG[2:0]	-
Default	011	00000

CCHG Internal Reference Capacitance Select

000 10pF
 001 20pF
 010 30pF
 011 40pF
 100 50pF
 101 60pF
 110 70pF
 111 80pF

155h TKIII Sleep Mode PUD Register (RW)

Bit	D3:D0		
Name	PUD[3:0]		
Default	0000		
Bit	D7	D6	D5:D4
Name	PUDIEN	PUDREN	-
Default	0	0	00

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance caused by a high capacitance key. Connecting a switching current

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source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor

PUDIEN Pull-up/Pull-down DC Current Enable

PUDREN Pull-up/Pull-down DC Resistor Enable

PUD	Pull up DC Current
1000	Enable 8uA current source.
0100	Enable 4uA current source.
0010	Enable 2uA current source.
0001	Enable 1uA current source.

PUD	Pull up Resistor
1000	Enable 5K resistor source.
0100	Enable 10K resistor source.
0010	Enable 20K resistor source.
0001	Enable 40K resistor source.

156h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

157h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

SLRC Sleep Mode Raw Count
Read-only. Value for reference

158h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

159h Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

SLB Sleep Mode Baseline
Read-only. Value for reference

15Ah-15Fh Reserved

Bit	D7:D0
Name	-
Default	---- ----

160h-167h Slider1 Map Register 1 (RW)

Bit	D7:D0
Name	S1Kx[7:0]
Default	xxxx xxxx

S1Kx Slider1 Keyx Map table
Slider1 KEYx is mapped to Touch Key S1Kx[3:0]

168h-16Fh Slider2 Map Register (RW)

Bit	D7:D0
Name	S2Kx[7:0]
Default	0000 0000

S2Kx Slider2 Keyx Map table
Slider2 KEYx is mapped to Touch Key S2Kx[7:0]

170h – 177h Reserved

Bit	D7:D0
Name	-
Default	---- ----

178h – 17Fh Reserved

Bit	D7:D0
Name	-
Default	---- ----

180h GPIO Value Register 1 (R/W)

Bit	D7:D0
Name	GPV [7:0]
Default	0000 0000

181h GPIO Value Register 2 (R/W)

Bit	D7:D0
Name	GPV [15:8]
Default	1100 0000

182h GPIO Value Register 3 (R/W)

Bit	D7:D0
Name	GPV [23:16]

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Default	0000 0001
---------	-----------

GPV GPIO Value

Define GPIO values

0 GPIO pin LOW

1 GPIO pin HIGH

Above GPIO pin HIGH or LOW will be set only when the corresponding bits of the register GPIO Pin Select registers (13Eh~140h) are enabled.

183h GPIO Enable Register 1 (R/W)

Bit	D7:D0
Name	GPE [7:0]
Default	0001 1100

184h GPIO Enable Register 2 (R/W)

Bit	D7:D0
Name	GPE [15:8]
Default	0000 0000

185h GPIO Enable Register 3 (R/W)

Bit	D7:D0
Name	GPE [23:16]
Default	0000 0000

GPE GPIO Enable

0 Disable GPIO function

1 Enable GPIO function

186h-19Dh GPIO Map Register (R/W)

Bit	D7:D0
Name	GMx [7:0]
Default	xxxx xxxx

GMx [7:0] Map touch key x to which IS32SE5120 pin according to the following table and the value of GMx [7:0].

IS32SE5120 Pin #	GMx [7:0]
P2	0
P3	1
P4	2
P5	3
P6	4
P7	5
P8	6
P9	7

P10	8
P11	9
P12	10
P13	11
P14	12
P15	13
P19	14
P23	15
P24	16
P26	17
P27	18
P28	19
P29	20
P30	21
P31	22
P32	23

19Eh GPIO Toggle Enable Register 1 (R/W)

Bit	D7:D0
Name	TOEN [7:0]
Default	0001 0000

19Fh GPIO Toggle Enable Register 2 (R/W)

Bit	D7:D0
Name	TOEN [15:8]
Default	0000 0000

1A0h GPIO Toggle Enable Register 3 (R/W)

Bit	D7:D0
Name	TOEN [23:16]
Default	0000 0000

TOENx Enable GPIO Toggle Mode

0 Disable Touch Key channel to enter GPIO Toggle Mode.

1 Enable Touch Key channel to enter GPIO Toggle Mode.

1A1h Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	-	TR	EN
Default	0000	00	00

TR

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Write 1 Trigger one scan
 Read 1 Busy
 Read 0 Data ready

Name	MARK[7:0]
Default	0000 0000

EN Enable Key Scan Once
 0 Continuous scan of all enabled keys
 1 Scan all enabled keys once

MARK

This register is used by the firmware to indicate parameters are correctly programmed.

Ready/Fail status

00 ready

Others not ready

1A2h Table Ready Mark Register (RO)

Bit	D7:D0
-----	-------

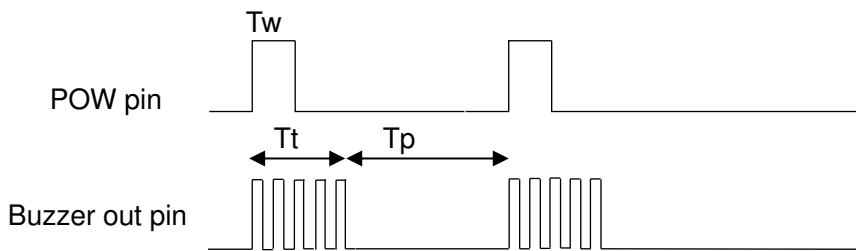
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BUZZER / MELODY APPLICATION

09h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

1st byte	2nd byte	3rd byte	4th byte
Scale ID	Tt	Tw	Tp



Tt, Tw and Tp range from 0 to 255 @ 4ms step

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%

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	6	freq	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B

09h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

Clear Melody buffer and stop play.

09h Buzzer/Melody Register (R)

Bit	D7:D0
Name	BM
Default	0000 1010

BM Buzzer/Melody Register Read. It shows the available tone buffer size. IS32SE5120 has 10 built-in note buffers.

I2C command format - Each note is composed of 4-byte data, and the incomplete note will be ignored. The incoming note data will be ignored if the FIFO is full.

0x78, 0x09, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp),

0x78, 0x09, 0xFF stop the melody play and clear the FIFO

0x78, 0x09 Set the register number to 0xF0

0x79 Read FIFO remaining length

Reference schematic and tone waveform are introduced as follows:

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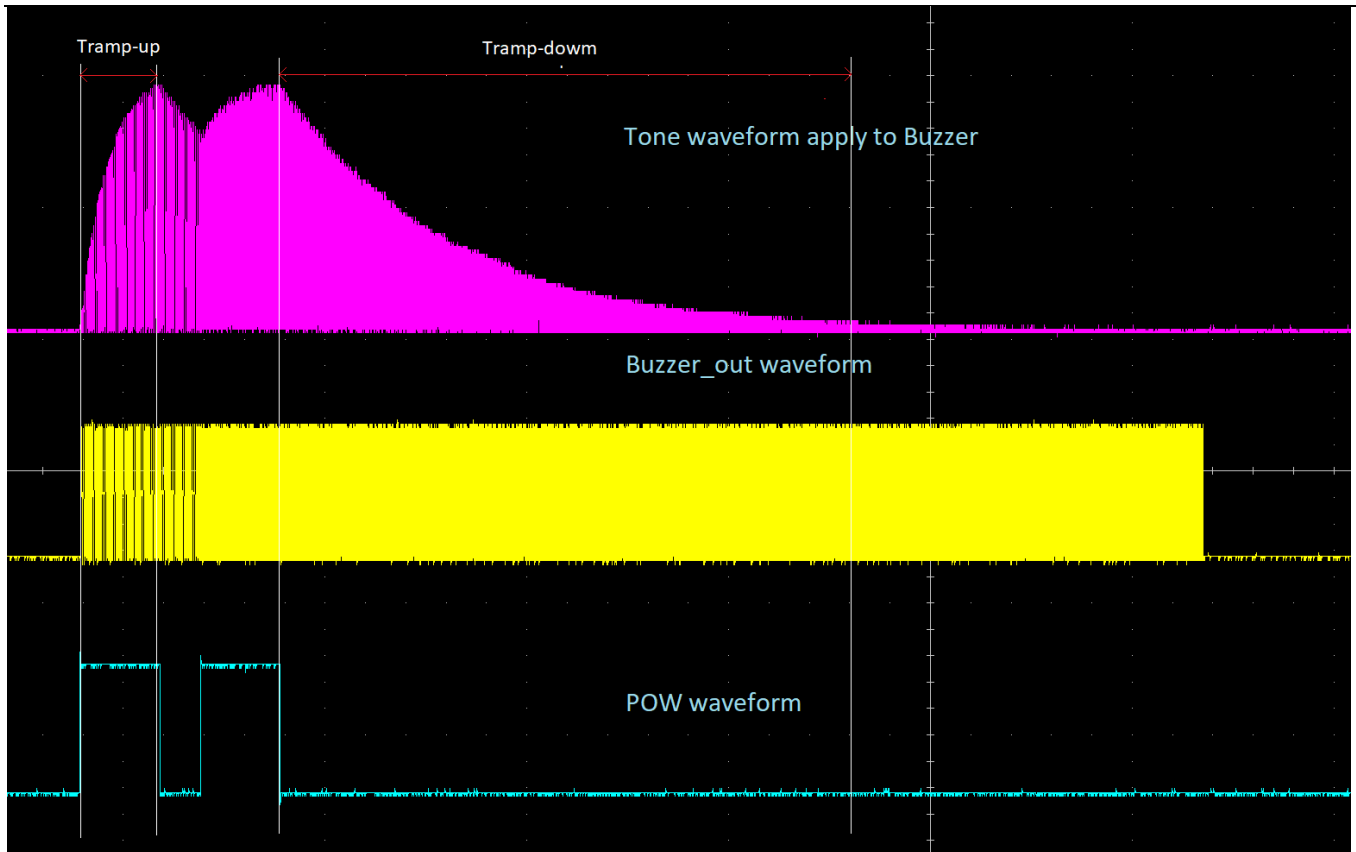


Figure 10: Buzzer/ Melody waveform example

Note:

$T_{\text{ramp-up}}$: 100R as below figure 11 decides the signal ramp-up rate.

$T_{\text{ramp-down}}$: The signal ramps down because POW is low and 47uF capacitor as below figure 11 decides the ramp-down rate.

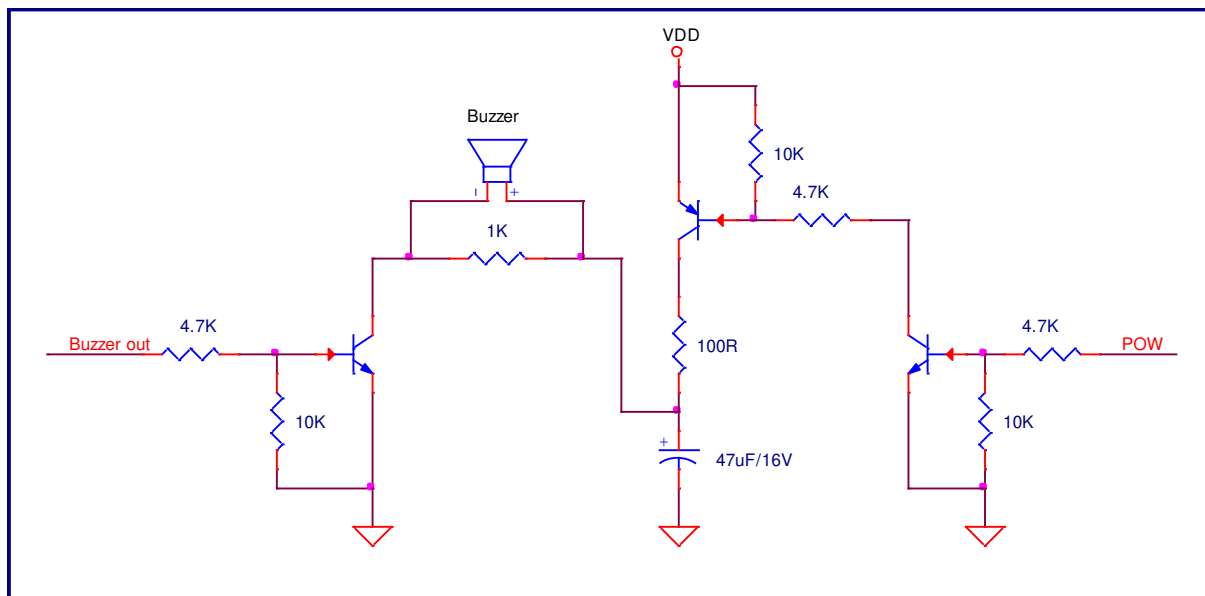


Figure 11: Typical application circuit for Melody

IS32SE5120

TYPICAL APPLICATION INFORMATION

The IS32SE5120 is an ultra-low-power, fully integrated 24-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor or internal register.

A higher capacitor value will yield lower detection sensitivity. A lower capacitor value will yield higher detection sensitivity.

INTERRUPT

Touch key detection event will trigger the INTB pin. The INTB pin will be driven low when the selected channel is pressed or released.

Sleep Mode

IS32SE5120 can be put in sleep mode to save power consumption and the device can be woken up by touching the selected keys. For the detailed application, please refer to the Lumissil application note “**How to program SE5117_SE5118_SE5120 into auto sleep mode?**”. We also provide a sample code for this application.

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CLASSIFICATION REFLOW PROFILE

Profile Feature	Pb-Free Assembly
Preheat & Soak	
Temperature min (T _{smin})	150°C
Temperature max (T _{smax})	200°C
Time (T _{smin} to T _{smax}) (t _s)	60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L)	217°C
Time at liquidous (t _L)	60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak	8 minutes max.

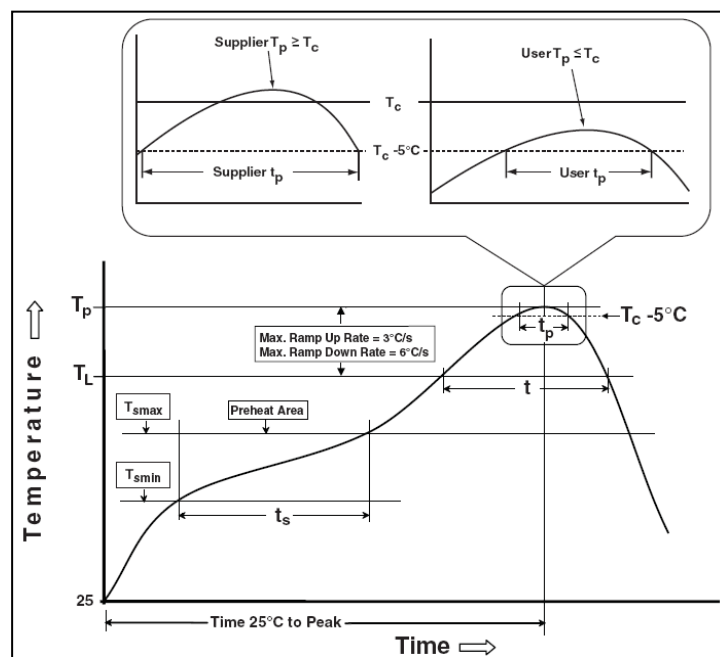
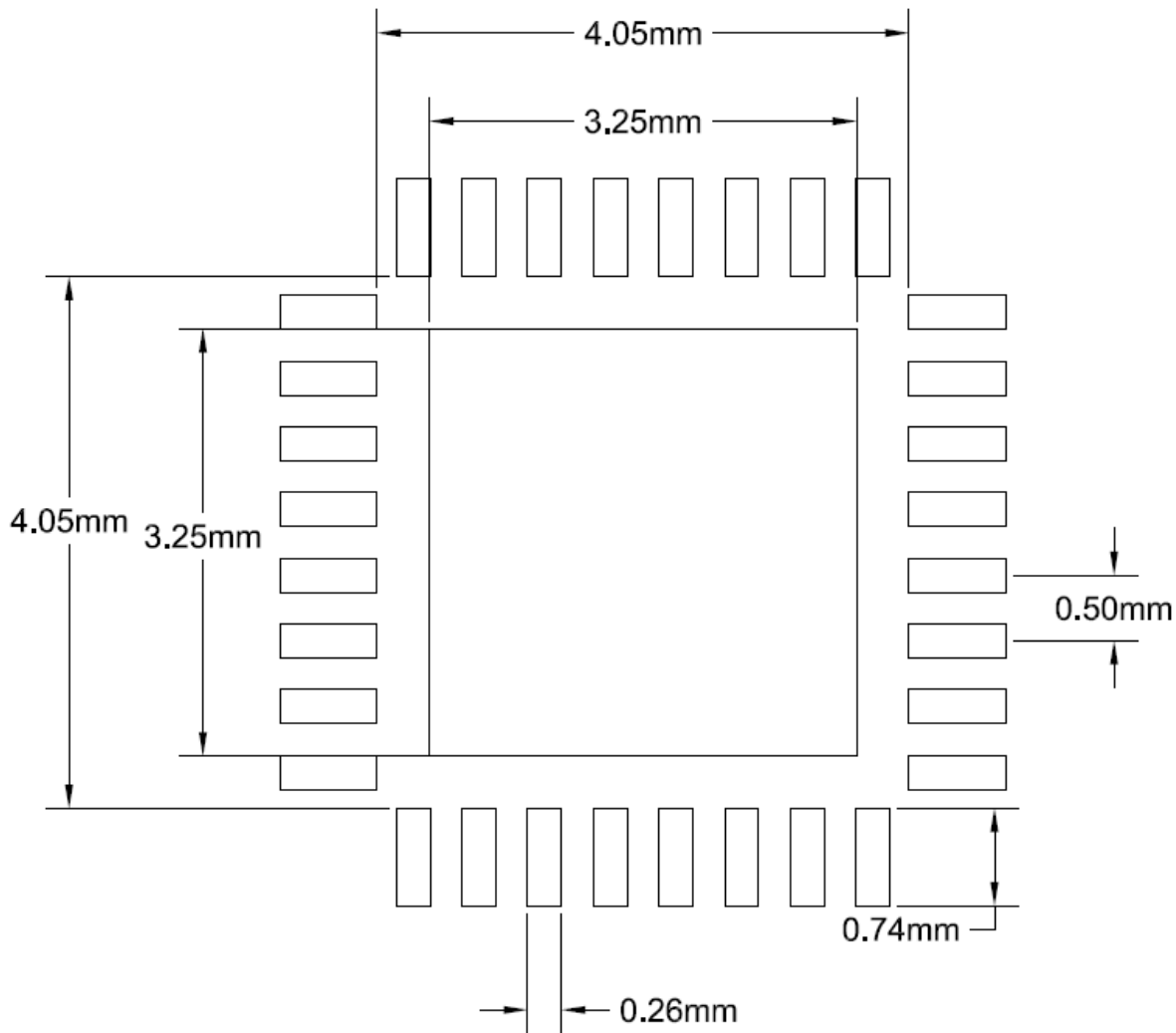


Figure 12: Classification Profile

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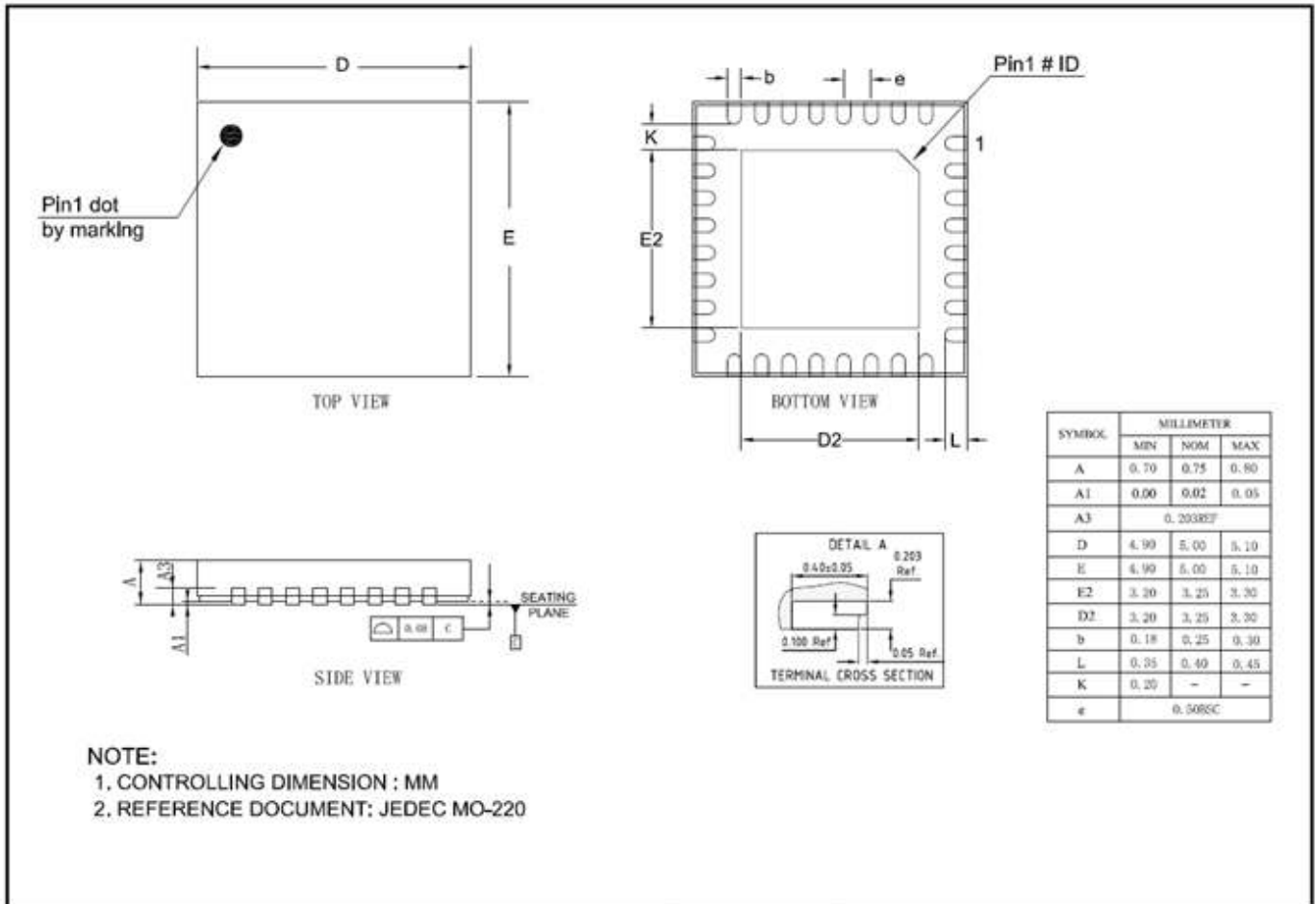
32-pin WQFN

RECOMMENDED LAND PATTERN



IS32SE5120

POD



IS32SE5120

REVISIONS

Revision	Detailed Information	Date
A	First formal release	2022.07.20
B	<ol style="list-style-type: none"> 1. Add support for proximity sensing 2. Add “Halogen-Free compliant” claim for product features 	2022.09.28
C	<ol style="list-style-type: none"> 1. Add GPIO DC Characteristics in <u>Section DC ELECTRICAL CHARACTERISTICS</u> 2. Add detailed definitions for 183h GPIO Enable 1, 184h GPIO Enable 2, and 185h GPIO Enable 3 in page 1 register list table and clear description/table for GMx [7:0] for touch key to GPIO function 3. Add detailed information for registers 13Eh ~ 140h GPIO Pin Select and registers 180h GPIO value 1 ~ 182h GPIO value 3 4. Modify pin number mapping table in GPIO Map Register 5. Register 6, register 7, and register 8 need to be read to acquire key status and interrupt will be clear after register 8 is read 6. Add “AEC-Q100 qualification” support 7. Modify PIN description table 8. Reword some content for clearer descriptions 9. Add TSCA compliance 10. Add baseline update description for Figure 4: Baseline Process based on the difference between baseline and raw count in <u>Section Function Block Diagram</u> 	2023.07.26