

# 2N7002T

## N-channel TrenchMOS FET

Rev. 01 — 17 November 2005

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Logic level threshold compatible
- Surface-mounted package
- Very fast switching
- TrenchMOS technology

### 1.3 Applications

- Logic level translator
- High-speed line driver

### 1.4 Quick reference data

- $V_{DS} \leq 60 \text{ V}$
- $R_{DS(on)} \leq 5 \ \Omega$
- $I_D \leq 300 \text{ mA}$
- $P_{tot} \leq 0.83 \text{ W}$

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 SOT23	 mbb076
2	source (S)		
3	drain (D)		

### 3. Ordering information

**Table 2: Ordering information**

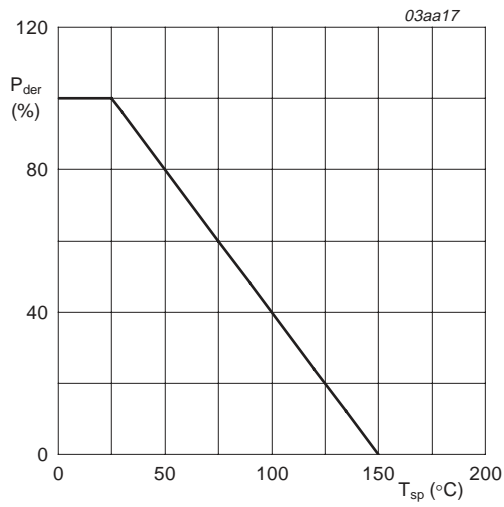
Type number	Package		Version
	Name	Description	
2N7002T	TO-236AB	plastic surface mounted package; 3 leads	SOT23

### 4. Limiting values

**Table 3: Limiting values**

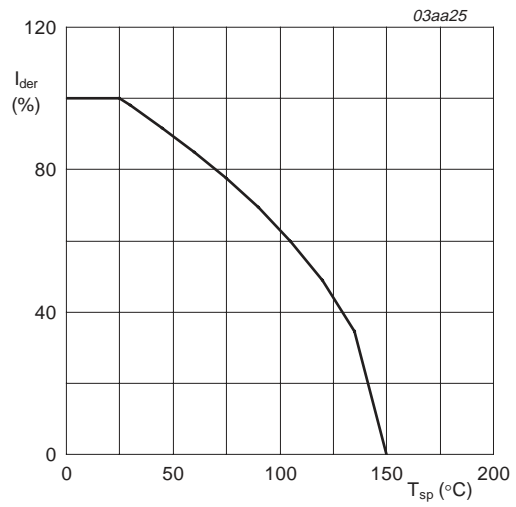
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage		-	$\pm 30$	V
$V_{GSM}$	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$ ; pulsed; duty cycle = 25 %	-	$\pm 40$	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	300	mA
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	190	mA
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	1.2	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	0.83	W
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-65	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	300	mA
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	1.2	A



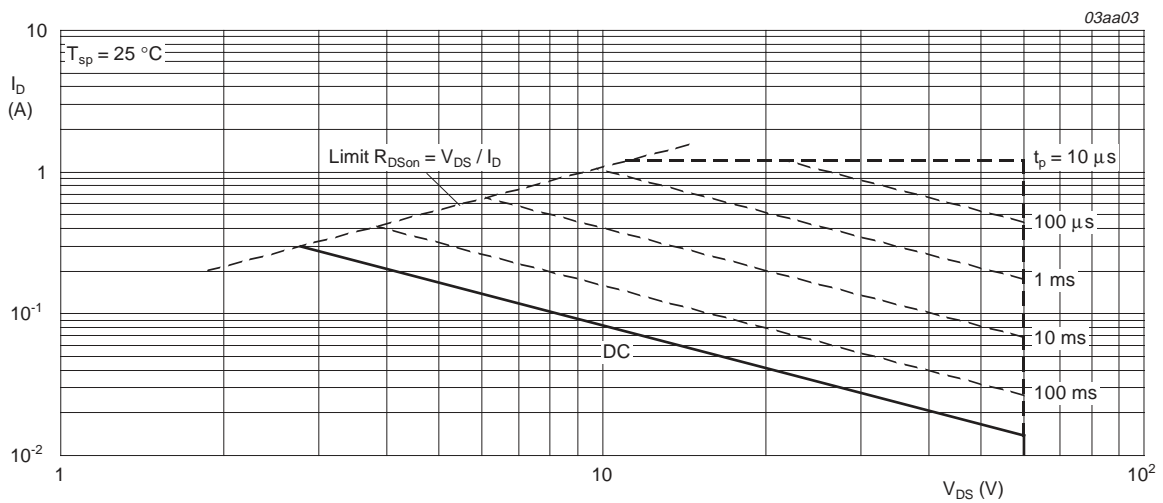
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	150	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	350	K/W

[1] Mounted on a printed-circuit board; minimum footprint; vertical in still air

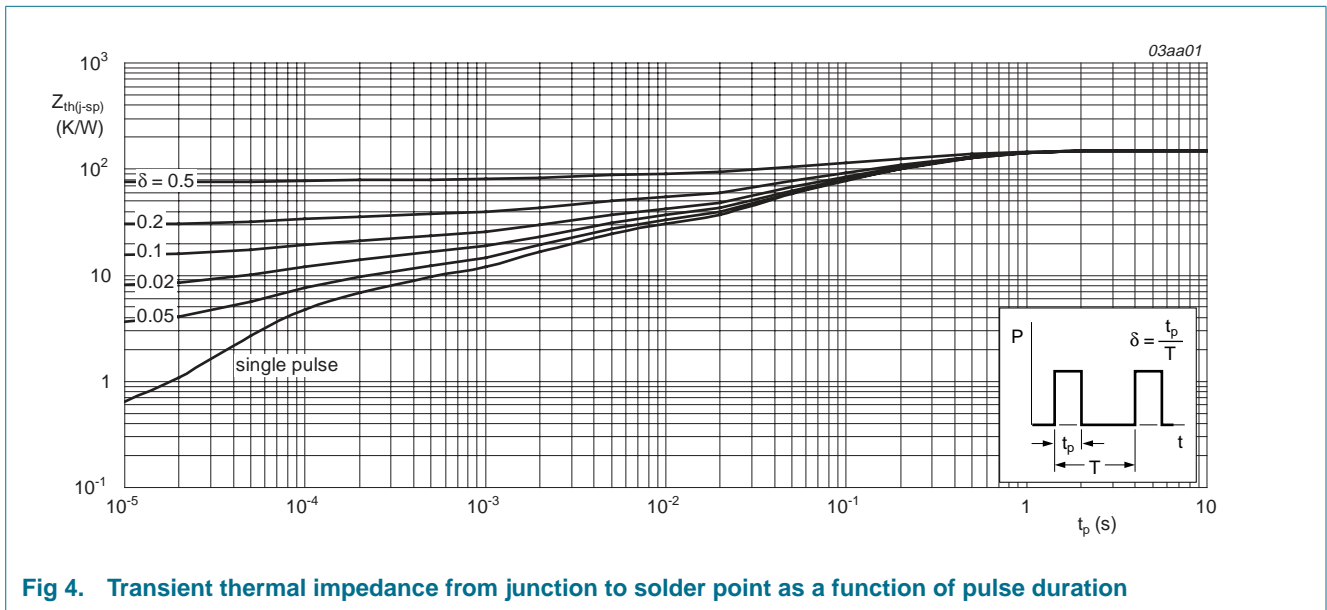
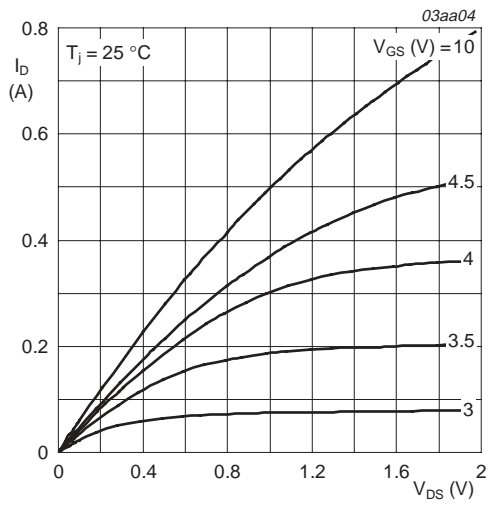


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

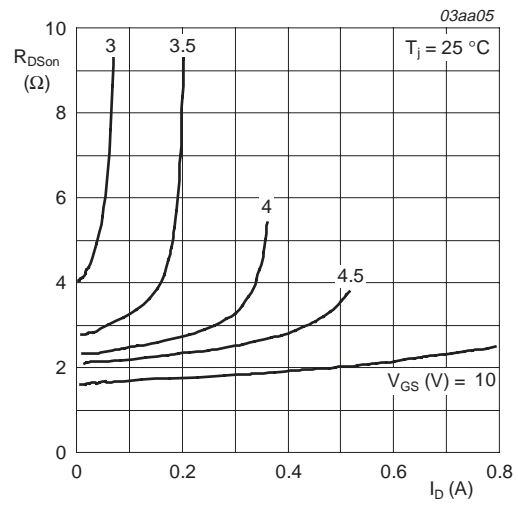
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	60	-	-	V
		T <sub>j</sub> = -55 °C	55	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		T <sub>j</sub> = 25 °C	1	2	2.5	V
		T <sub>j</sub> = 150 °C	0.6	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.75	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.01	1	μA
		T <sub>j</sub> = 150 °C	-	-	10	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±15 V; V <sub>DS</sub> = 0 V	-	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 500 mA; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		T <sub>j</sub> = 25 °C	-	2.8	5	Ω
		T <sub>j</sub> = 150 °C	-	-	9.25	Ω
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 75 mA; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	3.8	5.3	Ω
<b>Dynamic characteristics</b>						
g <sub>fs</sub>	transfer conductance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 200 mA; see <a href="#">Figure 11</a>	100	300	-	mS
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 10 V; f = 1 MHz; see <a href="#">Figure 12</a>	-	25	40	pF
C <sub>oss</sub>	output capacitance		-	18	30	pF
C <sub>rss</sub>	reverse transfer capacitance		-	7.5	10	pF
t <sub>on</sub>	turn-on time	V <sub>DS</sub> = 50 V; R <sub>L</sub> = 250 Ω; V <sub>GS</sub> = 10 V;	-	3	10	ns
t <sub>off</sub>	turn-off time	R <sub>G</sub> = 50 Ω; R <sub>GS</sub> = 50 Ω	-	12	12	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 300 mA; V <sub>GS</sub> = 0 V; see <a href="#">Figure 13</a>	-	0.85	1.5	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 300 mA; di <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	30	-	ns
Q <sub>r</sub>	recovered charge		-	30	-	nC



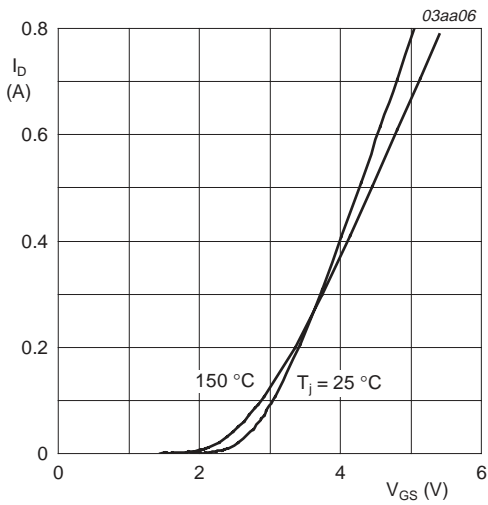
T<sub>j</sub> = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



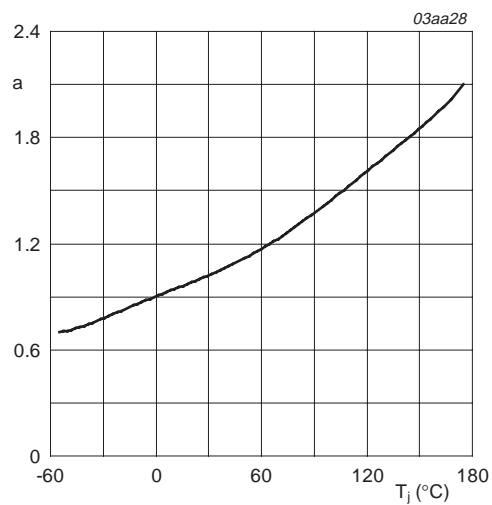
T<sub>j</sub> = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



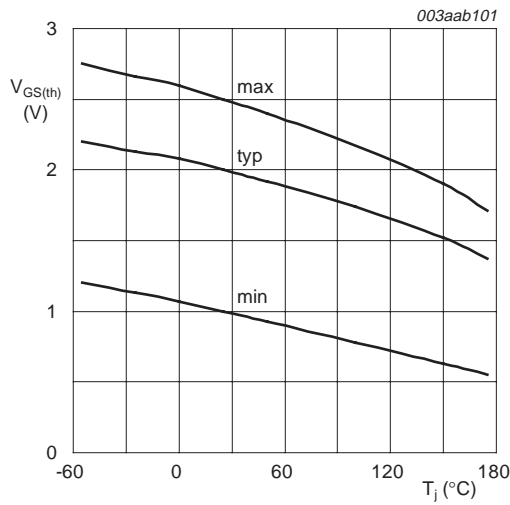
T<sub>j</sub> = 25 °C and 150 °C; V<sub>DS</sub> > I<sub>D</sub> × R<sub>DSon</sub>

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



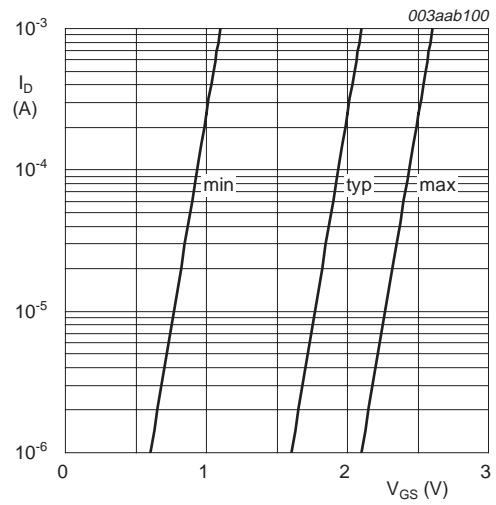
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



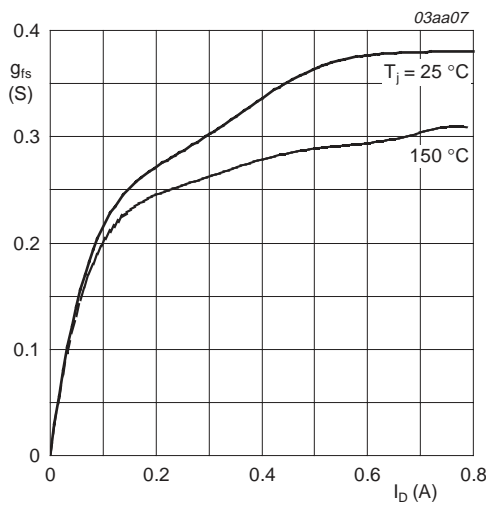
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



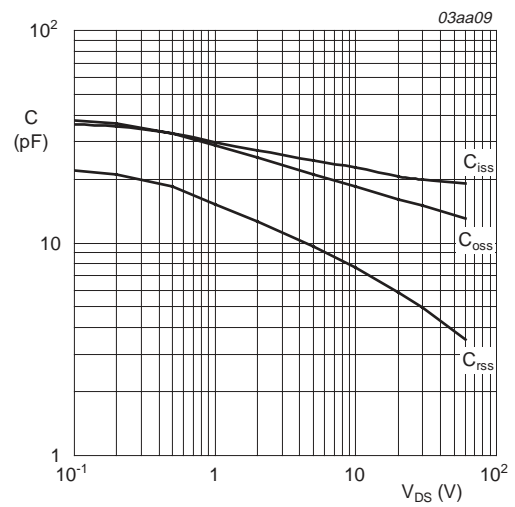
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



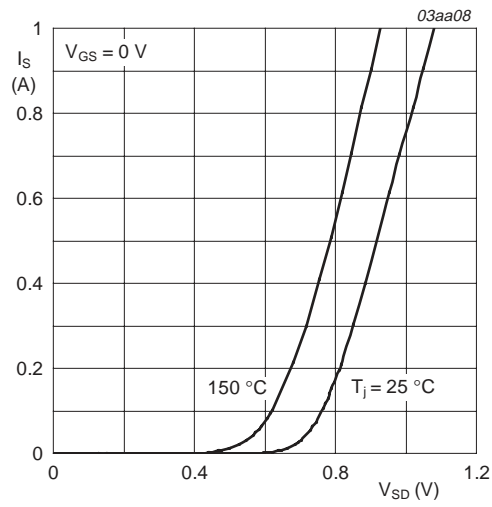
$T_j = 25 \text{ }^\circ\text{C and } 150 \text{ }^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

Fig 11. Transfer conductance as a function of drain current; typical values



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25$  °C and  $150$  °C;  $V_{GS} = 0$  V

**Fig 13. Source current as a function of source-drain voltage; typical values**



7. Package outline

Plastic surface mounted package; 3 leads

SOT23

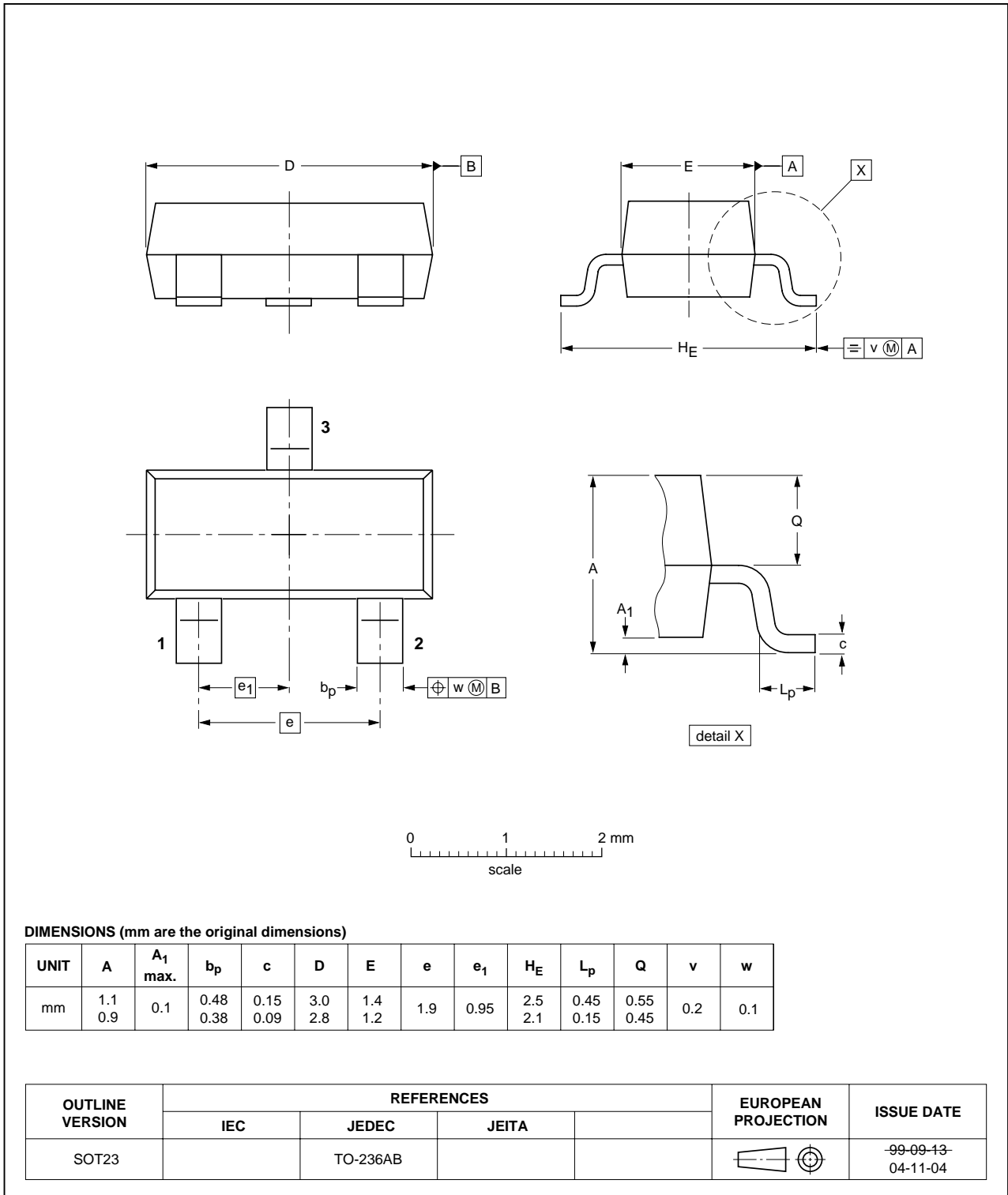


Fig 14. Package outline SOT23

## 8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
2N7002T_1	20051117	Product data sheet	-	-	-

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Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
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