FAIRCHILD SEMICONDUCTOR®

October 2001

Si3454DV

N-Channel PowerTrench® MOSFET

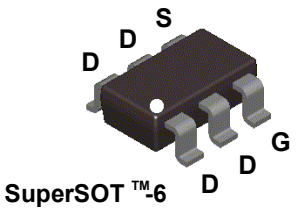
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

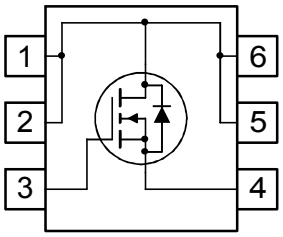
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 4.2 A, 30 V. $R_{DS(ON)}$ = 65 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 95 mΩ @ V_{GS} = 4.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge (9.4 nC typical)
- High power and current handling capability



SuperSOT ™-6



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 1a)	4.2	A
	– Pulsed		20	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.454	Si3454DV	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J=70°C			25	
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	1.5	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		– 4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 4.2 A V_{GS} = 4.5 V, I_D = 3.4 A		33 44	65 95	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.2 A		10		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		460		pF
C_{oss}	Output Capacitance			115		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DS} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5	20	nS
t_r	Turn–On Rise Time			8	30	nS
$t_{d(off)}$	Turn–Off Delay Time			17	35	nS
t_f	Turn–Off Fall Time			13	20	nS
t_{rr}	Source-Drain Reverse Recovery Time	I_F = 1.7 A, di/dt = 100 A/uS			80	nS
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 4.2 A, V_{GS} = 10 V		9.4	15	nC
Q_{gs}	Gate–Source Charge			1.2		nC
Q_{gd}	Gate–Drain Charge			1.1		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.7	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 78°C/W when mounted on a 1in^2 pad of 2oz copper on FR-4 board.

b. 156°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

Figure 3. On-Resistance Variation withTemperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.

Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Package marking	Packing method
SI3454DV	Full Production	$0.346	SuperSOT	6	.454	TAPE REEL

* 1,000 piece Budgetary Pricing

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