AS1751, AS1752, AS1753

DataSheet

High-Speed, Low-Voltage, Single-Supply, 0.9Ω, Quad SPST Analog Switches

1 General Description

The AS1751/AS1752/AS1753 are high-speed, low-voltage, quad single-pole/single-throw (SPST) analog switches.

Fast switching speeds, low ON-resistance, and low power consumption make these devices ideal for single-cell battery powered applications.

These highly-reliable devices operate from a single +1.6 to +3.6V supply, and are differentiated by the type and number of switches:

- AS1751 – Four normally open (NO) switches
- AS1752 – Four normally closed (NC) switches
- AS1753 – Two NO switches and Two NC switches

The AS1753 supports break-before-make switching.

With very low ON-resistance (R_{ON}), R_{ON} matching and R_{ON} flatness, the devices can accurately switch signals for sample and hold circuits, digital filters, and op-amp gain switching networks.

The AS1751/AS1752/AS1753 digital logic input is 1.8V CMOS-compatible when using a +3V supply, and all devices can handle Rail-to-Rail signals.

The devices are available in a 3mm x 3mm 16-pin TQFN package and a 14-pin TSSOP package.

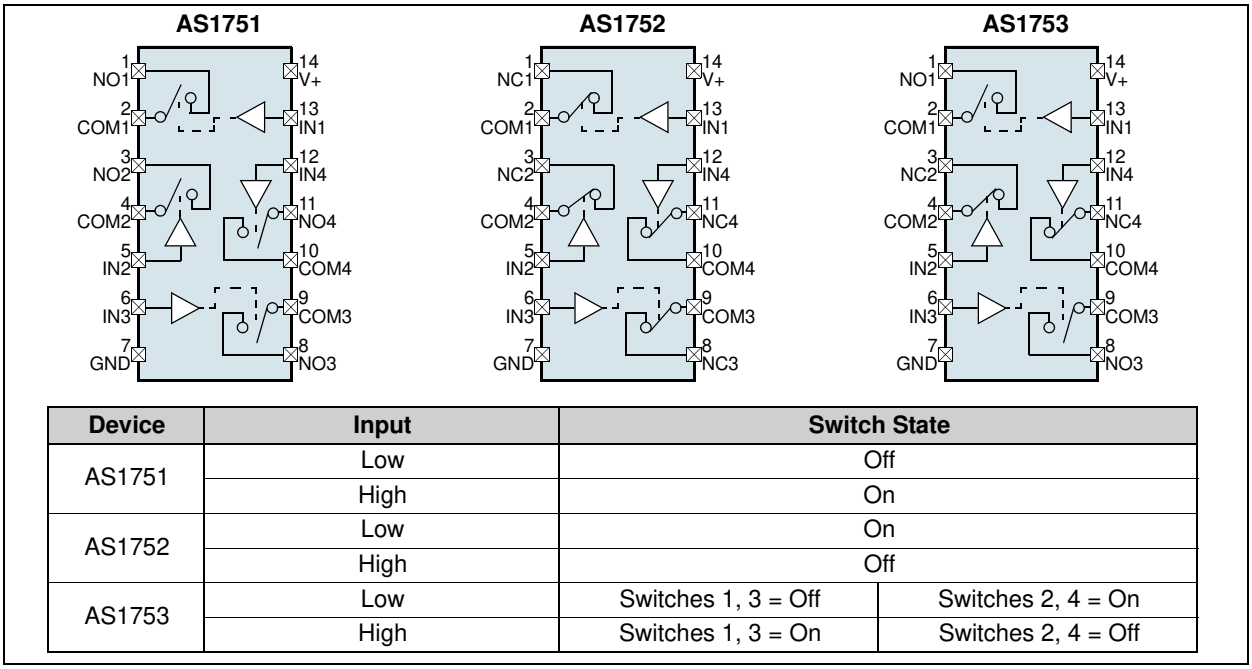
2 Key Features

- ON-Resistance:
  - 0.9Ω (+3V supply)
  - 2.5Ω (+1.8V supply)
- R_{ON} Matching:
  - 0.12Ω (+3V supply)
  - 0.25Ω (+1.8V supply)
- R_{ON} Flatness: 0.1Ω (+3V Supply)
- Supply Voltage Range: +1.6 to +3.6V
- Switching Speed: t_{ON} = 22ns, t_{OFF} = 14ns
- Current-Handling: 250mA Continuous
- Break-Before-Make Switching (AS1753)
- Rail-to-Rail Signal Handling
- 1.8V CMOS Logic Compatible (+3V Supply)
- Operating Temperature Range: -40 to +85ºC
- Package Types:
  - 16-pin TQFN (3mm x 3mm)
  - 14-pin TSSOP

3 Applications

The devices are ideal for use in power routing systems, cordless and mobile phones, MP3 players, CD and DVD players, PDAs, handheld computers, digital cameras, hard drives, and any other application where high-speed signal switching is required.

Figure 1. 14-pin TSSOP Block Diagrams



Device	Input	Switch State	
AS1751	Low	Off	
	High	On	
AS1752	Low	On	
	High	Off	
AS1753	Low	Switches 1, 3 = Off	Switches 2, 4 = On
	High	Switches 1, 3 = On	Switches 2, 4 = Off

4 Pinout

Pin Assignments

Figure 2. TQFN Pin Assignments (Top View)

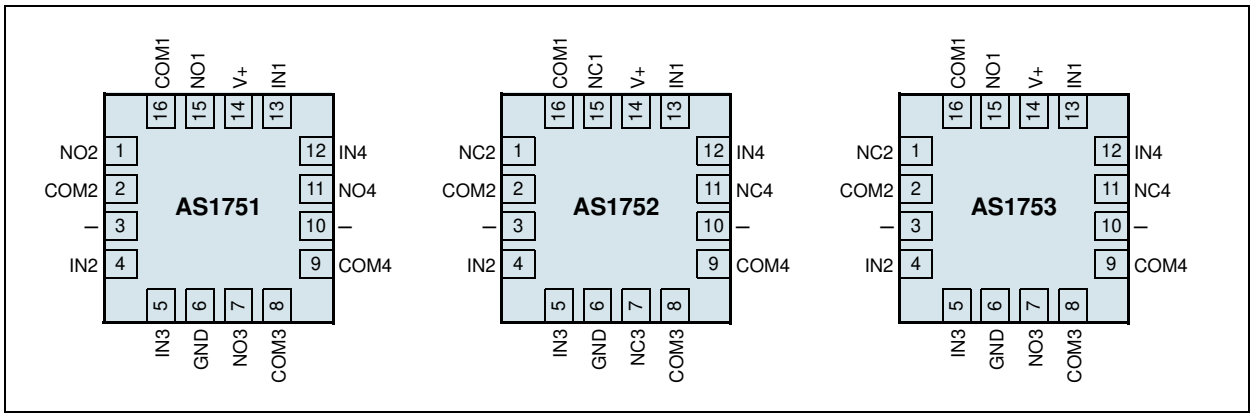
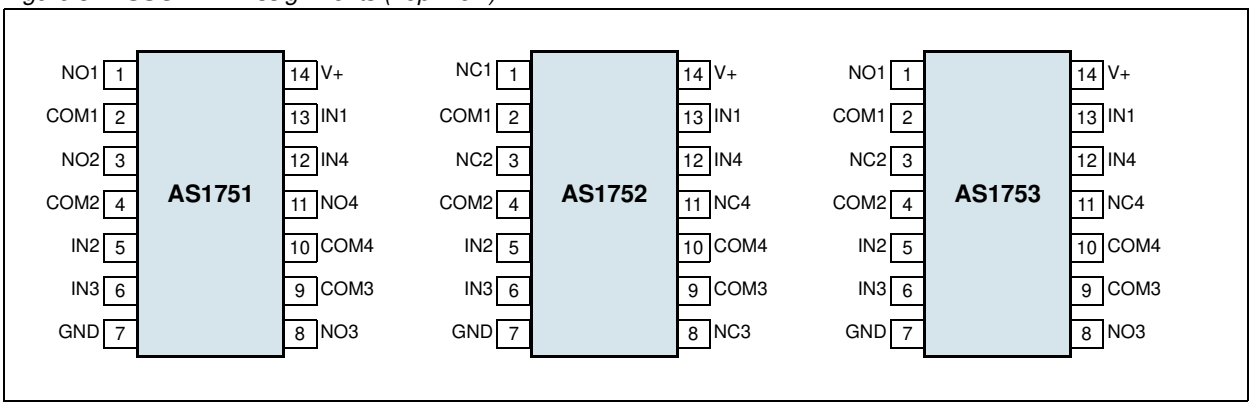


Figure 3. TSSOP Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
(see Figure 2 and Figure 3)	COM1:COM4	**Analog Switch 1, 2, 3, 4 Common**
	GND	**Ground**
	IN1:IN4	**Analog Switch 1, 2, 3, 4 Logic Control Input**
	NC1:NC4	**Analog Switch 1, 2, 3, 4 Normally Closed Terminal**
	NO1:NO4	**Analog Switch 1, 2, 3, 4 Normally Open Terminal**
	V+	**Input Supply Voltage**. +1.6 to +3.6V

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Comments
V+, IN*x* to GND		-0.3	+5	V	
COM*x*, NO*x*, NC*x* to GND †		-0.3	V+ + 0.3	V	
COM*x*, NO*x*, NC*x* Continuous Current		-250	+250	mA	
COM*x*, NO*x*, NC*x* Peak Current		-350	+350	mA	Pulsed at 1ms 10% duty cycle
Continuous Power Dissipation (T_{AMB} = +70ºC)	16-pin TQFN		727	mW	Derate at 9.1W/ºC above +70ºC
	14-pin TSSOP		1349		Derate at 16.9W/ºC above +70ºC
Operating Temperature Range		-40	+85	ºC	
Electro-Static Discharge			2500	V	*HBM Mil-Std883E 3015.7* methods
Latch Up Immunity			250	mA	Norm: *JEDEC 17*
Junction Temperature			+150	ºC	
Storage Temperature Range		-65	+150	ºC	
Package Body Temperature			+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*

† Signals on pins COM1, COM3, NO1, NO2, NC1, or NC2 that exceed V+ or GND are clamped by internal diodes. Forward-diode current should be limited to the maximum current rating.

6 Electrical Characteristics

Table 3. Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V+	Power Supply Range	T_{AMB} = T_{MIN} to T_{MAX}	1.6		3.6	V
I+	Positive Supply Current	V+ = 3.6V, V_{INx} = 0 or V+, T_{AMB} = +25ºC			0.1	µA

V+ = +2.7 to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values @ V+ = +3.0V, T_{AMB} = +25ºC.

Table 4. +3V Supply Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Analog Switch							
V_{COMx}, V_{NOx}, V_{NCx}	Analog Signal Range			0		V+	V
R_{ON}	ON-Resistance	V+ = 2.7V, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 1.5V	T_{AMB} = +25ºC		0.4	0.9	Ω
			T_{AMB} = T_{MIN} to T_{MAX}			1	
ΔR_{ON}	ON-Resistance Match Between Channels [1]	V+ = 2.7V, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 1.5V	T_{AMB} = +25ºC		0.03	0.12	Ω
			T_{AMB} = T_{MIN} to T_{MAX}			0.15	
$R_{FLAT(ON)}$	ON-Resistance Flatness [2]	V+ = 2.7V, I_{COMx} = 100mA, V_{NOx} or V_{NCx} = 1, 1.5, or 2V	T_{AMB} = +25ºC		0.02	0.1	Ω
			T_{AMB} = T_{MIN} to T_{MAX}			0.12	
$I_{NOx(OFF)}$, $I_{NCx(OFF)}$	NO*x* or NC*x* Off-Leakage Current	V+ = 3.6V, V_{COMx} = 0.3 or 3.6V, V_{NOx} or V_{NCx} = 3.6 or 0.3V	T_{AMB} = +25ºC	-2.5		+2.5	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-10		+10	
$I_{COMx(OFF)}$	COM*x* Off-Leakage Current	V+ = 3.6V, V_{COMx} = 0.3 or 3.6V, V_{NOx} or V_{NCx} = 3.6 or 0.3V	T_{AMB} = +25ºC	-2.5		+2.5	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-10		+10	
$I_{COMx(ON)}$	COM*x* On-Leakage Current	V+ = 3.6V, V_{COMx} = 0.3 or 3.6V, V_{NOx} or V_{NCx} = 0.3 or 3.6V	T_{AMB} = +25ºC	-2.5		+2.5	nA
			T_{AMB} = T_{MIN} to T_{MAX}	-10		+10	
Switch Dynamic Characteristics							
t_{ON}	Turn On Time [3]	V_{NOx} or V_{NCx} = 1.5V, R_{LOAD} = 50Ω, C_{LOAD} = 35pF, Figures 13, 14	T_{AMB} = +25ºC		16	22	ns
			T_{AMB} = T_{MIN} to T_{MAX}			24	
t_{OFF}	Turn Off Time [3]	V_{NOx} or V_{NCx} = 1.5V, R_{LOAD} = 50Ω, C_{LOAD} = 35pF, Figures 13, 14	T_{AMB} = +25ºC		5	14	ns
			T_{AMB} = T_{MIN} to T_{MAX}			15	
t_{BBM}	Break-Before-Make [3]	V_{NOx} or V_{NCx} = 1.5V, R_{LOAD} = 50Ω, C_{LOAD} = 35pF, Figure 15 (AS1753)	T_{AMB} = +25ºC		11		ns
			T_{AMB} = T_{MIN} to T_{MAX}	2			
Q	Charge Injection	V_{GEN} = V+, R_{GEN} = 0, C_{LOAD} = 1.0nF, Figure 16			2		pC
C_{OFF}	NO*x*, NC*x* Off-Capacitance	f = 1MHz, Figure 17			45		pF
$C_{COMx(OFF)}$	COM*x* Off-Capacitance	f = 1MHz, Figure 17			49		pF
$C_{COMx(ON)}$	COM*x* On-Capacitance	f = 1MHz, Figure 17			85		pF

Table 4. +3V Supply Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Off-Isolation [4]	f = 10MHz, R_{LOAD} = 50Ω, C_{LOAD} = 5pF, Figure 18		-40		dB
		f = 1MHz, R_{LOAD} = 50Ω, C_{LOAD} = 5pF, Figure 18		-55		
	Crosstalk [5]	f = 10MHz, R_{LOAD} = 50Ω, C_{LOAD} = 5pF, Figure 18		-70		dB
		f = 1MHz, R_{LOAD} = 50Ω, C_{LOAD} = 5pF, Figure 18		-80		
THD	Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COMx} = 2Vp-p, R_{LOAD} = 32Ω		0.033		%
Logic Input						
V_{IH}	Input Logic High		1.4			V
V_{IL}	Input Logic Low				0.5	V
I_{IN}	Input Leakage Current	V_{INx} = 0 or V+	-1	0.0001	+1	µA

V+ = +1.8V, V_{IH} = +1.0V, V_{IL} = 0.4V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified). Typ values @ T_{AMB} = +25ºC.
Table 5. +1.8V Supply Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Analog Switch							
V_{COMx}, V_{NOx}, V_{NCx}	Analog Signal Range			0		V+	V
R_{ON}	ON-Resistance	V+ = 1.8V, I_{COMx} = 10mA, V_{NOx} or V_{NCx} = 0.9V	T_{AMB} = +25ºC		0.9	2.5	Ω
			T_{AMB} = T_{MIN} to T_{MAX}			3	
ΔR_{ON}	ON-Resistance Match Between Channels [1]	V+ = 1.8V, I_{COMx} = 10mA, V_{NOx} or V_{NCx} = 0.9V	T_{AMB} = +25ºC		0.05	0.25	Ω
			T_{AMB} = T_{MIN} to T_{MAX}			0.25	
Switch Dynamic Characteristics							
t_{ON}	Turn On Time [3]	V_{NOx} or V_{NCx} = 1.0V, R_{LOAD} = 50Ω, C_{LOAD} = 35pF, Figures 13, 14	T_{AMB} = +25ºC		22	30	ns
			T_{AMB} = T_{MIN} to T_{MAX}			35	
t_{OFF}	Turn Off Time [3]	V_{NOx} or V_{NCx} = 1.0V, R_{LOAD} = 50Ω, C_{LOAD} = 35pF, Figures 13, 14	T_{AMB} = +25ºC		12	20	ns
			T_{AMB} = T_{MIN} to T_{MAX}			25	
Q	Charge Injection	V_{GEN} = V+, R_{GEN} = 0, C_{LOAD} = 1.0nF, Figure 16			1		pC
Logic Input							
V_{IH}	Input Logic High			1.0			V
V_{IL}	Input Logic Low					0.4	V
I_{IN}	Input Leakage Current	V_{INx} = 0 or V+		-1	0.0001	+1	µA

1. ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.
2. Flatness is defined as the difference between the maximum and the minimum value of ON-resistance as measured over the specified analog signal ranges.
3. Guaranteed by design.
4. Off-Isolation = 20log10(V_{COMx}/V_{NOx}), V_{COMx} = output, V_{NOx} = input to off switch.
5. Between two switches.

7 Typical Operating Characteristics

Figure 4. Frequency Response

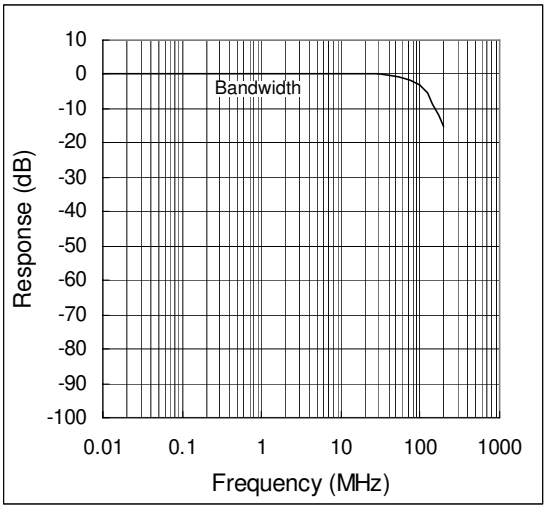


Figure 5. Total Harmonic Distortion vs. Frequency

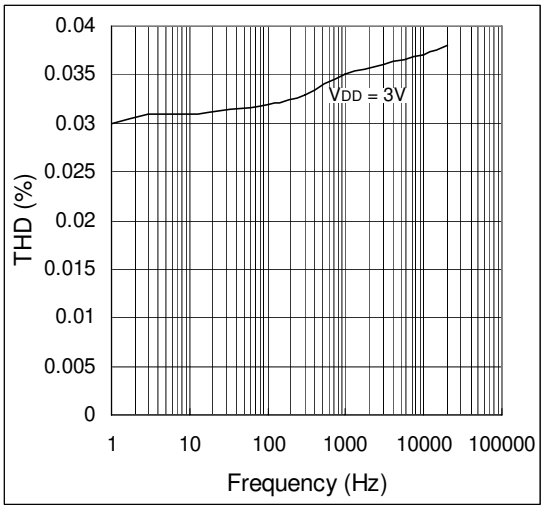


Figure 6. Turn On/Turn Off Time vs. Temperature

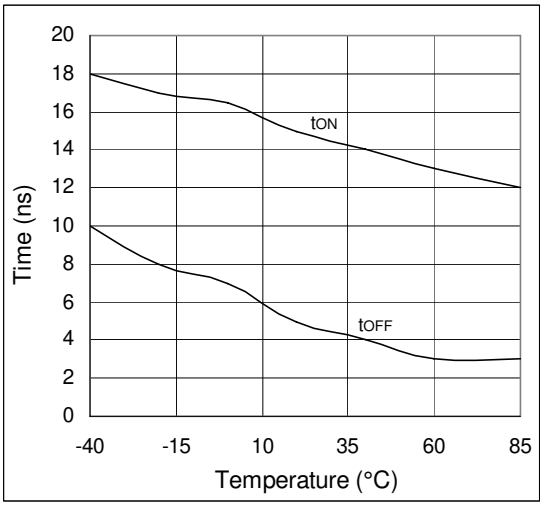


Figure 7. Turn On/Off Time vs. Supply Voltage

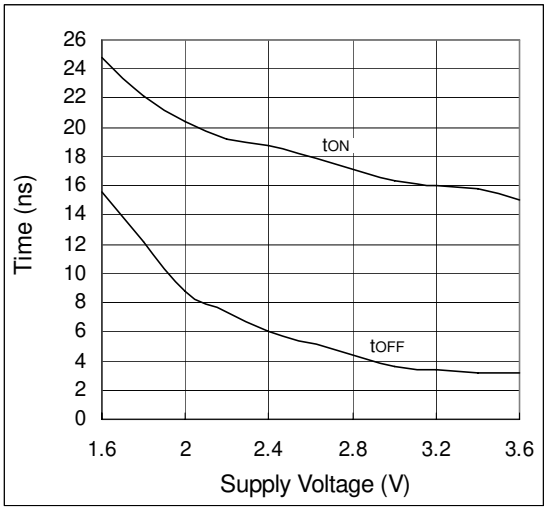


Figure 8. RON vs. VCOM and Temperature; VDD = 2.7V

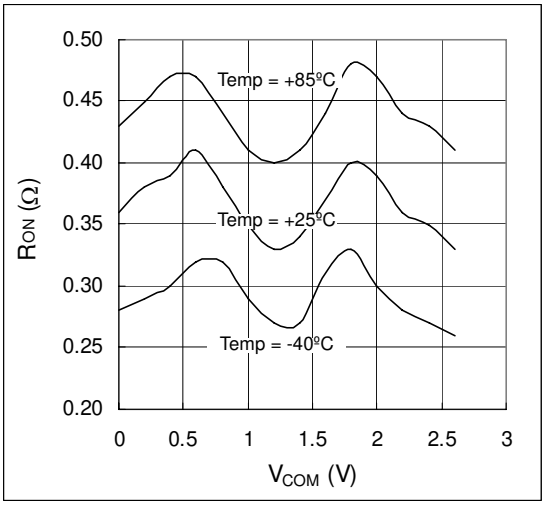


Figure 9. RON vs. VCOM

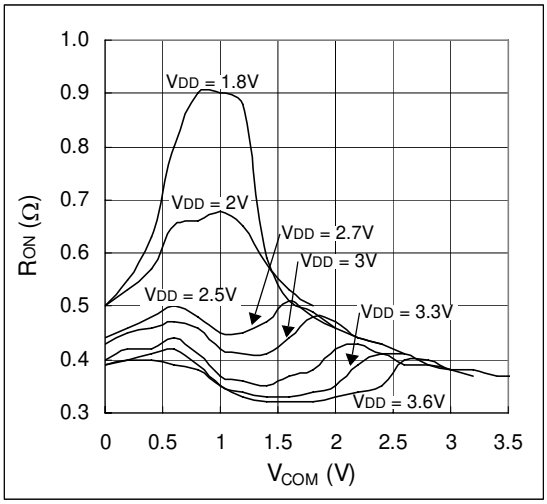
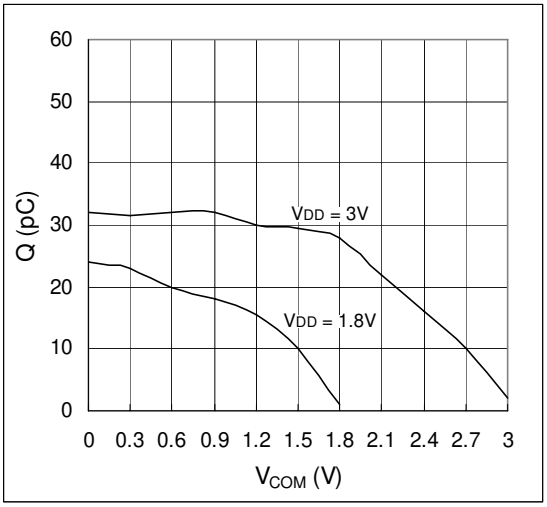


Figure 10. Charge Injection vs. VCOM



8 Detailed Description

The AS1751/AS1752/AS1753 are low ON-resistance, low-voltage, quad analog SPST switches that operate from a single +1.6 to +3.6V supply.

CMOS process technology allows switching of analog signals that are within the supply voltage range (GND to V+).

Figure 11. 16-pin TQFN Block Diagrams

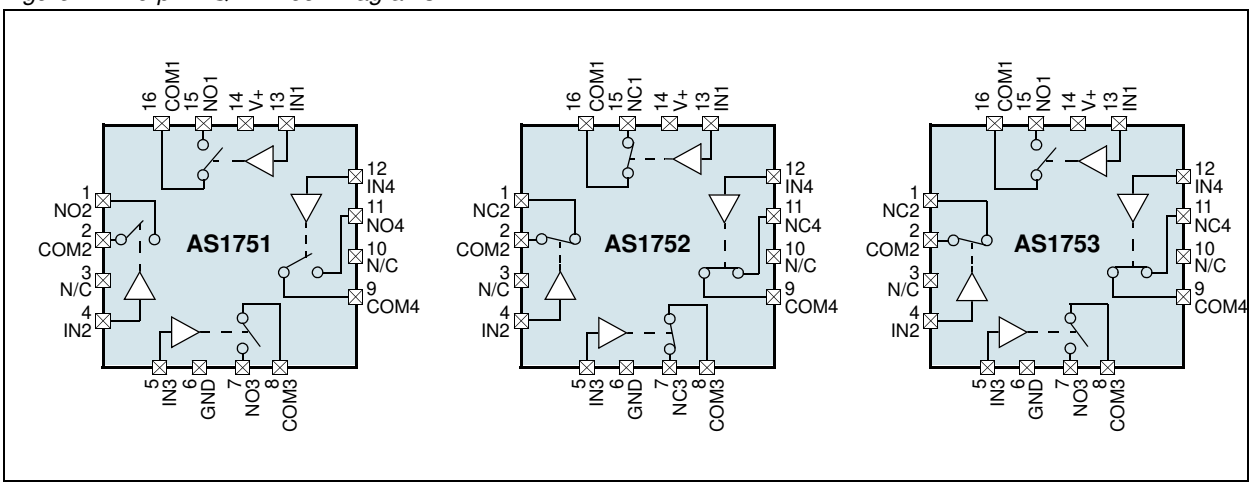


Table 6. Truth Tables

Device	Input	Switch State	
AS1751	Low	Off	
	High	On	
AS1752	Low	On	
	High	Off	
AS1753	Low	Switches 1, 3 = Off	Switches 2, 4 = On
	High	Switches 1, 3 = On	Switches 2, 4 = Off

ON-Resistance

When powered from a +3V supply, the low (0.9Ω, max) ON-resistance allows high-speed, continuous signals to be switched in a variety of applications.

Bi-Directional Switching

Pins NO*x*, NC*x*, and COM*x* are bi-directional, thus they can be used as inputs to- or outputs from other components.

Analog Signal Levels

Analog signals ranging over the entire supply voltage range (V+ to GND) can be switched with very little change in ON-resistance (see Typical Operating Characteristics on page 6).

Logic Inputs

The devices' logic inputs can be driven up to +3.6V regardless of the supply voltage value. For example, with a +1.8V supply, IN*x* may be driven low to GND and high to +3.6V. This allows the devices to interface with +3V systems using a supply of less than 3V.

9 Application Information

Power Supply Sequencing

Proper power-supply sequencing is critical for proper switch operation. The power supplies should be started up in the following sequence:

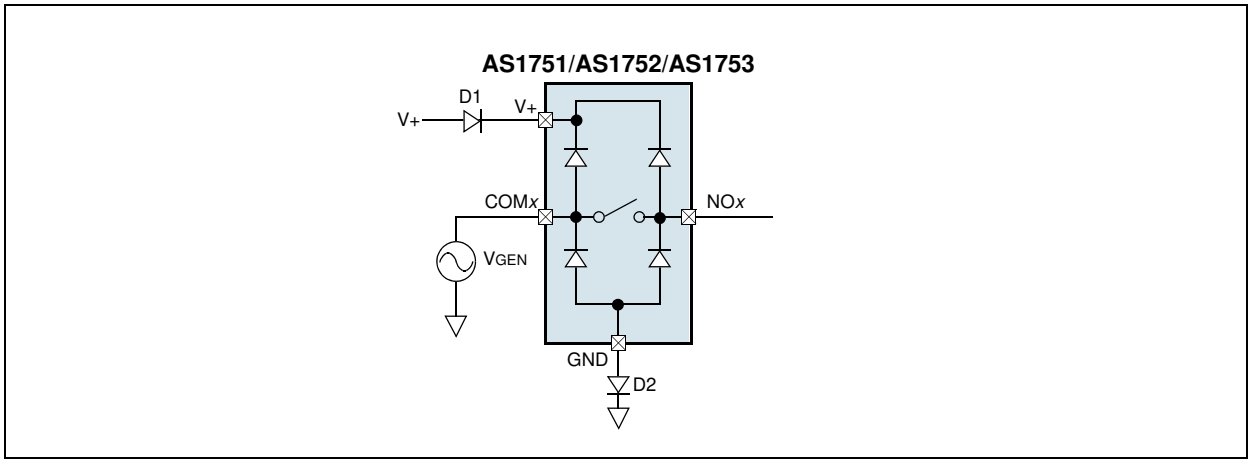
1. V+
2. NO*x*, NC*x*, COM*x*

Note: Do not exceed the absolute maximum ratings (see page 2).

Overvoltage Protection

ON-resistance increases slightly at lower supply voltages.

Figure 12. Overvoltage Protection using 2 External Blocking Diodes



Adding diode D2 to the circuit shown in Figure 12 causes the logic threshold to be shifted relative to GND. Diodes D1 and D2 also protect against overvoltage conditions.

For example, in the circuit shown in Figure 12, if the supply voltage goes below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Power Supply Bypass

Power supply connections to the devices must maintain a low impedance to ground. This can be done using a bypass capacitor, which will also improve noise margin and prevent switching noise propagation from the V+ supply to other components.

A 0.1µF bypass capacitor, connected from V+ to GND (see Figure 18 on page 11), is adequate for most applications.

Logic Inputs

Driving IN*x* Rail-to-Rail will help minimize power consumption.

Layout Considerations

High-speed switches require proper layout and design procedures for optimum performance.

- Short, wide traces should be used to reduce stray inductance and capacitance.
- Bypass capacitors should be as close to the device as possible.
- Large ground planes should be used wherever possible.

Timing Diagrams and Test Setups

Figure 13. AS1751/AS1753 Test Circuit and Timing Diagram

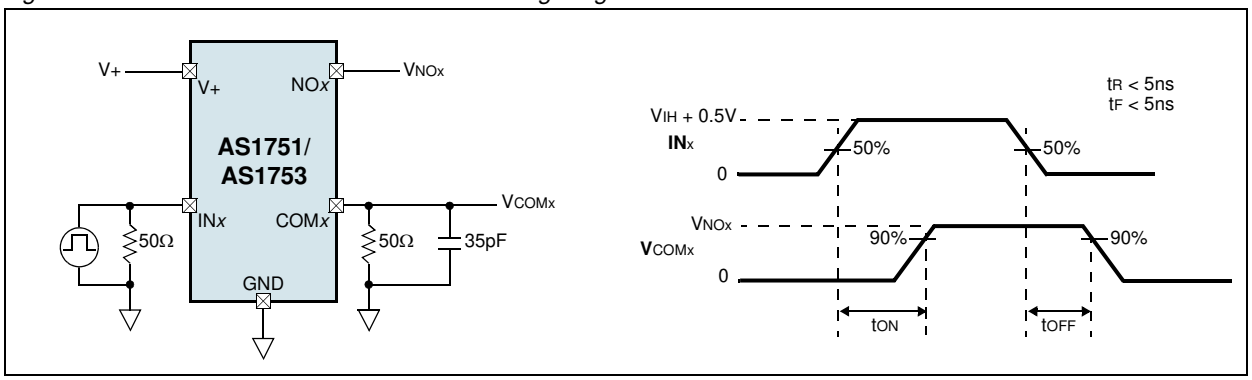


Figure 14. AS1752/AS1753 Test Circuit and Timing Diagram

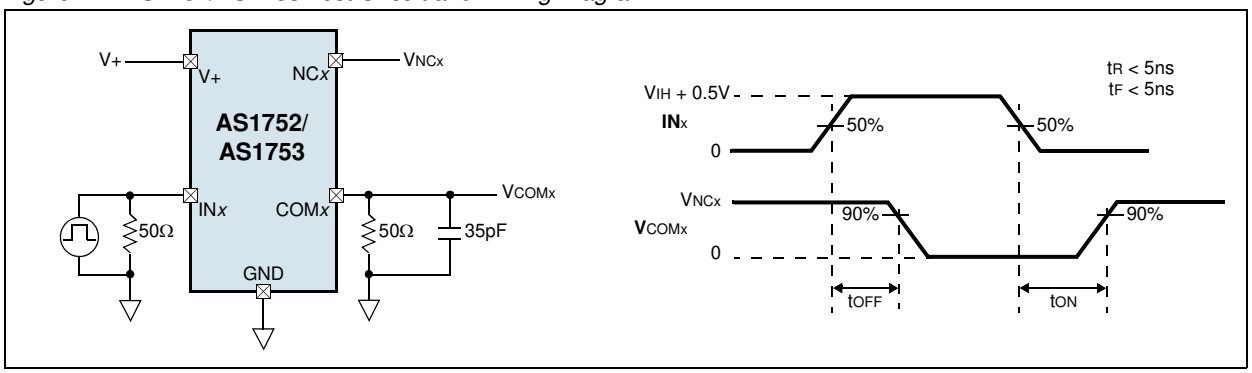


Figure 15. AS1753 Test Circuit and Timing Diagram

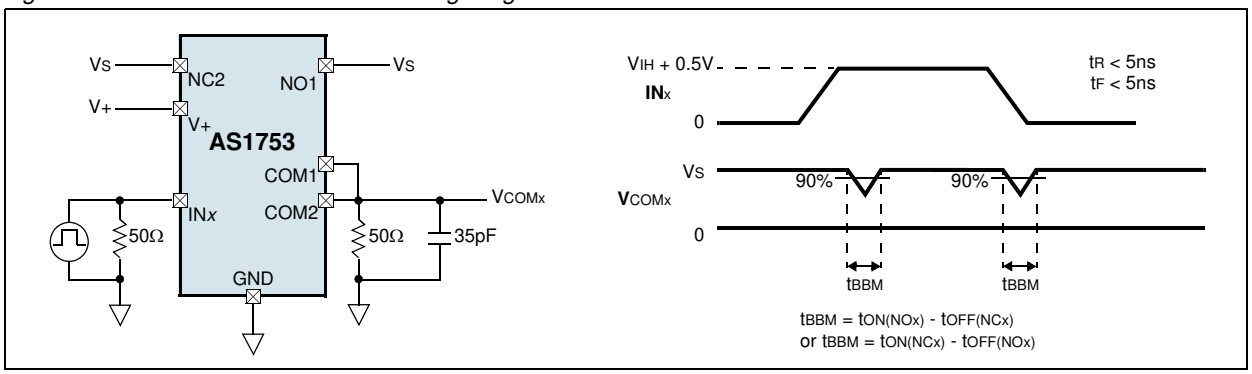


Figure 16. Charge Injection

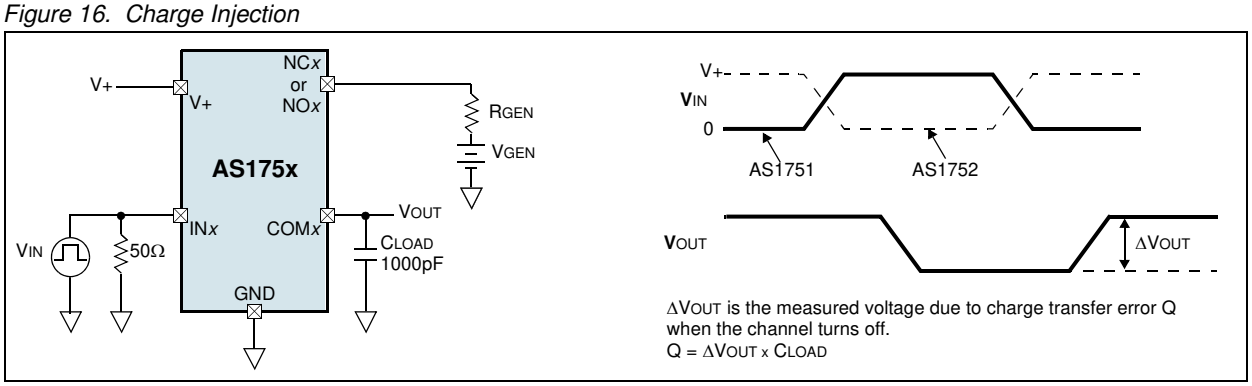


Figure 17. NOx, NCx, and COMx Capacitance

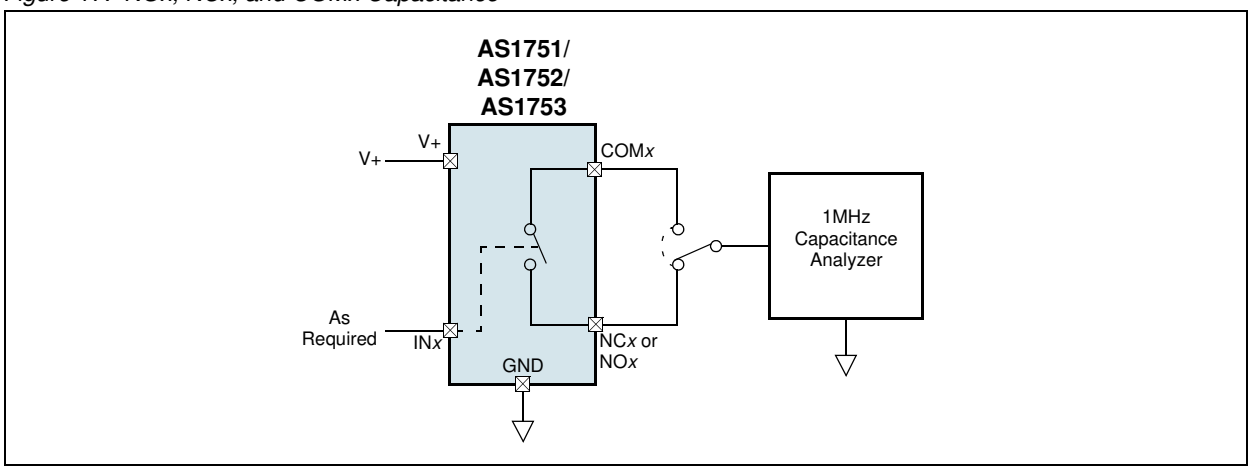
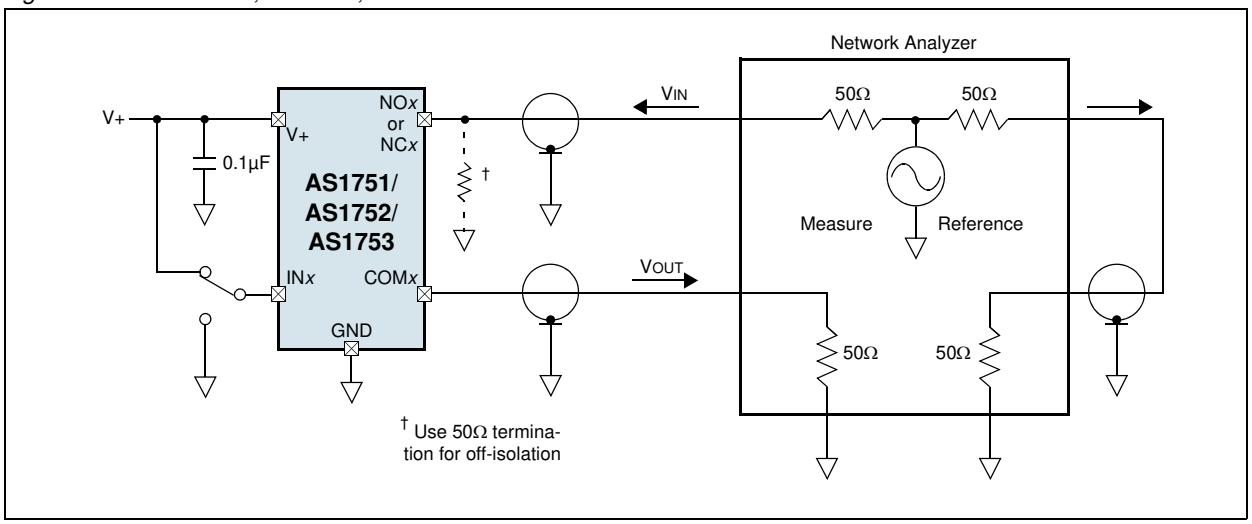


Figure 18. Off-Isolation, On-Loss, and Crosstalk



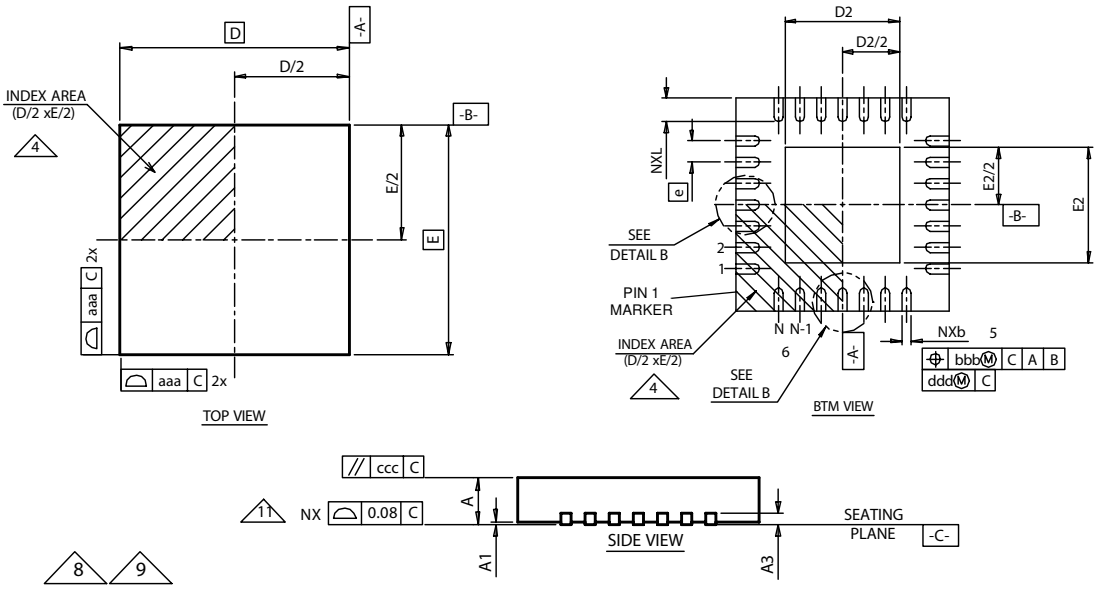
Notes:

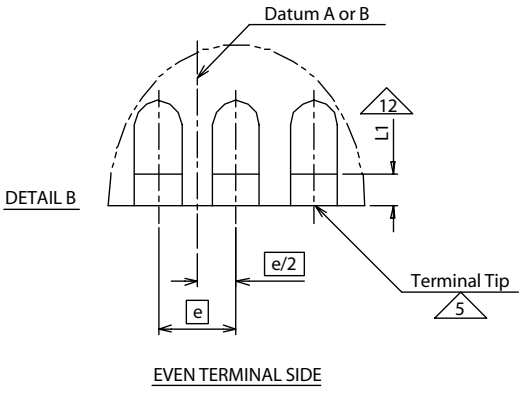
1. Measurements are standardized against short-circuit at socket terminals.
2. Off-isolation is measured between COM*x* and the off NC*x*/NO*x* terminal on each switch. Off-isolation = 20log (V_{OUT}/V_{IN}).
3. On-loss is measured between COM*x* and the on NC*x*/NO*x* terminal on each switch. On-loss = 20log (V_{OUT}/V_{IN}).
4. Signal direction through the switch is reversed; worst values are recorded.

Package Drawings and Markings

The devices are available in an 16-pin TQFN package and an 14-pin TSSOP package.

Figure 19. 16-pin TQFN Package



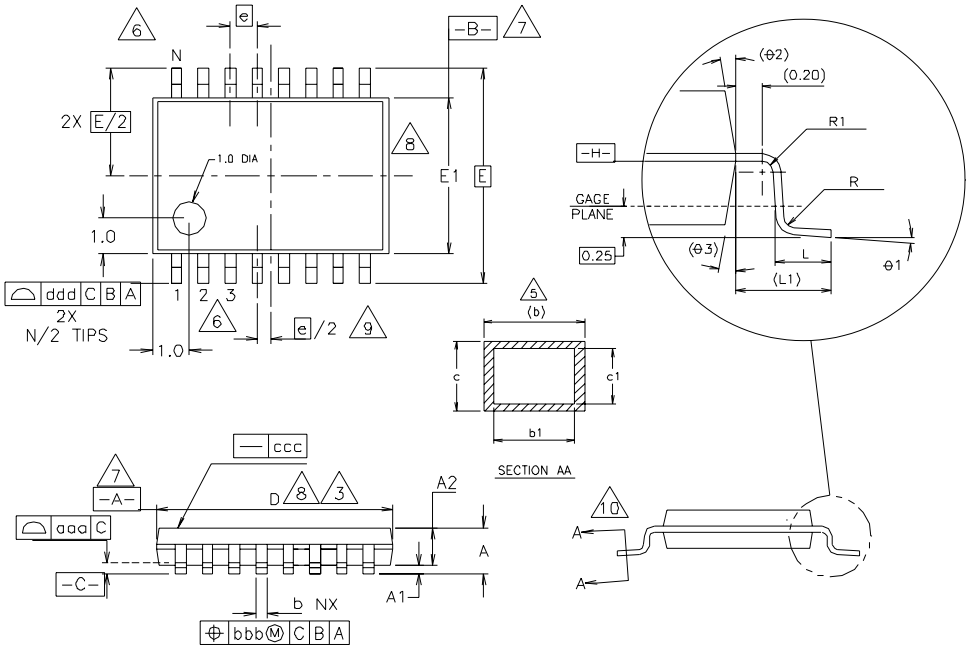


Common Dimensions				
Symbol	**Min**	**Nom**	**Max**	**Notes**
aaa		0.15		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
L1	0.03		0.15	
D BSC		3.00		1, 2, 10
E BSC		3.00		1, 2, 10
D2	1.30	1.45	1.55	1, 2, 10
E2	1.30	1.45	1.55	1, 2, 10
L	0.30	0.40	0.50	1, 2, 10
N		16		1, 2, 10
ND		4		1, 2, 10
NE		4		1, 2, 10

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters; angles in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to *JEDEC 95 SPP-012*. Details of terminal #1 identifier are optional but must be located within the zone indicated. The terminal #1 identifier may be either a mold or marked feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip. If one end of the terminal has the optional radius, the b dimension should not be measured in that radius area.
6. Dimensions ND and NE refer to the number of terminals on each D and E side, respectively.
7. Depopulation is possible in a symmetrical fashion.
8. Figure 19 is shown for illustration only and does not represent any specific variation.
9. All variations may be constructed per Figure 19, however variations may alternately be constructed between square or rectangle shape per dimensions D and E.
10. Refer to the Dimensions Table for a complete set of dimensions.
11. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
12. Depending on the method of lead termination at the edge of the package, pullback (L1) may be present. L minus L1 to be $\geq$ 0.33mm.
13. For variations with more than one lead count for a given body size and terminal pitch, each lead count for that variation is denoted by a dash number (e.g., -1 or -2).
14. NJR designates non-JEDEC registered package.

Figure 20. 14-pin TSSOP Package



Symbol	0.65mm Lead Pitch [1, 2]			Note	Symbol	0.65mm Lead Pitch [1, 2]			Note
	Min	Nom	Max			Min	Nom	Max	
A	-	-	1.10		θ1	0º	-	8º	
A1	0.05	-	0.15		L1	1.0 Ref			
A2	0.85	0.90	0.95		aaa	0.10			
L	0.50	0.60	0.75		bbb	0.10			
R	0.09	-	-		ccc	0.05			
R1	0.09	-	-		ddd	0.20			
b	0.19	-	0.30	5	e	0.65 BSC			
b1	0.19	0.22	0.25		θ2	12º Ref			
c	0.09	-	0.20		θ3	12º Ref			
c1	0.09	-	0.16						
Variations									
D	4.90	5.00	5.10	3, 8	e	0.65 BSC			
E1	4.30	4.40	4.50	4, 8	N	14			6
E	6.4 BSC								

Notes:

1. All dimensions are in millimeters; angles in degrees.
2. Dimensions and tolerancing per *ASME Y14.5M-1994*.
3. Dimension D does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per side.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of dimension b at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
6. Terminal numbers shown are for reference only.
7. Datums A and B to be determined at datum plane H.
8. Dimensions D and E1 to be determined at datum plane H.
9. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per package, the center lead must be coincident with the package centerline, datum A.
10. Cross section A-A to be determined at 0.10 to 0.25mm from the leadtip.

10 Ordering Information

The devices are available as the standard products shown in Table 7.

Table 7. Ordering Information

Model	Description	Delivery Form	Package
AS1751S	SPST Switch	Tube	14-TSSOP
AS1751S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1751V †	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1751V-T †	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm
AS1752S	Quad SPST Switch	Tube	14-TSSOP
AS1752S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1752V †	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1752V-T †	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm
AS1753S	Quad SPST Switch	Tube	14-TSSOP
AS1753S-T	Quad SPST Switch	Tape and Reel	14-TSSOP
AS1753V †	Quad SPST Switch	Tray	16-TQFN 3mmx3mm
AS1753V-T †	Quad SPST Switch	Tape and Reel	16-TQFN 3mmx3mm

† Future Product

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