

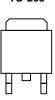
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RoHS

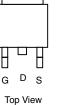
COMPLIANT

N-Channel 75 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
75	0.007 at V _{GS} = 10 V	110 ^d	69



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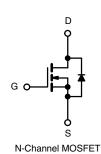


FEATURES

- TrenchFET[®] Power MOSFETS
- 100 % $\rm R_g$ and UIS Tested Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

• Synchronous Rectification



Ordering Information: SUM110N08-07P-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS	G (T _C = 25 °C, unless ot	herwise noted)			
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	75	V	
Gate-Source Voltage		V _{GS}	± 20	v	
Continuous Drain Current ($T_1 = 150 \ ^{\circ}C$)	T _C = 25 °C	1-	110 ^d		
Continuous Drain Current (1) = 150°C)	T _C = 70 °C	I	103	A	
Pulsed Drain Current		I _{DM}	180	7	
Avalanche Current		I _{AS}	50		
Single Avalanche Energy ^a	e Avalanche Energy ^a L = 0.1 mH		125	mJ	
Marian David Discipational	T _C = 25 °C	Р	208.3 ^b	W	
Maximum Power Dissipation ^a	T _A = 25 °C ^c	– P _D –	3.75		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)	R _{thJC}	0.6	- C/W	

Notes:

a. Duty cycle \leq 1 %.

b. See SOA curve for voltage derating.

c. When mounted on 1" square PCB (FR-4 material).

d. Package limited.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 V, I_{D} = 250 \mu A$	75			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	2.5		4.5	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 250	nA
Zero Gate Voltage Drain Current		$V_{DS} = 75 V, V_{GS} = 0 V$			1	μΑ
	I _{DSS}	V_{DS} = 75 V, V_{GS} = 0 V, T_{J} = 125 °C			50	
		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 ^{\circ}\text{C}$			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	70			Α
Drain-Source On-State Resistance ^a	Б	V _{GS} = 10 V, I _D = 20 A		0.0057	0.0070	Ω
	R _{DS(on)}	V_{GS} = 10 V, I _D = 20 A, T _J = 125 °C		0.0092	0.0112	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		43		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		4250		pF
Output Capacitance	C _{oss}			580		
Reverse Transfer Capacitance	C _{rss}			230		
Total Gate Charge ^c	Qg			69	105	nC
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 10$ V, $I_{D} = 50$ A		23		
Gate-Drain Charge ^c	Q _{gd}			21		
Gate Resistance	R _g	f = 1 MHz		1.2	2.4	Ω
Turn-On Delay Time ^c	t _{d(on)}			17	30	
Rise Time ^c	t _r	$V_{DD} = 30 \text{ V}, \text{ R}_{\text{L}} = 0.6 \Omega$ $\text{I}_{\text{D}} \cong 50 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		5	10	ns
Turn-Off Delay Time ^c	t _{d(off)}			22	40	
Fall Time ^c	t _f			6	15	
Source-Drain Diode Ratings and Cha	aracteristics T	_C = 25 °C ^b			· 1	
Continuous Current	۱ _S				110	٨
Pulsed Current	I _{SM}	1			180	A
Forward Voltage ^a	V _{SD}	$I_{F} = 20 \text{ A}, V_{GS} = 0 \text{ V}$		0.83	1.5	V
Reverse Recovery Time	t _{rr}			65	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 75 A, dI/dt = 100 A/μs		2.5	5	А
Reverse Recovery Charge	Q _{rr}			85	150	nC

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

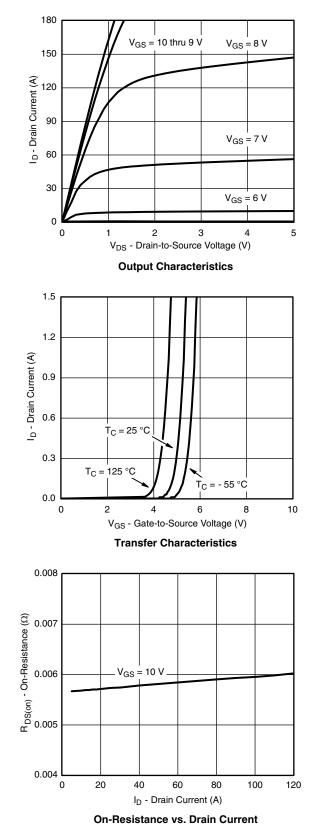
c. Independent of operating temperature.

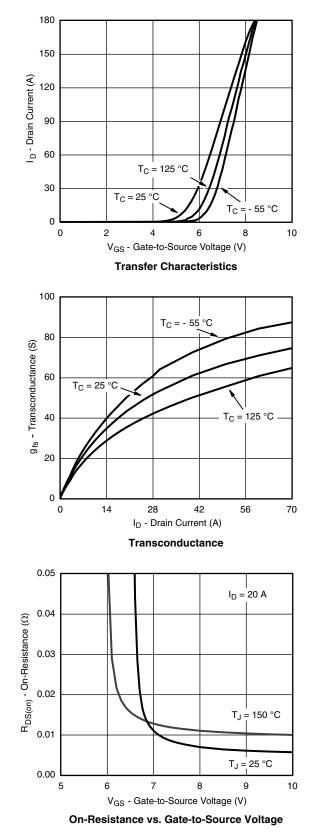
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

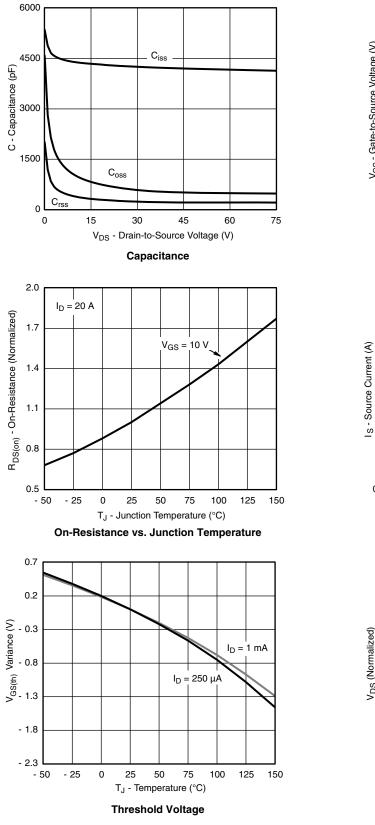


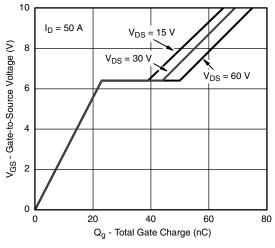


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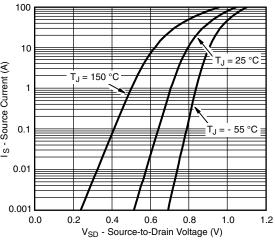
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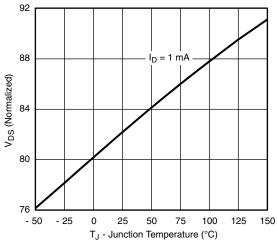


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Gate Charge



Source-Drain Diode Forward Voltage



Drain Source Breakdown vs. Junction Temperature

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For technical questions, contact: pmostechsupport@vishay.com

www.vishay.com

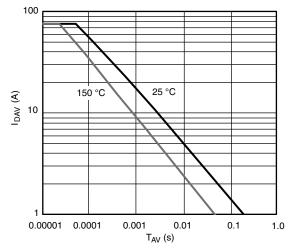
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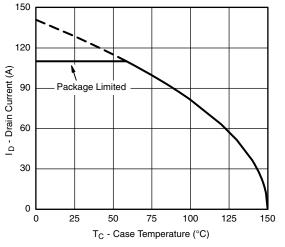


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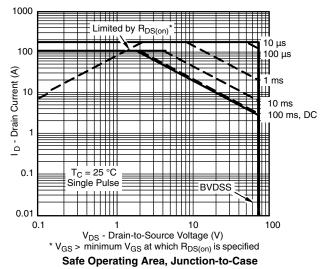
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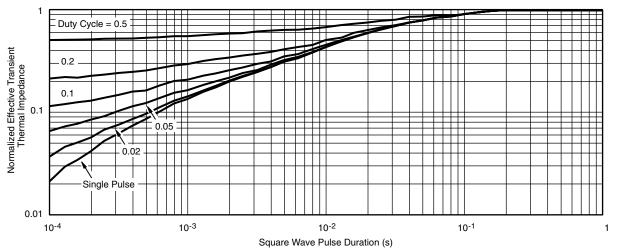
Single Pulse Avalanche Current Capability vs. Time



Current Derating*, Junction-to-Case



 * The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Case

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