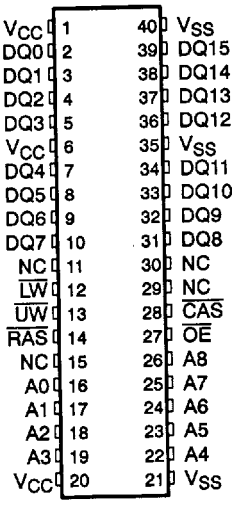
This data sheet is applicable to all TMS45165/Ps symbolized with Revision "B" and subsequent revisions as described on page 4-134.

- **Organization . . . 262144 × 16**
- **Single 5-V Supply (±10% Tolerance)**
- **Performance Ranges:**

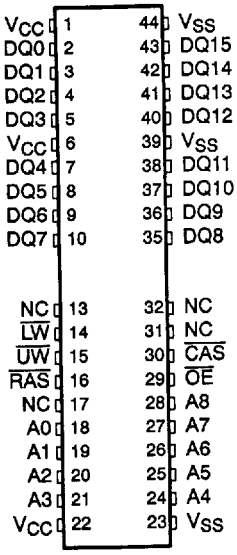
	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
'45165/P-70	70 ns	20 ns	35 ns	130 ns
'45165/P-80	80 ns	20 ns	40 ns	150 ns
'45165/P-10	100 ns	25 ns	45 ns	180 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **Long Refresh Period**
  512-Cycle Refresh in 8 ms (Max)
  64 ms for Low Power With Self-Refresh Version (TMS45165P)
- **3-State Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs, Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Low-Power With Self-Refresh**
- **Upper and Lower Byte Control During Write Operations**

DZ PACKAGE
(TOP VIEW)



DGE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ0–DQ15	Data In/Data Out
$\overline{LW}$	Lower Write Enable
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{UW}$	Upper Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

ADVANCE INFORMATION

description

The TMS45165 series are high-speed, 4194304-bit dynamic random access memories organized as 262144 words of sixteen bits each.

The TMS45165P series are high-speed, low-power with self-refresh, 4194304-bit dynamic random-access memories organized as 262144 words by sixteen bits each.

They employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at low cost. These devices feature maximum $\overline{RAS}$ access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 660 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

The TMS45165 and TMS45165P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS45165 and TMS45165P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of the last $\overline{CAS}$).

address (A0–A8)

Eighteen address bits are required to decode 1 of 262144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the TMS45165 and TMS45165P $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{UW}$, $\overline{LW}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{UW}$, $\overline{LW}$) input. $\overline{LW}$ controls DQ0–DQ7, and $\overline{UW}$ controls DQ8–DQ15. A logic high on the $\overline{UW}$ and $\overline{LW}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{UW}$ or $\overline{LW}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation with $\overline{OE}$ grounded.

NOTE: Either $\overline{UW}$ or $\overline{LW}$ can be brought low in a given write cycle and only eight data bits are written into. The user can bring both $\overline{UW}$ and $\overline{LW}$ low at the same time and all 16 data bits are written into.

data in (DQ0–DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$, $\overline{UW}$, or $\overline{LW}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{UW}$ or $\overline{LW}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ is already low, the data is strobed in by $\overline{UW}$ or $\overline{LW}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines. The $\overline{LW}$ pin controls DQ0–DQ7. The $\overline{UW}$ pin controls DQ8–DQ15.

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data out (DQ0–DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

$\overline{RAS}$-only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS45165P) to retain data. This can be achieved by strobing each of the 512 rows (A0–A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR)

CBR refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 µA refresh current is available on the TMS45165P. Data integrity is maintained using CBR refresh with a period of 125 µs holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels must be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

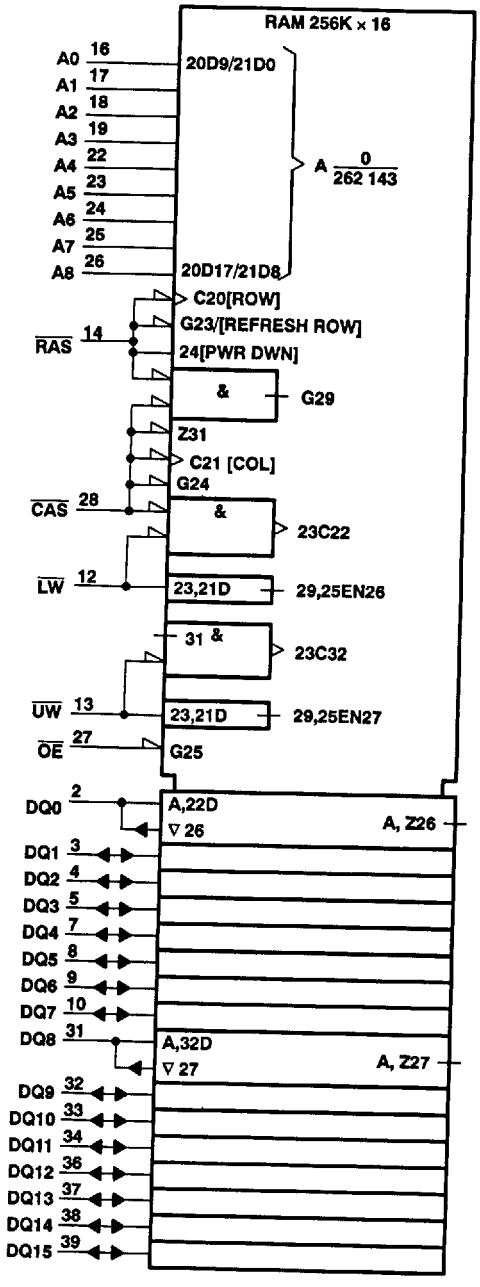
self-refresh (TMS45165P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown correspond to the DZ package.

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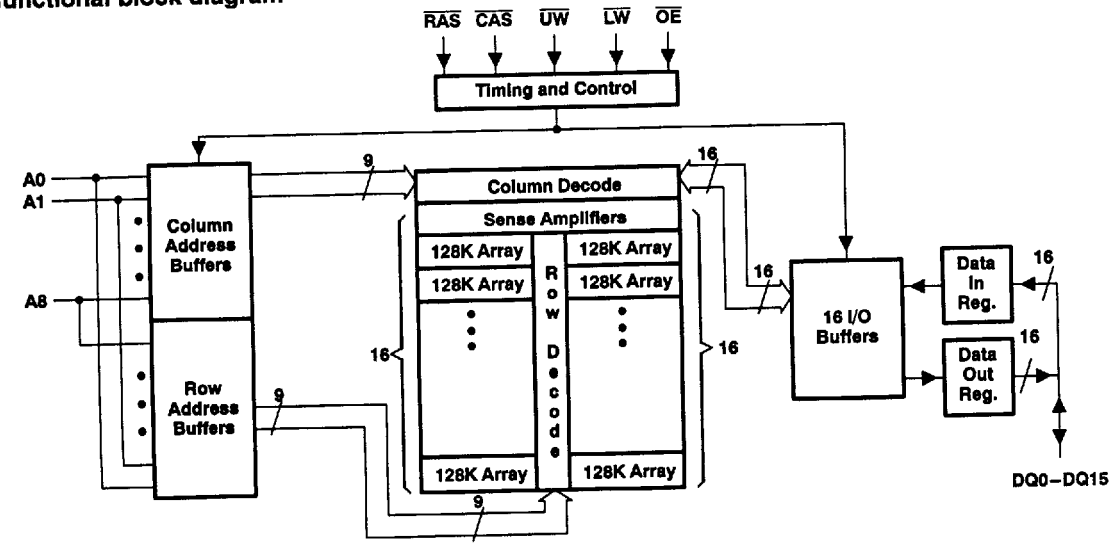
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... –1 V to 7 V
Supply voltage range on V_{CC} ..... –1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	–1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All other pins = 0 V to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			160		140		120	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS) After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'45165		1		1		1	mA
			'45165P		200		200		200	µA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, ($\overline{RAS}$ only), $\overline{RAS}$ cycling, $\overline{CAS}$ high (CBR only) $\overline{RAS}$ low after $\overline{CAS}$ low			160		140		120	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			160		140		120	mA
I_{CC5}‡	Battery backup operating current (equivalent refresh time is 64 ms) (CBR only)	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{UW}$, $\overline{LW}$ and $\overline{OE}$=V_{IH}, Address and data stable			300		300		300	µA
I_{CC6}†‡	Self refresh current	$\overline{CAS}$ < 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			200		200		200	µA

† Measured with outputs open
‡ For TMS45165P only
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A8		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_O	Output capacitance		7	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'45165-70 '46165P-70		'45165-80 '46165P-80		'45165-10 '46165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		20		20		25	ns
t_{AA}	Access time from column address		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80		100	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		20		25	ns
t_{CPA}	Access time from column precharge		40		45		50	ns
t_{CLZ}	$\overline{CAS}$ low to output in the low-impedance state	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	20	0	20	0	25	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read (see Note 8)	130		150		180		ns
t_{WC}	Cycle time, write	130		150		180		ns
t_{RWC}	Cycle time, read-modify-write	185		205		245		ns
t_{PC}	Cycle time, page-mode read or write (see Note 9)	45		50		55		ns
t_{PRWC}	Cycle time, page-mode read-modify-write	90		105		120		ns
t_{RASP}	Pulse duration, page mode, $\overline{RAS}$ low (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t_{RAS}	Pulse duration, nonpage mode, $\overline{RAS}$ low (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	20	10 000	25	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	50		60		70		ns
t_{WP}	Pulse duration, write	15		15		20		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{xW}$ low (see Note12)	0		0		0		ns
t_{RCS}	Setup time, read before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ high	20		20		25		ns
t_{RWL}	Setup time, $\overline{xW}$ low before $\overline{RAS}$ high	20		20		25		ns
t_{WCS}	Setup time, $\overline{xW}$ low before $\overline{CAS}$ low (early-write operation only)	0		0		0		ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
8. All cycle times assume t_T = 5 ns.
9. $t_{PC} > t_{CP}$ min + t_{CAS} min + $2t_T$.
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this can require additional $\overline{CAS}$ low time (t_{CAS}).
11. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this can require additional $\overline{RAS}$ low time (t_{RAS}).
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations

ADVANCE INFORMATION

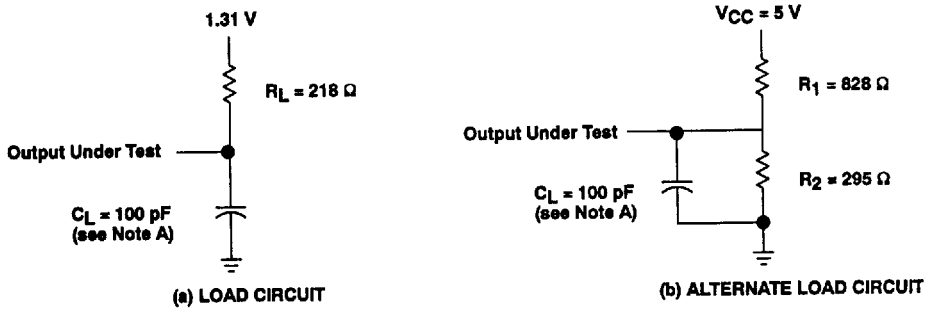
timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7) (concluded)

	PARAMETER	'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Hold time, column address after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{DHR}	Hold time, data after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low (see Note 12)	15		15		20		ns
t_{AR}	Hold time, column address after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		15		ns
t_{RCH}	Hold time, read after $\overline{CAS}$ high (see Note 14)	0		0		0		ns
t_{RRH}	Hold time, read after $\overline{RAS}$ high (see Note 14)	0		0		0		ns
t_{WCH}	Hold time, write after $\overline{CAS}$ low (early-write operation only)	15		15		20		ns
t_{WCR}	Hold time, write after $\overline{RAS}$ low (see Note 13)	35		35		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	20		20		25		ns
t_{AWD}	Delay time, column address to $\overline{xW}$ low (see Note 15)	65		70		80		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (CBR refresh only)	15		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		100		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (CBR refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{xW}$ low (see Note 16)	50		50		60		ns
t_{OED}	Delay time, $\overline{OE}$ high before data at DQ	20		20		25		ns
t_{ROH}	Delay time, $\overline{OE}$ low to $\overline{RAS}$ high	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 16)	15	35	15	40	20	55	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	35		40		45		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		45		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 16)	20	50	20	60	25	75	ns
t_{RPC}	Delay time, RAS high to CAS low (CBR refresh only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		20		25		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{xW}$ low (see Note 15)	100		110		135		ns
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	130		150		180		ns
t_{RASS}	Self-refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{REF}	Refresh time interval (TMS45165 only)		8		8		8	ms
t_{REF}	Refresh time interval, low power (TMS45165P only)		64		64		64	ms
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high	−50		−50		−50		ns
t_T	Transition time	2	50	2	50	2	50	ns

NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
12. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Read-modify-write operation only
16. Maximum value specified only to assure access time.

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

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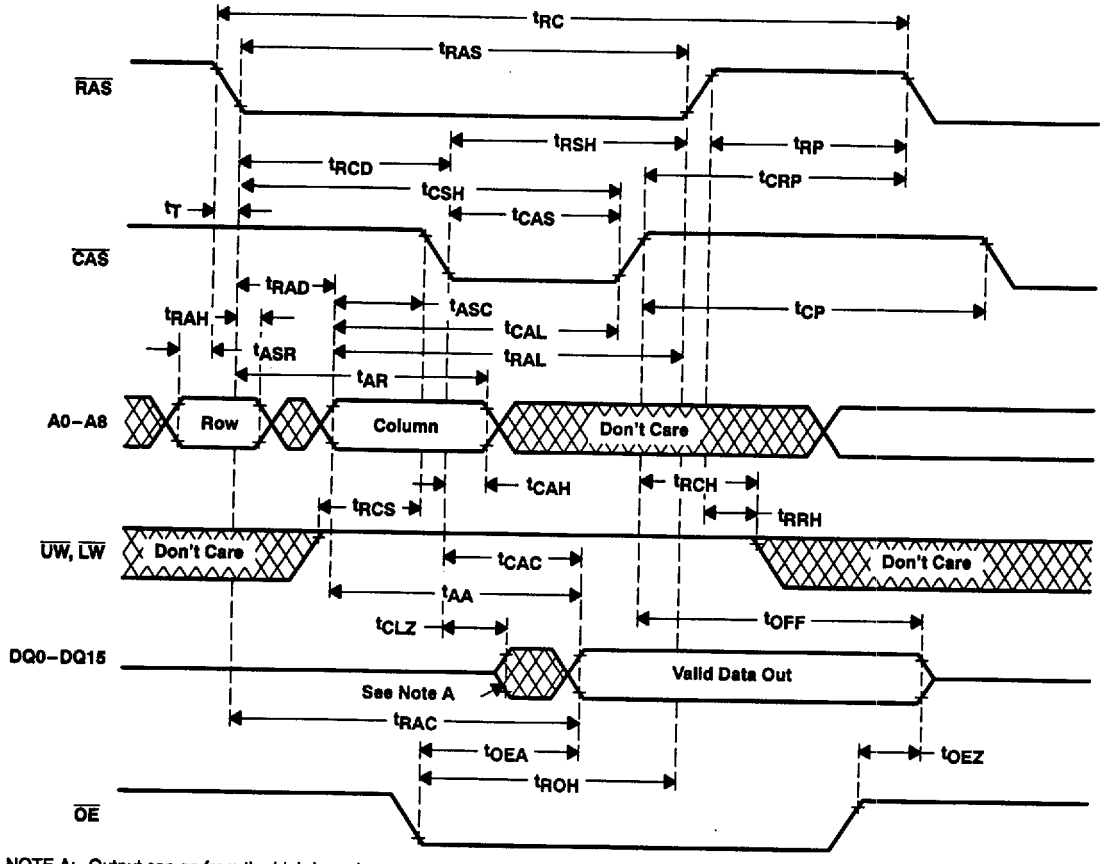
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

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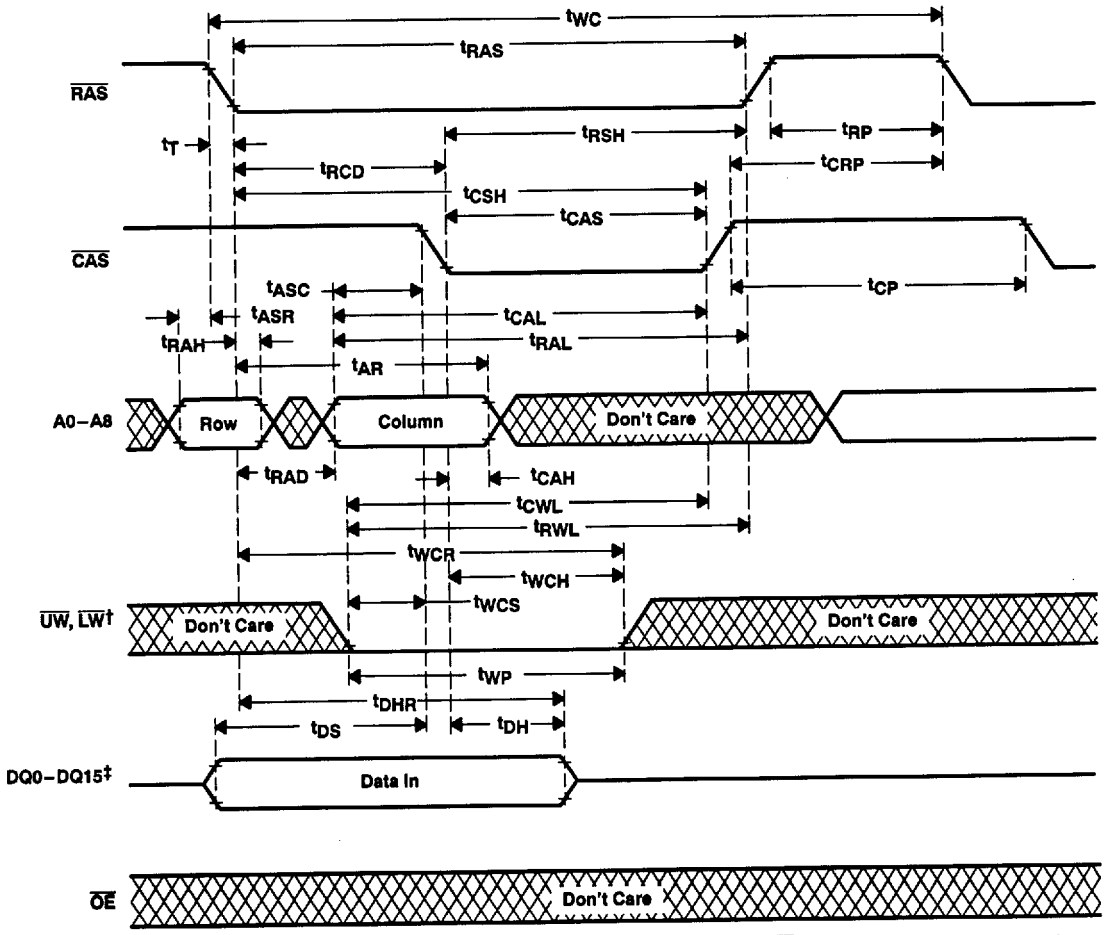
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 3. Early-Write-Cycle Timing

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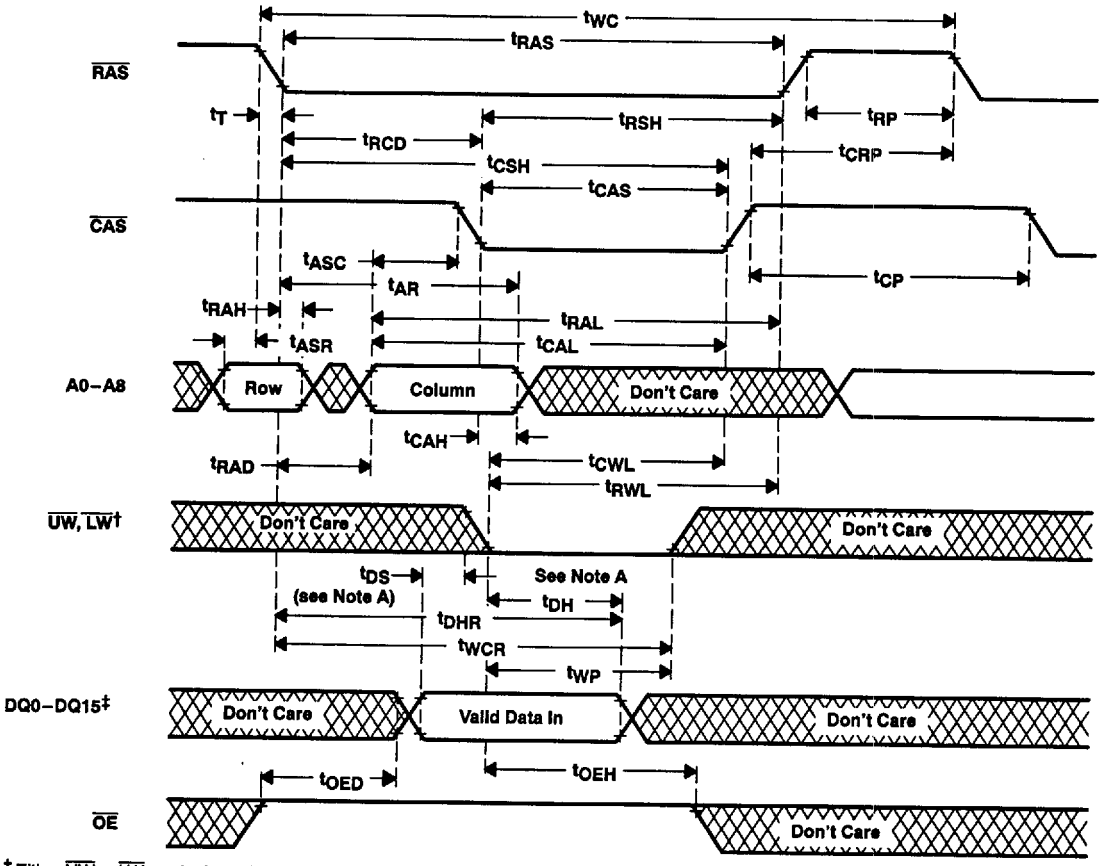
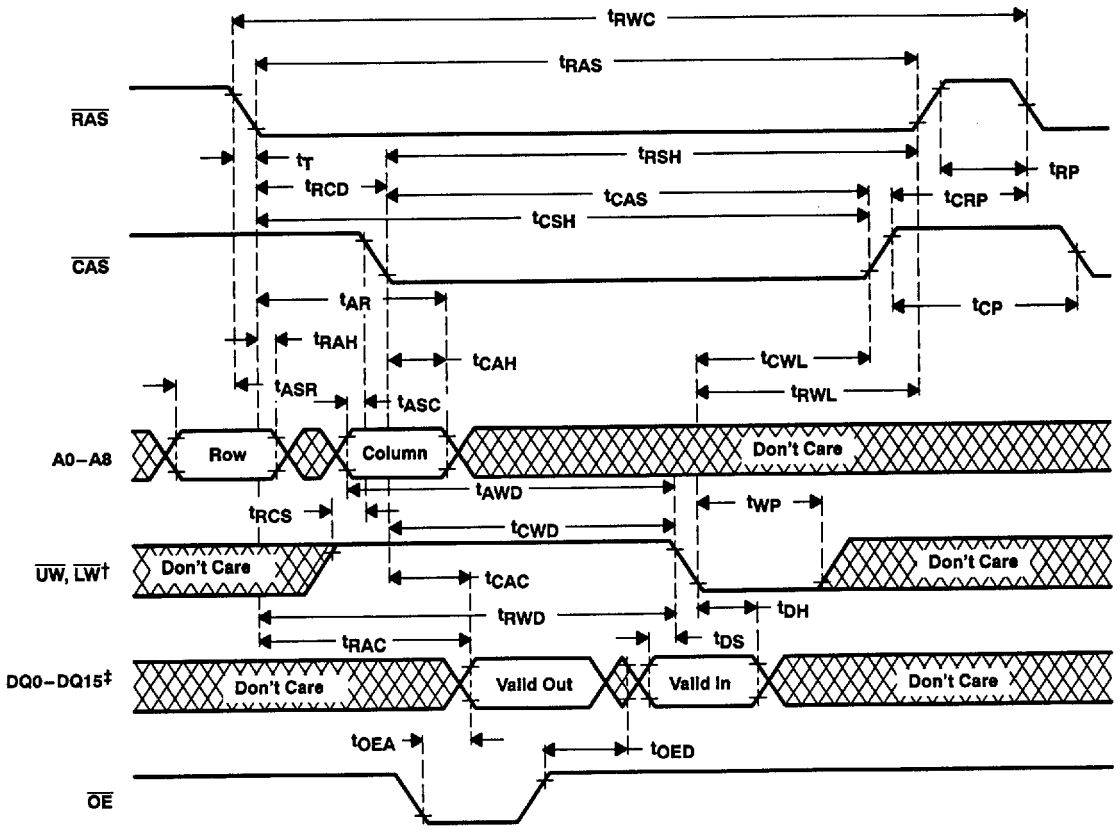
PARAMETER MEASUREMENT INFORMATION



† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state while $\overline{OE}$ is high.
NOTE A: Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.

Figure 4. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

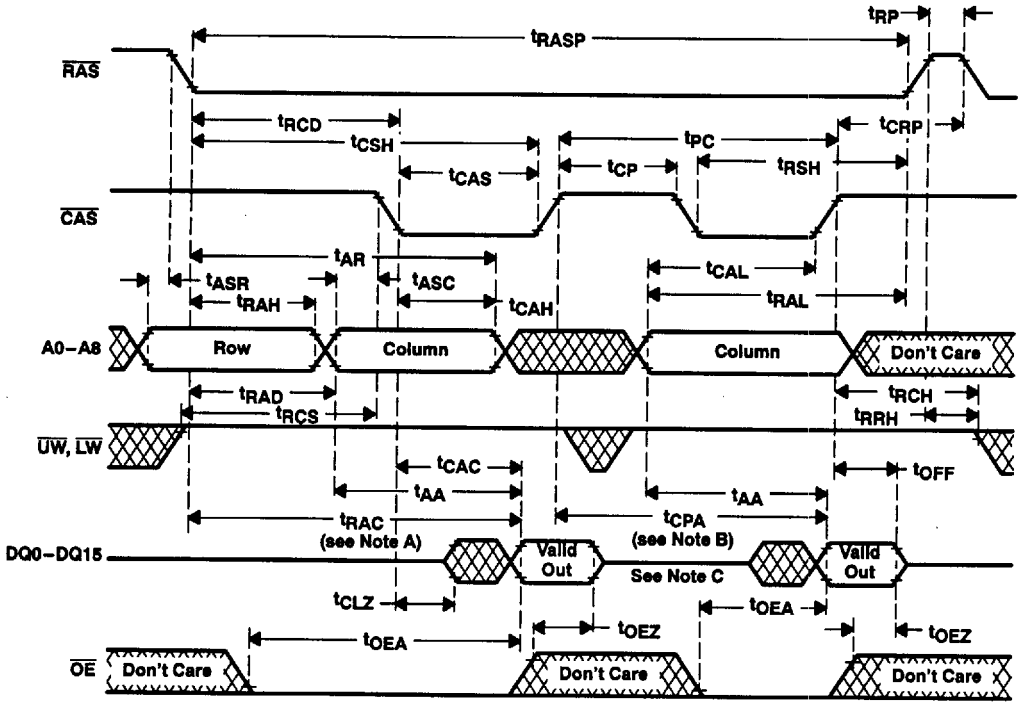


† Either $\overline{UW}$ or $\overline{LW}$ can be brought low and the user can write into eight DQ locations, or $\overline{UW}$ and $\overline{LW}$ can be brought low at the same time and all 16 DQ locations are written into.
‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 5. Read-Modify-Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

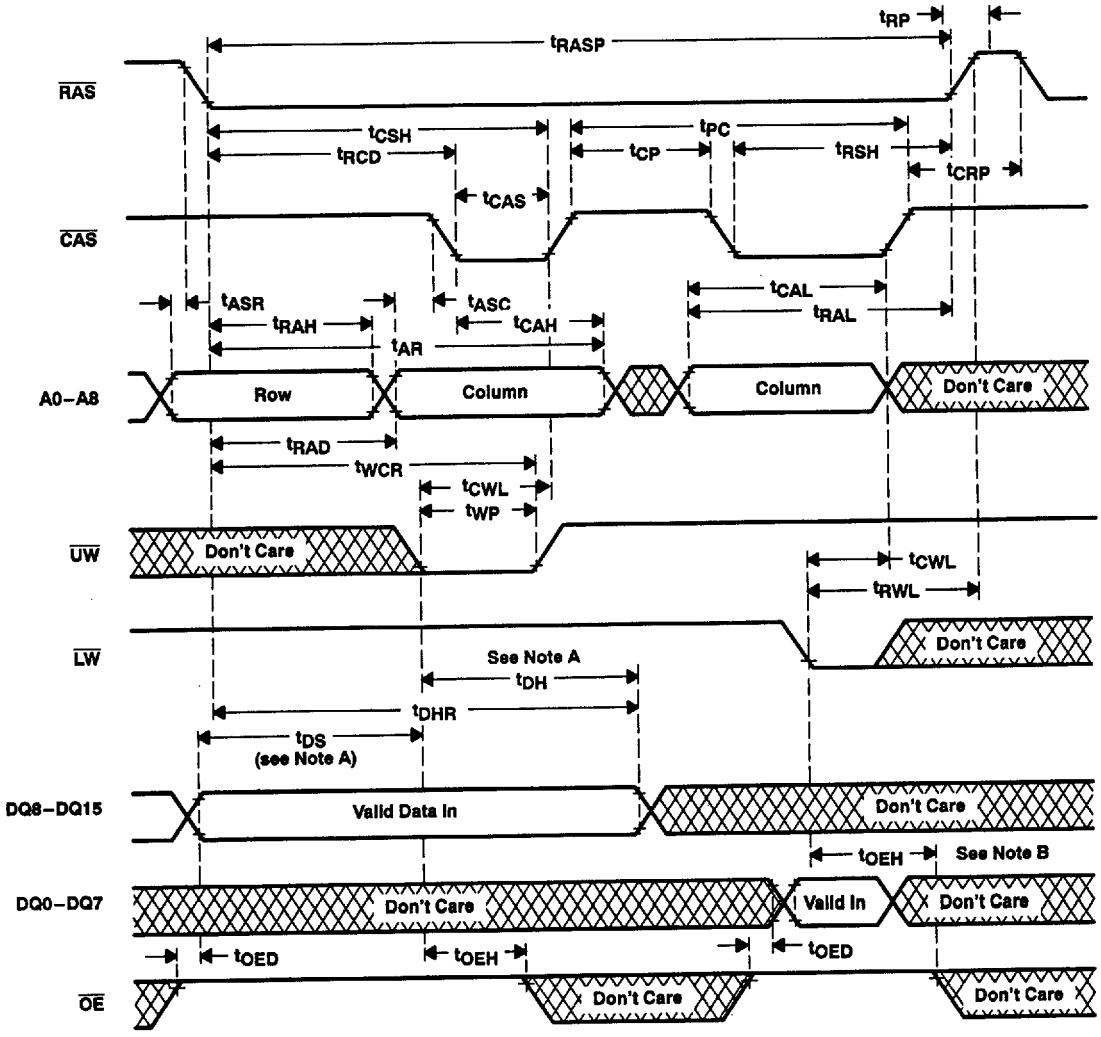


NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. Access time is t_{CPA} or t_{AA} dependent.
C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

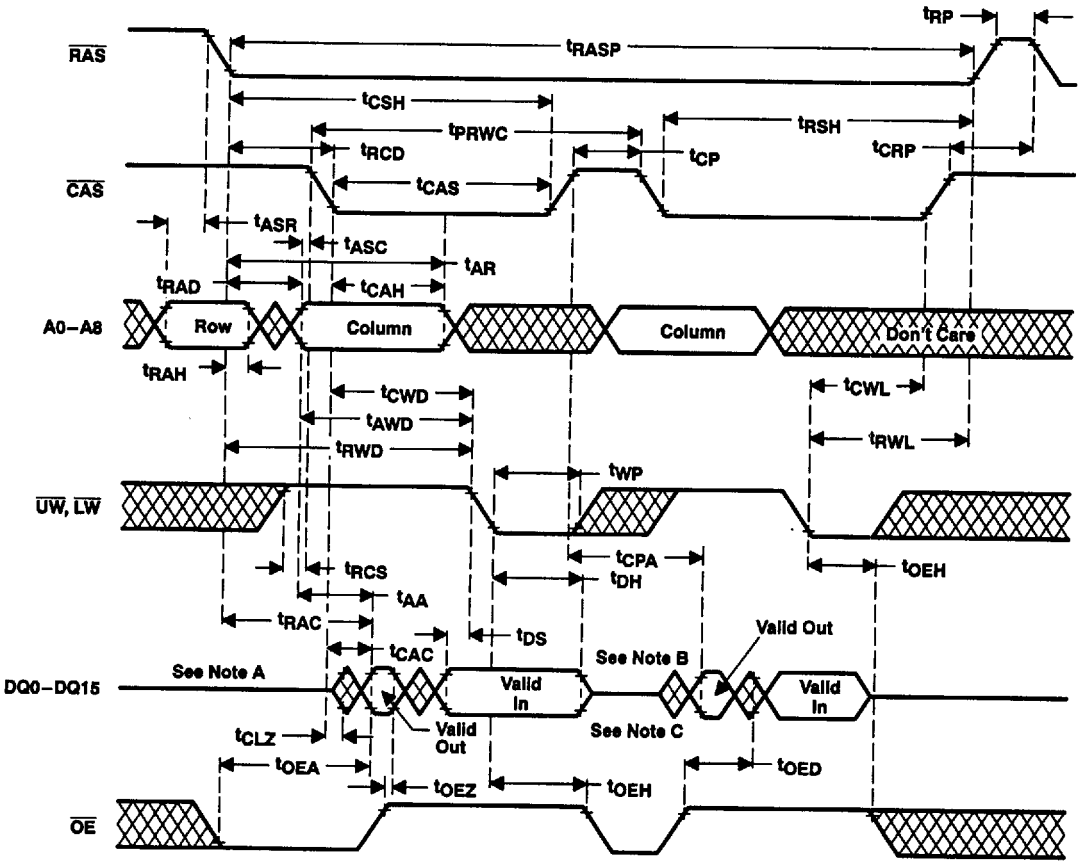


NOTES: A. Later of $\overline{CAS}$ or $\overline{xW}$ in write operations.
B. A read-cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
B. A read- or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
C. Access time is t_{CPA} or t_{AA} dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

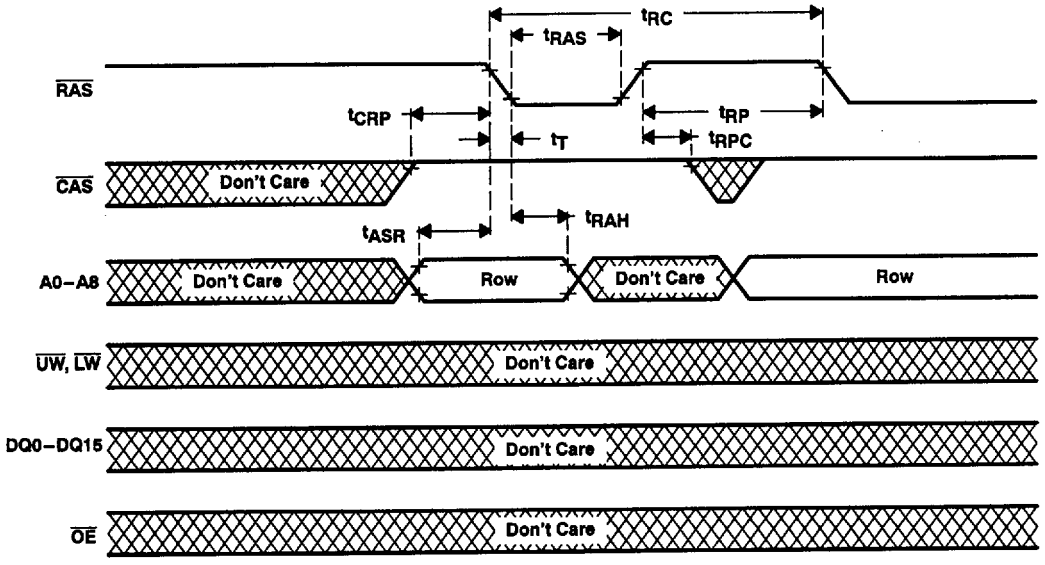


Figure 9. RAS-Only Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

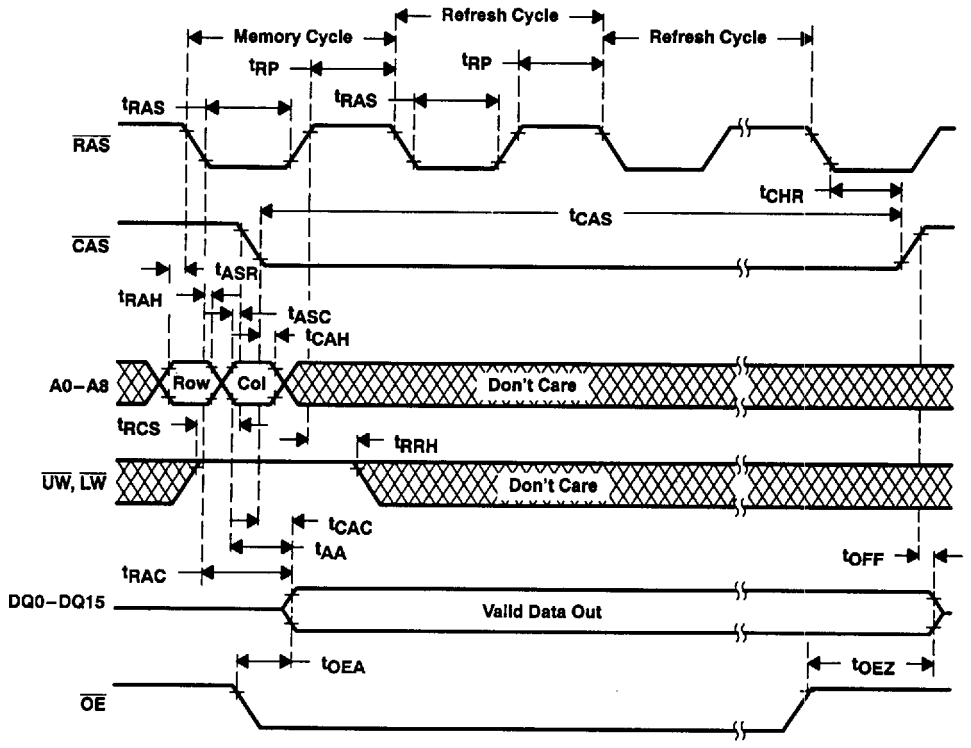
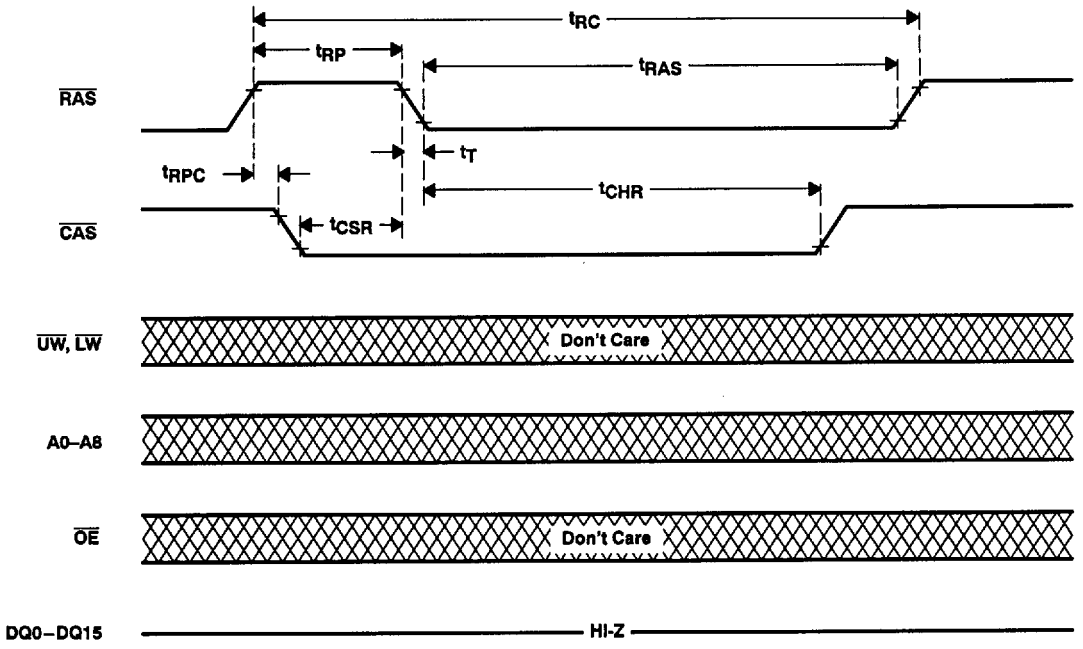


Figure 10. Hidden-Refresh-Cycle Timing

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION



NOTE A: 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic-CBR-Refresh-Cycle Timing

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PARAMETER MEASUREMENT INFORMATION

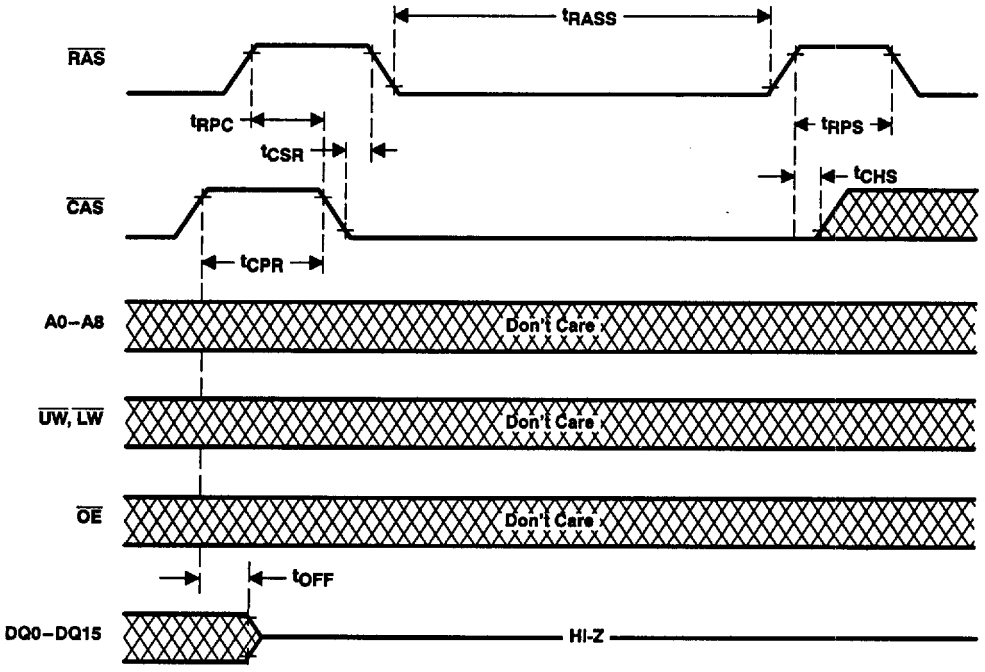
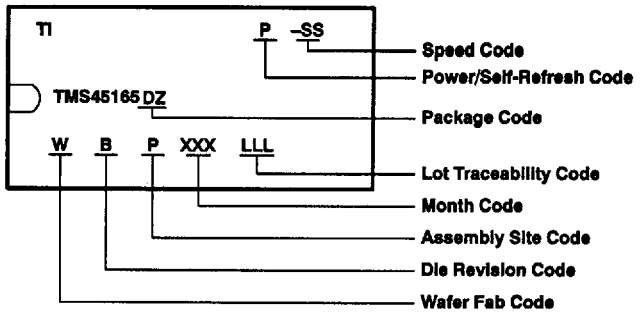


Figure 12. Self-Refresh-Cycle Timing

device symbolization



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