

MOSFET

StrongIRFET™ 2 Power-Transistor

Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

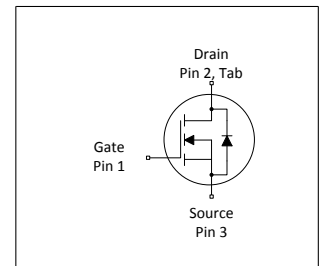
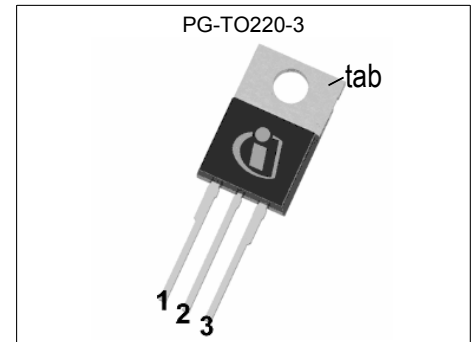


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------------|
| V_{DS} | 80 | V |
| $R_{DS(on),max}$ | 2.4 | m Ω |
| I_D | 182 | A |
| Q_{oss} | 105 | nC |
| Q_G | 89 | nC |



RoHS

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|------------|----------|---------------|
| IPP024N08NF2S | PG-TO220-3 | 024N08NS | - |

Table of Contents

| | |
|---|----|
| Description | 1 |
| Maximum ratings | 3 |
| Thermal characteristics | 3 |
| Electrical characteristics | 4 |
| Electrical characteristics diagrams | 6 |
| Package Outlines | 10 |
| Revision History | 11 |
| Trademarks | 11 |
| Disclaimer | 11 |

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------------|--------|------|-------------------------|------|--|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 182 139 128 28 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 728 | A | $T_A=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 303 | mJ | $I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 214 3.8 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$ |
| Operating and storage temperature | T_j , T_{stg} | -55 | - | 175 | °C | - |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 0.7 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾ | R_{thJA} | - | - | 40 | °C/W | - |
| Thermal resistance, junction - ambient, minimal footprint | R_{thJA} | - | - | 62 | °C/W | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------------|------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 80 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.2 | 3 | 3.8 | V | $V_{DS}=V_{GS}$, $I_D=139\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance ¹⁾ | $R_{DS(on)}$ | - | 2.1 2.6 | 2.4 3.3 | m Ω | $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$ |
| Gate resistance | R_G | - | 1.8 | - | Ω | - |
| Transconductance ²⁾ | g_{fs} | 94 | - | - | S | $ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=100\text{ A}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------------------|--------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 6200 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance | C_{oss} | - | 1000 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance | C_{rss} | - | 45 | - | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 19 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 59 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 42 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Fall time | t_f | - | 20 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |

Table 6 Gate charge characteristics³⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 29 | - | nC | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 19 | - | nC | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge | Q_{gd} | - | 19 | - | nC | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 30 | - | nC | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ²⁾ | Q_g | - | 89 | 133 | nC | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 4.7 | - | V | $V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge | Q_{oss} | - | 105 | - | nC | $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$ |

¹⁾ $R_{DS(on)}$ is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 m Ω /mm per leg.

²⁾ Defined by design. Not subject to production test.

³⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 142 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 728 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.91 | 1.2 | V | $V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$ |
| Reverse recovery time | t_{rr} | - | 39 | - | ns | $V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$ |
| Reverse recovery charge | Q_{rr} | - | 242 | - | nC | $V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$ |

4 Electrical characteristics diagrams

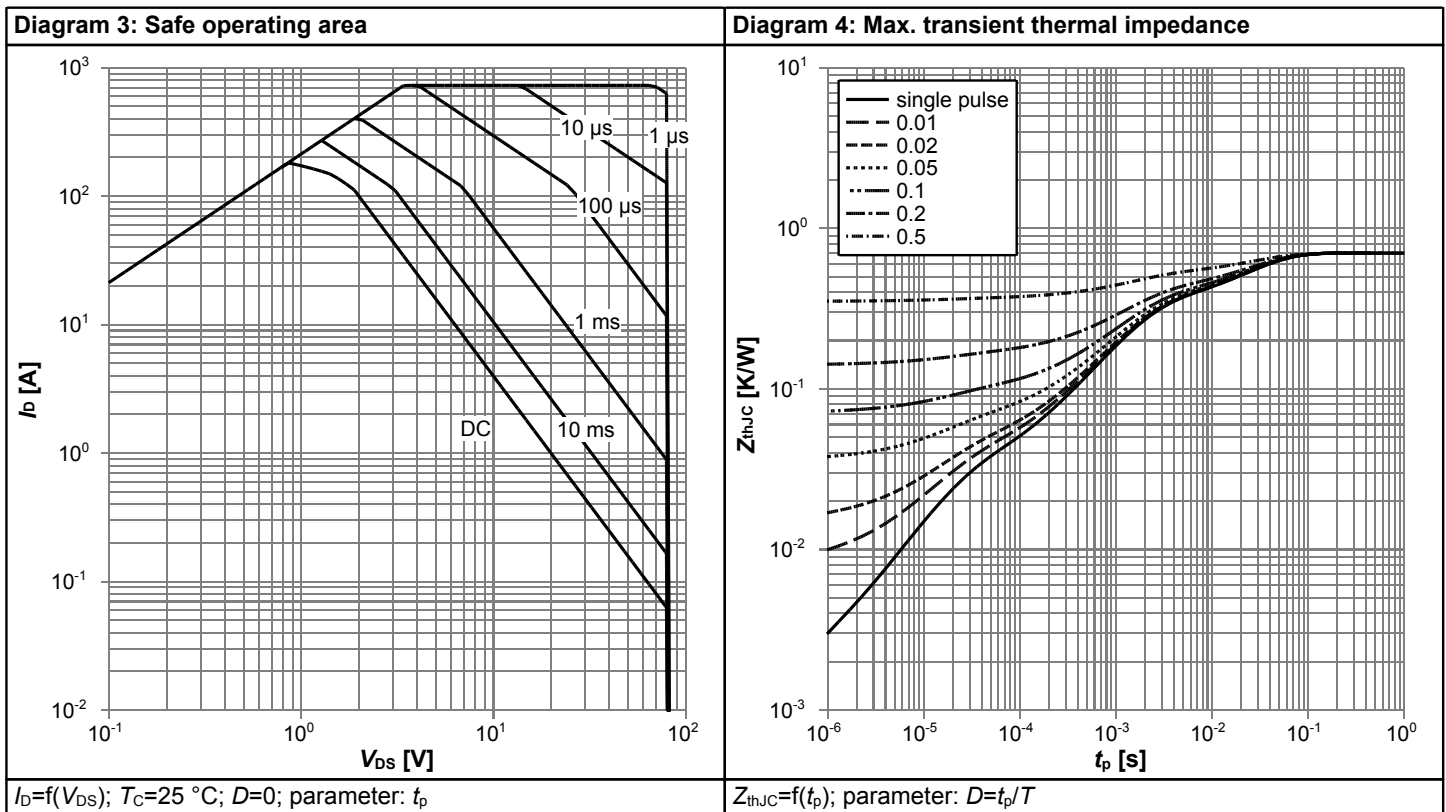
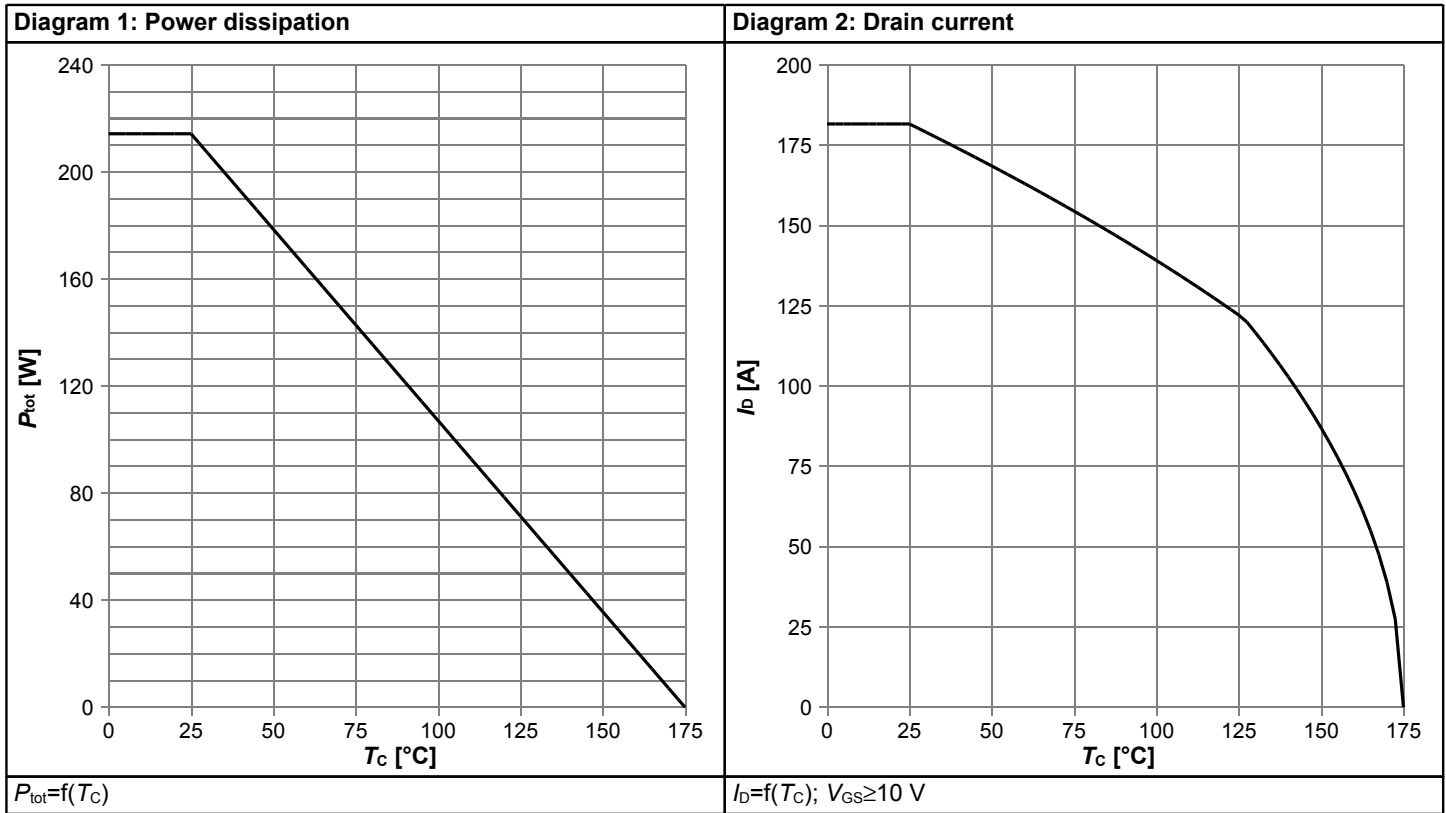
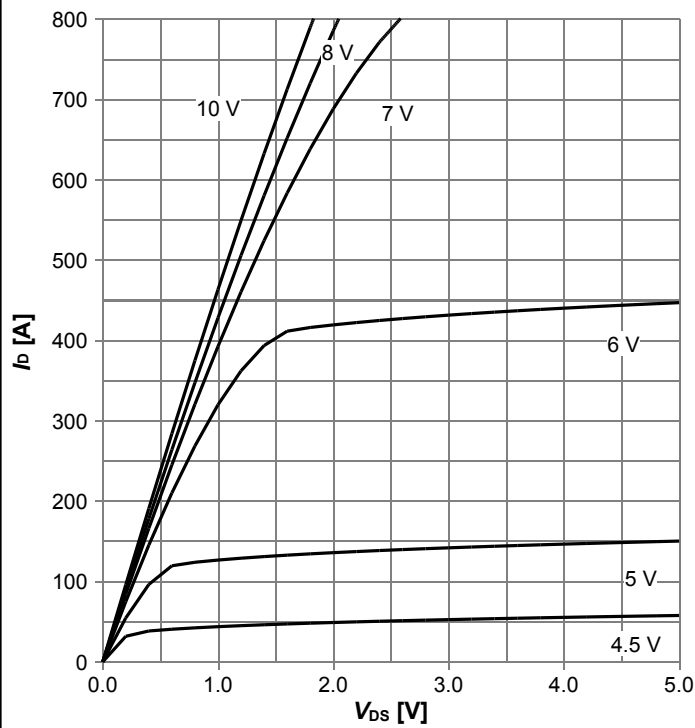
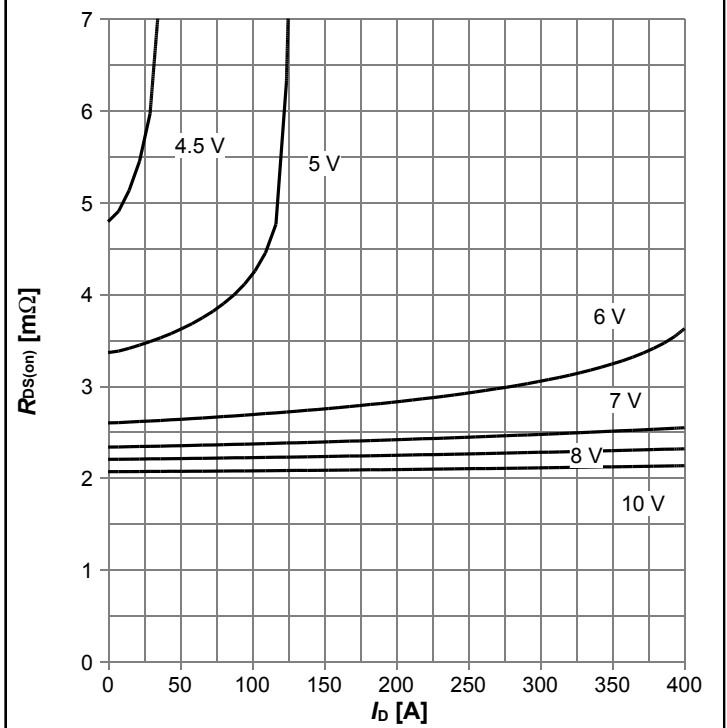


Diagram 5: Typ. output characteristics



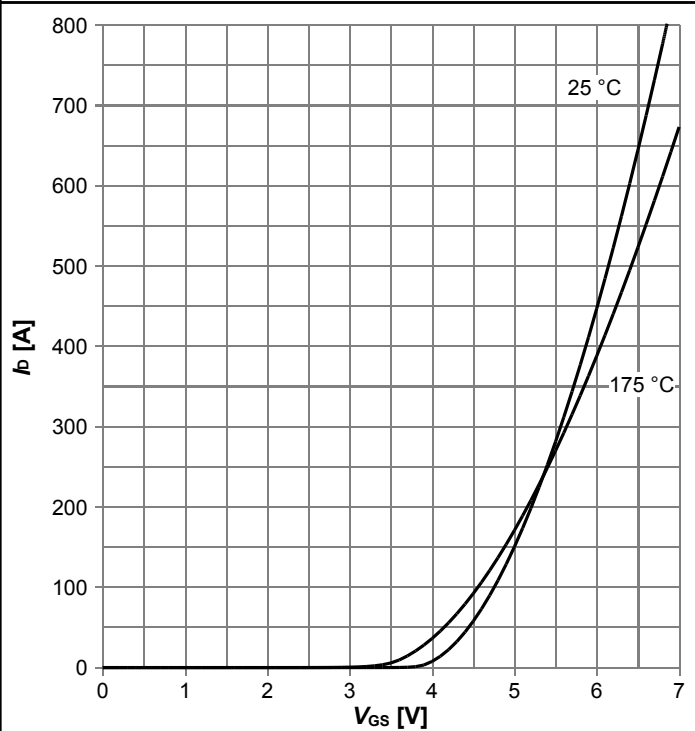
$I_D = f(V_{DS}), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



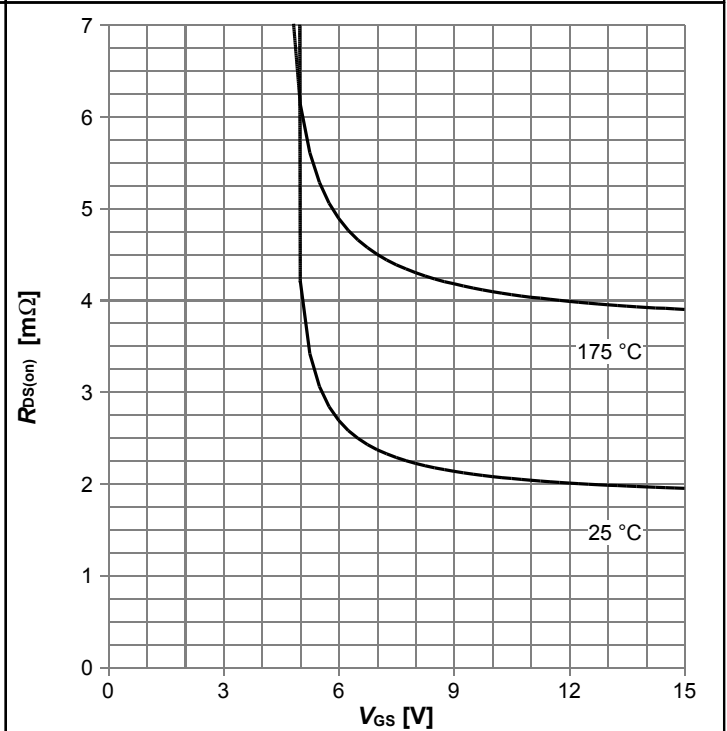
$R_{DS(on)} = f(I_D), T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



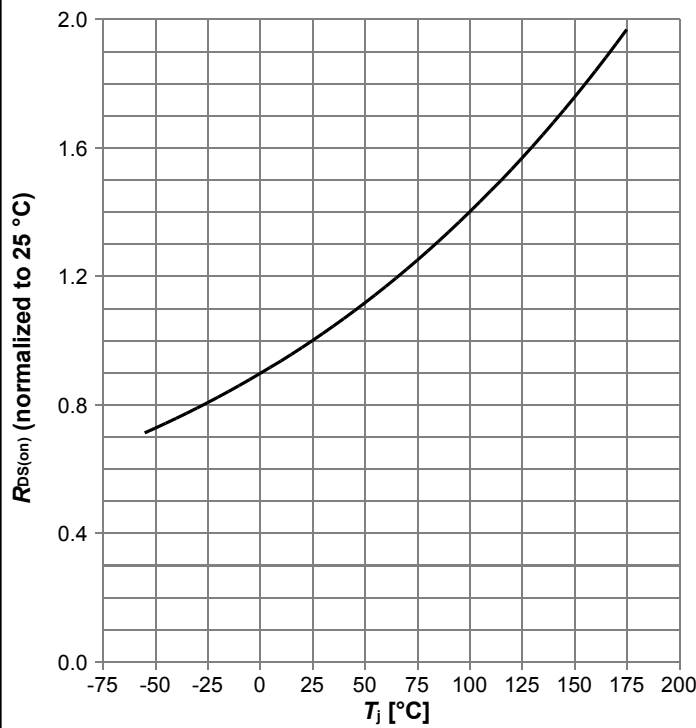
$I_D = f(V_{GS}), |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. drain-source on resistance



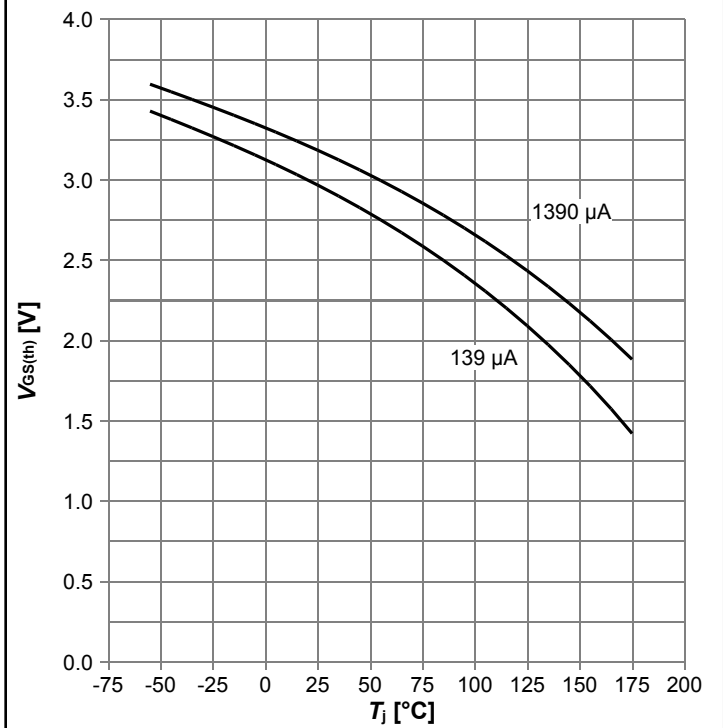
$R_{DS(on)} = f(V_{GS}), I_D = 100\text{ A};$ parameter: T_j

Diagram 9: Normalized drain-source on resistance



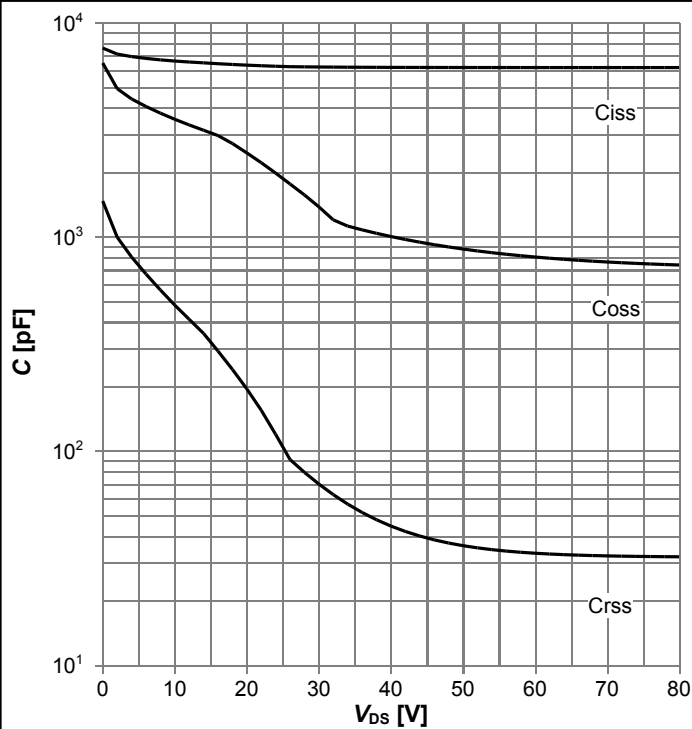
$R_{DS(on)}=f(T_j)$, $I_D=100$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



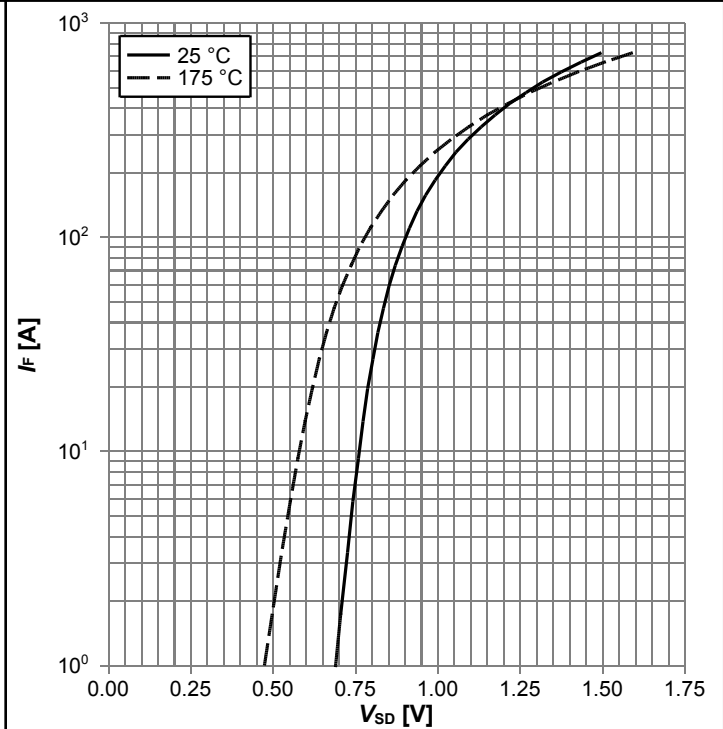
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



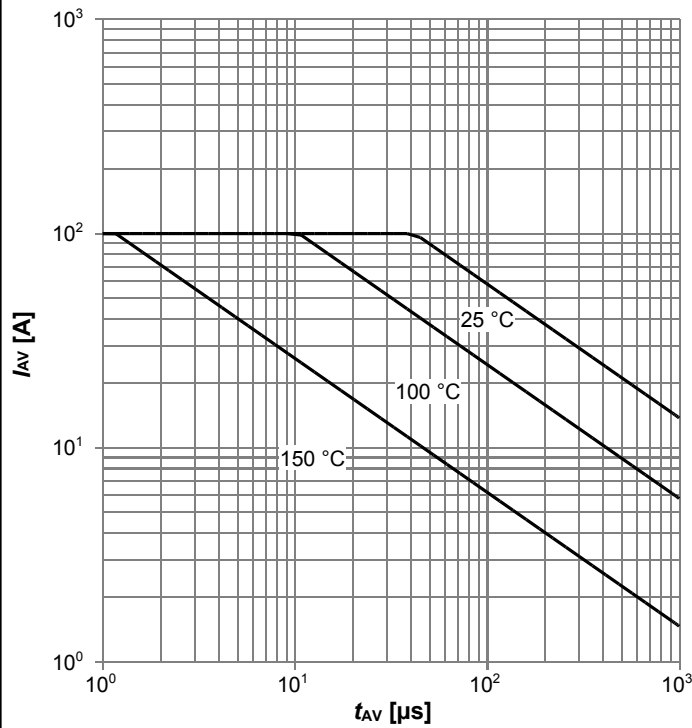
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode



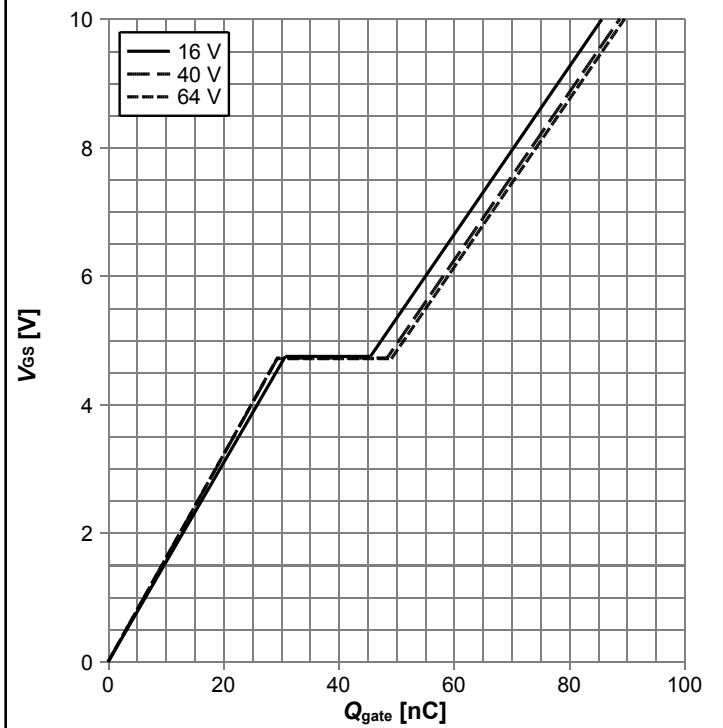
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



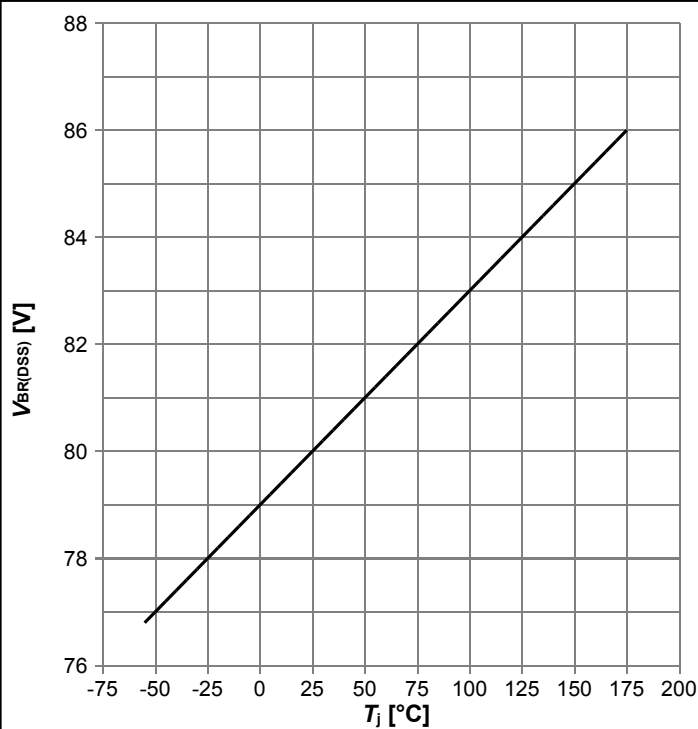
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}), I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

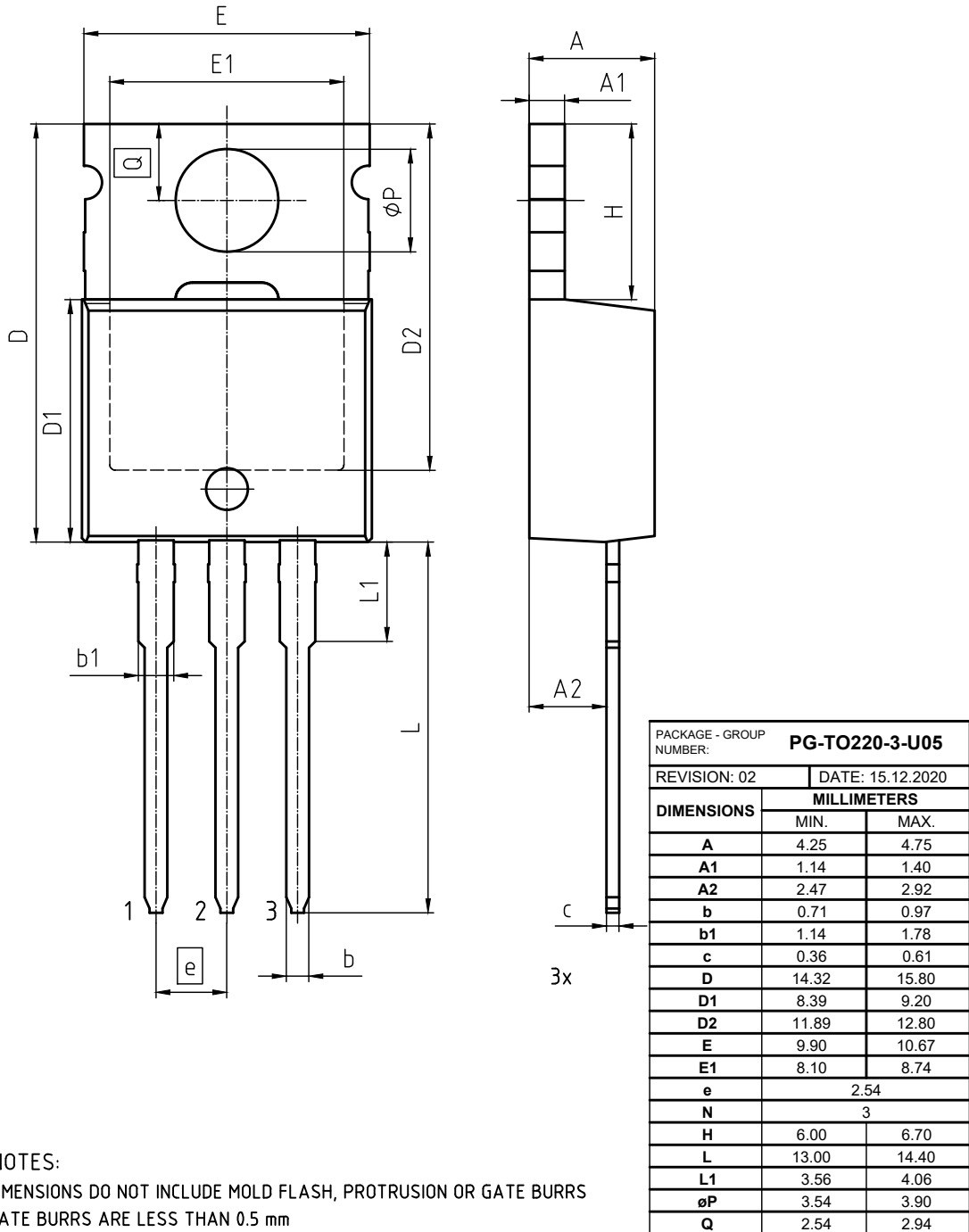


$V_{BR(DSS)}=f(T_j); I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



NOTES:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
 GATE BURRS ARE LESS THAN 0.5 mm

Figure 1 Outline PG-TO220-3, dimensions in mm

Revision History

IPP024N08NF2S

Revision: 2022-06-15, Rev. 2.1

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2020-12-18 | Release of final version |
| 2.1 | 2022-06-15 | Skip condition "Operating and storage tempt.", update trr and Qrr, footnotes and Diagram 12. |

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by

Infineon Technologies AG

81726 München, Germany

© 2022 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffungsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.