# Async/Page CellularRAM™ 1.0

## MT45W4MW16PCGA

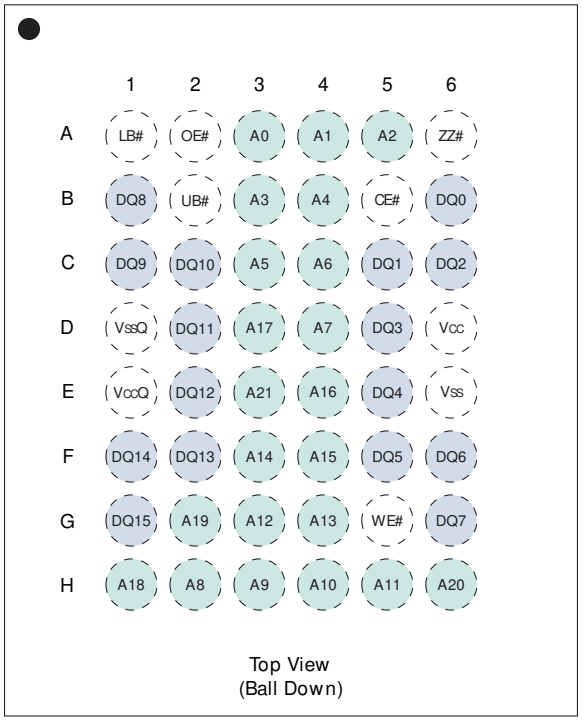
## Features

- Single device supports asynchronous and page operations
- VCC, VCCQ voltages
  - 1.7–1.95V VCC
  - 1.7–3.3V VCCQ
- Random access time: 70ns
- Page mode read access
  - Sixteen-word page size
  - Interpage read access: 70ns
  - Intrapage read access: 20ns
- Low power consumption
  - Asynchronous READ: <25mA
  - Intrapage READ: <15mA
  - Standby: <35µA (TYP at 25°C)
  - Deep power-down: <3µA (TYP)
- Low-power features
  - On-chip temperature-compensated refresh (TCR)
  - Partial-array refresh (PAR)
  - Deep power-down (DPD) mode

| Options | Designator |
|---|---|
| • Configuration | MT45W4MW16PC |
| – 4 Meg x 16 | |
| – VCC core voltage supply: 1.7–1.95V | |
| – VCCQ I/O voltage supply: 1.7–3.3V | |
| • Package | |
| – 48-ball VFBGA (green) | GA |
| • Access time | |
| – 70ns | –70 |
| • Standby power at 85°C | |
| – Standard: 140µA (MAX) | None |
| – Low-power: 120µA (MAX) | L |
| • Operating temperature range | |
| – Wireless (–30°C to +85°C) | WT[1] |
| – Industrial (–40°C to +85°C) | IT |

Notes: 1. WT of –30°C exceeds CellularRAM Workgroup 1.0 specification of –25°C.

**Figure 1: 48-Ball VFBGA Ball Assignment**




Top View
(Ball Down)

*Part Number Example:*

**MT45W4MW16PCGA-70LWT**

# General Description

Micron® CellularRAM™ products are high-speed CMOS PSRAM memory devices developed for low-power, portable applications. The MT45W4MW16PCGA is a 64Mb DRAM core device, organized as 4 Meg x 16 bits. This device includes an industry-standard asynchronous memory interface found on other low-power SRAM or PSRAM offerings.

For seamless operation on an asynchronous memory bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

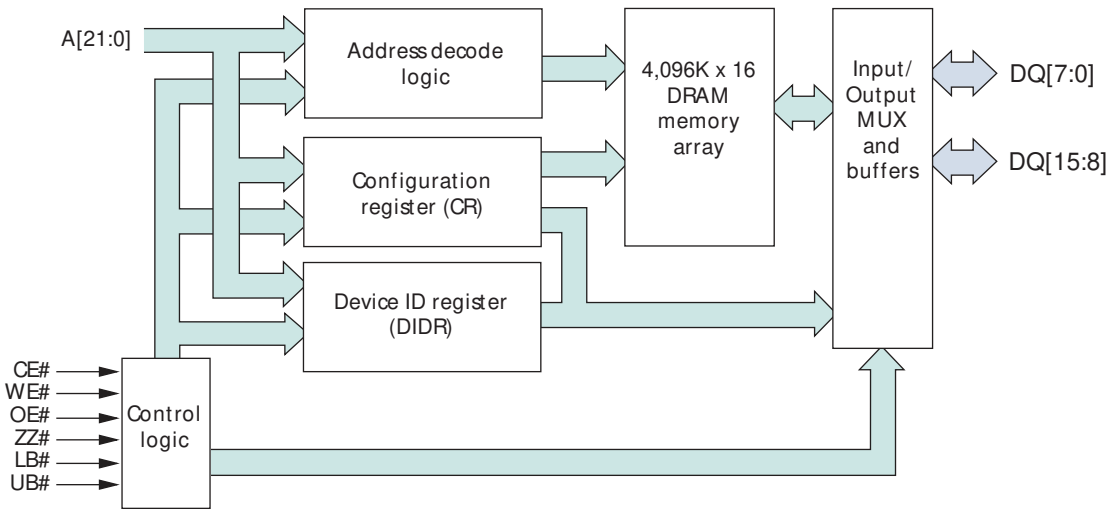
A user-accessible configuration register (CR) defines how the CellularRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current.

1. Partial-array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data.
2. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby.
3. Deep power-down (DPD) enables the system to halt the REFRESH operation altogether when no vital information is stored in the device.

This CellularRAM device is compliant with the industry-standard CellularRAM 1.0 feature set established by the CellularRAM Workgroup. The device also includes support for a device ID register.

**Figure 2: Functional Block Diagram – 4 Meg x 16**




Notes: 1. Functional block diagrams illustrate simplified device operation. For detailed information, see ball descriptions in Table 1 on page 3, bus operations in Table 2 on page 3, and timing diagrams starting on page 19.

**Table 1: VFBGA Ball Descriptions**

| VFBGA Assignment | Symbol | Type | Description |
|---|---|---|---|
| E3, H6, G2, H1, D3, E4, F4, F3, G4, G3, H5, H4, H3, H2, D4, C4, C3, B4, B3, A5, A4, A3 | A[21:0] | Input | Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the CR. |
| A6 | ZZ# | Input | Sleep enable: When ZZ# is LOW, the CR can be loaded or the device can enter one of two low-power modes (DPD or PAR). |
| B5 | CE# | Input | Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode. |
| A2 | OE# | Input | Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled. |
| G5 | WE# | Input | Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array. |
| A1 | LB# | Input | Lower byte enable: DQ[7:0]. |
| B2 | UB# | Input | Upper byte enable: DQ[15:8]. |
| G1, F1, F2, E2, D2, C2, C1, B1, G6, F6, F5, E5, D5, C6, C5, B6 | DQ[15:0] | Input/ output | Data inputs/outputs. |
| D6 | $V_{CC}$ | Supply | Device power supply: (1.7–1.95V) Power supply for device core operation. |
| E1 | $V_{CCQ}$ | Supply | I/O power supply: (1.7–3.3V) Power supply for input/output buffers. |
| E6 | $V_{SS}$ | Supply | $V_{SS}$ must be connected to ground. |
| D1 | $V_{SSQ}$ | Supply | $V_{SSQ}$ must be connected to ground. |

**Table 2: Bus Operations**

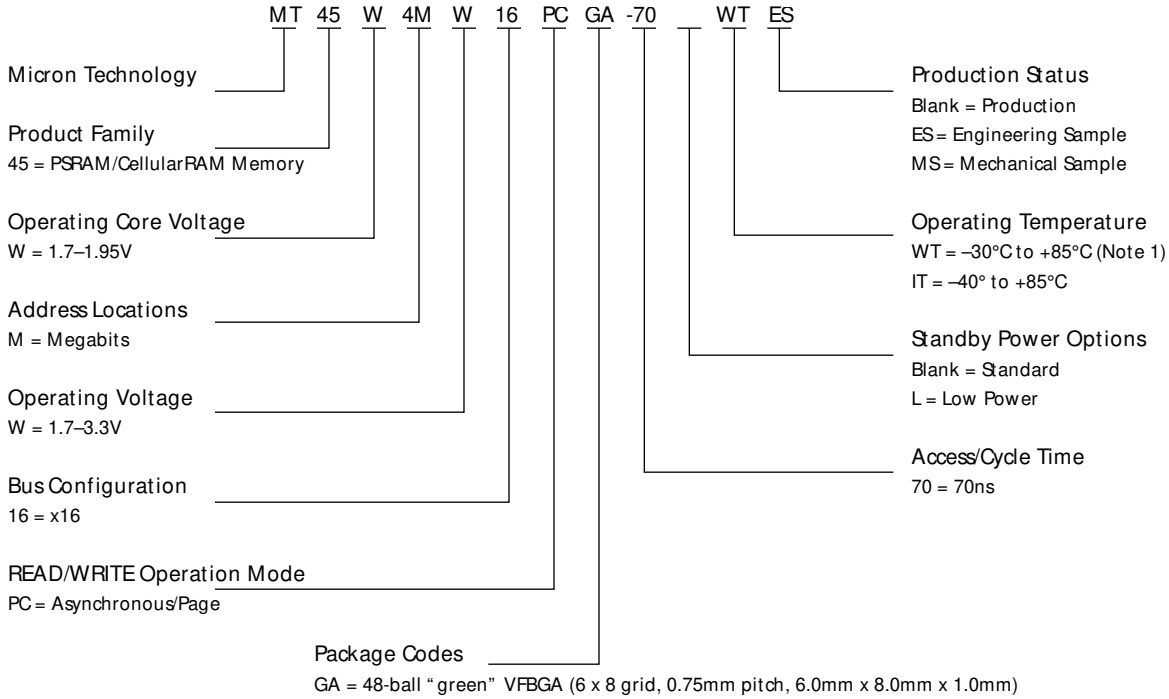
| Mode | Power | CE# | WE# | OE# | LB#/UB# | ZZ# | DQ[15:0][1] | Notes |
|---|---|---|---|---|---|---|---|---|
| Read | Active | L | H | L | L | H | Data-out | 3 |
| Write | Active | L | L | X[2] | L | H | Data-in | 3 |
| Standby | Standby | H | X | X | X | H | High-Z | 4, 5 |
| No operation | Idle | L | X | X | X | H | X | 3, 4 |
| Load configuration register | Active | L | L | X | X | L | High-Z | |
| Read configuration register | Active | L | H | L | L | H | Configuration register out | |
| PAR | Active | H | X | X | X | L | High-Z | |
| DPD | DPD | H | X | X | X | L | High-Z | 6 |

Notes:
1. When LB# and UB# are in select mode (LOW), DQ[15:0] are enabled. When only LB# is in select mode, DQ[7:0] are enabled. When only UB# is in the select mode, DQ[15:8] are enabled.
2. X = "Don't Care."
3. The device will consume active power in this mode whenever addresses are changed.
4. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
5. $V_{IN}$ = $V_{CCQ}$ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
6. DPD is initiated when CE# transitions from LOW to HIGH after writing CR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW and is held LOW for $^{t}$DPDX.

# Part Numbering Information

Micron CellularRAM devices are available in several different configurations and densities (see Figure 3).

**Figure 3: Part Number Chart**




Notes:
1. WT of –30°C exceeds CellularRAM Workgroup 1.0 specification of –25°C.
2. Valid part number combinations: After building the part number from the part numbering chart, use the Micron Parametric Part Search Web site at www.micron.com/partsearch to verify that the part number is offered and valid. If the device required is not on this list, contact the factory.
3. Device marking: Due to the size of the package, the Micron standard part number is not printed on the top of the device. Instead, an abbreviated device mark consisting of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/partsearch. To view the location of the abbreviated mark on the device, refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

# Functional Description

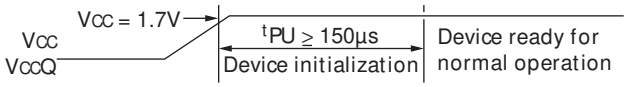
In general, the MT45W4MW16PCGA device is a high-density alternative to SRAM and pseudo-SRAM products, popular in low-power, portable applications.

The MT45W4MW16PCGA contains a 67,108,864-bit DRAM core, organized as 4,194,304 addresses by 16 bits. This device implements the industry-standard, asynchronous memory interface found on other low-power SRAM or PSRAM offerings. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

# Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the register with the default settings. $V_{CC}$ and $V_{CCQ}$ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

**Figure 4: Power-Up Initialization Timing**




# Bus Operating Modes

The MT45W4MW16PCGA CellularRAM product incorporates the industry-standard asynchronous interface found on other low-power SRAM or PSRAM offerings. This bus interface supports asynchronous READ and WRITE transfers as well as bandwidth-enhancing page mode READ operations. The specific interface supported is defined by the value loaded into the CR.

## Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 5 on page 6) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 6 on page 6) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). WE# LOW time must be limited to $^{t}$CEM.

**Figure 5: READ Operation**

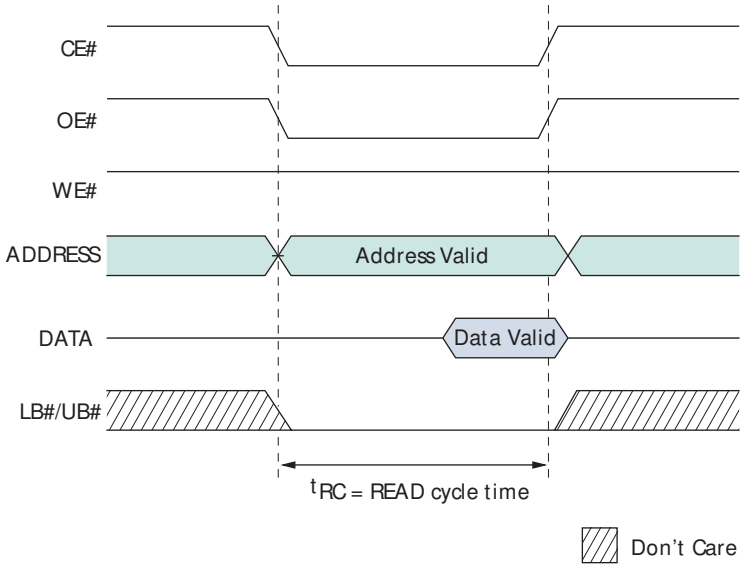
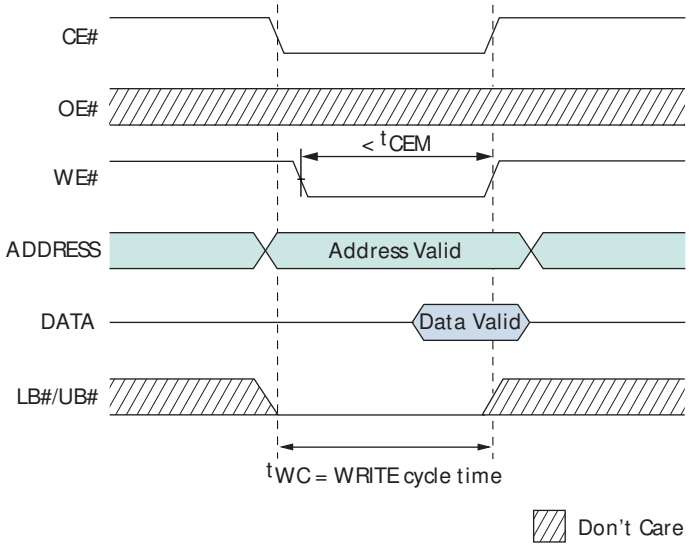



**Figure 6: WRITE Operation**

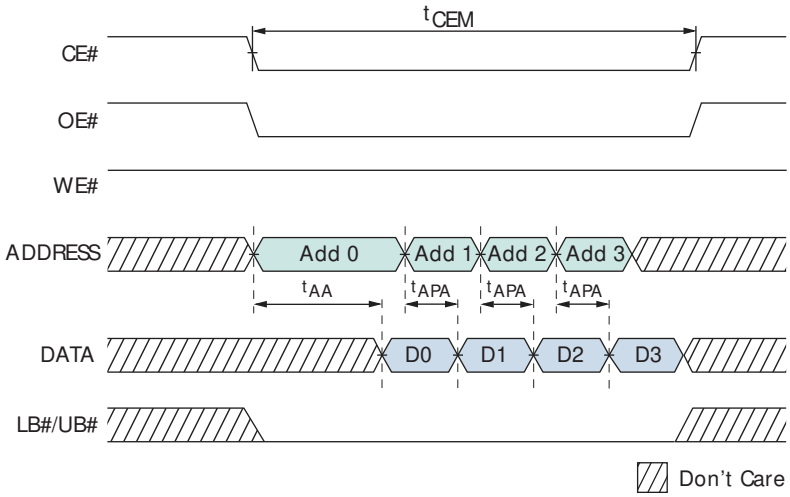


## Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, after an initial asynchronous read access is performed, adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Any change in addresses A[4] or higher will initiate a new $^{t}$AA access time. Figure 7 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

Due to refresh considerations, CE# must not remain LOW longer than $^{t}$CEM.

**Figure 7: Page Mode READ Operation**




## LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During WRITE cycles, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB#/UB# must be LOW during READ cycles.

When both LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

# Low-Power Operation

## Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# and ZZ# are HIGH.

The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

## Temperature-Compensated Refresh (TCR)

This CellularRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually adjusts the refresh rate to match that temperature.

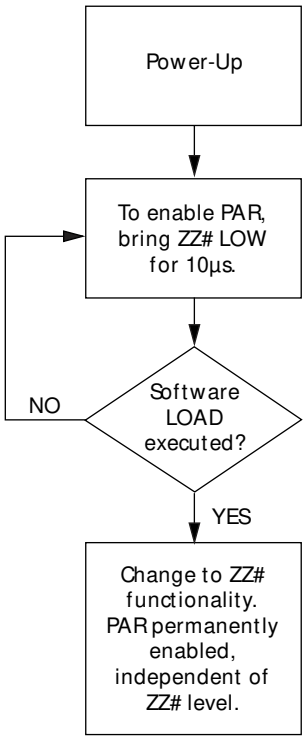
## Partial-Array Refresh (PAR)

PAR restricts REFRESH operation to a portion of the total memory array. This feature enables the system to reduce refresh current by refreshing only that part of the memory array that is absolutely necessary. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. Data stored in addresses not receiving refresh will become corrupted. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 3 on page 10).

READ and WRITE operations are ignored during PAR operation. The device only enters PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by bringing ZZ# LOW for longer than 10µs. Returning ZZ# HIGH will cause an exit from PAR and the entire array will be immediately available for READ and WRITE operations.

Alternatively, PAR can be initiated using the CR software access sequence (see "Software Access to the Configuration Register" on page 12). PAR is enabled immediately upon setting CR[4] to "1" using this method. However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, although ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up (see Figure 8 on page 9).

**Figure 8: Software Access PAR Functionality**




## Deep Power-Down Operation (DPD)

DPD operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is entered. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.

The device can only enter DPD if the SLEEP bit in the CR has been set LOW (CR[4] = 0). DPD is initiated by bringing ZZ# LOW for longer than 10µs. Returning ZZ# HIGH will cause the device to exit DPD and begin a 150µs initialization process. During this 150µs period, the current consumption will be higher than the specified standby levels but considerably lower than the active current specification.

Driving ZZ# LOW will place the device in the PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).

The device should not be put into DPD using CR software access.

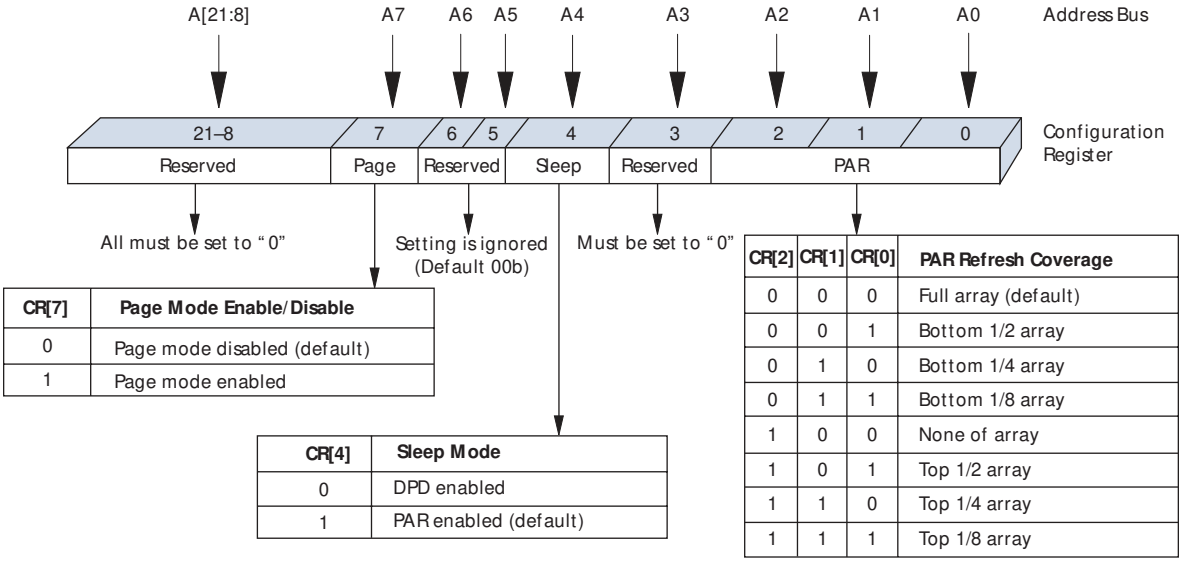
# Device Registers

There are two registers on this device: the configuration register (CR) and the device ID register (DIDR).

## Configuration Register (CR) Operation

The CR defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption in standby mode. Page mode control is also embedded in the CR. This register can be updated any time the device is operating in a standby state. Figure 9 describes the control bits used in the CR. At power-up, the CR is set to 0010h.

**Figure 9: Configuration Register Definition**




| CR[7] | Page Mode Enable/Disable |
|---|---|
| 0 | Page mode disabled (default) |
| 1 | Page mode enabled |

| CR[4] | Sleep Mode |
|---|---|
| 0 | DPD enabled |
| 1 | PAR enabled (default) |

| CR[2] | CR[1] | CR[0] | PAR Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | Full array (default) |
| 0 | 0 | 1 | Bottom 1/2 array |
| 0 | 1 | 0 | Bottom 1/4 array |
| 0 | 1 | 1 | Bottom 1/8 array |
| 1 | 0 | 0 | None of array |
| 1 | 0 | 1 | Top 1/2 array |
| 1 | 1 | 0 | Top 1/4 array |
| 1 | 1 | 1 | Top 1/8 array |

### Partial-Array Refresh (CR[2:0]) Default = Full-Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 3).

**Table 3: 64Mb Address Patterns for PAR (CR[4] = 1)**

| CR[2] | CR[1] | CR[0] | Active Section | Address Space | Size | Density |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Full die | 000000h–3FFFFFh | 4 Meg x 16 | 64Mb |
| 0 | 0 | 1 | One-half of die | 000000h–1FFFFFh | 2 Meg x 16 | 32Mb |
| 0 | 1 | 0 | One-quarter of die | 000000h–0FFFFFh | 1 Meg x 16 | 16Mb |
| 0 | 1 | 1 | One-eighth of die | 000000h–07FFFFh | 512K x 16 | 8Mb |
| 1 | 0 | 0 | None of die | 0 | 0 Meg x 16 | 0Mb |
| 1 | 0 | 1 | One-half of die | 200000h–3FFFFFh | 2 Meg x 16 | 32Mb |
| 1 | 1 | 0 | One-quarter of die | 300000h–3FFFFFh | 1 Meg x 16 | 16Mb |
| 1 | 1 | 1 | One-eighth of die | 380000h–3FFFFFh | 512K x 16 | 8Mb |

### Sleep Mode (CR[4]) Default = PAR Enabled

The sleep mode bit determines which low-power mode is to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software access sequence. Note that this then disables ZZ# initiation of PAR. DPD cannot be enabled or disabled using the software access sequence; the DPD setting can be changed only by using ZZ# to access the CR.

### Page Mode Operation (CR[7]) Default = Disabled

The page mode operation bit determines whether page mode is enabled for READ operations. In the power-up default state, page mode is disabled.

## Device Identification Register (DIDR)

The DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is not part of the CellularRAM 1.0 Workgroup specification. Table 4 describes the bit fields in the DIDR.

The DIDR is accessed through the register access software sequence with DQ = 0002h on the third cycle.

**Table 4: Device Identification Register Mapping**

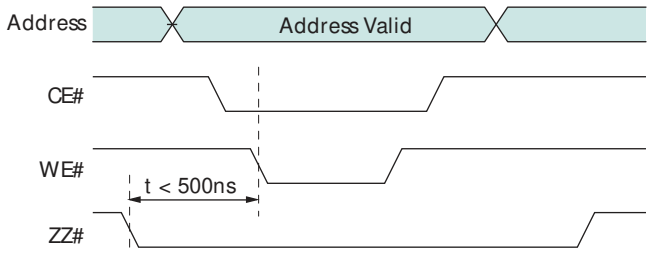
| Bit Field | DIDR[15] | DIDR[14:11] | | DIDR[10:8] | DIDR[7:5] | DIDR[4:0] |
|---|---|---|---|---|---|---|
| Field name | Row length | Device version | | Device density | CellularRAM generation | Vendor ID |
| Bit setting | 0b | 0000b | 1st | 010b | 010b | 00011b |
| | | 0001b | 2nd | | | |
| | | … | … | | | |
| Meaning | 128 words | | | 64Mb | n/a[1] | Micron |

Notes: 1. CellularRAM generation is shown as 010b and has no meaning in terms of this device.

## Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (Figure 10). The values placed on addresses A[21:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

**Figure 10: Load Configuration Register Operation**



## Software Access to the Configuration Register

The contents of the CR can be read and modified using a software sequence. The nature of this access mechanism may eliminate the need for the ZZ# ball.

If the software mechanism is used, ZZ# can simply be tied to VCCQ. The port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to VCCQ if the system will use DPD, since DPD cannot be enabled or disabled using the software access sequence.

The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 11). The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 12 on page 13). Note that a third READ cycle of the highest address cancels the sequence until a different address is read.

The address used during all READ and WRITE operations is the highest address of the CellularRAM device being accessed (3FFFFFh for 64Mb); the content at this address is changed by using this sequence. The data bus is used to transfer data into or out of bits 15–0 of the CR.

Writing to the CR using the software sequence modifies the function of ZZ#. Once the software sequence loads the CR, the ZZ# level no longer enables PAR operation. PAR operation will be updated whenever the software sequence loads a new value into the CR. This ZZ# functionality will continue until the next time the device is powered up. The operation of ZZ# is not affected if the software sequence is only used to read the contents of the CR. The use of the software sequence does not affect the ability to perform the standard (ZZ# controlled) method of loading the CR.

**Figure 11: Software Access Load Configuration Register**

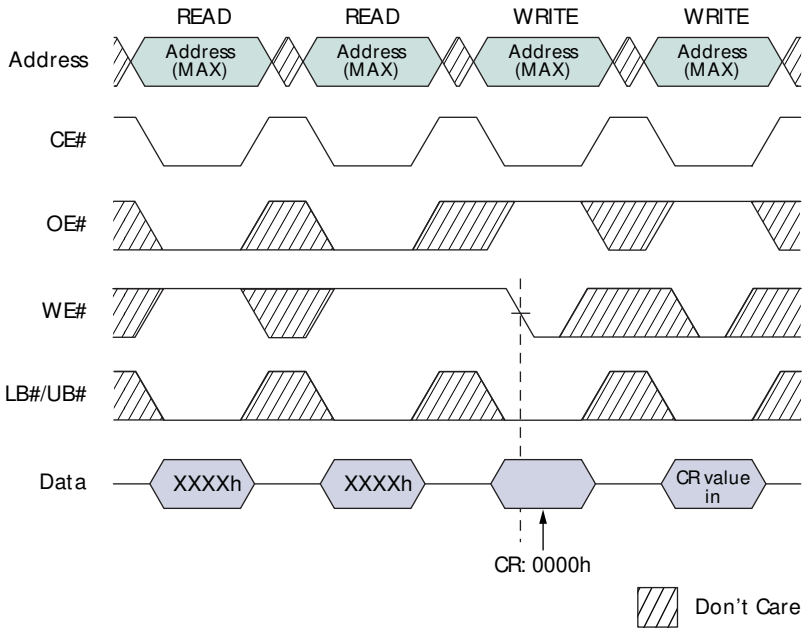
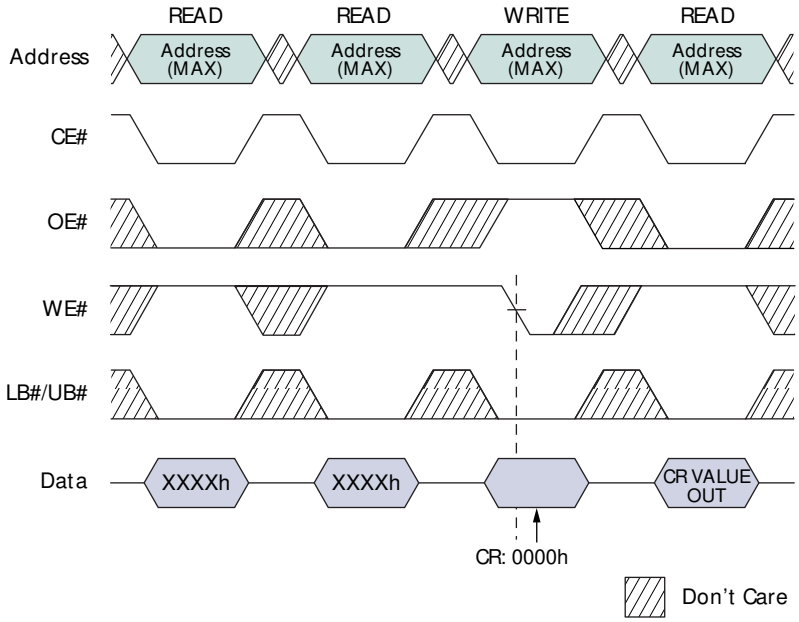


**Figure 12: Software Access Read Configuration Register**



# Electrical Characteristics

Stresses greater than those listed in Table 5 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 5: Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Voltage to any ball except $V_{CC}$, $V_{CCQ}$ relative to $V_{SS}$ | –0.5V to (4.0V or $V_{CCQ}$ +0.3V, whichever is less) |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | –0.2V to +2.45V |
| Voltage on $V_{CCQ}$ supply relative to $V_{SS}$ | –0.2V to +4.0V |
| Storage temperature (plastic) | –55°C to +150°C |
| Operating temperature (case)<br>Wireless[1]<br>Industrial | <br>–30°C to +85°C<br>–40°C to +85°C |
| Soldering temperature and time<br>10s (solder ball only) | <br>+260°C |

Notes: 1. –30°C exceeds CellularRAM Workgroup 1.0 specification of –25°C.

**Table 6: Electrical Characteristics**

Wireless temperature (–30ºC < $T_C$ < +85ºC)[1]; Industrial temperature (–40ºC < $T_C$ < +85ºC)

| Description | Conditions | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | | $V_{CC}$ | 1.7 | 1.95 | V | |
| I/O supply voltage | | $V_{CCQ}$ | 1.7 | 3.3 | V | |
| Input high voltage | | $V_{IH}$ | $V_{CCQ}$ - 0.4 | $V_{CCQ}$ + 0.2 | V | 2 |
| Input low voltage | | $V_{IL}$ | –0.2 | 0.4 | V | 3 |
| Output high voltage | $I_{OH}$ = –0.2mA | $V_{OH}$ | 0.8 $V_{CCQ}$ | | V | |
| Output low voltage | $I_{OL}$ = +0.2mA | $V_{OL}$ | | 0.2 $V_{CCQ}$ | V | |
| Input leakage current | $V_{IN}$ = 0 to $V_{CCQ}$ | $I_{LI}$ | | 1 | µA | |
| Output leakage current | OE# = $V_{IH}$ or chip disabled | $I_{LO}$ | | 1 | µA | |

Notes: 1. WT of –30°C exceeds CellularRAM Workgroup 1.0 specification of –25°C.
2. Input signals may overshoot to $V_{CCQ}$ + 1V for periods less than 2ns during transitions.
3. Input signals may undershoot to $V_{SS}$ - 1V for periods less than 2ns during transitions.

## Table 7: Operating Conditions

Wireless temperature (–30ºC < $T_C$ < +85ºC)[1]; Industrial temperature (–40ºC < $T_C$ < +85ºC)

| Operating Current | Conditions | Symbol | | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Asynchronous random READ/WRITE | $V_{IN}$ = $V_{CCQ}$ or 0V chip enabled, $I_{OUT}$ = 0 | $I_{CC1}$ | –70 | | 25 | mA | 2 |
| Asynchronous page READ | | $I_{CC1P}$ | –70 | | 15 | mA | 2 |
| Standby current | $V_{IN}$ = $V_{CCQ}$ or 0V CE# = $V_{CCQ}$ | $I_{SB}$ | Standard | 50 | 140 | µA | 3, 4 |
| | | | Low-power (L) | | 120 | | |

Notes:
1. WT of –30°C exceeds CellularRAM Workgroup 1.0 specification of –25°C.
2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
3. $I_{SB}$ (MAX) values measured with PAR set to full array and at +85°C. In order to achieve low standby current, all inputs must be driven to either $V_{CCQ}$ or $V_{SS}$. $I_{SB}$ might be slightly higher for up to 500ms after power-up, or when entering standby mode.
4. $I_{SB}$ (TYP) is the average $I_{SB}$ at 25°C and $V_{CC}$ = $V_{CCQ}$ = 1.8V. This parameter is verified during characterization and is not 100 percent tested.

## Table 8: Partial-Array Refresh Specifications and Conditions

| Description | Conditions | Symbol | | Array Partition | Max | Unit |
|---|---|---|---|---|---|---|
| Partial-array refresh standby current | $V_{IN}$ = $V_{CCQ}$ or 0V, CE# = $V_{CCQ}$ | $I_{PAR}$ | Standard power (no designation) | Full | 140 | µA |
| | | | | 1/2 | 120 | |
| | | | | 1/4 | 110 | |
| | | | | 1/8 | 105 | |
| | | | | 0 | 95 | |
| | | | Low-power option (L) | Full | 120 | µA |
| | | | | 1/2 | 105 | |
| | | | | 1/4 | 95 | |
| | | | | 1/8 | 90 | |
| | | | | 0 | 85 | |

Notes:
1. $I_{PAR}$ (MAX) values measured at 85°C. $I_{PAR}$ might be slightly higher for up to 500ms after changes to the PAR array partition or when entering standby mode. In order to achieve low standby current, all inputs must be driven to either $V_{CCQ}$ or $V_{SS}$.

**Figure 13: Typical Refresh Current vs. Temperature (ITCR)**

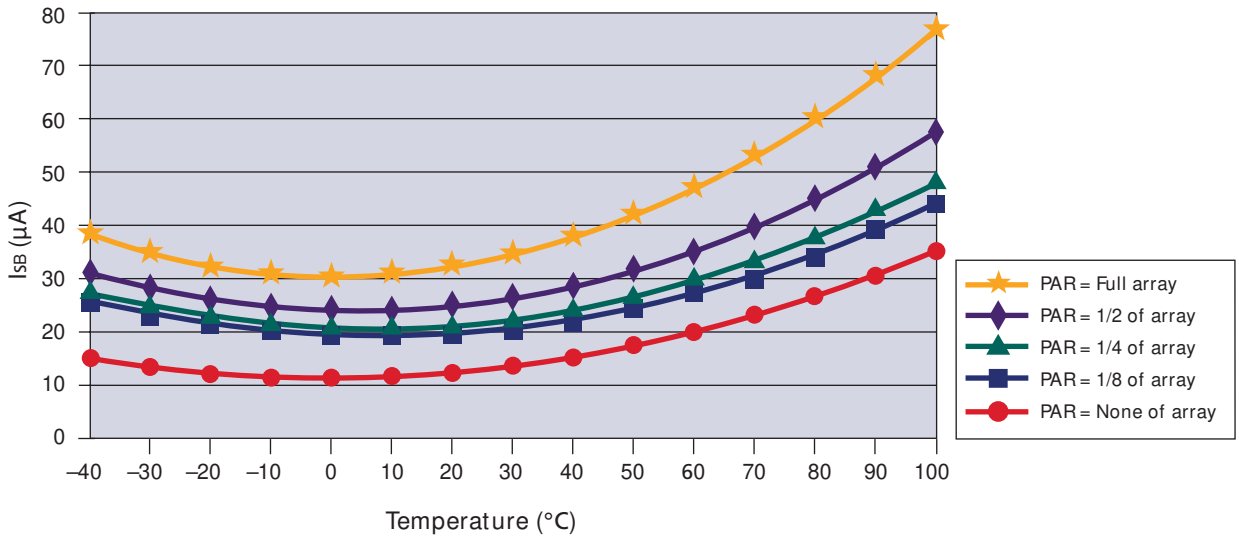



**Table 9: Deep Power-Down Specifications**

| Description | Conditions | Symbol | Typ | Max | Unit |
|---|---|---|---|---|---|
| Deep power-down | VIN = VCCQ or 0V; VCC, VCCQ = 1.95V; +85°C | IZZ | 3 | 10 | µA |

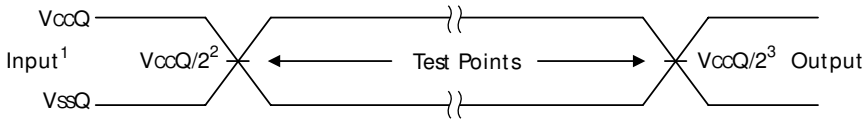
Notes: 1. Typical (TYP) IZZ value applies across all operating temperatures and voltages.

**Table 10: Capacitance**

| Description | Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $T_C$ = +25°C; f = 1 MHz; VIN = 0V | CIN | 2.0 | 6 | pF |
| Input/output capacitance (DQ) | | CIO | 3.5 | 6 | pF |

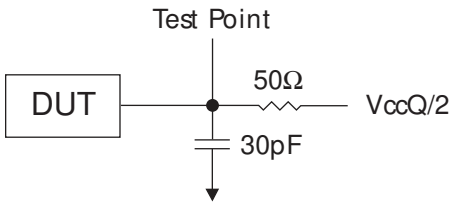
Notes: 1. These parameters are verified in device characterization and are not 100 percent tested.

**Figure 14: AC Input/Output Reference Waveform**




Notes: 1. AC test inputs are driven at VCCQ for a logic 1 and VSSQ for a logic 0. Input rise and fall times (10 percent to 90 percent) < 1.6ns.
2. Input timing begins at VCCQ/2.
3. Output timing ends at VCCQ/2.

**Figure 15: AC Output Load Circuit**



# Timing Requirements

**Table 11: Asynchronous READ Cycle Timing Requirements**

| Parameter | Symbol | 70ns | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Address access time | $^{t}AA$ | | 70 | ns | |
| Page access time | $^{t}APA$ | | 20 | ns | |
| LB#/UB# access time | $^{t}BA$ | | 70 | ns | |
| LB#/UB# disable to DQ High-Z output | $^{t}BHZ$ | | 8 | ns | 1 |
| LB#/UB# enable to Low-Z output | $^{t}BLZ$ | 10 | | ns | 2 |
| Maximum CE# pulse width | $^{t}CEM$ | | 4 | µs | 3 |
| Chip select access time | $^{t}CO$ | | 70 | ns | |
| Chip disable to DQ High-Z output | $^{t}HZ$ | | 8 | ns | 1 |
| Chip enable to Low-Z output | $^{t}LZ$ | 10 | | ns | 2 |
| Output enable to valid output | $^{t}OE$ | | 20 | ns | |
| Output hold from address change | $^{t}OH$ | 5 | | ns | |
| Output disable to DQ High-Z output | $^{t}OHZ$ | | 8 | ns | 1 |
| Output enable to Low-Z output | $^{t}OLZ$ | 3 | | ns | 2 |
| Page cycle time | $^{t}PC$ | 20 | | ns | |
| READ cycle time | $^{t}RC$ | 70 | | ns | |

Notes:
1. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 16. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CCQ}/2$.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 16. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either $V_{OH}$ or $V_{OL}$.
3. Page mode enabled only.

**Table 12: Asynchronous WRITE Cycle Timing Requirements**

| Parameter | Symbol | 70ns | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Address and ADV# LOW setup time | $^{t}$AS | 0 | | ns | |
| Address valid to end of WRITE | $^{t}$AW | 70 | | ns | |
| LB#/UB# select to end of WRITE | $^{t}$BW | 70 | | ns | |
| CE# HIGH time during WRITEs between subsequent async operations | $^{t}$CPH | 5 | | ns | |
| Chip enable to end of WRITE | $^{t}$CW | 70 | | ns | |
| Data hold from WRITE time | $^{t}$DH | 0 | | ns | |
| Data WRITE setup time | $^{t}$DW | 20 | | ns | |
| Chip enable to Low-Z output | $^{t}$LZ | 10 | | ns | 2 |
| End WRITE to Low-Z output | $^{t}$OW | 5 | | ns | 2 |
| WRITE cycle time | $^{t}$WC | 70 | | ns | |
| WRITE to DQ High-Z output | $^{t}$WHZ | | 8 | ns | 1 |
| WRITE pulse width | $^{t}$WP | 45 | | ns | 3 |
| WRITE pulse width HIGH | $^{t}$WPH | 10 | | ns | |
| WRITE recovery time | $^{t}$WR | 0 | | ns | |

Notes:
1. Low-Z to High-Z timings are tested with the circuit shown in Figure 15 on page 16. The High-Z timings measure a 100mV transition from either $V_{OH}$ or $V_{OL}$ toward $V_{CCQ}/2$.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 15 on page 16. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CCQ}/2$) level toward either $V_{OH}$ or $V_{OL}$.
3. WE# LOW time must be limited to $^{t}$CEM (4µs).

# Timing Diagrams

**Figure 16: Initialization Period**

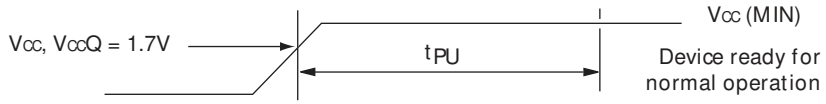



**Figure 17: DPD Entry and Exit Timing**


**Table 13: Initialization Timing Parameters**

| Parameter | Symbol | 70ns | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Time from DPD entry to DPD exit | tDPD | 10 | | µs | |
| CE# LOW time to exit DPD | tDPDX | 10 | | µs | |
| Initialization period (required before normal operations) | tPU | | 150 | µs | |

**Figure 18: Load Configuration Register**

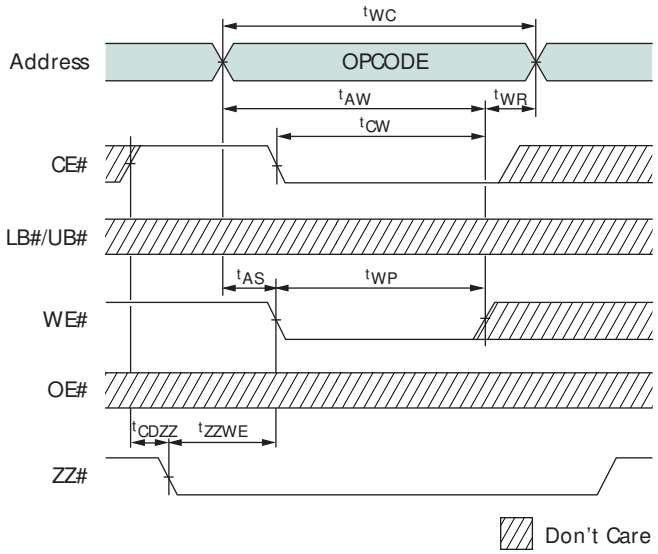



**Figure 19: Asynchronous READ (WE# = VIN)**

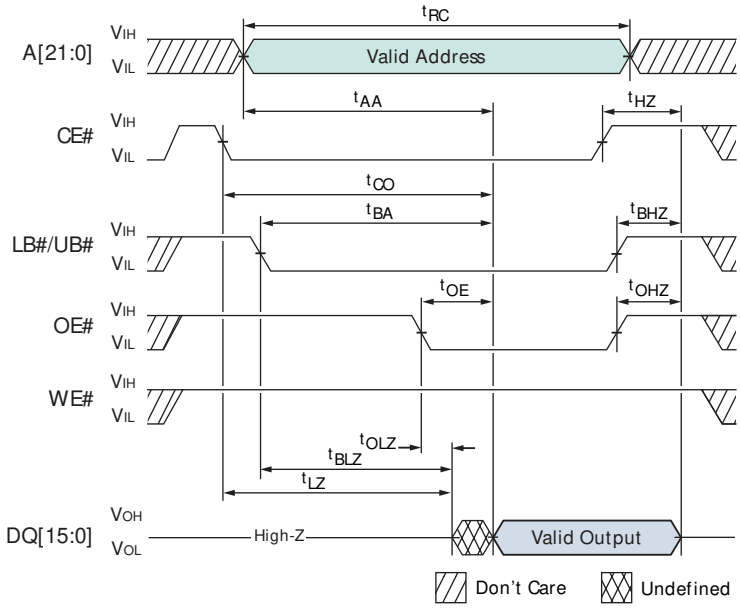


**Figure 20: Page Mode READ (WE# = VIN)**

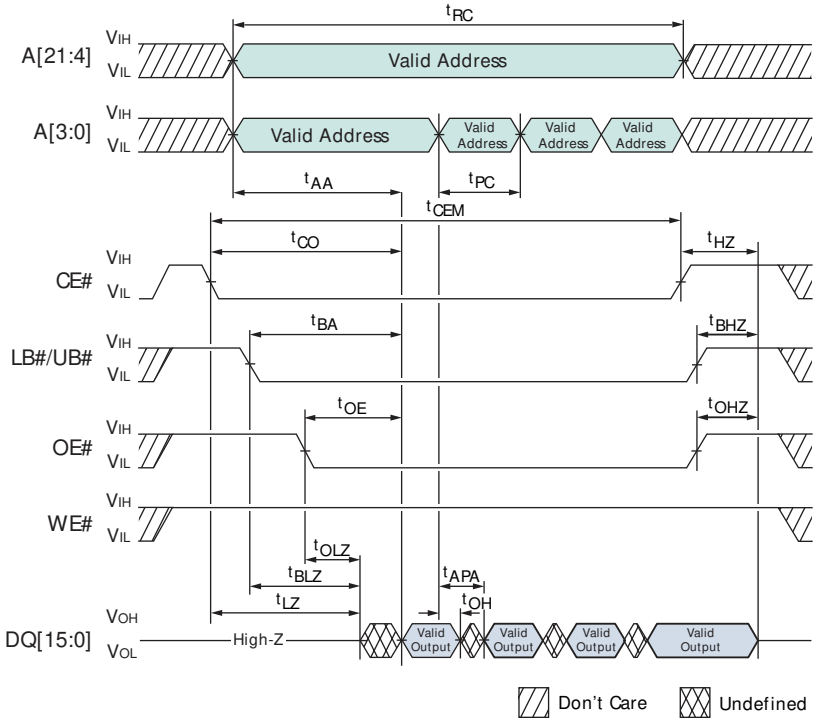



**Figure 21: CE#-Controlled Asynchronous WRITE**

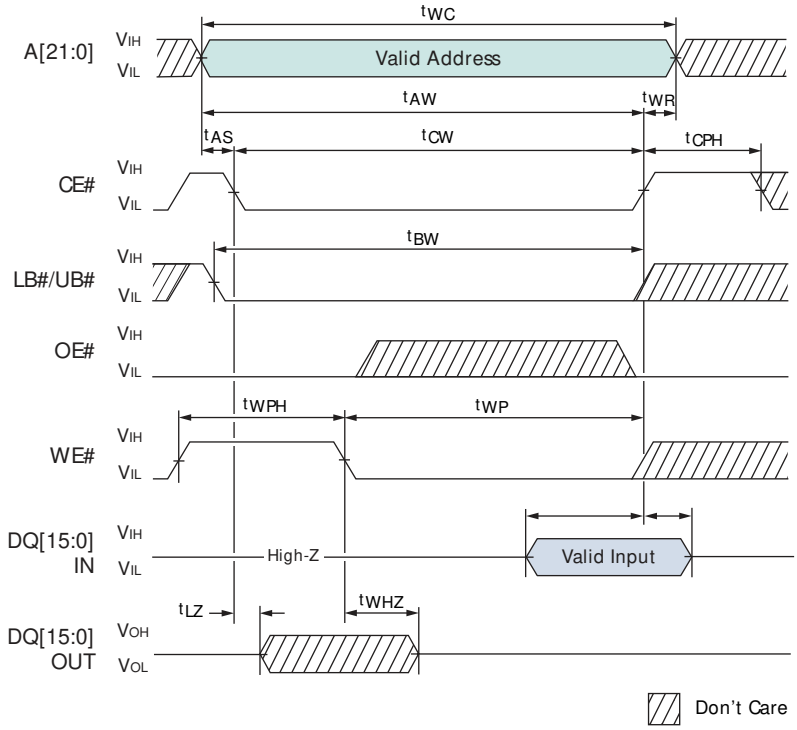


**Figure 22: LB#/UB#-Controlled Asynchronous WRITE**

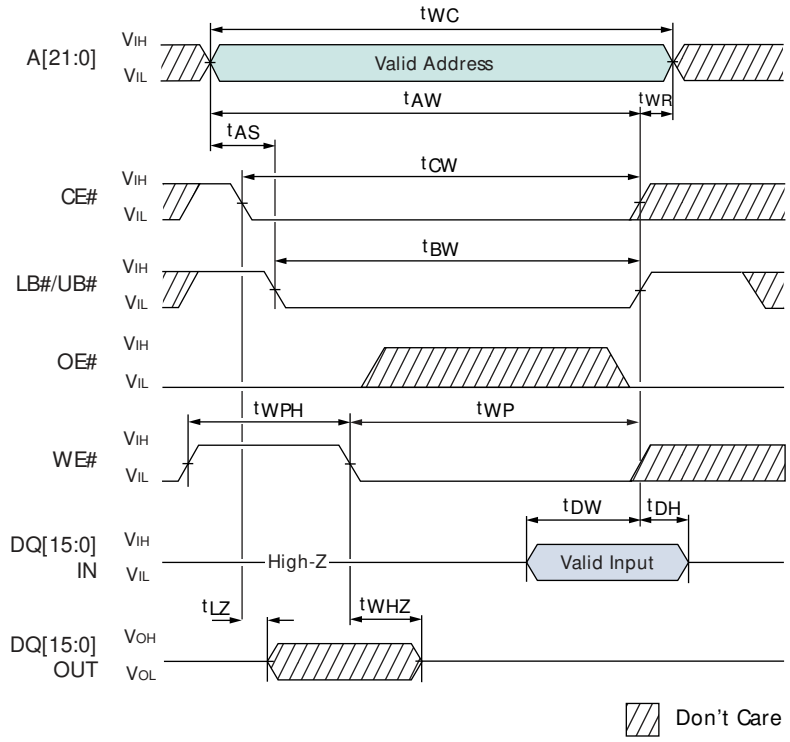
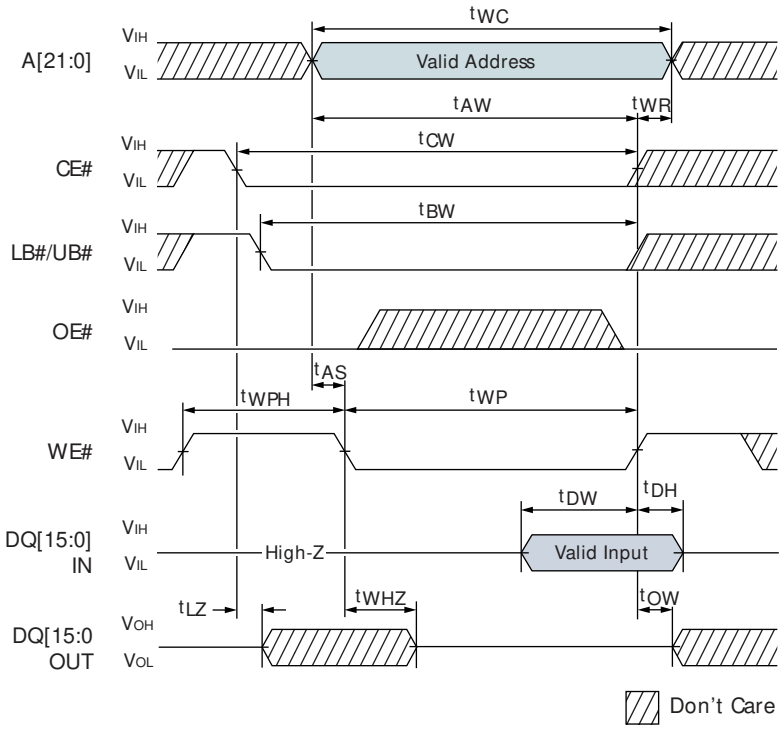
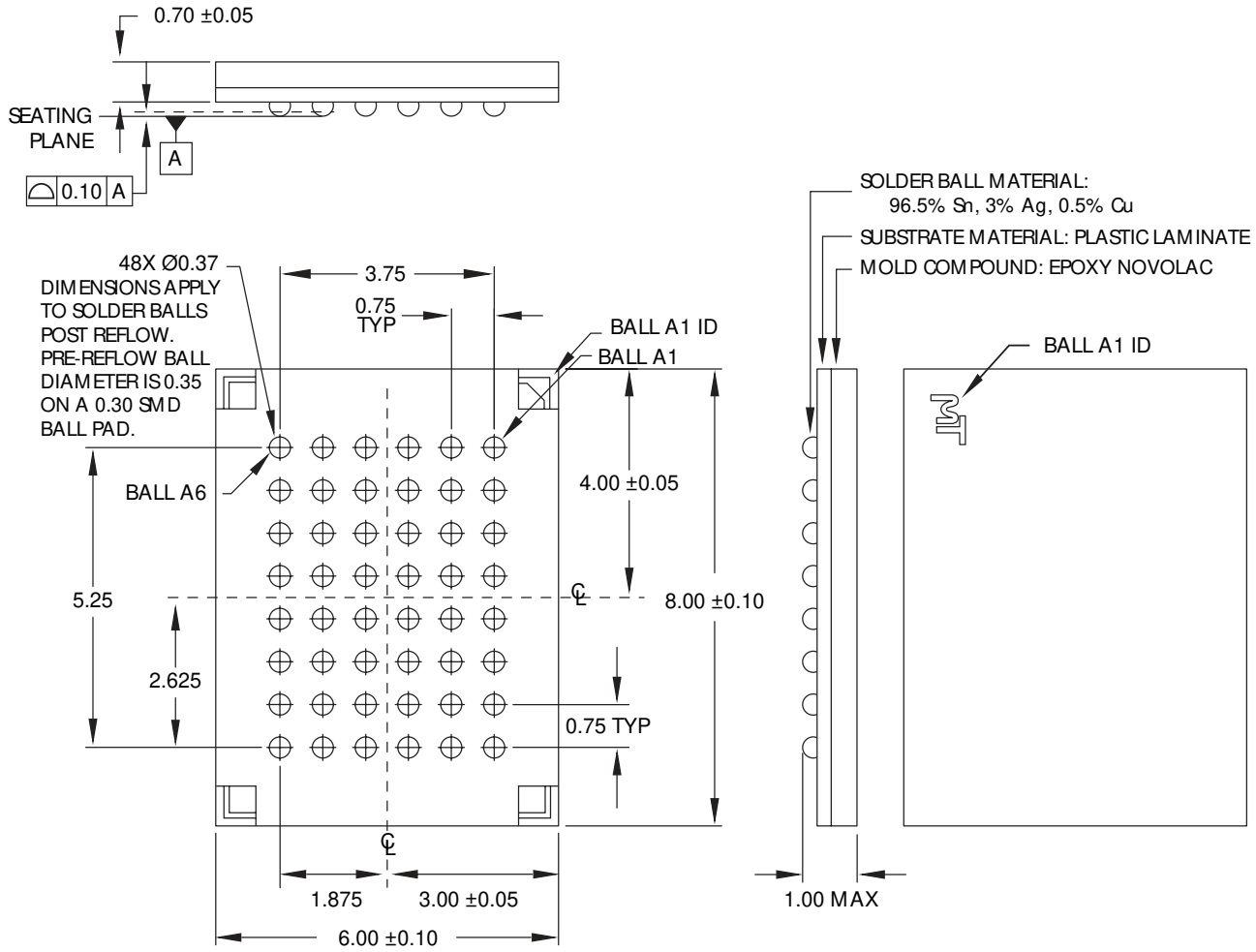



**Figure 23: WE#-Controlled Asynchronous WRITE**



# Package Dimensions

**Figure 24: 48-Ball VFBGA**




Notes:
1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.
3. The MT45W4MW16PCGA uses "green" packaging.

**8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900**
**prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992**