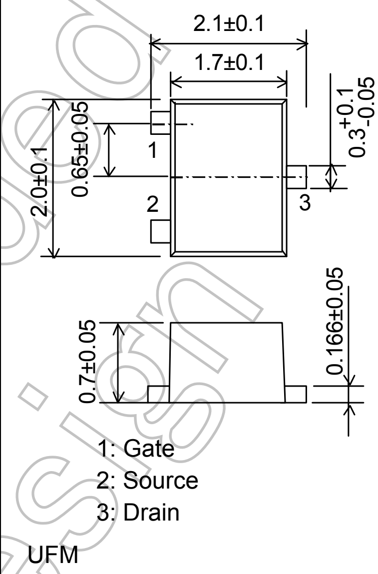
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K106TU

High-Speed Switching Applications

- 4 V drive
- Low ON-resistance: R_{on} = 530 mΩ (max) (@V_{GS} = 4 V)
  R_{on} = 310 mΩ (max) (@V_{GS} = 10 V)

Unit: mm



JEDEC	―
JEITA	―
TOSHIBA	2-2U1A

Weight: 6.6 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	1.2	A
	Pulse	I_{DP}	2.4	
Drain power dissipation		P_D (Note 1)	800	mW
		P_D (Note 2)	500	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 mm^2)

Note 2: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

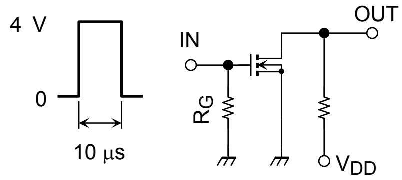
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0	20	―	―	V
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	―	―	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	―	―	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 5 V, I_D = 0.1 mA	1.1	―	2.3	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 0.6 A (Note 3)	0.58	1.16	―	S
Drain-source ON-resistance		$R_{DS(ON)}$	I_D = 0.6 A, V_{GS} = 10 V (Note 3)	―	230	310	mΩ
			I_D = 0.6 A, V_{GS} = 4 V (Note 3)	―	390	530	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	36	―	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	30	―	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	―	10	―	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.6 A,	―	21	―	ns
	Turn-off time	t_{off}	V_{GS} = 0 to 4 V, R_G = 10 Ω	―	8	―	
Drain-source forward voltage		V_{DSF}	I_D = −1.2 A, V_{GS} = 0 V (Note 3)	―	−1.0	−1.4	V

Note 3: Pulse test

Start of commercial production
2005-02

Switching Time Test Circuit

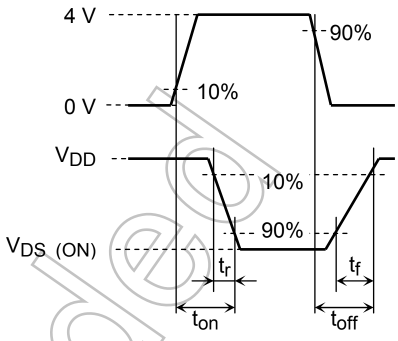
(a) Test Circuit



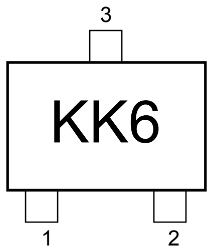
V_{DD} = 10 V
R_G = 10 Ω
Duty ≤ %
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

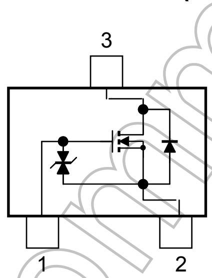
(c) V_{OUT}



Marking



Equivalent Circuit (top view)



Note

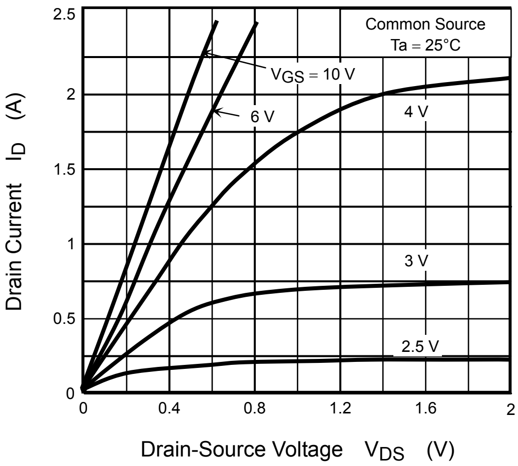
V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = 0.1 mA for this product. For normal switching operation, $V_{GS (on)}$ requires a higher voltage than V_{th}, and $V_{GS (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS (off)} < V_{th} < V_{GS (on)}$.)

Take this into consideration when using the device.

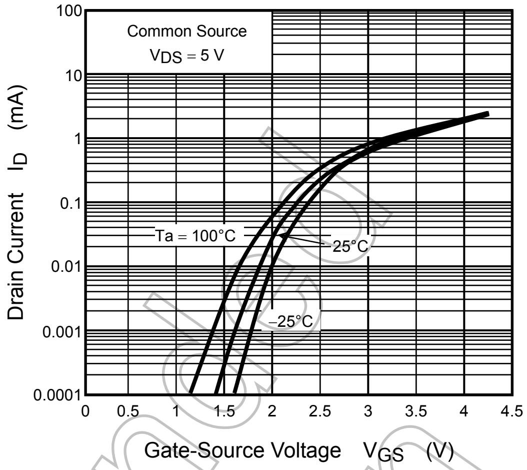
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, be sure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

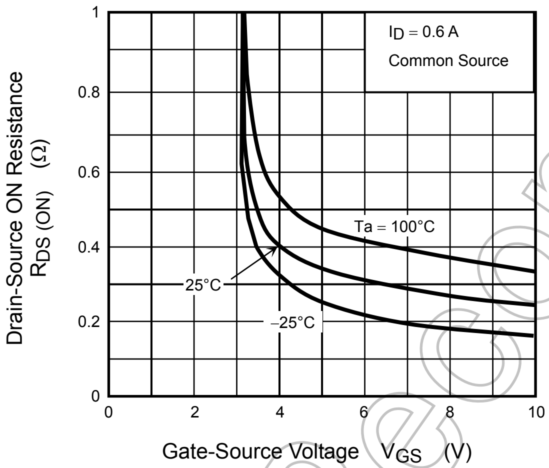
I_D – V_{DS}



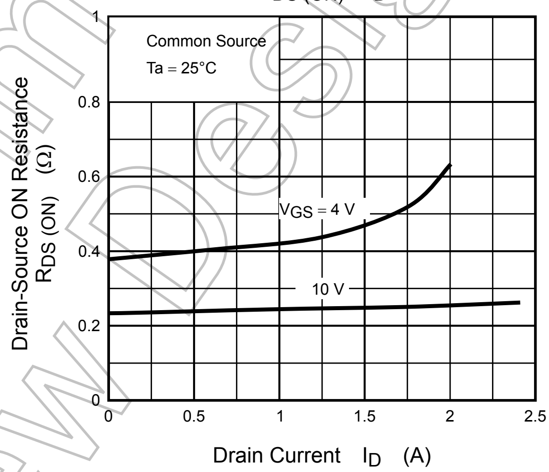
I_D – V_{GS}



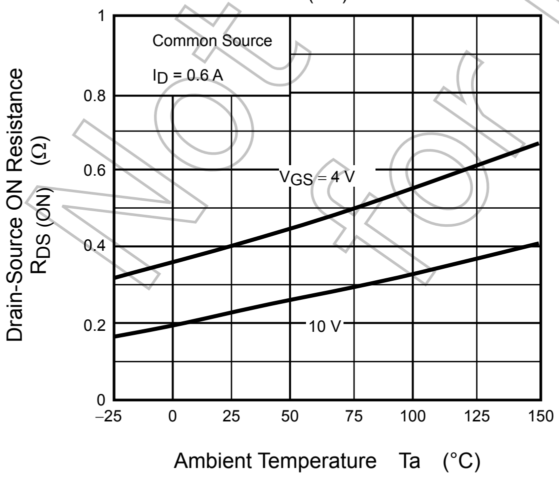
$R_{DS (ON)}$ – V_{GS}



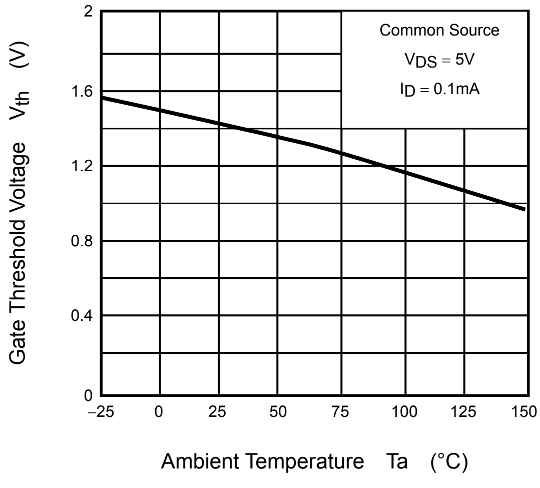
$R_{DS (ON)}$ – I_D

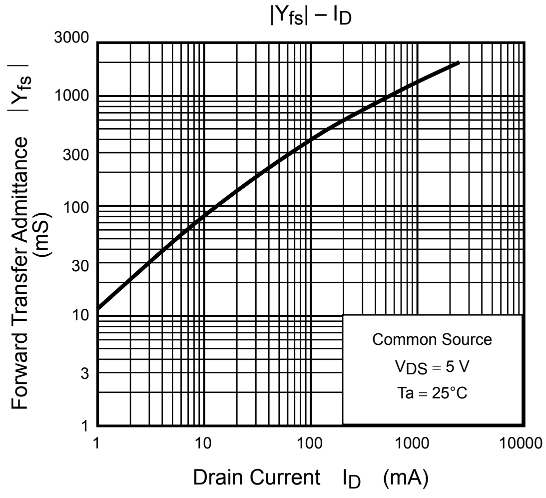


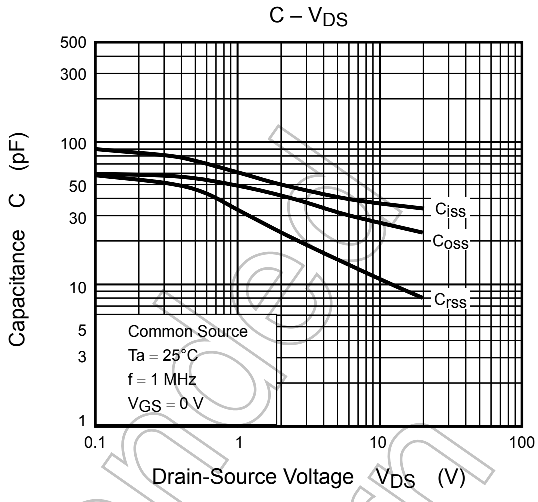
$R_{DS (ON)}$ – Ta

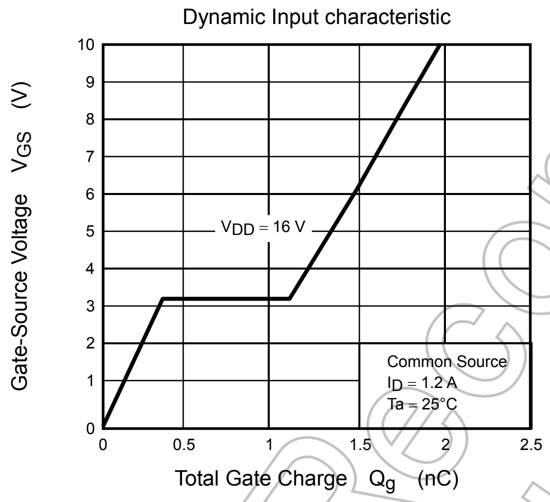


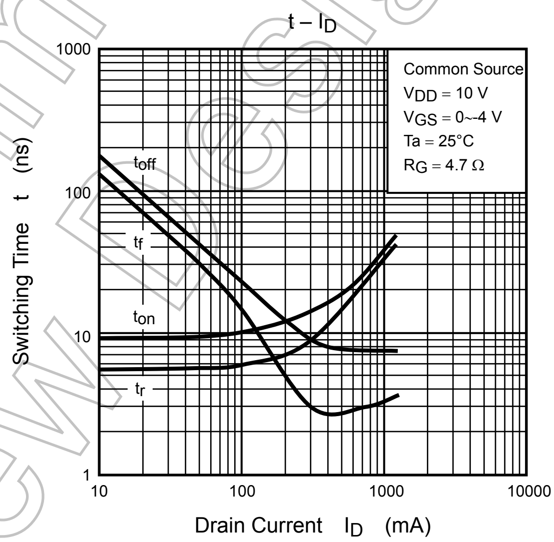
V_{th} – Ta

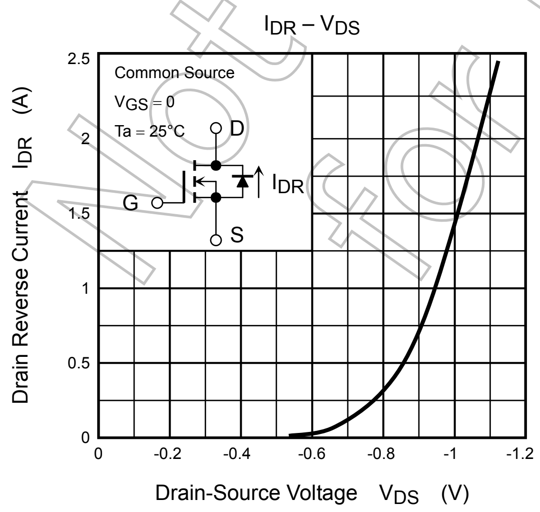


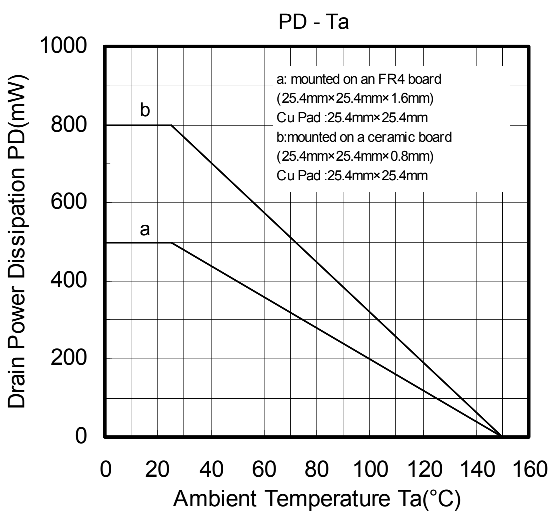

|Yfs| – ID
Forward Transfer Admittance |Yfs| (mS)
Common Source
VDS = 5 V
Ta = 25°C
Drain Current ID (mA)

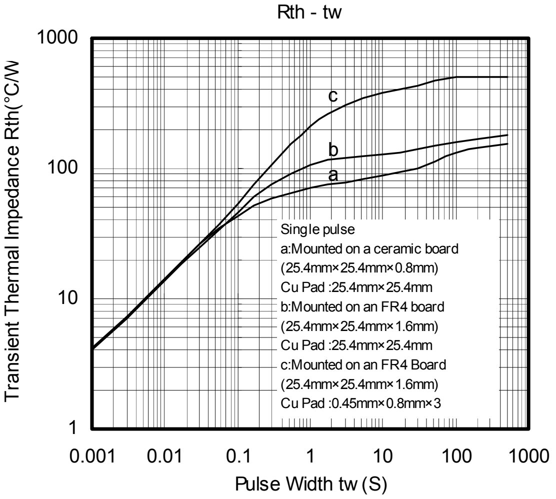

C – VDS
Capacitance C (pF)
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Drain-Source Voltage VDS (V)


Dynamic Input characteristic
Gate-Source Voltage VGS (V)
VDD = 16 V
Common Source
ID = 1.2 A
Ta = 25°C
Total Gate Charge Qg (nC)


t – ID
Switching Time t (ns)
Common Source
VDD = 10 V
VGS = 0~4 V
Ta = 25°C
RG = 4.7 Ω
toff
tf
ton
tr
Drain Current ID (mA)


IDR – VDS
Drain Reverse Current IDR (A)
Common Source
VGS = 0
Ta = 25°C
D
G
S
IDR
Drain-Source Voltage VDS (V)


PD - Ta
Drain Power Dissipation PD(mW)
a: mounted on an FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
b:mounted on a ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b
a
Ambient Temperature Ta(°C)


Rth - tw
Transient Thermal Impedance Rth(°C/W
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse Width tw (S)
c
b
a
Single pulse
a:Mounted on a ceramic board
(25.4mm×25.4mm×0.8mm)
Cu Pad :25.4mm×25.4mm
b:Mounted on an FR4 board
(25.4mm×25.4mm×1.6mm)
Cu Pad :25.4mm×25.4mm
c:Mounted on an FR4 Board
(25.4mm×25.4mm×1.6mm)
Cu Pad :0.45mm×0.8mm×3

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