

## Half-Bridge N-Channel MOSFET Driver for DC/DC Conversion

### DESCRIPTION

The SiP41109 and SiP41110 are high-speed half-bridge MOSFET drivers for use in high frequency, high current, multiphase dc-to-dc synchronous rectifier buck power supplies. They are designed to operate at switching frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving N-channel MOSFETs.

They feature adaptive shoot-through protection to prevent simultaneous conduction of the external MOSFETs. There are two options available for the voltage of the high-side and low-side drivers. In the SiP41109, the regulator supplies gate drive voltage to the high-side driver and  $V_{CC}$  supplies the low-side driver. In the SiP41110, the regulator supplies the high- and low-side gate drive voltage.

The SiP41109 and SiP41110 are assembled in a lead (Pb)-free 8-pin SOIC package for operation over the industrial operating range (-40 °C to 85 °C).

### FEATURES

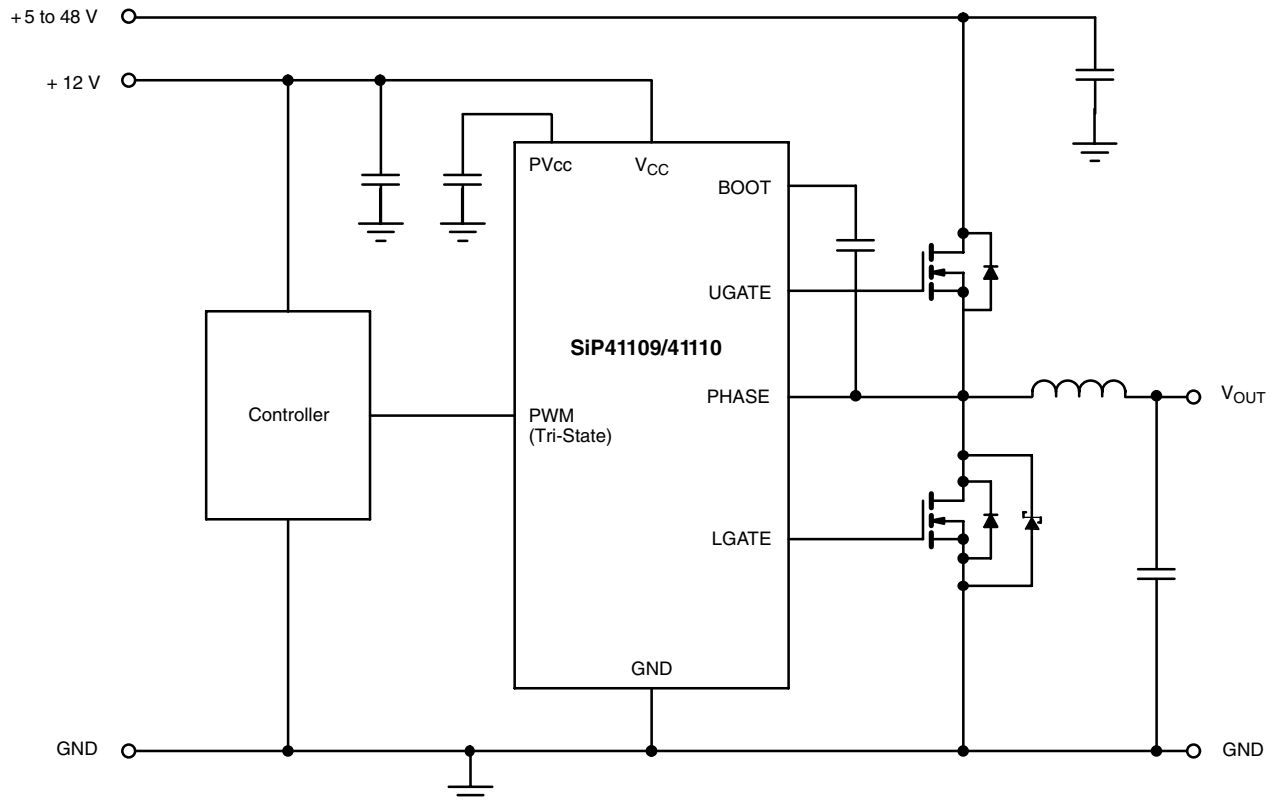
- PWM with tri-state enable
- 12 V low-side gate drive (SiP41109)
- 8 V low-side gate drive (SiP41110)
- Undervoltage lockout
- Internal bootstrap diode
- Switching frequency up to 1 MHz
- 30 ns max. propagation delay
- Drive MOSFETs in 5 V to 48 V systems
- Adaptive shoot-through protection



### APPLICATIONS

- Multi-phase DC/DC conversion
- High current low voltage DC/DC converters
- High frequency DC/DC converters
- Mobile and desktop computer DC/DC converters
- Core voltage supplies for PC micro-processors

### TYPICAL APPLICATION CIRCUIT



<b>ABSOLUTE MAXIMUM RATINGS</b> (all voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{CC}, PV_{CC}$		- 0.3 to 15	V
BOOT, PHASE		- 0.3 to 55	
BOOT to PHASE		- 0.3 to 15	
Storage Temperature		- 40 to 150	°C
Operating Junction Temperature		125	
Power Dissipation <sup>a</sup>	SO-8	770	mW
Thermal Impedance ( $\Theta_{JA}$ ) <sup>b</sup>		130	°C/W

Notes:

a. Device Mounted with all leads soldered or welded to PC board.

b. Derate 7.7 mW/°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<b>RECOMMENDED OPERATING RANGE</b> (all voltages referenced to GND = 0 V)			
Parameter		Limit	Unit
$V_{CC}$		10.8 to 13.2	V
$V_{LX}$		48	
$C_{BOOT}$		100 nF to 1 $\mu$ F	
BOOT to PHASE		8	V
Operating Temperature Range		- 40 to 85	°C

<b>SPECIFICATIONS<sup>a</sup></b>						
Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}, V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ }^\circ\text{C to }85\text{ }^\circ\text{C}$	Limits			Unit
			Min. <sup>a</sup>	Typ. <sup>b</sup>	Max. <sup>a</sup>	
<b>Power Supplies</b>						
Supply Voltage	$V_{DD}$		10.8		13.2	V
Quiescent Current	$I_{CCQ}$	PWM non-switching		5.6	9.5	mA
Supply Current	$I_{DD}$	$f_{PWM} = 100\text{ kHz}, C_{LOAD} = 3\text{ nF}$		12.5		
				11.0		
Tristate (Shutdown) Current	$I_{CCT}$	PWM = open		850	1200	$\mu$ A
<b>Reference Voltage</b>						
Break-Before-Make	$V_{BBM}$			2.5		V
<b>PWM Input</b>						
Input High	$V_{IH}$		4.0		$V_{DD}$	V
Input Low	$V_{IL}$				1.0	
Bias Current	$I_B$	PWM 5 V or 0 V		$\pm 600$	$\pm 1000$	$\mu$ A
Tristate Threshold	High	$V_{TSH}$	3.0			V
	Low	$V_{TSL}$			2.0	
Tristate Holdoff Timeout <sup>c</sup>	$t_{TST}$			240		ns
<b>Bootstrap Diode</b>						
Forward Voltage	$V_F$	$I_F = 40\text{ mA}, T_A = 25\text{ }^\circ\text{C}$	0.70	0.85	1.0	V



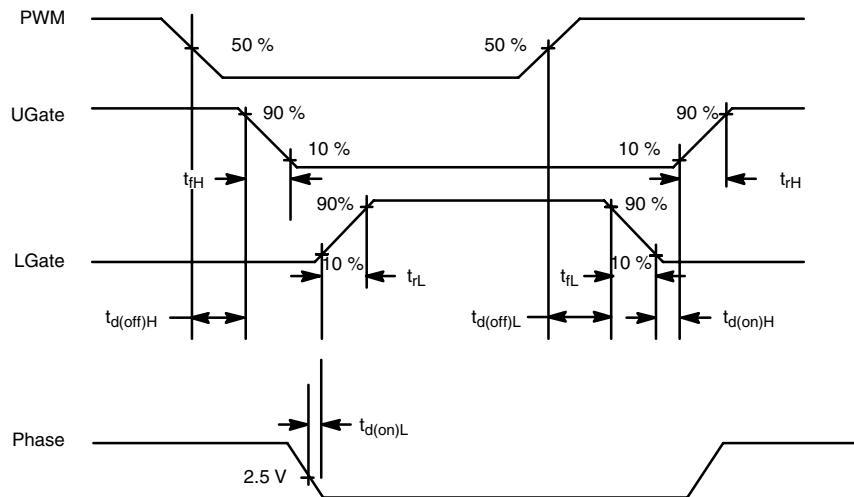
SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Specified $V_{CC} = 12\text{ V}$ , $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$		Limits			Unit
				Min. <sup>a</sup>	Typ. <sup>b</sup>	Max. <sup>a</sup>	
<b>MOSFET Drivers</b>							
High-Side Drive Current <sup>c</sup>	$I_{PKH(source)}$	$V_{BOOT} - V_{PHASE} = 8\text{ V}$			0.8		A
	$I_{PKH(sink)}$				1.0		
Low-Side Drive Current <sup>c</sup>	$I_{PKL(source)}$	$V_{PVCC} = 8\text{ V}$	SiP41110		0.9		
	$I_{PKL(sink)}$				1.2		
	$I_{PKL(source)}$	$V_{PVCC} = 12\text{ V}$	SiP41109		1.4		
	$I_{PKL(sink)}$				1.8		
High-Side Driver Impedance	$R_{DH(source)}$	$V_{BOOT} - V_{PHASE} = 8\text{ V}$ , PHASE = GND			2.3	4.2	$\Omega$
	$R_{DH(sink)}$				1.9	3.5	
Low-Side Driver Impedance	$R_{DL(source)}$	$V_{PVCC} = 8\text{ V}$	SiP41110		2.9	5.2	
	$R_{DL(sink)}$				1.3	2.4	
	$R_{DL(source)}$	$V_{PVCC} = 12\text{ V}$	SiP41109		2.4	4.3	
	$R_{DL(sink)}$				1.2	2.2	
High-Side Rise Time	$t_{rH}$	10% - 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ , $C_{LOAD} = 3\text{ nF}$			45		ns
High-Side Fall Time	$t_{fH}$				35		
High-Side Rise Time Bypass		10% - 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ , $C_{LOAD} = 3\text{ nF}$			45		
High-Side Fall Time Bypass					35		
High-Side Propagation Delay <sup>c</sup>	$t_{d(off)H}$	See Timing Waveforms			15		
	$t_{d(on)H}$				15		
Low-Side Rise Time	$t_{rL}$	10% to 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41110		40		
		10% to 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41109		40		
Low-Side Fall Time	$t_{fL}$	10% to 90%, $V_{BOOT} - V_{PHASE} = 8\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41110		30		
		10% to 90%, $V_{BOOT} - V_{PHASE} = 12\text{ V}$ $C_{LOAD} = 3\text{ nF}$	SiP41109		30		
Low-Side Propagation Delay	$t_{d(off)L}$	See Timing Waveforms			15		
	$t_{d(on)L}$				15		
<b>PHASE Timer</b>							
PHASE Falling Timeout <sup>c</sup>	$t_{PHASE}$				380		ns
<b>PV<sub>CC</sub> Regulator</b>							
Output Voltage	$V_{VCC}$			7.6	8	8.4	V
Output Current	$I_{PVCC}$				80	100	mA
Current Limit	$I_{LIM}$	$V_{DRV} = 0\text{ V}$		120	200	280	
Line Regulation	LNR	$V_{CC} = 10.8\text{ V}$ to $13.2\text{ V}$			0.05	0.5	%/V
Load Regulation	LDR	5 mA to 80 mA			0.1	1.0	%
<b>PV<sub>CC</sub> Regulator UVLO</b>							
PV <sub>CC</sub> Rising	$V_{UVLO2}$				6.7	7.2	V
PV <sub>CC</sub> Falling					6.4	6.9	
Hysteresis	Hyst			100	300	500	mV
<b>High-Side Undervoltage Lockout</b>							
Threshold	$V_{UVHS}$	Rising or falling		2.5	3.35	4.0	V
<b>V<sub>CC</sub> Undervoltage Lockout</b>							
Threshold	$V_{UVLO1}$			5.0	5.3	5.6	V
Power on Reset Time	POR				2.5		ms
<b>Thermal Shutdown</b>							
Temperature	$T_{SD}$	Temperature rising			165		$^\circ\text{C}$
Hysteresis	$T_H$	Temperature falling			25		

Notes:

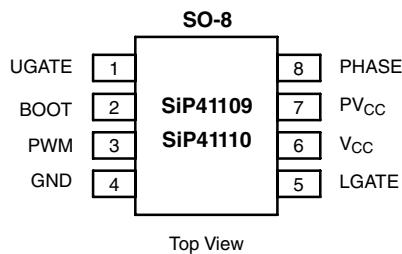
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing and are measured at  $V_{CC} = 12\text{ V}$  unless otherwise noted.

## TIMING WAVEFORMS



## PIN CONFIGURATION AND TRUTH TABLE



TRUTH TABLE		
PWM	UGATE	LGATE
L	L	H
L	H	L
Tri-State	L	L

ORDERING INFORMATION		
Part Number	Temperature Range	Marking
SiP41109DY-T1-E3	- 40 °C to 85 °C	41109
SiP41110DY-T1-E3		41110
Eval Kit	Temperature Range	
SiP41109DB	- 40 °C to 85 °C	
SiP41110DB		

PIN DESCRIPTION		
Pin Number	Name	Function
1	UGATE	8 V high-side MOSFET gate drive
2	BOOT	Bootstrap supply for high-side driver. The bootstrap capacitor is connected between BOOT and PHASE.
3	PWM	Input signal for the MOSFET drivers and tri-state enable
4	GND	Ground
5	LGATE	Synchronous or low-side MOSFET gate drive
6	V <sub>CC</sub>	12 V supply. Connect a bypass capacitor ≥ 1 μF from here to ground
7	PV <sub>CC</sub>	8 V voltage regulator Output. Connect a bypass capacitor ≥ 1 μF from here to ground
8	PHASE	Connection to source of high-side MOSFET, drain of the low-side MOSFET, and the inductor

**FUNCTIONAL BLOCK DIAGRAM**

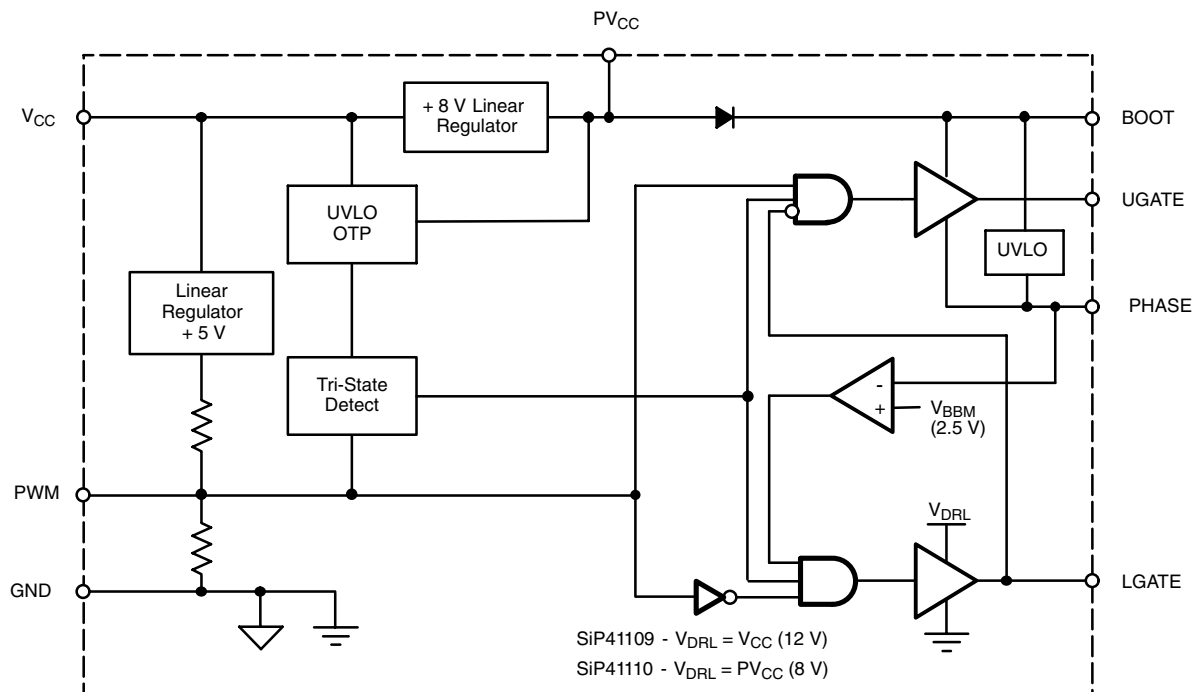


Figure 1.

**DETAILED OPERATION**

**PWM/Tri-State Enable**

The PWM pin controls the switching of the external MOSFETs. The driver logic operates in a noninverting configuration. The PWM input stage should be driven by a signal with fast transition times, like those provided by a PWM controller or logic gate, (< 200 ns). The PWM input functions as a logic input and is not intended for applications where a slow changing input voltage is used to generate a switching output when the input switching threshold voltage is reached.

**Shutdown**

The SiP41109/41110 enters shutdown mode when the signal driving PWM enters the tri-state window for more than 240 ns. The shutdown state is removed when the PWM signal moves outside the tri-state window. If the PWM is left open, the pin is held to 2.5 V by an internal voltage divider, thus forcing the tri-state condition.

**Low-Side Driver**

In the SiP41109, the low-side driver voltage is supplied by  $V_{CC}$ . In the SiP41110, the low-side driver voltage is supplied by  $PV_{CC}$ . During shutdown, LGATE is held low.

**High-Side Driver**

The high-side driver is isolated from the substrate to create a floating high-side driver so that an N-channel MOSFET can be used for the high-side switch. The high-side driver voltage is supplied by  $PV_{CC}$ . The voltage is maintained by a floating bootstrap capacitor, which is continually recharged by the switching action of the output. During shutdown UGATE is held low.

**Gate Drive Voltage ( $PV_{CC}$ ) Regulator**

An integrated 80 mA, 8 V regulator supplies voltage to the  $PV_{CC}$  pin and it current limits at 200 mA typical when the output is shorted to ground. A capacitor (1  $\mu$ F minimum) must be connected to the  $PV_{CC}$  pin to stabilize the regulator output. The voltage on  $PV_{CC}$  is supplied to the integrated bootstrap diode.  $PV_{CC}$  is used to recharge the bootstrap capacitor and powers the SiP41110 low-side driver.  $PV_{CC}$  pin can be externally connected to  $V_{CC}$  to bypass the 8 V regulator and increase high-side gate drive to 12 V. If the  $PV_{CC}$  pin is connected to  $V_{CC}$  the system voltage should not exceed 43 V.

**Bootstrap Circuit**

The internal bootstrap diode and an external bootstrap capacitor supply voltage to the BOOT pin. An integrated bootstrap diode replaces the external diode normally needed

## Vishay Siliconix

for the bootstrap circuit; only a capacitor is necessary to complete the bootstrap circuit. The bootstrap capacitor is sized according to

$$C_{BOOT} = (Q_{GATE} / (\Delta V_{BOOT} - V_{PHASE})) \times 10$$

where  $Q_{GATE}$  is the gate charge needed to turn on the high-side MOSFET and  $\Delta V_{BOOT} - V_{PHASE}$  is the amount of droop allowed in the bootstrapped supply voltage when the high-side MOSFET is driven high. The bootstrap capacitor value is typically 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ . The bootstrap capacitor voltage rating must be greater than  $V_{CC} + 12\text{ V}$  to withstand transient spikes and ringing.

### Shoot-Through Protection

The external MOSFETs are prevented from conducting at the same time during transitions. Break-before-make circuits monitor the voltages on the PHASE pin and the LGATE pin and control the switching as follows: When the signal on PWM goes low, UGATE will go low after an internal propagation delay. After the voltage on PHASE falls below 2.5 V by the inductor action, the low-side driver is enabled and LGATE goes high after some delay. When the signal on PWM goes high, LGATE will go low after an internal propagation delay. After the voltage on LGATE drops below

2.5 V the high-side driver is enabled and UGATE will go high after an internal propagation delay. If PHASE does not drop below 2.5 V within 380 ns after UGATE goes low, LGATE is forced high until the next PWM transition.

### $V_{CC}$ Bypass Capacitor

MOSFET drivers draw large peak currents from the supplies when they switch. A local bypass capacitor is required to supply this current and reduce power supply noise. Connect a 1  $\mu\text{F}$  ceramic capacitor as close as practical between the  $V_{CC}$  and GND pins.

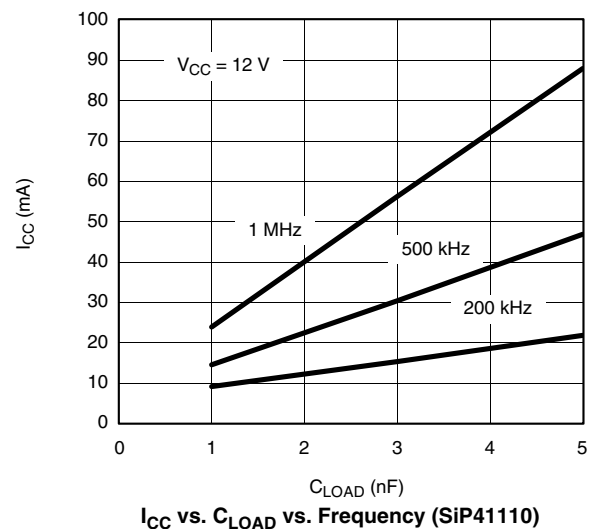
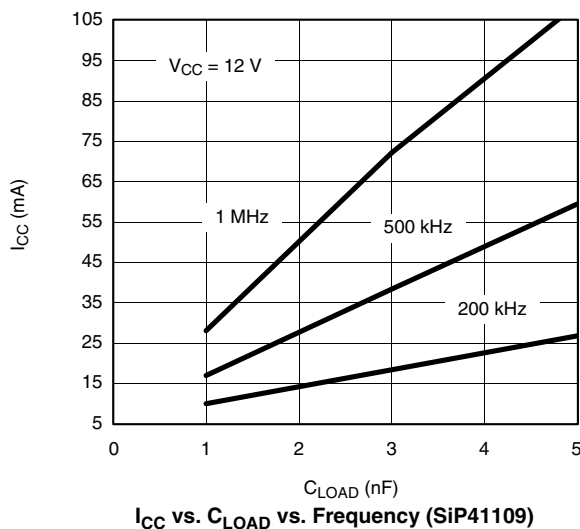
### Undervoltage Lockout

Undervoltage lockout prevents control of the circuit until the supply voltages reach valid operating levels. The UVLO circuit forces LGATE and UGATE to low when  $V_{CC}$  is below its specified voltage. A separate UVLO forces UGATE low when the voltage between BOOT and PHASE is below the specified voltage.

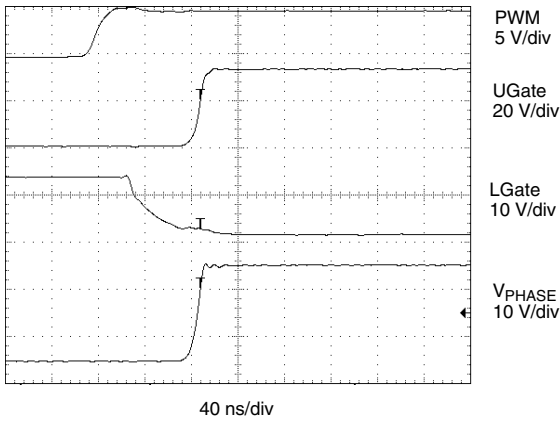
### Thermal Protection

If the die temperature rises above 165  $^{\circ}\text{C}$ , the thermal protection disables the drivers. The drivers are re-enabled after the die temperature has decreased below 140  $^{\circ}\text{C}$ .

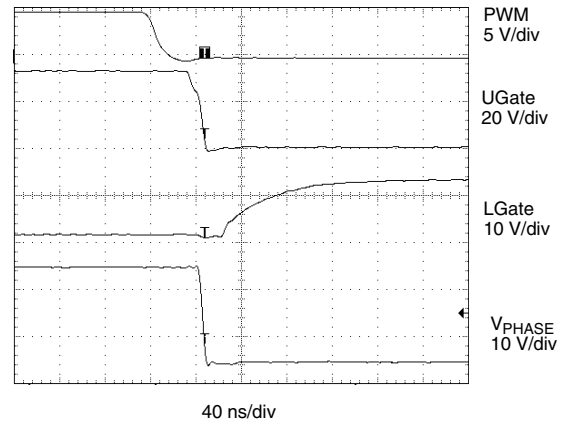
## TYPICAL CHARACTERISTICS



**TYPICAL WAVEFORMS**



**Figure 2. PWM Signal vs. HS Gate, LS Gate and PHASE (Rising)**



**Figure 3. PWM Signal vs. HS Gate, LS Gate and PHASE (Falling)**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?73023](http://www.vishay.com/ppg?73023).



## Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk and agree to fully indemnify and hold Vishay and its distributors harmless from and against any and all claims, liabilities, expenses and damages arising or resulting in connection with such use or sale, including attorneys fees, even if such claim alleges that Vishay or its distributor was negligent regarding the design or manufacture of the part. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.