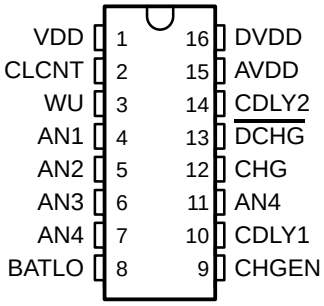
SLUS236B – JANUARY 1999 – REVISED SEPTEMBER 2002

THREE- OR FOUR-CELL LITHIUM-ION PROTECTOR CIRCUIT

FEATURES

- **Three- or Four-Cell Operation**
- **Two-Tier Overcurrent Limiting**
- **30-μA Typical Supply-Current Consumption**
- **3.5-μA Typical Supply Current in Sleep Mode**
- ***Smart Discharge* Minimizes Losses in Overcharge Mode**
- **6.5-V to 20-V VDD Supply Range**
- **Highly Accurate Internal Voltage Reference**
- **Externally Adjustable Delays in Overcurrent Controller**
- **Detection of Loss-of-Cell Sense Connections**

M PACKAGE
(TOP VIEW)



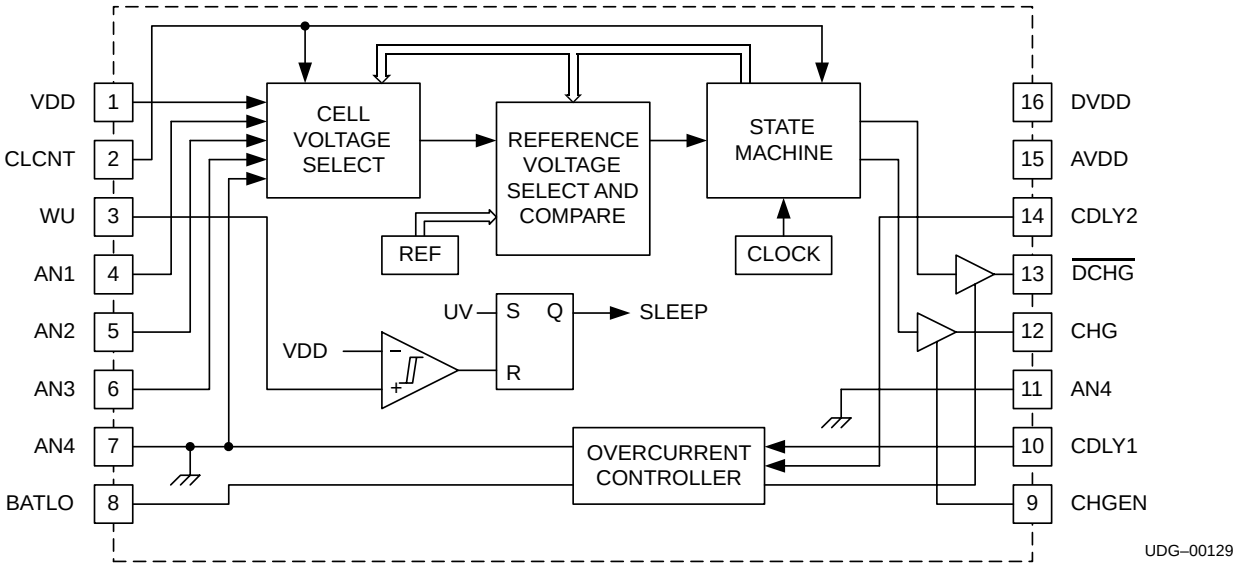
DESCRIPTION

The UCC3957 is a BiCMOS three- or four-cell lithium-ion battery pack protector designed to operate with external P-channel MOSFETs. Utilizing external P-channel MOSFETs provides the benefits of no loss-of-system ground in an overdischarge state, and protects the IC as well as battery cells from damage during an overcharge state. An internal state machine runs continuously to protect each lithium-ion cell from overcharge and overdischarge. A separate overcurrent-protection block protects the battery pack from excessive discharge currents.

If any cell voltage exceeds the overvoltage threshold, the appropriate external P-channel MOSFET is turned off, preventing further charge current. An external N-channel MOSFET is required to level shift to this high-side P-channel MOSFET. Discharge current can still flow through the second P-channel MOSFET. Likewise, if any cell voltage falls below the undervoltage limit, the second P-channel MOSFET is turned off and only charge current is allowed. Such a cell-voltage condition causes the chip to go into low-power sleep mode. Attempting to charge the battery pack wakes up the chip. A cell-count pin (CLCNT) is provided to program the IC for three- or four-cell operations.

A two-tiered overcurrent controller and external current shunt protect the battery pack from excessive discharge currents. If the first overcurrent threshold level is exceeded, an internal timing circuit charges an external capacitor to provide a user programmable blanking time. If at the end of the blanking time the overcurrent condition still exists, the external discharge FET is turned off for a period 17 times longer than the first blanking period, and then the discharge FET is turned back on. If at any time a second higher overcurrent threshold is exceeded for more than a user programmable time, the discharge FET is turned off, and remains off for the same period as the first tier off time. This two tiered overcurrent-protection scheme allows for charging capacitive loads while retaining effective short-circuit protection.

block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply voltage (VDD) . . . . . 20 V
Supply current . . . . . 25 mA
Output current . . . . . 25 mA
Input voltage: (WU) . . . . . 24 V
(AN1, AN2, AN3) . . . . . VAN4 – VDD
(CLCNT, CHGEN) . . . . . 15 V
Input voltage range (BATLO) . . . . . –0.3 V to 2.5 V
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Operating virtual junction temperature range, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 seconds) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals. Consult *Packaging Information* section of the *Portable Products Databook* (TI Literature No. SLUD001) for thermal limitations and considerations of packages. All voltages are referenced to the AN4 terminal.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES† SSOP (M)			
	NORMAL TO OVERCHARGE VOLTAGE (V)			
	4.20	4.25	4.30	4.35
–20°C to 70°C	UCC3957M–1	UCC3957M–2	UCC3957M–3	UCC3957M–4

† The M package is available taped and reeled. Add TR suffix to device type (e.g. UCC3957M–1TR) to order quantities of 2500 devices per reel.

electrical characteristics over recommended operating free-air temperature range, VDD = 16 V, –20°C < T_A < 70°C, T_A = T_J. (unless otherwise noted)

supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_{min}	Minimum VDD			5.0	5.5	V
IDD	Supply current			30	40	µA
I_{SL}	Sleep-mode supply current	VDD = 10.4 V		3.5	7.5	µA
V_{IN}	Input voltage for WU	See Note 2			20	V

output

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{\overline{DCHG}}$	$\overline{DCHG}$ output current	Driving-logic low,	V_O = 1 V	40	70	100	µA
		Driving-logic high,	V_O = (VDD – 1)		–13	–3	mA
I_{CHG}	CHG ouput current	Driving-logic low,	V_O = 1 V	40	70	100	µA
		Driving-logic high,	V_O = (VDD – 1V)		–15	–3	mA

state transitions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OV}	Normal to overcharge voltage	See Note 1	UCC3957–1	4.15	4.20	4.25	V
V_{OVR}	Overcharge to normal voltage			3.95	4.00	4.05	V
V_{OV}	Normal to overcharge voltage	See Note 1	UCC3957–2	4.20	4.25	4.30	V
V_{OVR}	Overcharge to normal voltage			4.00	4.05	4.10	V
V_{OV}	Normal to overcharge voltage	See Note 1	UCC3957–3	4.25	4.30	4.35	V
V_{OVR}	Overcharge to normal voltage			4.05	4.10	4.15	V
V_{OV}	Normal to overcharge voltage	See Note 1	UCC3957–4	4.30	4.35	4.40	V
V_{OVR}	Overcharge to normal voltage			4.10	4.15	4.20	V
V_{UV}	Undercharge to normal voltage	See Note 1		2.5	2.6	2.7	V
V_{UVR}	Normal to undercharge voltage			2.2	2.3	2.4	V
td_{OV}	Overvoltage to CHG delay			8	17	23	ms
td_{UV}	Undervoltage to $\overline{DCHG}$ Delay			8	17	23	ms
t_S	Cell sample rate			4	8.5	11.5	ms
V_{SM}	Smart discharge threshold	BATLO voltage		4	15	25	mV
V_{WU}	Wakeup input threshold	With respect to VDD		50	230	750	mV
V_{CE}	Charge-enable input threshold			0.8	1.3	2.6	V

short-circuit protection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CL1}	First-tier threshold level	V_{BATLO}	120	150	190	mV
V_{CL2}	Second-tier threshold level	V_{BATLO}	275	375	450	mV
t_{B1}	First-tier blanking time	CDLY1 = 0.1 µF	30	50	70	ms
t_{RST}	Restart time	CDLY1 = 0.1 µF	300	500	700	ms
t_{B2}	Second-tier blanking time	CDLY2 = 10 pF	100	400	600	µs

NOTE 1: Other overvoltage or undervoltage thresholds are available. Please consult the factory.

2: Refer to Figure 6, for WU leakage characteristics.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AN1	4	I	Connects to the negative terminal of the top battery cell and the positive terminal of the second battery cell.
AN2	5	I	Connects to the bottom terminal of the second battery cell and the top terminal of the third battery cell.
AN3	6	I	Connects to the bottom terminal of the third battery cell and the top terminal of the fourth battery cell in a four cell stack. In a three cell pack it connects to the bottom terminal of the third battery and to AN4.
AN4	7	I	Connects to the bottom terminal of the battery stack and the top of the current sense resistor.
AVDD	15	O	Internal analog supply bypass cap pin. Connect a 0.1-μF capacitor between this pin and AN4. This pin is nominally 7.3 V.
BATLO	8	I	Connects to the bottom of the current sense resistor and the negative terminal of the battery pack.
CHGEN	9	I	The charge enable input for the protection IC. This point must be driven high to DVDD or AVDD to allow charging of the battery pack. This pin has a very weak pulldown.
CDLY1	10	O	Delay control pin for the short-circuit protection feature. A capacitor connected between this point and AN4 determines the time delay from when an overcurrent situation is detected to when the FET is turned off. This capacitor also controls the hiccup mode timeout period.
CDLY2	14	O	An external cap can be tied between this pin and AN4 to extend the blanking time on the second current limit tier.
CLCNT	2	I	This pin programs the IC for three or four cell operation. Tying this pin low (to AN4) sets four cell operation, while tying it high (to DVDD or AVDD) sets three cell operation. This pin is internally pulled low, so open circuit conditions always result in four-cell mode.
$\overline{\text{DCHG}}$	13	O	This pin is used to prevent overdischarge. If the state machine indicates that any cell is undervoltage, this pin is driven high with respect to chip substrate so that the external P-channel MOSFET prevents further discharge. If all cell voltages are above the minimum threshold, this pin is driven low.
CHG	12	O	This pin is used to control an external N-channel MOSFET, which in turn drives a P-channel MOSFET. If at least one cell voltage is over the overvoltage threshold, this pin is driven low with respect to AN4. If all cell voltages are below this threshold, this pin is driven high.
DVDD	16	O	Internal digital supply bypass capacitor pin. Connect a 0.1-μF capacitor between this pin and AN4. This pin is nominally 7.3V.
VDD	1	I	Supply voltage to the IC. Connect this point to the top of the lithium-ion battery stack.
WU	3	I	This pin is used to provide a wakeup signal to the IC during sleep mode. Connect this pin to the drain of the N-channel level shift MOSFET.

APPLICATION INFORMATION

overview

The UCC3957 provides complete protection against overdischarge, overcharge and overcurrent for a three- or four-cell lithium-ion battery pack. It uses a *flying capacitor* technique to sample the voltage across each battery cell and compare it to a precision reference. If any cell is in overvoltage or undervoltage, the internal-state machine takes the appropriate action to prevent further charge or discharge. High-side P-channel MOSFETs are used to independently control charge and discharge current. Figure 1 shows a three-cell lithium-ion protector application diagram with the optional charge-enable switch. In this application, the diode D1 protects the MOSFET Q2 from inductive kick at turn-off.

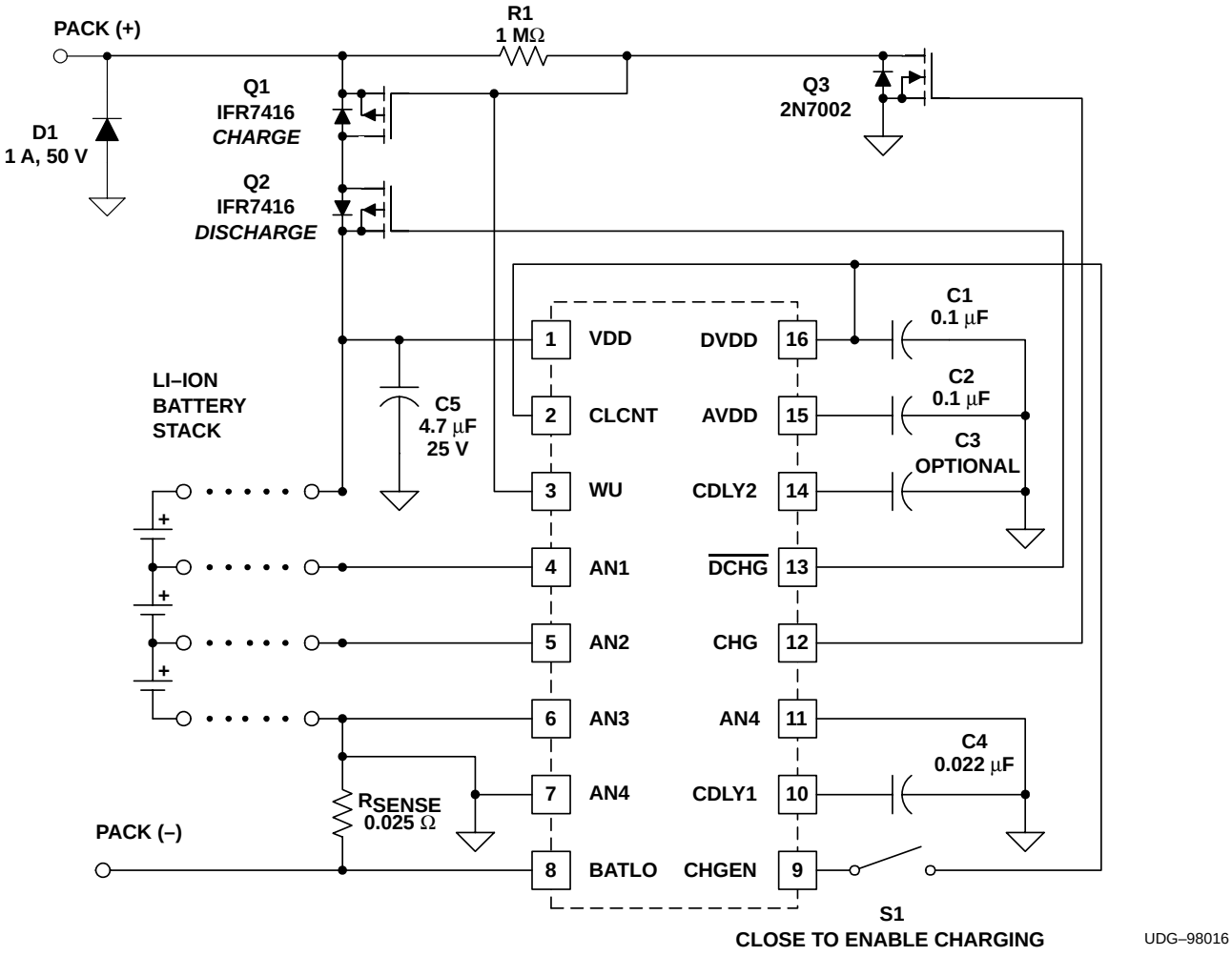


Figure 1. Three-Cell Lithium-Ion Protector Application Diagram

APPLICATION INFORMATION

overview (continued)

Figure 2 shows a four-cell protector with optional components to protect the charge FET from excessive gate-to-source transients. In this application, the Zener diode VR1 and the resistor R2 are optional. They protect the MOSFET Q1 from excessive open-circuit charger voltage. Diode D1 protects MOSFET Q2 from inductive kick during turn-off.

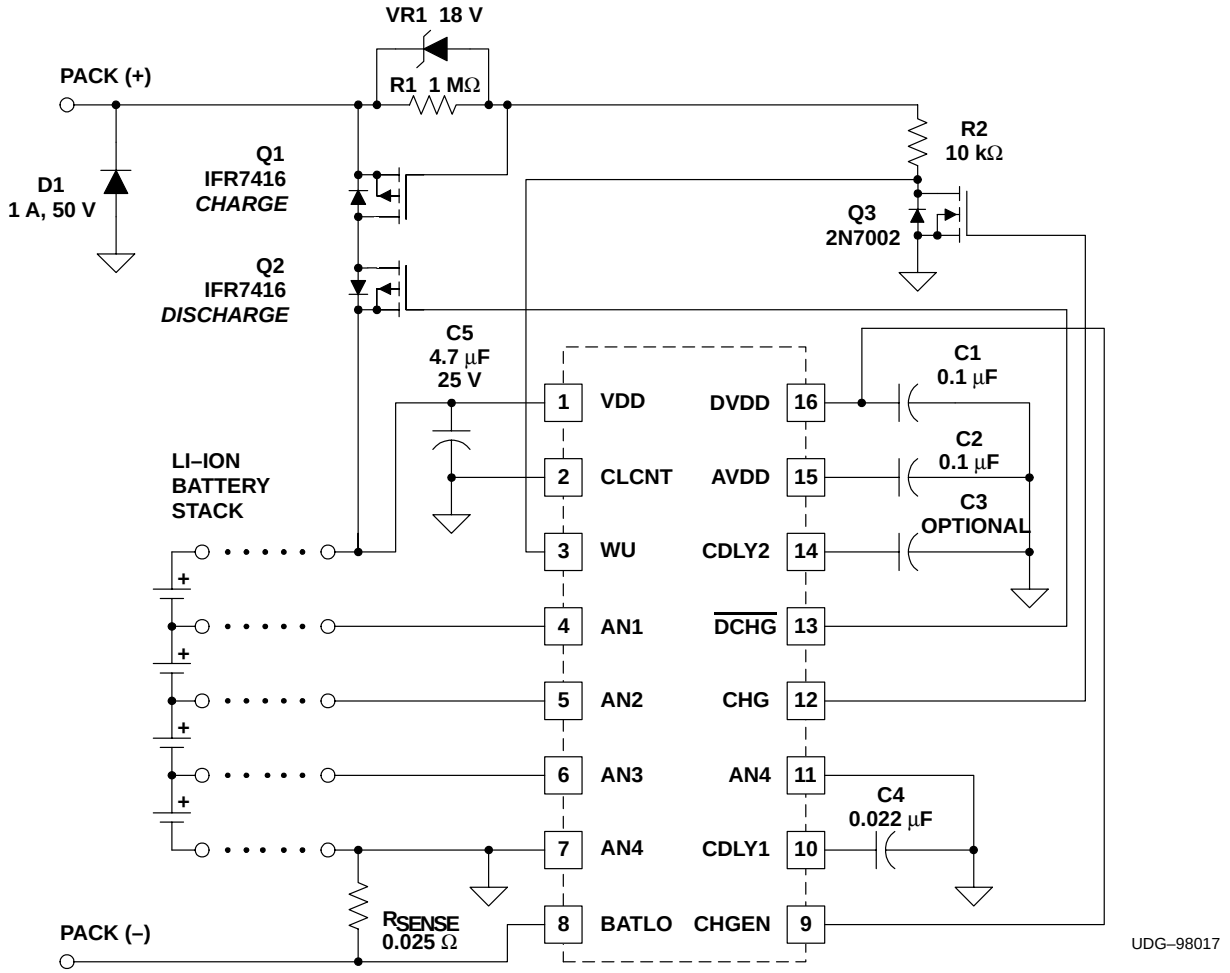


Figure 2. Four-Cell Lithium-Ion Protector Application Diagram

connecting the cell stack

When connecting the cell stack to the circuit, it is important to do so in the proper order. First, the bottom of the stack should be connected to AN4 . Next, the top of the stack should be connected to VDD. The cell taps can then be connected to AN1, AN2, and AN3 in any order.

choosing three or four cells

For three-cell packs, the cell-count pin (CLCNT) should be connected to the DVDD pin, and the AN3 pin should be tied to the AN4 pin. For four-cell applications, the CLCNT pin should be grounded (to AN4) and the AN3 pin is connected to the positive terminal of the bottom cell in the stack.

APPLICATION INFORMATION

undervoltage protection

When any cell is found to be overdischarged (below the normal-to-undercharge threshold), the state machine turns off both high-side FETs and enters the sleep mode, where current consumption drops to about 3.5 μA. It remains in sleep mode until the application of a charger is sensed by the wakeup pin (WU) being raised above VDD.

charging

Once a charger has been applied, the charge FET is turned on as long as the charge-enable input pin (CHGEN) is pulled up to the DVDD pin. If the CHGEN input is left open (or connected to AN4), the charge FET remains off.

During charge, the charge and discharge FETs cycle on and off while the device is in the sleep state (undercharge mode), until the cell voltages are all above the undercharge-to-normal threshold. Once the cell voltages are above this threshold, the device enters the normal state and the FETs remain on continuously. While the device is charging and in undercharge mode, there is an approximate on time of 8 ms corresponding to one sampling period, with a very short off time corresponding to undercharge-voltage detect and sleep-mode; once WU is pulled back up to PACK(+), wake-up detect again occurs, and a new sampling period/charge cycle is initiated.

open wire protection

The UCC3957 provides protection against broken-cell sense connections within the pack. If the sense connection to one of the cells (pins AN1, AN2, or AN3) should become disconnected, weak internal-current sources make the cells that are connected to that wire appear to be in overcharge and charging of the pack is prevented.

overvoltage protection and the *smart discharge* feature

If any cell is charged to a voltage exceeding the normal-to-overcharge threshold, the charge FET is turned off, preventing further charge current. Hysteresis keeps the charge FET off until the cell voltages have dropped below the overcharge-to-normal threshold. In most protector designs, the charge FET is held off completely within this voltage band. During this time, discharge current must be conducted through the body diode of the charge FET. This forward voltage drop can be as high as 1 V, causing significant power dissipation in the charge FET and wasting precious battery power.

The UCC3957 has a unique *smart discharge* feature that allows the charge FET to return to on mode (for discharge only) while still in the overcharge hysteresis band. This greatly reduces power dissipation in the charge FET. This is accomplished by sensing the voltage drop across the current-sense resistor. If this drop exceeds 15 mV (corresponding to 0.6 A of discharge current using a .025 Ω sense resistor), the charge FET is turned back on. This threshold assures that only discharge current is conducted. In an example using a 20-mW FET with a 1-V body diode drop and a 1-A load, the power dissipation in Q1 would be reduced from 1 W to 0.02 W.

> **NOTE:** A similar technique is not used during charge (when the discharge MOSFET is off due to cells being in undervoltage) because the charge current should be low while the cells are in undervoltage.

APPLICATION INFORMATION

protection against a runaway charger

The use of a small N-channel level shifter (Q3 in the application diagrams) allows the IC to interface with the high-side charge FET (Q1), even in the presence of a runaway charger. Only the drain-source voltage rating of the charge FET limits the charge voltage that the protection circuit can withstand. The wakeup (WU) pin is designed to handle input voltages greater than VDD, as long as the current is limited. In the examples shown, the charge FET's gate-source resistor (R1) provides this current limiting. Note that in Figure 2, a resistor and zener (R2 and VR1) have been added to protect Q1 against any possibility of a voltage transient exceeding its maximum gate-source rating.

overcurrent protection

The UCC3957 protects the battery pack from an overload or a hard short circuit using a two-tier overcurrent protection scheme. The overcurrent protection is designed to go into a hiccup mode when the voltage drop across an external-sense resistor (connected to the AN4 and BATLO pins) exceeds a certain threshold. In this mode, the discharge FET is periodically turned off and on until the fault is removed. Once the fault is removed, normal operation is automatically resumed.

To facilitate charging large capacitive loads, there are two overcurrent threshold voltages, each with its own user-programmable time delay. This two-tier approach provides fast response to short circuits, while enabling the battery pack to provide short-duration surge currents. It also facilitates the charging of large filter caps without causing nuisance overcurrent trips.

The first-tier threshold is 150 mV nominal, corresponding to 6 A using a .025-Ω sense resistor as shown in the examples of Figure 1 and Figure 2. If the pack-discharge current exceeds this amount for a period of time, determined by the capacitor on the CDLY1 pin, it then enters the hiccup mode. The first-tier hiccup duty cycle is fixed at approximately 6%, minimizing power dissipation in the event of a sustained overload. The absolute on and off times of the discharge FET (Q2) are controlled by the CDLY1 capacitor. A curve relating the delay (on time) to this capacitor value is shown in Figure 4. The off time is approximately 17 times longer than the on time.

The second-tier overcurrent threshold is nominally 375 mV, corresponding to 15 A using a .025-Ω sense resistor. If the pack current exceeds this value for a period of time, determined by the capacitor on the CDLY2 pin, it then enters the hiccup-mode with a much lower duty cycle, typically less than 1%. The relationship of this time delay (on time) to the CDLY2 capacitor value is shown in the curve of Figure 5. The off time during this hiccup mode is still determined by the CDLY1 capacitor, as previously described. This technique greatly reduces the stress and power dissipation in the FETs during short-circuit conditions.

In the examples shown in Figure 1 and Figure 2 (with CDLY1 = .022 μF), the first-tier overcurrent on time is approximately 10 msec, while the off time is approximately 170 msec, resulting in a 5.9% duty cycle for currents over 6 A (but less than 15 A). If no CDLY2 capacitor is used, the second-tier on time is less than 200 μsec (assuming no stray capacitance), resulting in a duty cycle of about 0.1% for currents over 15 A. If CDLY2 = 22pF, the typical on time for currents exceeding 15 A is approximately 800 μsec, resulting in a duty cycle of 0.5%.

APPLICATION INFORMATION

protecting against inductive kick at turn-off

In the case of a short circuit, the di/dt that occurs when the discharge FET is turned off can result in a significant voltage undershoot at the pack output due to stray inductance. This undershoot can potentially exceed the breakdown voltage rating of the discharge FET. A clamp diode (D1 in Figure 1, Figure 2, and Figure 3), or a capacitor across the pack output, protects against this possibility. A diode also provides protection from a reverse-polarity charger.

During turn-off, a voltage overshoot can occur at the top of the cell stack, due to wiring inductance and the cells' internal equivalent series inductance (ESL). During very high di/dt conditions, such as occurs when turning off in response to a short circuit, this voltage overshoot can be significant and potentially damage the IC or the discharge FET (Q2). For this reason, it is strongly recommended that a capacitor (C5) be placed across the cell stack, from VDD to AN4, and that stray inductance be minimized in the battery-current path. Additional methods to reduce di/dt across the cell stack are discussed in the following section.

controlling discharge FET turn-on and turn-off times

Slew-rate limiting the pack output voltage at turn-on greatly reduces the surge current into large capacitive loads.

This allows the designer to select shorter overcurrent-delay times, minimizing the stress on Q1 and Q2 in the event of a shorted pack output. A simple method of implementing slew-rate limiting is shown in Figure 3. It consists of an RC network (R3 and C6) between gate and drain of the discharge FET (Q2) to control its turn-on time. This circuit relies on the relatively high-sink impedance (about 20 kΩ) of the UCC3957's $\overline{\text{DCHG}}$ output. The values shown for R3 and C6 provide a pack output voltage rise time of about 4.5 ms when the discharge FET (Q2) is turned on. Note that the addition of R3 and C6 has made it possible to eliminate the CDLY2 capacitor, for the quickest response to a true short circuit. While this circuit does not prevent a large surge current when inserting a *live* battery pack into a highly-capacitive load, it does allow it to restart (after one hiccup cycle) if this initial surge-current trips the overcurrent protection.

Increasing the turn-off time of the discharge FET (Q2) reduces the inductive kick that results during turn-off after an overcurrent condition. This is accomplished by adding a resistor (R4) in series with the $\overline{\text{DCHG}}$ output. This reduction of di/dt at turn-off minimizes the need for a capacitor across the battery stack. It is recommended that this resistor value not exceed a few hundred Ohms, in which case the ability to turn off quickly enough into a short may be compromised.

Due to the relatively low-charge currents (typically a few Amperes max), controlling the turn-on and turn-off times of the charge FET is not beneficial. In fact, the turn-off time of the charge FET is slow due to the large value of R1, the gate-to-source resistor.

APPLICATION INFORMATION

controlling discharge FET turn-on and turn-off times

Figure 3 shows a four-cell protector with slew-rate limiting the discharge FET. In this application, VR1 and R2 are optional, They protect Q1 from excessive open-circuit charger voltage. R3 and C6 are chosen based on capacitive load that must be driven. R4 minimizes inductive kick at turn-off.

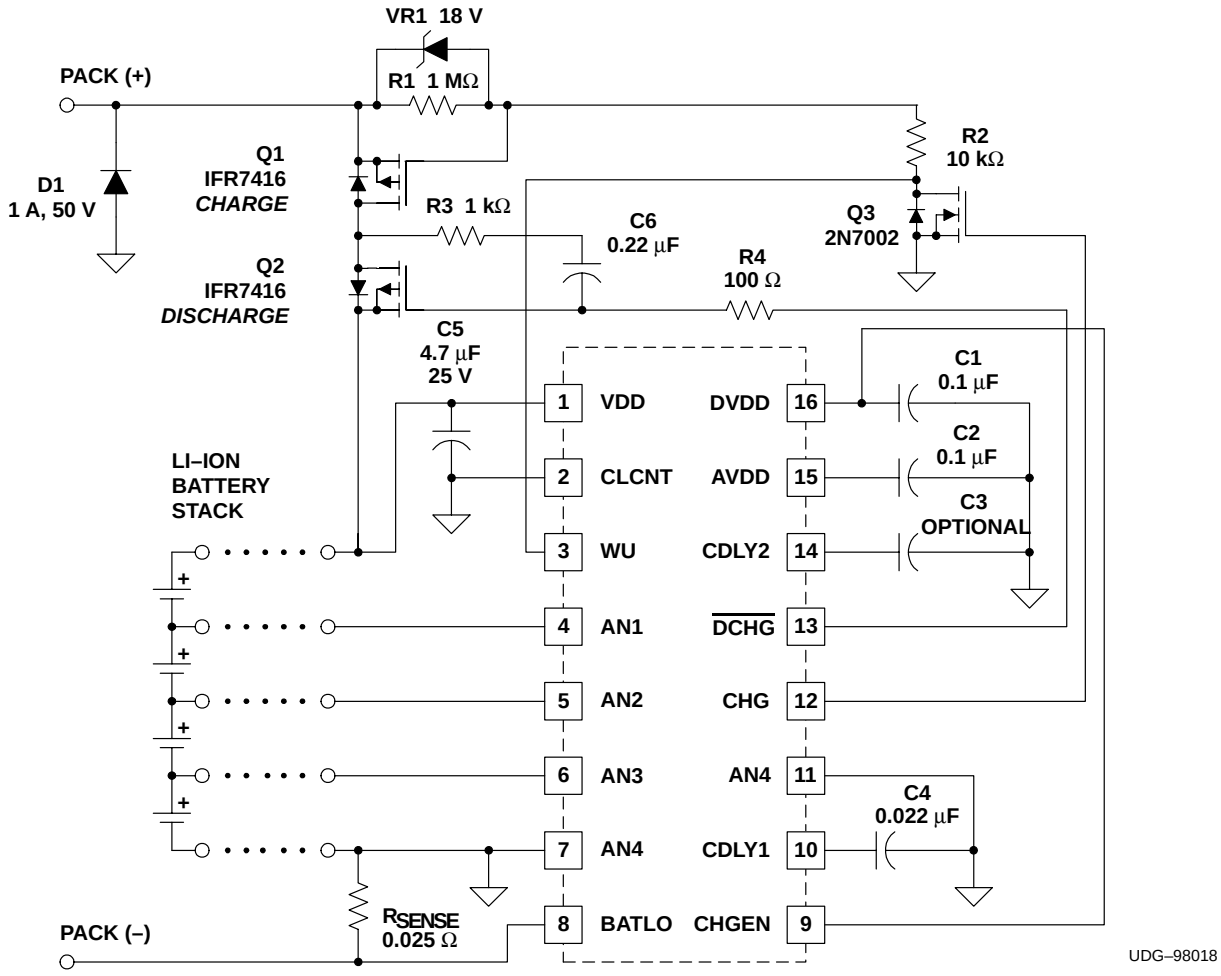


Figure 3. Four-Cell Lithium-Ion Protector Application Diagram

TYPICAL CHARACTERISTICS

TYPICAL TIER-ONE OVERCURRENT DELAY TIME vs DELAY CAPACITANCE

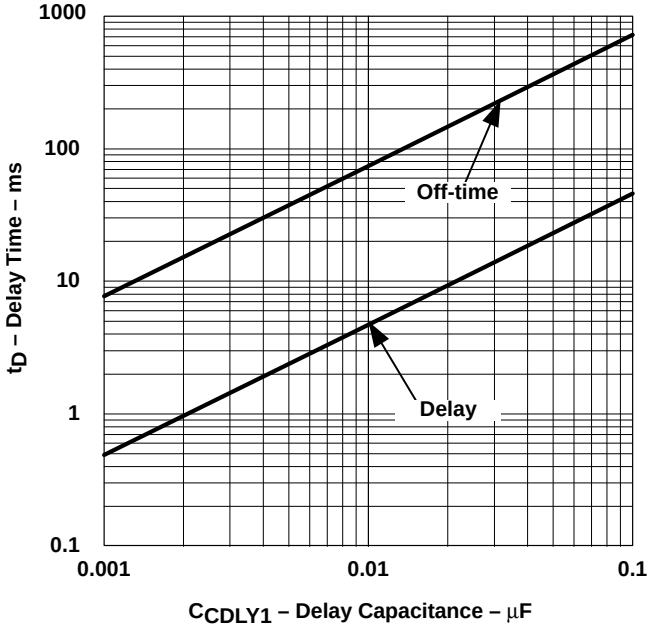


Figure 4

TYPICAL TIER-TWO OVERCURRENT DELAY TIME vs DELAY CAPACITANCE

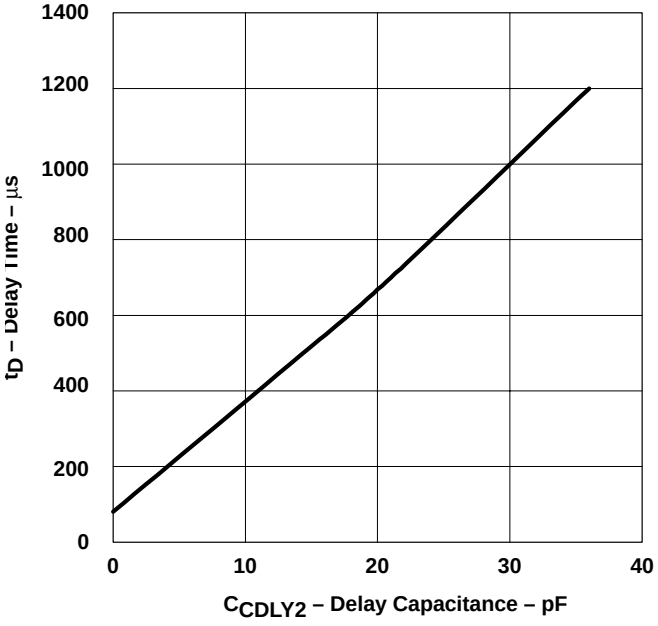


Figure 5

WU LEAKAGE CURRENT vs INPUT VOLTAGE

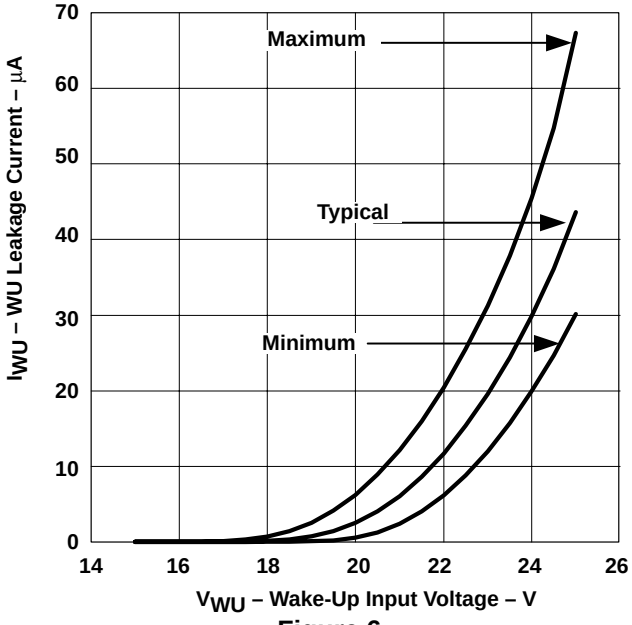


Figure 6

PACKAGING INFORMATION

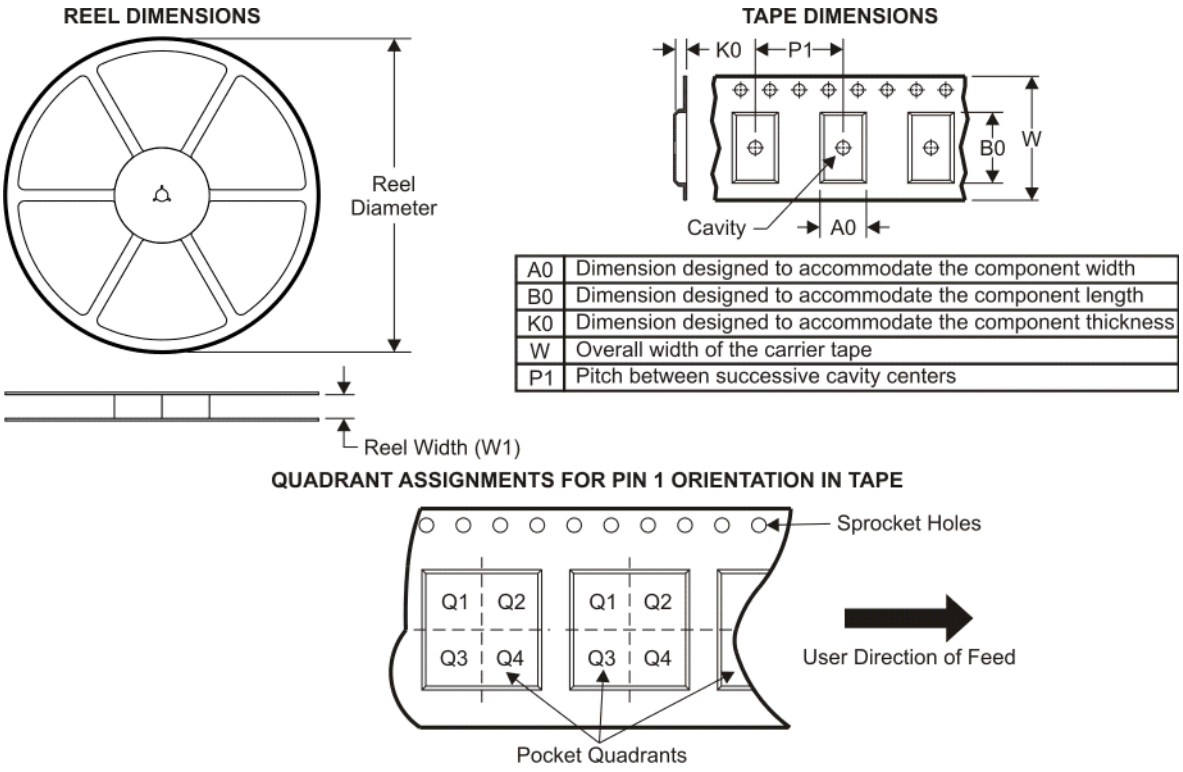
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC3957M-1	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-1G4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-2	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-2G4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-3	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-3G4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957M-4G4	ACTIVE	SSOP/ QSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-1	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
UCC3957MTR-1G4	ACTIVE	SSOP/ QSOP	DBQ	16		TBD	Call TI	Call TI
UCC3957MTR-2	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-2G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-3	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-3G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3957MTR-4G4	ACTIVE	SSOP/ QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

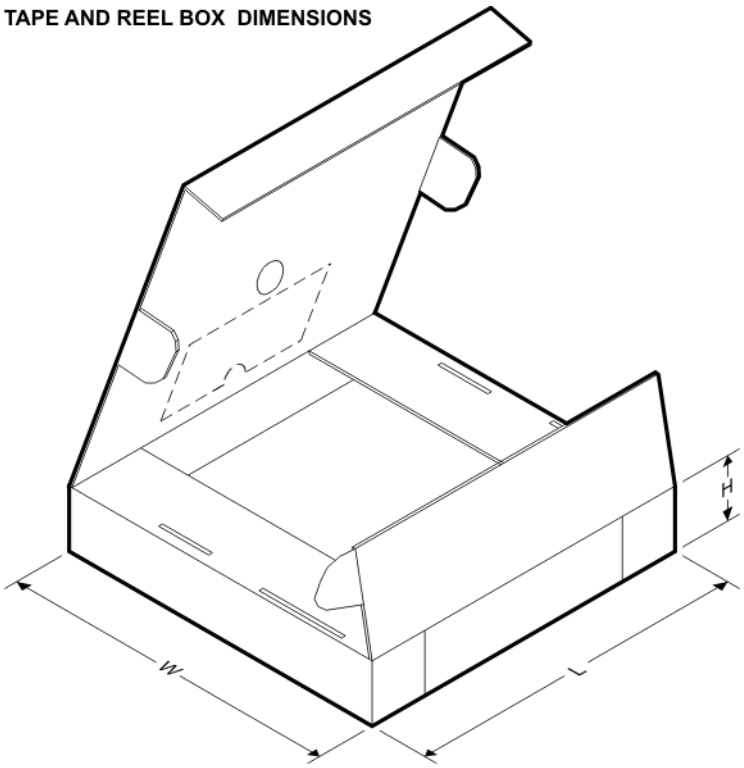


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3957MTR-2	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3957MTR-3	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3957MTR-4	SSOP/ QSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

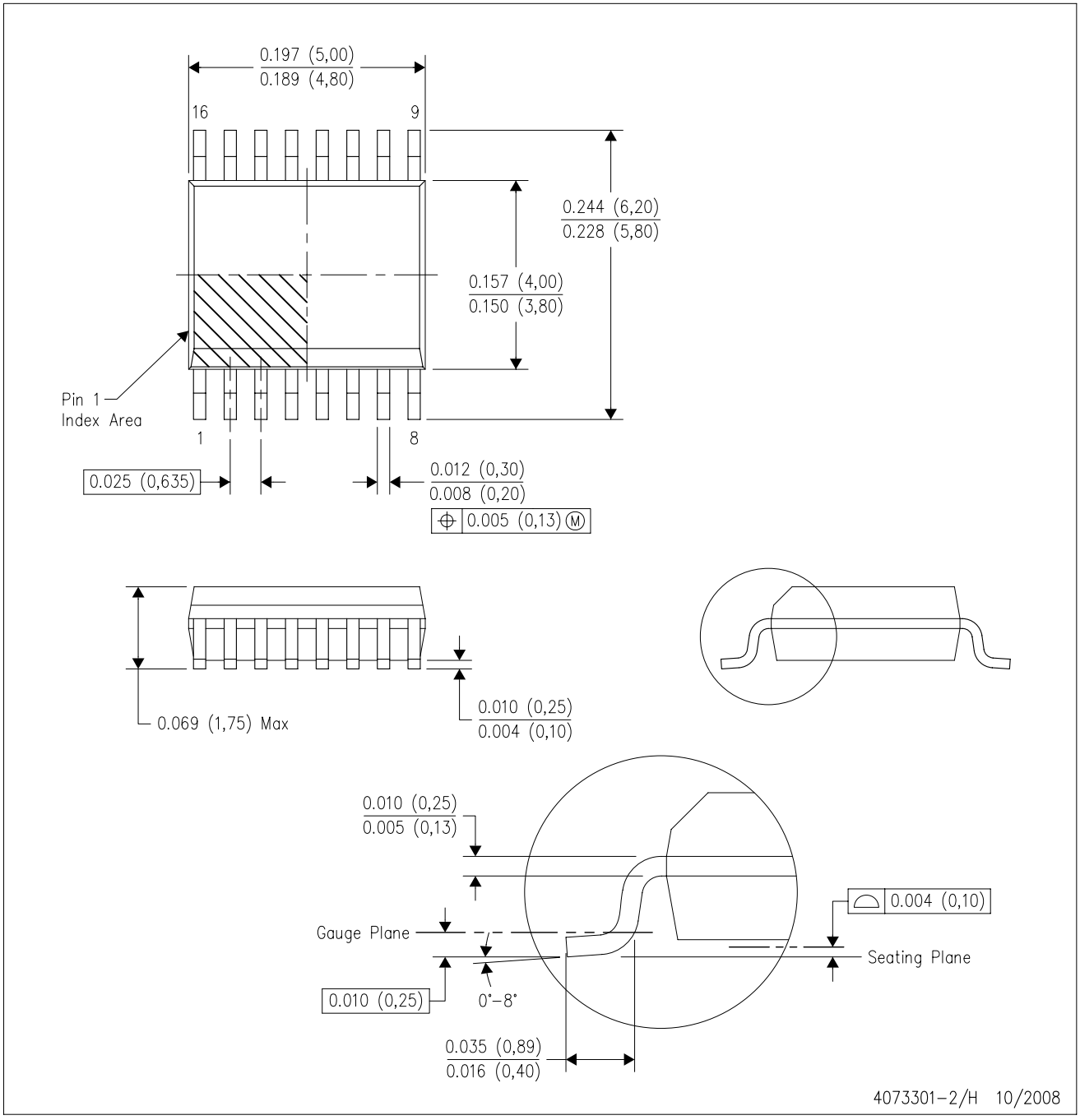
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

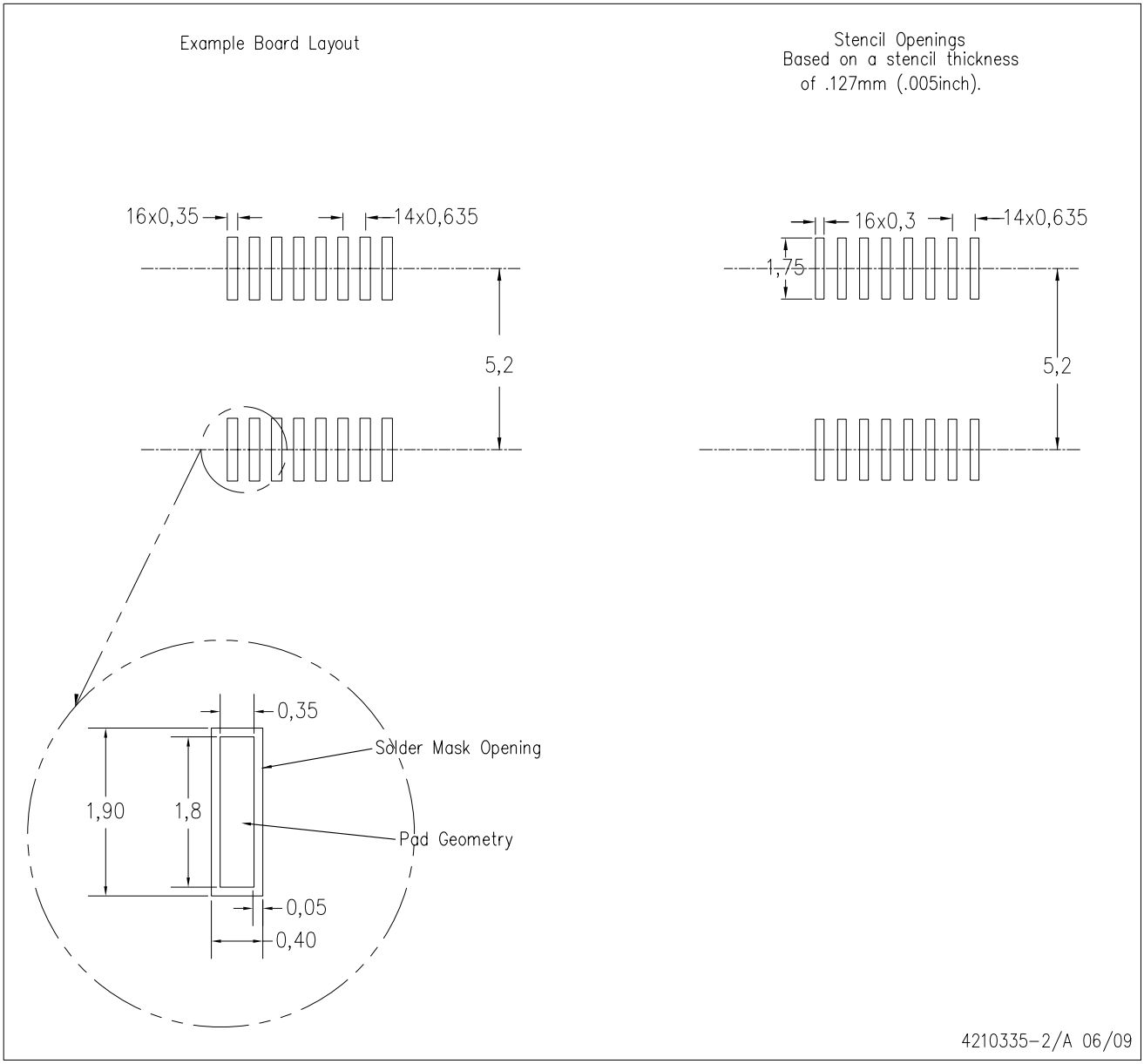
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3957MTR-2	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0
UCC3957MTR-3	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0
UCC3957MTR-4	SSOP/QSOP	DBQ	16	2500	346.0	346.0	29.0

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

DBQ (R–PDSO–G16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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