good memories start here

MTS800 – SATA III 6Gb/s M.2 SSD

Transcend MTS800 series are M.2 SSDs with high performance and quality Flash Memory assembled on a printed circuit board. These M.2 SSDs feature cutting-edge technology to enhance product life and data retention. MTS800 is designed specifically for various applications such as Ultrabooks, industrial PCs, vehicle PCs and road surveillance recording.

- Power Supply: 3.3V±5%
- Fully compatible with devices and OS that support the SATA III 6.0Gb/s standard
- Compliant with M.2 standards in SATA specification

Features

- Advanced global wear-Leveling and block management for reliability
- Built-in ECC (Error Correction Code) functionality
- Features a DDR3 DRAM cache
- Supports Advanced Garbage Collection
- Supports enhanced S.M.A.R.T. function
- Real time full drive encryption with Advanced Encryption Standard (AES) (Optional)
- Power Shield to prevent data loss in the event of a sudden power outage
- Supports partial and slumber mode
- Supports security command
- Supports Hardware purge and write protect (Optional)
- Supports Transcend SSD scope pro (Optional)
- RoHS compliant

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Specifications

Physical Specification					
Form Factor		M.2 TYPE 2280-D2-B-M			
Storage Capacities		32~512GB			
	Length	$80.00\pm0.15~\text{mm}$	$3.150\pm0.006~\text{inch}$		
Dimensions	Width	$22.00\pm0.15~\text{mm}$	$0.866\pm0.006\text{ inch}$		
	Height	$3.50\pm0.15~\text{mm}$	$0.138\pm0.006\text{ inch}$		
Input Voltage		$3.3V \pm 5\%$			
Weight		9 g ± 5%			
Connector		M.2 module notch B+M			

Environmental Specifications					
Operating Temperature		-10 ℃ to 80 ℃			
Storage Temperature		-40 °C to 85 °C			
Operating		0% to 95% (Non-condensing)			
Humidity	Non-Operating	0% to 95% (Non-condensing)			

Performance								
	ATTO			CrystalDiskMark			IOMeter	
Model P/N	Max Read*	Max Write*	Sequential Read**	Sequential Write**	Random Read (4KB QD32)**	Random Write (4KB QD32)**	IOPS Random Read (4KB QD32)***	IOPS Random Write (4KB QD32)***
TS32XBTMM0000A	230	40	230	40	90	40	20K	10K
TS64XBTMM0000A	450	80	440	80	170	80	40K	20K
TS128XBTMM0000A	540	170	520	160	270	160	70K	40K
TS256XBTMM0000A	550	320	520	320	300	300	75K	75K
TS512XBTMM0000A	550	460	520	460	290	310	70K	75K

Note: Maximum transfer speed recorded

* 25 °C, test on GIGABYTE GA-Z87X-D3H, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility ATTO (version 2.41), unit MB/s

** 25 °C, test on GIGABYTE GA-Z87X-D3H, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility CrystalDiskMark (version 3.0.1), copied file 1000MB, unit MB/s

*** 25 °C, test on GIGABYTE GA-Z87X-D3H, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility IOmeter2006 with 4K file size and queue depth of 32, unit IOPs **** The recorded performance is obtained while the SSD is not operating as an OS disk Physical Specification



Actual Capacity				
Model P/N	User Max. LBA	Cylinder	Head	Sector
TS32XBTMM0000A	62,533,296	16,383	16	63
TS64XBTMM0000A	125,045,424	16,383	16	63
TS128XBTMM0000A	250,069,680	16,383	16	63
TS256XBTMM0000A	500,118,192	16,383	16	63
TS512XBTMM0000A	1,000,215,216	16,383	16	63

Power Consumption					
Input Voltage		$3.3V \pm 5\%$			
Model P/N / Power Consum	nption	Average (mA)			
	Max Write	236			
TS32XBTMM0000A	Max Read	226			
	ldle	75			
	Max Write	335			
TS64XBTMM0000A	Max Read	243			
	ldle	76			
	Max Write	508			
TS128XBTMM0000A	Max Read	244			
	ldle	76			
	Max Write	660			
TS256XBTMM0000A	Max Read	292			
	ldle	81			
	Max Write	661			
TS512XBTMM0000A	Max Read	300			
	ldle	82			

*Tested with IOmeter running sequential reads/writes and idle mode



Reliability					
Data Reliability	Supports BCH ECC 60 bit per 1024 byte				
MTBF	1,500,000 hours				
	32G	45 (TB)			
	64G	80 (TB)			
Endurance (Terabytes Written)	128G	150 (TB)			
	256G	280 (TB)			
	512G	550 (TB)			

*Tested under JESD218A endurance test method and JESD219A endurance workloads specification.

Vibration				
Operating	3.0G, 5 - 800Hz			
Non-Operating	5.0G, 5 - 800Hz			

Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

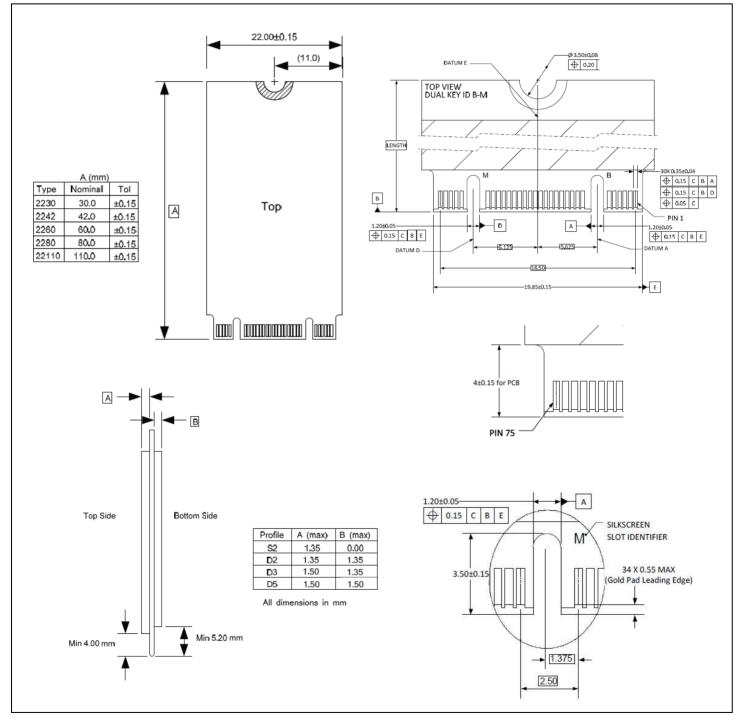
Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500G, 0.5ms, 3 times/dir., total 18 times.

Regulations	
Compliance	CE, FCC and BSMI



Package Dimensions

The figure below illustrates the Transcend M.2 Type 2280-D2-B-M Solid State Drive. All dimensions are in mm.



Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	CONFIG_3*	02	3.3V	39	GND	40	NC
03	GND	04	3.3V	41	TX+	42	NC
05	NC	06	NC	43	TX-	44	NC
07	NC	08	NC	45	GND	46	NC
09	NC	10	DAS/DSS**	47	RX-	48	NC
11	NC	12	NOTCH	49	RX+	50	NC
13	NOTCH	14	NOTCH	51	GND	52	NC
15	NOTCH	16	NOTCH	53	NC	54	NC
17	NOTCH	18	NOTCH	55	NC	56	MFG1****
19	NOTCH	20	NC	57	GND	58	MFG2****
21	CONFIG_0*	22	NC	59	NOTCH	60	NOTCH
23	NC	24	NC	61	NOTCH	62	NOTCH
25	NC	26	NC	63	NOTCH	64	NOTCH
27	GND	28	NC	65	NOTCH	66	NOTCH
29	NC	30	NC	67	NC	68	NC
31	NC	32	NC	69	CONFIG_1*	70	3.3V
33	GND	34	NC	71	GND	72	3.3V
35	NC	36	NC	73	GND	74	3.3V
37	NC	38	DEVSLP***	75	CONFIG_2*		

* For SATA application, these pins connect to GND internally

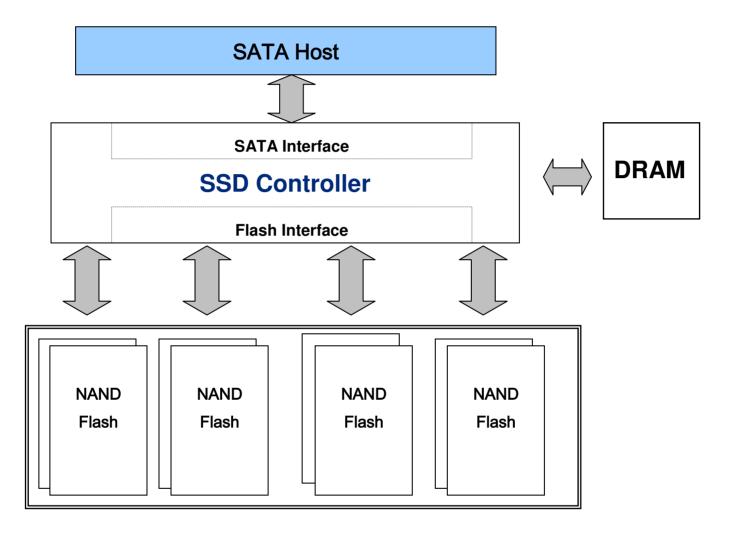
** Device Activity Signal / Disable Staggered Spin-up

*** Device Sleep, Input. If driven high the host is informing the SSD to enter a low power state

**** Manufacturing pins. Do not connect



Block Diagram





Features

• Global Wear Leveling – Advanced algorithms to enhance wear-leveling efficiency.

Global wear leveling ensures that every block has an even erase count. This helps to extend the life expectancy of an SSD.

There are three main processes in global wear leveling:

- Record the block erase count and save this in the wear-leveling table.
- Find the static-block and save this in the wear-leveling pointer.
- Check the erase count when a block is pulled from the pool of spare blocks. If the block erase count is larger than WEARCNT, then swap the static-block and over-count-block.

ECC Algorithm

The controller uses BCH 40 Bit ECC algorithm per 1024 bytes depending on the structure of the flash. BCH40 may correct up to 40 random error bits within 1024 data bytes. With the help of BCH40 ECC, the endurance of Transcend SSD is greatly improved.

Bad Block Management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as a bad block. This will prevent the usage of bad blocks which may result in data loss in the future.

Advanced Garbage Collection

Transcend SSD has perfect garbage collection mechanism to help SSD improve performance. Advanced Garbage collection can efficiently manage memory management to let SSD can always has stable performance. With Transcend advanced flash management, the drive can still keep high performance after long time operation

• Enhanced S.M.A.R.T. function

Transcend SSD supports S.M.A.R.T. command (Self-Monitoring, Analysis, and Reporting Technology) that allows the user to read the health information of the SSD. Transcend also define some innovated S.M.A.R.T. features which allows the user to evaluate the status of the SSD in a much more efficient way.

Power Shield

The controller uses internal power shield circuit to prevent SSD from damage when a sudden power outage occurs. The SSD's internal power detect mechanism can monitor power provided by host. When a sudden power outage happens, the SSD can execute power shield mechanism to protect data in the SSD.

Hardware Purge and Write Protect

The SSD has optional features which include hardware trigger for quick data erase and write protect. These features may be enabled by simply connecting a switch to the designated pins.

StaticDataRefresh Technology



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Normally, ECC engine corrections are taken place without affecting the host normal operations. As time passes by, the number of error bits accumulated in the read transaction exceeds the correcting capability of the ECC engine, resulting in corrupted data being sent to the host. To prevent this, the controller monitors the error bit levels at each read operation; when it reaches the preset threshold value, the controller automatically performs data refresh to "restore" the correct charge levels in the cell. This implementation practically restores the data to its original, error-free state, and hence, lengthening the life of the data.



ATA Command Register

This table and the following paragraphs summarize the ATA command set.

Command Table						
Support ATA/ATAPI Command	Code	Protocol				
General Feature Set						
EXECUTE DIAGNOSTICS	90h	Device diagnostic				
FLUSH CACHE	E7h	Non-data				
IDENTIFY DEVICE	ECh	PIO data-In				
Initialize Drive Parameters	91h	Non-data				
READ DMA	C8h	DMA				
READ LOG Ext	2Fh	PIO data-In				
READ MULTIPLE	C4h	PIO data-In				
READ SECTOR(S)	20h	PIO data-In				
READ VERIFY SECTOR(S)	40h or 41h	Non-data				
SET FEATURES	EFh	Non-data				
SET MULTIPLE MODE	C6h	Non-data				
WRITE DMA	Cah	DMA				
WRITE MULTIPLE	C5h	PIO data-out				
WRITE SECTOR(S)	30h	PIO data-out				
NOP	00h	Non-data				
READ BUFFER	E4h	PIO data-In				
WRITE BUFFER	E8h	PIO data-out				
Power Management Feature Set						
CHECK POWER MODE	E5h or 98h	Non-data				
IDLE	E3h or 97h	Non-data				
IDLE IMMEDIATE	E1h or 95h	Non-data				
SLEEP	E6h or 99h	Non-data				
STANDBY	E2h or 96h	Non-data				
STANDBY IMMEDIATE	E0h or 94h	Non-data				
Security Mode Feature Set						
SECURITY SET PASSWORD	F1h	PIO data-out				
SECURITY UNLOCK	F2h	PIO data-out				
SECURITY ERASE PREPARE	F3h	Non-data				
SECURITY ERASE UNIT	F4h	PIO data-out				
SECURITY FREEZE LOCK	F5h	Non-data				
SECURITY DISABLE PASSWORD	F6h	PIO data-out				
SMART Feature Set						
SMART Disable Operations	B0h	Non-data				
SMART Enable/Disable Autosave	B0h	Non-data				
SMART Enable Operations	B0h	Non-data				
SMART Execute Off-Line Immediate	B0h	Non-data				
SMART Read LOG	B0h	PIO data-In				
SMART Read Data	B0h	PIO data-In				
SMART Read THRESHOLD	B0h	PIO data-In				
SMART Return Status	B0h	Non-data				
SMART SAVE ATTRIBUTE VALUES	B0h	Non-data				
SMART WRITE LOG	B0h	PIO data-out				
Host Protected Area Feature Set						

Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	Eah	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Other		
Data Set Management	06h	DMA
SEEK	70h	Non-data



SMART Data Structure

BYTE	F / V	Description			
0-1	х	Revision code			
2-361	Х	Vendor specific			
362	V	Off-line data collection status			
363	Х	Self-test execution status byte			
364-365	V	Total time in seconds to complete off-line data collection activity			
366	Х	Vendor specific			
367	F	Off-line data collection capability			
368-369	F	SMART capability			
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported			
371	Х	Vendor specific			
372	F	Short self-test routine recommended polling time (in minutes)			
373	F	Extended self-test routine recommended polling time (in minutes)			
374	F	Conveyance self-test routine recommended polling time (in minutes)			
375-385	R	Reserved			
386-395	F	Firmware Version/Date Code			
396-397	F	Reserved			
398-399	V	Reserved			
400-406	V	TS6500			
407-415	Х	Vendor specific			
416	F	Reserved			
417	F	Program/write the strong page only			
418-419	V	Number of spare block			
420-423	v	Average Erase Count			
424-510	х	Vendor specific			
511	V	Data structure checksum			

F = content (byte) is fixed and does not change.

V= content (byte) is variable and may change depending on the state of the device or the commands executed by the device.

X= content (byte) is vendor specific and may be fixed or variable.

R= content (byte) is reserved and shall be zero.



SMART Attributes

Attribute ID (hex)	C .		Raw Attril	Attribute Name			
01	MSB	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	Reallocated sectors count
09	LSB	-	-	MSB	00	00	Reserved
0C	LSB	MSB	00	00	00	00	Power Cycle Count
A0	LSB	-	-	MSB	00	00	Uncorrectable sectors count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare blocks
A3	LSB	MSB	00	00	00	00	Number of initial invalid blocks
A4	LSB	-	-	MSB	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	Minimum erase count
A7	LSB	-	-	MSB	00	00	Average erase count
C0	LSB	MSB	00	00	00	00	Power-off retract Count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB	-	-	MSB	00	00	Hardware ECC recovered
C4	LSB	-	-	MSB	00	00	Reallocation event count
C7	LSB	MSB	00	00	00	00	UltraDMA CRC Error Count
F1	LSB	-	-	MSB	00	00	Total LBA written (each write unit = 32MB)
F2	LSB	-	-	MSB	00	00	Total LBA read (each read unit = 32MB)

The following table shows the vendor specific data in byte 2 to 361 of the 512-byte SMART data



Revision History					
Version	Date	Modification Content			
V1.0	2014/06/04	Initial Release			
V1.1	2014/08/04	Improve TS512GMTS800 performance			
V1.2	2014/10/14	Update performance			
V1.3	2015/01/08	Update performance / power consumption / package dimensions			