BVA7242

High linearity Flat Gain Digital Variable Gain Amplifier

3000MHz – 4200MHz

Device Features

- Integrated AMP1 + DSA + AMP2
- Frequency Range : 3.0GHz - 4.2GHz
- Wide VDD Range : 3.3V to 5.25V
- Low Current : 98mA @ 3.3V, 170mA @ 5.0V
- High Gain : 34.5dB Gain @ 3.6GHz
- Excellent Gain Flatness
  Under 0.8dB @ 800MBW (3.2 - 4GHz)
- 1.8dB Noise Figure @ 3.6GHz, ATT = 0dB (Max gain)
- 20dBm Output P1dB @ 3.6GHz , VDD = 5.0V
- High Output IP3 @ VDD = 5.0V
  38dBm @3.6GHz, ATT = 0dB (Max gain)
  35.5dBm @3.6GHz, ATT = 15dB
- Attenuation Range : 0 - 31.75 dB / 0.25 dB step
- Glitch-less attenuation state during transitions
- High attenuation accuracy
  ±(0.25dB + 5% x ATT. Setting) @ 3.2 - 4.0GHz
- Serial Programming Interface only
- Power Down Mode (P/D)
- Lead-free/RoHS2-compliant 28-pin 6mm x 6mm x 1.07mm LGA SMT Package

Product Description

The BVA7242 is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm LGA package, with a frequency range of 3GHz to 4.2GHz at VDD range 3.3V to 5.25V.

BVA7242 is a high performance and high dynamic range makes it ideally suited for use in 5G/LTE wireless infrastructure and other high performance wireless RF applications.

The BVA7242 is an integration of a high performance digital 7bit step attenuator (DSA) that provides a 31.75 dB attenuation range in 0.25 dB steps and two amplifiers. Two amplifiers in BVA7242 provide high ACP and P1dB.

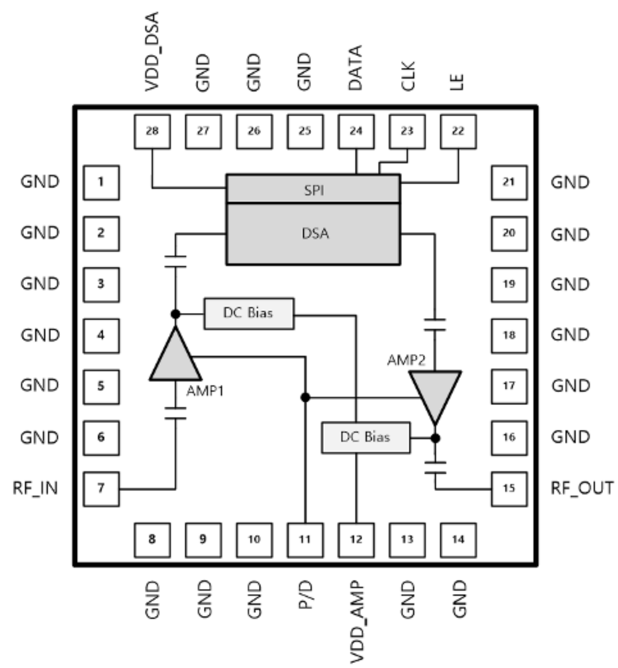
The BVA7242 digital control interface supports serial programming of the Step attenuator (DSA) and has a power down feature for power savings with Power Down (P/D) mode.

Furthermore, BVA7242 includes some matching and bias circuits to minimize external components. So, Implementation requires only a few external components, such as matching capacitors on input and output pins. (No need DC Blocking Capacitors on RF input and output pin.)

Figure 1. Package Type

28-pin 6mm x 6 mmx 1.07mm LGA

Figure 2. Functional Block Diagram



Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications @ VDD = 5.0V

Typical Performance measured on the BeRex Evaluation board at 25°C and Max. gain unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			3		4.2	GHz
Gain		ATT = 0dB, @ 3.6GHz	32	34.5	37	dB
Gain Flatness		3.2GHz to 4.2GHz		0.8		dBpp
		3GHz to 4.2GHz		1.5		dBpp
Attenuation Control range				0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	3.2GHz to 4GHz	Any bit or bit combination	- (0.25 + 5% of ATT setting)		+ (0.25 + 5% of ATT setting)	dB
	3GHz to 4.2GHz	Any bit or bit combination	- (0.5 + 6% of ATT setting)		+ (0.5 + 6% of ATT setting)	dB
Input Return Loss		ATT = 0dB		15		dB
Output Return Loss		ATT = 0dB		10		
Output Power for 1dB Compression		@ 3.6GHz		20		dBm
Output Third Order Intercept Point [1]		ATT = 0dB, @ 3.6GHz		38		dBm
		ATT = 15dB, @ 3.6GHz		35.5		dBm
Noise Figure		ATT = 0dB, @ 3.6GHz		1.8		dB
		ATT = 15dB, @ 3.6GHz		4.0		dB
Adjacent Channel Leakage Ratio [2]		ATT = 0dB, @ 3.6GHz		9.5		dBm
		ATT = 15dB, @ 3.6GHz		9		dBm
DSA Switching time		50% CTRL to 90% or 10% RF		275		ns
Power Down (P/D) Switching time		50% CTRL to 90% or 10% RF		150		ns
Control Interface		Serial mode		8		Bit
Impedance				50		Ω

1. OIP3 measured with two tones at an output of +3dBm per tone separated by 100MHz.
2. The measurement source condition for ACLR is 5GNR 100MBW, PAR = 9.6dB and the data is output power of ACLR 50dBc point at ±100MHz offset.

Table 2. Electrical Specifications @ VDD = 3.3V

Typical Performance measured on the BeRex Evaluation board at 25°C and Max. gain unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			3		4.2	GHz
Gain		ATT = 0dB, @ 3.6GHz	31.5	33.8	36.5	dB
Gain Flatness		3.2GHz to 4.2GHz		1.0		dBpp
		3GHz to 4.2GHz		1.5		dBpp
Attenuation Control range				0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	**3.2GHz to 4GHz**	Any bit or bit combination	- (0.25 + 5% of ATT setting)		+ (0.25 + 5% of ATT setting)	dB
	3GHz to 4.2GHz	Any bit or bit combination	- (0.5 + 6% of ATT setting)		+ (0.5 + 6% of ATT setting)	dB
Input Return Loss		ATT = 0dB		15		dB
Output Return Loss		ATT = 0dB		10		
Output Power for 1dB Compression		@ 3.6GHz		16.5		dBm
Output Third Order Intercept Point [1]		ATT = 0dB, @ 3.6GHz		35		dBm
		ATT = 15dB, @ 3.6GHz		31.8		dBm
Noise Figure		ATT = 0dB, @ 3.6GHz		1.8		dB
		ATT = 15dB, @ 3.6GHz		4.0		dB
Adjacent Channel Leakage Ratio [2]		ATT = 0dB, @ 3.6GHz		6.5		dBm
		ATT = 15dB, @ 3.6GHz		6		dBm
DSA Switching time		50% CTRL to 90% or 10% RF		275		ns
Power Down (P/D) Switching time		50% CTRL to 90% or 10% RF		150		ns
Control Interface		Serial mode		8		Bit
Impedance				50		Ω

1. OIP3 measured with two tones at an output of +3dBm per tone separated by 100MHz.
2. The measurement source condition for ACLR is 5GNR 100MBW, PAR = 9.6dB and the data is output power of ACLR 50dBc point at ±100MHz offset.

Table 3. Typical RF Performance @ VDD = 5.0V, 25°C

Parameter	Frequency					Unit
Frequency	**3**	**3.3**	**3.6**	**4**	**4.2**	**GHz**
Gain	33.4	34.5	34.6	34.0	33.5	dB
S11	-7.8	-14.6	-33.4	-21.4	-21.1	dB
S22	-7.3	-14.5	-26.5	-15.6	-12.0	dB
OIP3[1] (Max Gain, ATT=0dB)	36.4	37.5	38	37	36.2	dBm
OIP3[1] (ATT=15dB)	34.1	36	35.5	34.3	33.7	dBm
OP1dB	20.0	20.3	20.0	20.0	19.9	dBm
ACLR[2] (Max Gain, ATT=0dB)	9.4	9.6	9.6	9.3	8.9	dBm
ACLR[2] (ATT=15dB)	9.0	9.3	9.2	8.9	8.5	dBm
NF (Max Gain, ATT=0dB)	1.7	1.7	1.8	1.8	1.9	dB
NF (ATT=15dB)	3.9	3.9	4.0	4.3	4.4	dB

1. OIP3 measured with two tones at an output of +3dBm per tone separated by 100MHz.
2. The measurement source condition for ACLR is 5GNR 100MBW, PAR = 9.6dB and the data is output power of ACLR 50dBc point at ±100MHz offset.

Table 4. Typical RF Performance @ VDD = 3.3V, 25°C

Parameter	Frequency					Unit
Frequency	**3**	**3.3**	**3.6**	**4**	**4.2**	**GHz**
Gain	32.8	33.8	33.9	33.2	32.5	dB
S11	-7.2	-13.6	-27.2	-23.1	-22.8	dB
S22	-7.6	-15.5	-27.5	-14.8	-11.4	dB
OIP3[1] (Max Gain, ATT=0dB)	33.5	34.5	35.5	32.9	31.5	dBm
OIP3[1] (ATT=15dB)	31.0	32.3	31.8	29.6	29.2	dBm
OP1dB	16.8	17.1	16.5	16.5	16.6	dBm
ACLR[2] (Max Gain, ATT=0dB)	6.3	6.5	6.5	6.0	5.6	dBm
ACLR[2] (ATT=15dB)	5.8	6.0	6.1	5.5	5.2	dBm
NF (Max Gain, ATT=0dB)	1.7	1.7	1.7	1.8	1.9	dB
NF (ATT=15dB)	4.0	4.0	4.1	4.3	4.6	dB

1. OIP3 measured with two tones at an output of +3dBm per tone separated by 100MHz.
2. The measurement source condition for ACLR is 5GNR 100MBW, PAR = 9.6dB and the data is output power of ACLR 50dBc point at ±100MHz offset.

Table 5. Absolute Maximum Ratings[1]

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage	AMP / DSA			5.5	V
Supply Current	AMP			380	mA
	DSA			1000	uA
Digital input voltage	P/D	-0.3		5.5	V
	LE, DATA, CLK	-0.3		3.6	V
Maximum input power	CW			10	dBm
Storage Temperature		-55		150	°C
Junction Temperature				165	°C

1. Operation of this device above any of these parameters may result in permanent damage.

Table 6. Recommended Operating Conditions[1]

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		3000		4200	MHz
Supply Voltage, VDD	AMP VDD	3.3	5	5.25	V
	DSA VDD	2.7		5.5	V
Current, IDD	AMP ON @ VDD=5V		170		mA
	AMP ON @ VDD=3.3V		98		mA
	AMP OFF		6	14	mA
	DSA	100	200	300	uA
AMP Control Voltage [P/D]	AMP ON	0		0.5	V
	AMP OFF	1.17		VDD	V
DSA Control Voltage [LE, DATA, CLK]	Digital Input High	1.17		3.6	V
	Digital Input Low	-0.3		0.6	V
Thermal Resistance	$R_{TH}(\theta_{JC})$		26		˚C/W
Operating Temperature	AMP1 + DSA + AMP2	-40		105	°C

1. Specifications are not guaranteed over all recommended operating conditions

Programming Option

Programming Mode

The BVA7242 is only operating in Serial Mode.

Serial Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. This 8-bits make up the Attenuation Word that controls the internal DSA.

The Serial interface is controlled by using three CMOS compatible Signals : DATA, Clock (CLK) and LE. The DATA and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first. **Figure 4** illustrates an example timing diagram for a programming state.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Attenuation Word truth table is listed in **Table 7**. A programming example of the serial register is illustrated in **Figure 3**.

Table 7. Serial Attenuation word Truth Table

Attenuation Word								Attenuation setting
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Max. Gain
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Power-up Control Settings

The BVA7242 will be always initialized to the max. attenuation setting (Atten=31.75dB, minimum Gain state) on power-up sequence and will remain at the max. attenuation setting until user latches the next programming word.

Figure 3. Serial Register Map

MSB (last in) ↓ ... LSB (first in) ↓

Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
D7	D6	D5	D4	D3	D2	D1	D0

8 Bit Attenuation Word

Bit must be set to logic low (shaded: D7)

The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 15.75dB Attenuation state;

15.75 x 4 = 63
63 → 00111111

Serial DATA Input : 00111111

0	0	1	1	1	1	1	1
D7	D6	D5	D4	D3	D2	D1	D0

Glitch-less Attenuation State Transitions

The BVA7242 features a novel architecture to provide the best-in-class glitch-less transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced (≤0.3 dB) during attenuation state changes when comparing to previous generations of DSAs.

Figure 4. Serial Interface Timing Diagram

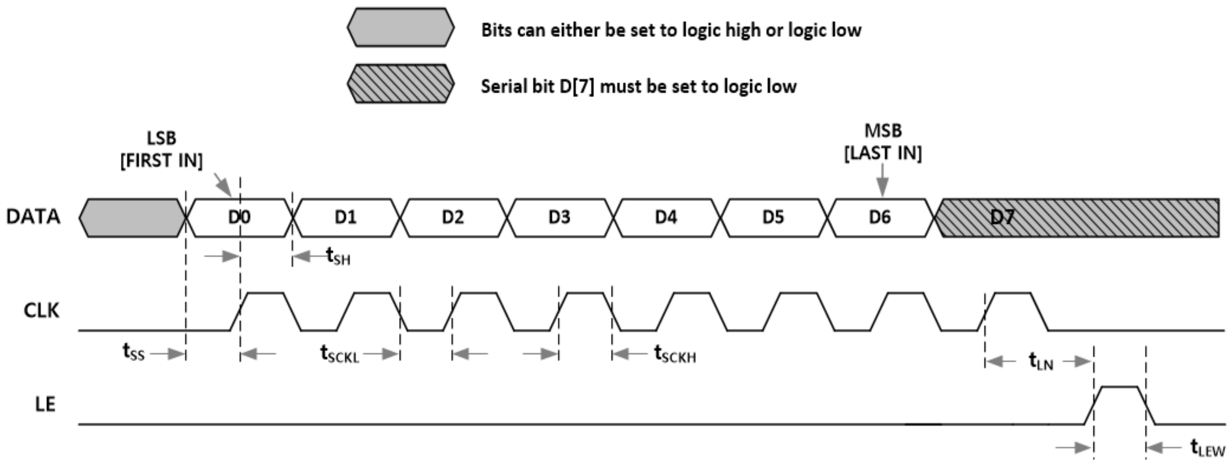


Table 8. Serial Interface AC Characteristics

VDD = 5.0V with DSA, -40°C ≤ TA ≤ 105°C, unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
F_{CLK}	Serial data clock frequency			10	MHz
T_{SCKH}	Serial clock HIGH time	30			ns
T_{SCKL}	Serial clock LOW time	30			ns
T_{LN}	Last Serial clock rising edge setup time to Latch Enable rising edge	10			ns
T_{LEW}	Latch Enable minimum pulse width	30			ns
T_{SS}	Serial data setup time	10			ns
T_{SH}	Serial data hold time	10			ns

Figure 5. Pin Configuration

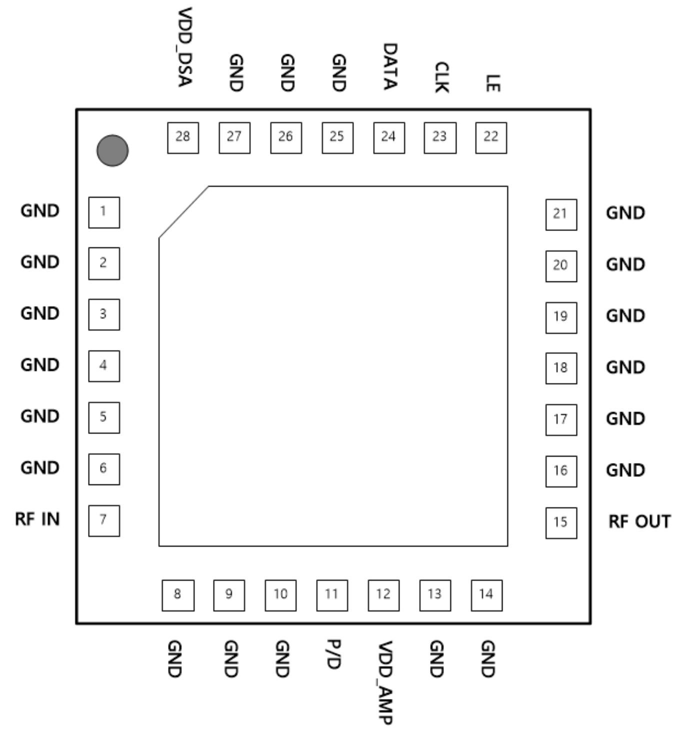


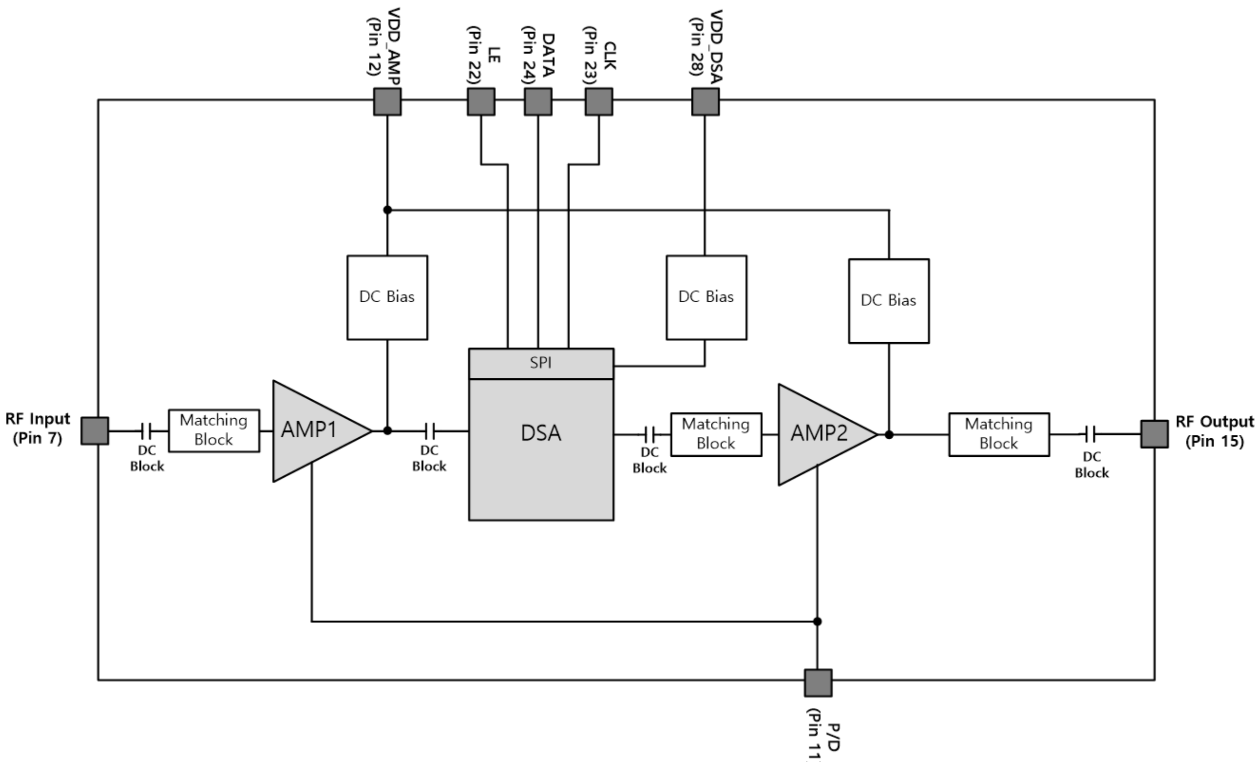
Table 9. Pin Description

Pin	Pin name	Description
1-6, 8-10, 13-14, 16-21, 25-27	GND	RF/DC Ground
7	RF IN	RF Input, matched to 50 ohm. Internally DC blocked.
11	P/D	VDD Power Down control Input. With Logic High(0.8 to 5V), Amplifier is Disabled. With Logic Low(0 to 0.5V), Amplifier is Enabled.
12	VDD_AMP	Supply Voltage to Amplifier (AMP1 and AMP2). This pin is connected internally to bypass capacitors followed by inductor inside the module.
15	RF OUT	RF output, matched to 50 ohm. Internally DC blocked.
22	LE	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
23	CLK	Serial Clock Input.
24	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
28	VDD_DSA	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
Exposed Pad	GND	RF/DC Ground

Figure 6. Internal Function Block Diagram

The BVA7242 is integrated two gain blocks (AMP1, AMP2) and one digital step attenuator (DSA) . Additionally, the BVA7242 includes an internal bias, DC blocking and RF Matching circuits to improve the RF performances at 3GHz - 4.2GHz and reduce the external components.

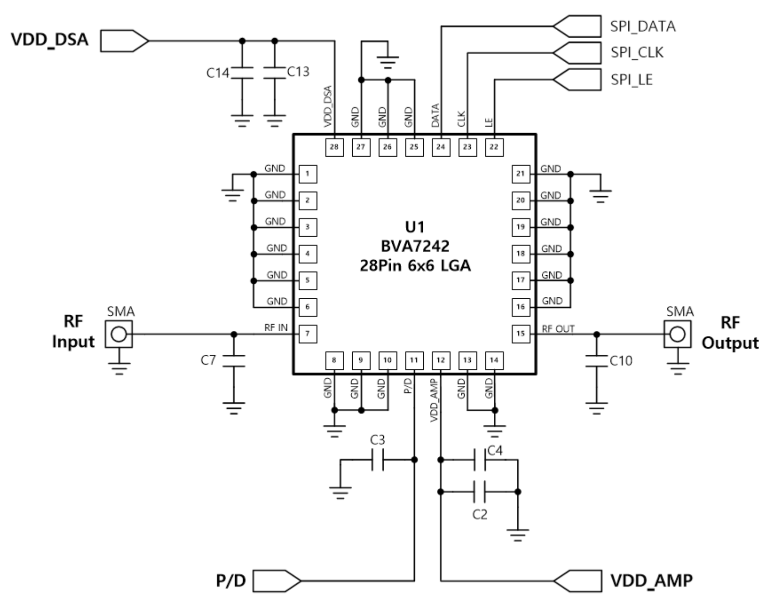
The block diagram of BVA7242 is shown below.



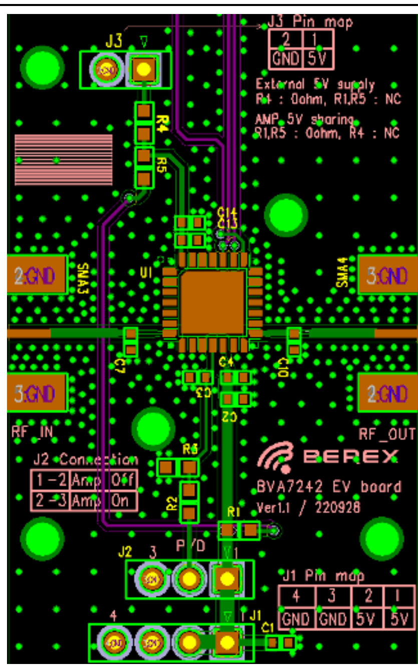
Typical RF Performance - BVA7242 EVK - PCB

Table 10. Application Circuits

Schematic Diagram



BOM Ref	BOM Size	BOM Value	Remark
C2	0402	NC	
C3	0402	NC	
C4	0402	100 nF	
C7	0402	0.5 pF	S11 Matching
C10	0402	NC	
C13	0402	100 nF	
C14	0402	NC	



NOTE

1. J1 Information
   - Pin 1, 2 : VDD_Amp (3.3V to 5V)
   - Pin 3, 4 : Ground
2. J2 Information (P/D)
   - Not connected (Floating) : Amp ON
   - Connected 1-2 : Amp OFF
   - Connected 2-3 : Amp ON
3. J3 Information
   - Pin 1 : VDD_DSA (3.3V to 5V)
   - Pin 2 : Ground

Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 11. Typical Performance @ 3.6GHz, VDD = 5V

Parameter	Typical Values			Units
Temperature	-40	25	105	°C
VDD	5	5	5	V
Current	178	170	161	mA
Gain	35.5	34.6	33.4	dB
S11	-39.0	-33.4	-30.1	dB
S22	-26.1	-26.5	-22.1	dB
OIP3[1]	38.7	38.8	38.3	dBm
OP1dB	19.4	20	20.3	dBm
NF	1.4	1.8	2.3	dB

1. OIP3 measured with two tones at an output of +3dBm per tone separated by 100MHz.
2. Above test parameters are measured at Max Gain State (ATT=0dB)

Table 12. Typical Performance @ 3.6GHz, VDD = 3.3V

Parameter	Typical Values			Units
Temperature	-40	25	105	°C
VDD	3.3	3.3	3.3	V
Current	104	98	95	mA
Gain	34.9	33.9	32.6	dB
S11	-29.6	-27.2	-26.1	dB
S22	-29.6	-27.5	-21.2	dB
OIP3[1]	33.9	35.5	35.4	dBm
OP1dB	15.9	16.5	16.8	dBm
NF	1.4	1.7	2.2	dB

Figure 7. Gain Flatness @ VDD = 5.0V
: ATT = 0dB, Max Gain State

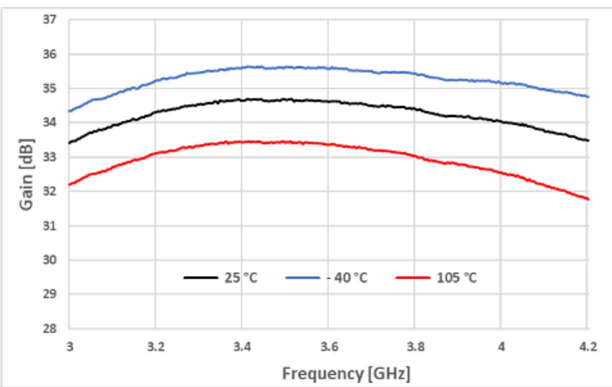


Figure 8. Gain Flatness @ VDD = 3.3V
: ATT = 0dB, Max Gain State

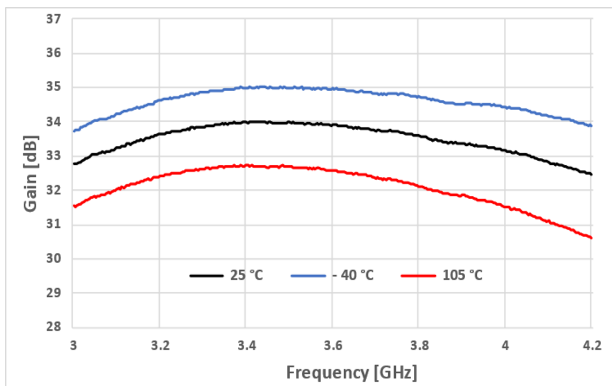


Figure 9. Gain Flatness @ VDD = 5.0V
: ATT = 31.75dB, Max Gain State

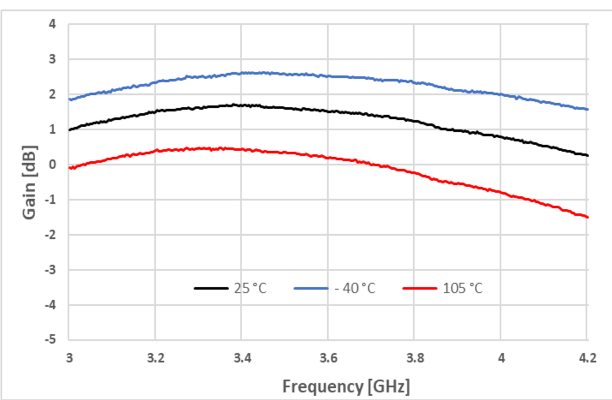
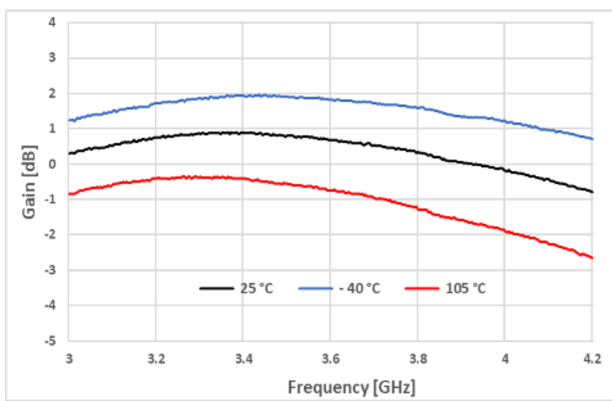


Figure 10. Gain Flatness @ VDD = 3.3V
: ATT=31.75dB, Min Gain State



Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 11. Gain vs Attenuation Settings
: VDD = 5.0V

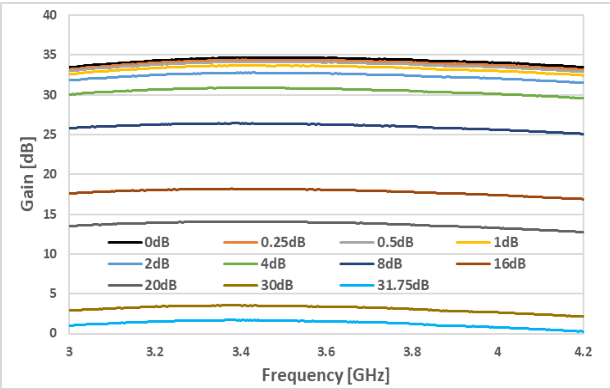


Figure 12. Gain vs Attenuation Settings

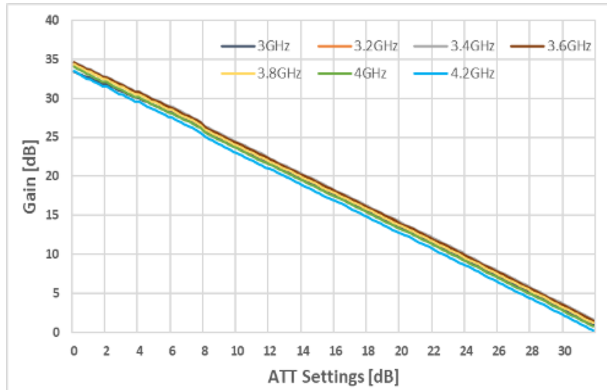


Figure 13. Input Return Loss
: VDD = 5.0V, Max Gain State

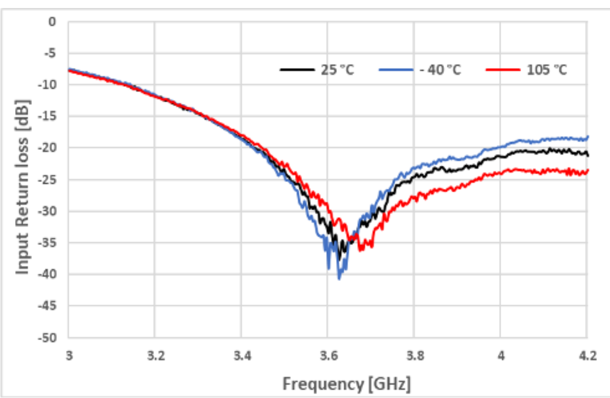


Figure 14. Input Return Loss
: VDD = 5.0V, Min Gain State

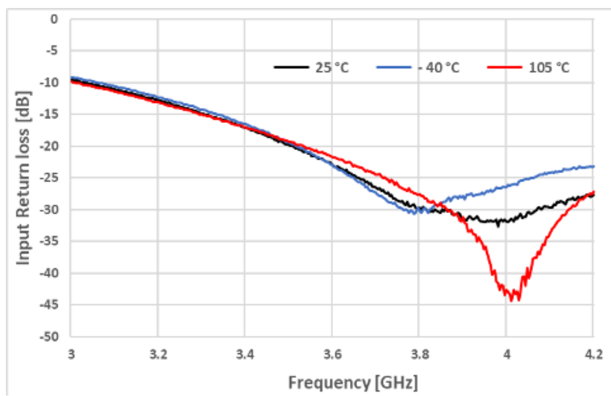


Figure 15. Output Return Loss
: VDD = 5.0V, Max Gain State

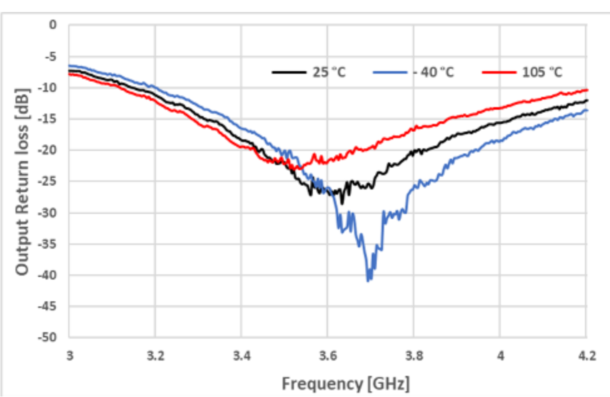
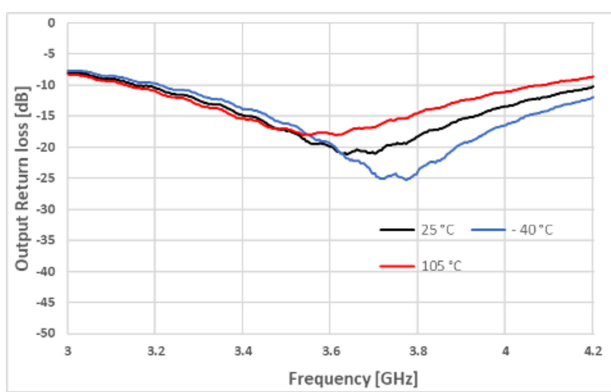


Figure 16. Output Return Loss
: VDD = 5.0V, Min Gain State



Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 17. Attenuation Error

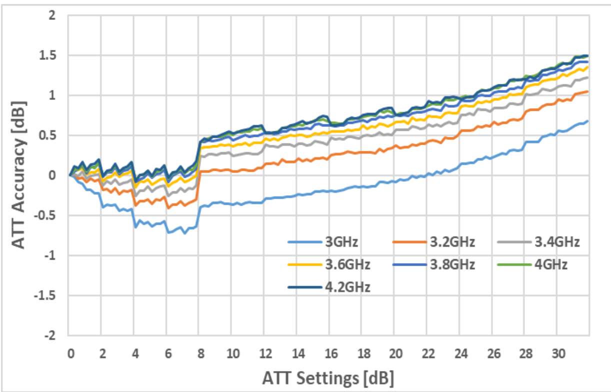


Figure 18. Attenuation Error
: 3.3GHz

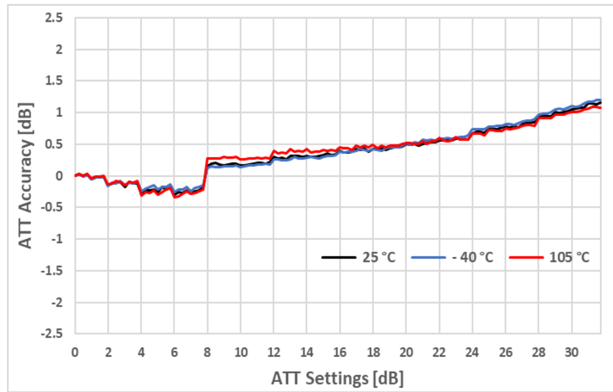


Figure 19. Attenuation Error
: 3.6GHz

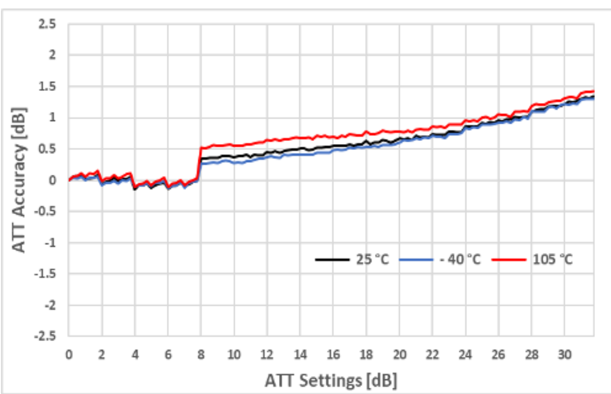


Figure 20. Attenuation Error
: 4.0GHz

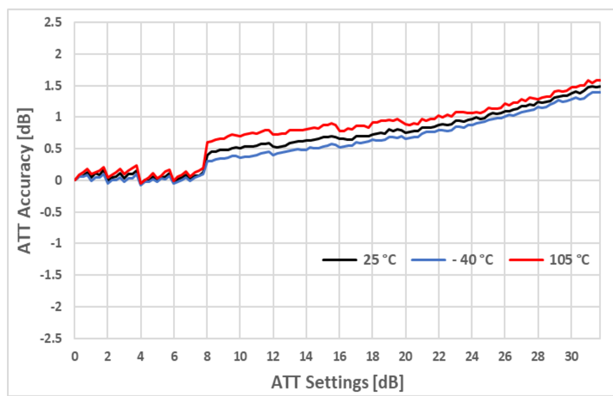


Figure 21. Attenuation Error
: Attenuation Step

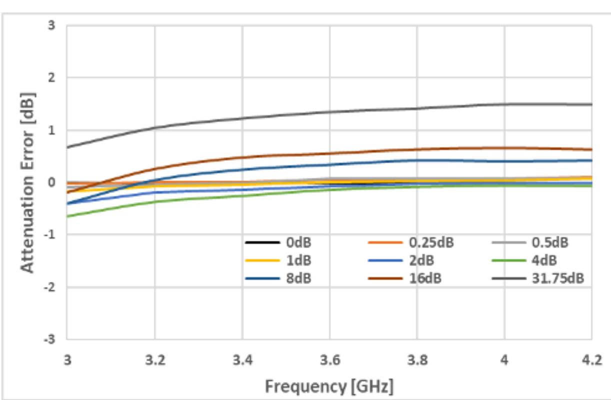
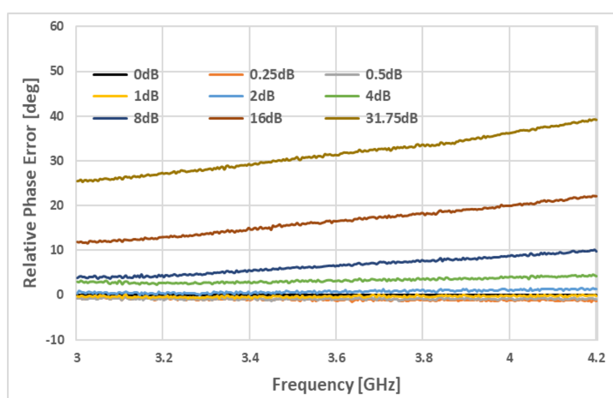


Figure 22. Relative Phase Error
: Attenuation Step



Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 23. OIP3 @ VDD = 5V
: ATT = 0dB, Output = +3dBm/tone, 100MHz interval

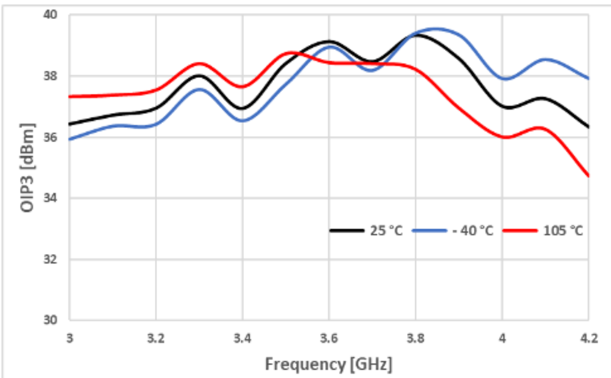


Figure 24. OIP3 @ VDD = 3.3V
: ATT = 0dB, Output = +3dBm/tone, 100MHz interval

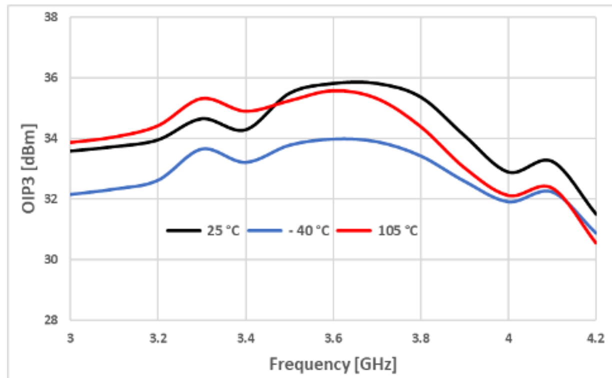


Figure 25. OIP3 @ VDD = 5V
: ATT = 15dB, Output = +3dBm/tone, 100MHz interval

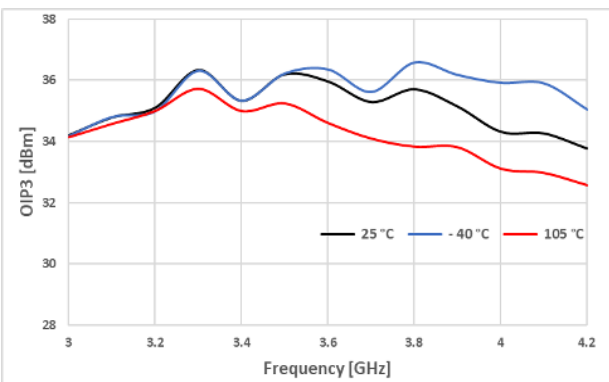


Figure 26. OIP3 @ VDD = 3.3V
: ATT = 15dB, Output = +3dBm/tone, 100MHz interval

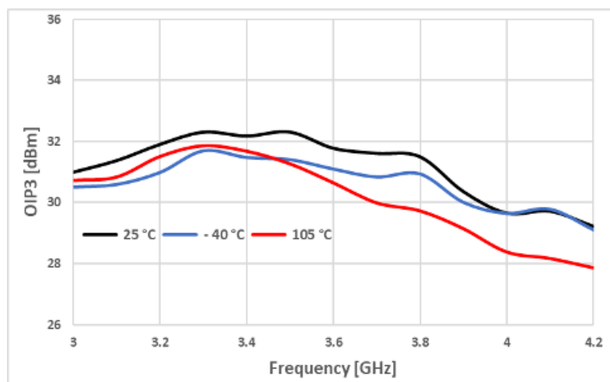


Figure 27. OP1dB @ VDD = 5V
: ATT = 0dB

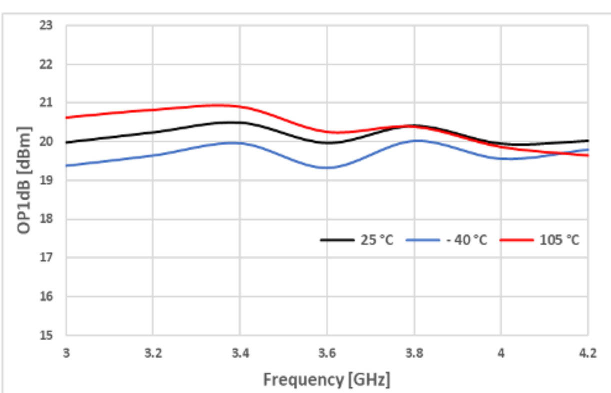
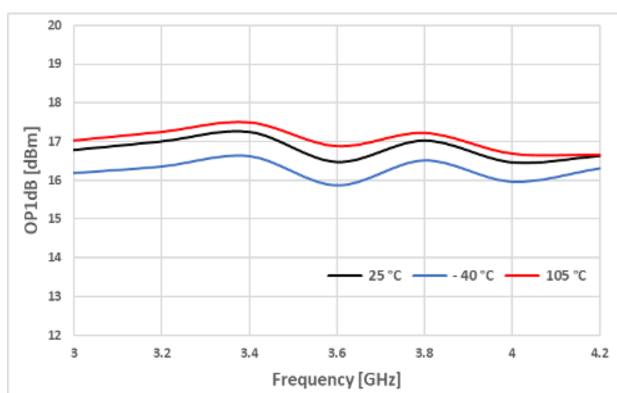


Figure 28. OP1dB @ VDD = 3.3V
: ATT = 0dB



Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 29. ACLR @ 3.6GHz
: VDD = 5.0V, ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

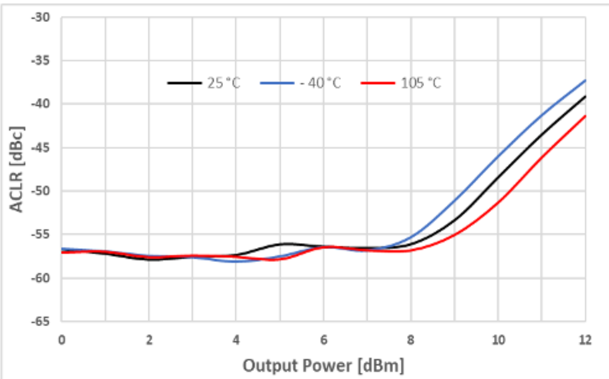


Figure 30. ACLR @ 3.6GHz
: VDD = 5.0V, ATT = 15dB, 5GNR 100MBW, PAR = 9.6dB

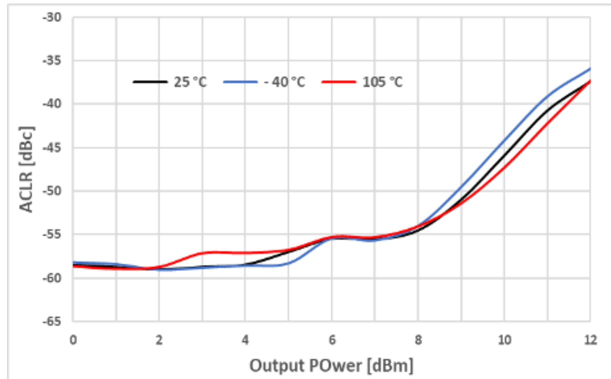


Figure 31. ACP @ 3.3GHz, VDD = 5.0V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

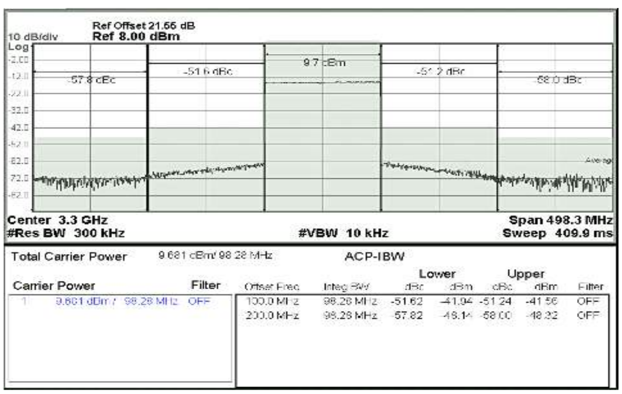


Figure 32. ACP @ 3.3GHz, VDD = 3.3V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

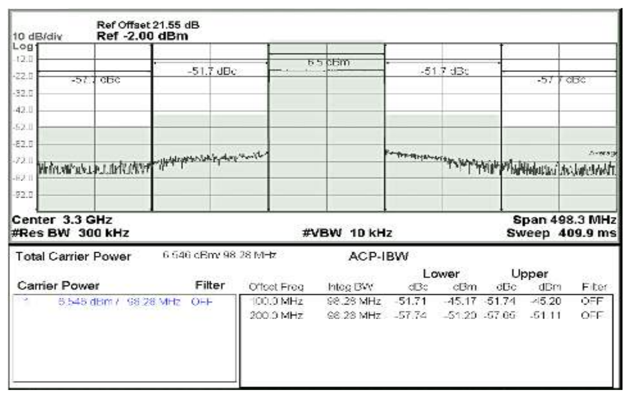


Figure 33. ACP @ 3.6GHz, VDD = 5.0V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

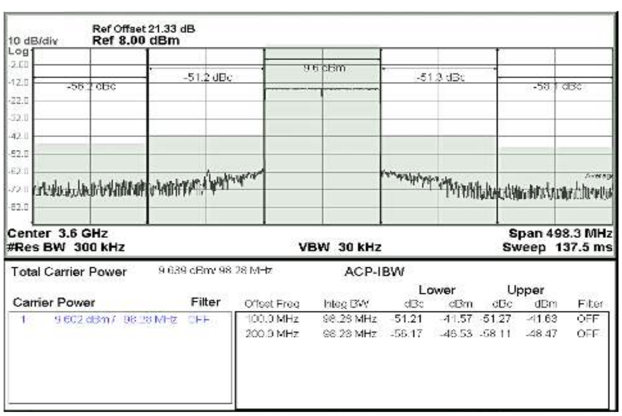
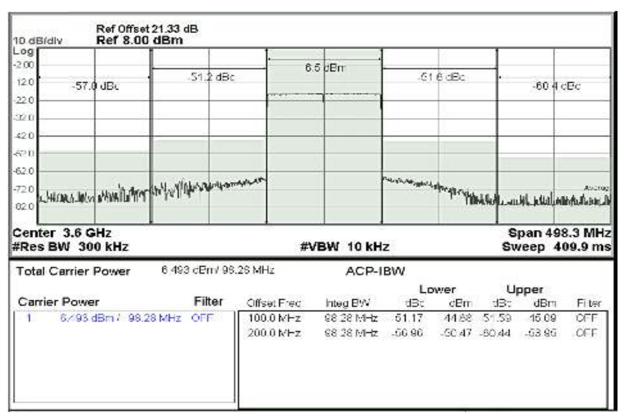


Figure 34. ACP @ 3.6GHz, VDD = 3.3V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB



Typical RF Performance - BVA7242 EVK

Typical Performance @ 25°C and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 35. ACP @ 4.0GHz, VDD = 5.0V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

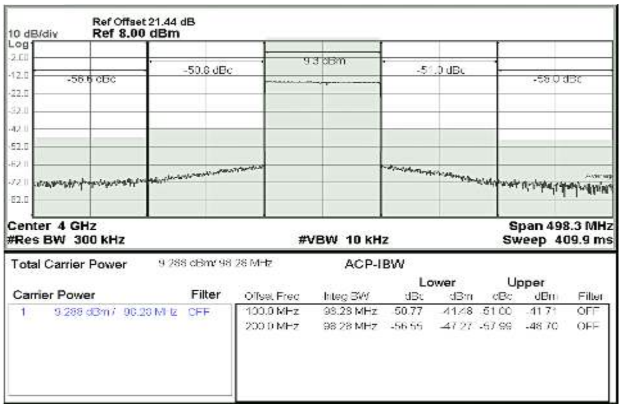


Figure 36. ACP @ 4.0GHz, VDD = 3.3V
: ATT = 0dB, 5GNR 100MBW, PAR = 9.6dB

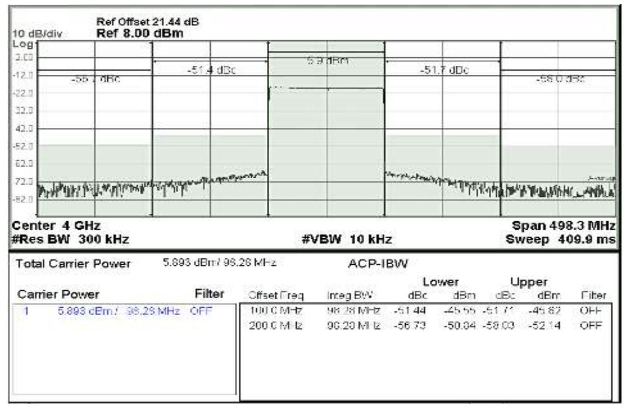


Figure 37. Noise Figure
: VDD = 5V, ATT = 0dB

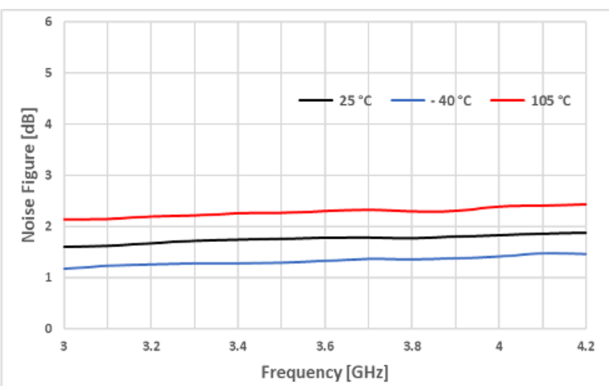


Figure 38. Noise Figure
: VDD = 5V, ATT = 15dB

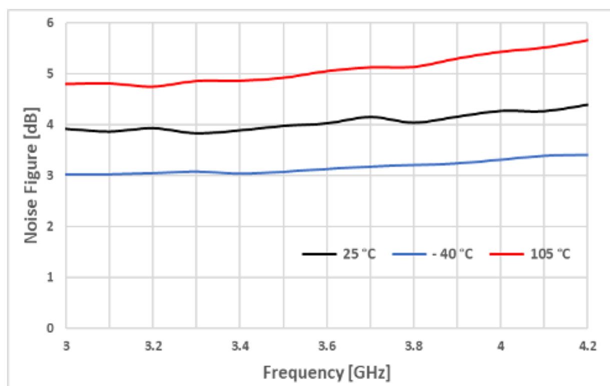


Figure 39. Power On/Off Time
: Rising Time (Control 50% to RF 90%)

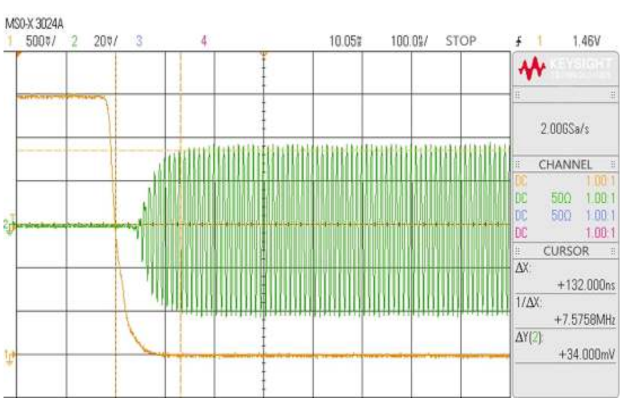


Figure 40. Power On/Off Time
: Falling Time (Control 50% to RF 10%)

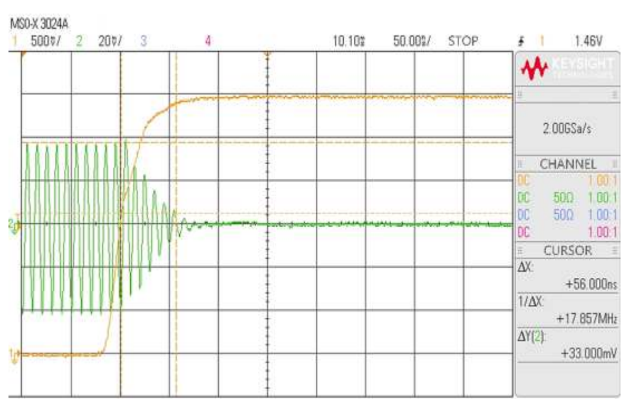


Figure 41. Evaluation Board Schematic

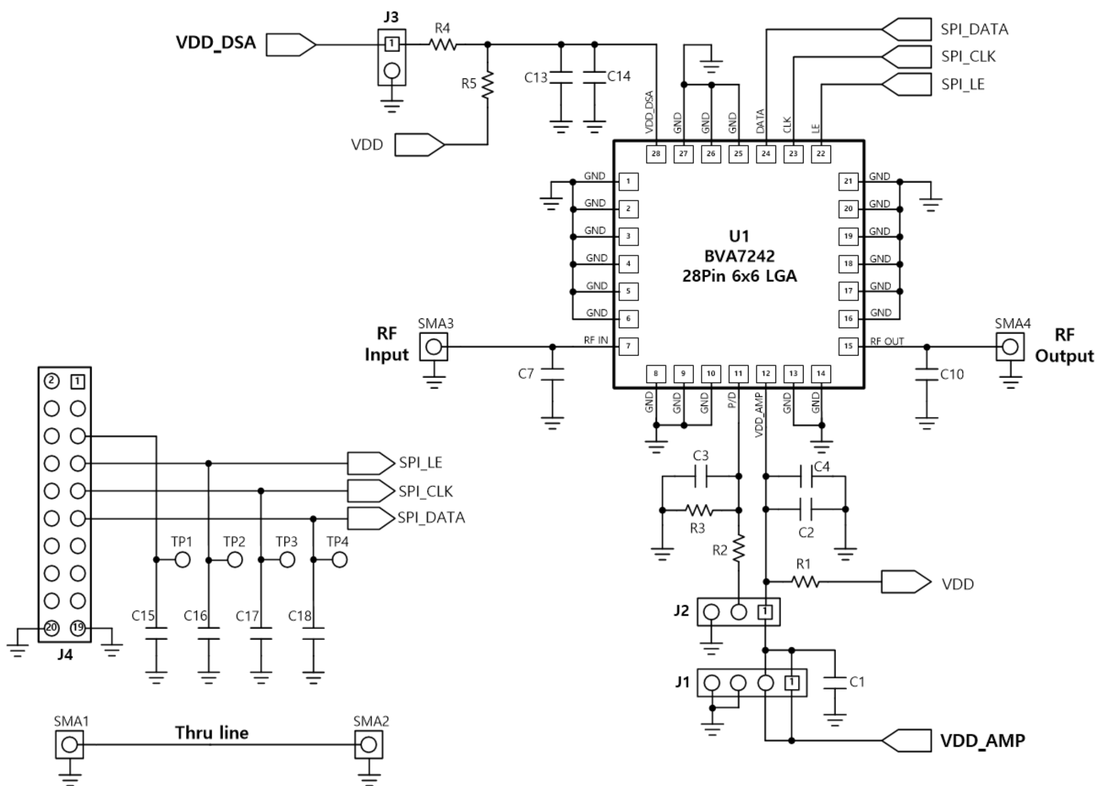
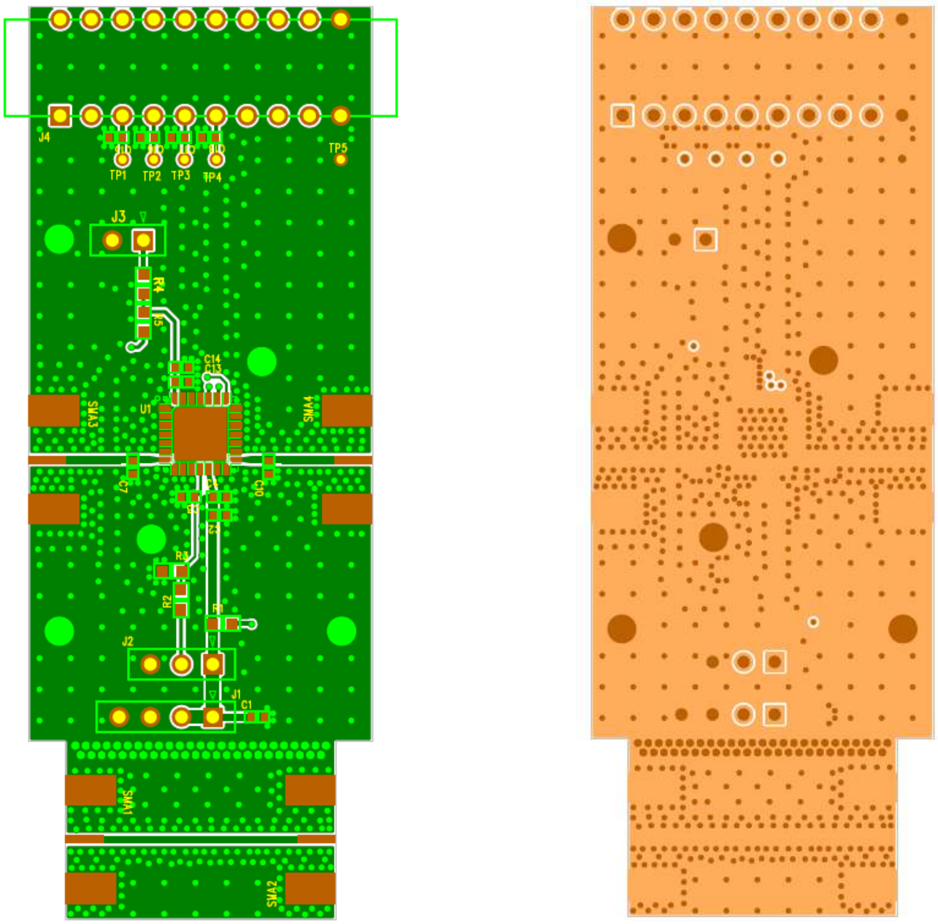


Table 13. Bill of material

No.	Ref. Number	Value	Description	Manufacturer
1	R2, R4	0 ohm	Resistor, 0603, Jumper	Walsin
2	R3	30 Kohm	Resistor, 0603, Chip, 5%	Walsin
3	C1	1 uF	Capacitor, 0402, Chip, 5%	Murata
4	C4, C14	100 nF	Capacitor, 0402, Chip, 5%	Murata
5	C7	0.5pF	Capacitor, 0402, Chip, 5%	Murata
6	SMA1, SMA2	SMA	SMA(F)_END_LAUNCH, PCB Mount	
7	SMA3, SMA4	SMA	SMA(F)_END_LAUNCH , PCB Mount	
8	J1	4pin	2.54mm Breakaway Male Header, Straight	
9	J2	3pin	2.54mm Breakaway Male Header, Straight	
10	J3	2pin	2.54mm Breakaway Male Header, Straight	
11	J4	20pin	Receptacle Connector, 5-532955-3, Female,RT/A Dual	AMP Connectors
12	R1, R5	DNI	Do not include	
13	C2,C3,C10,C13	DNI	Do not include	
14	C15,C16,C17,C18	DNI	Do not include	

Figure 42. Evaluation Board Layout



[Top View] [Bottom View]

Figure 43. Evaluation Board PCB Layer Information

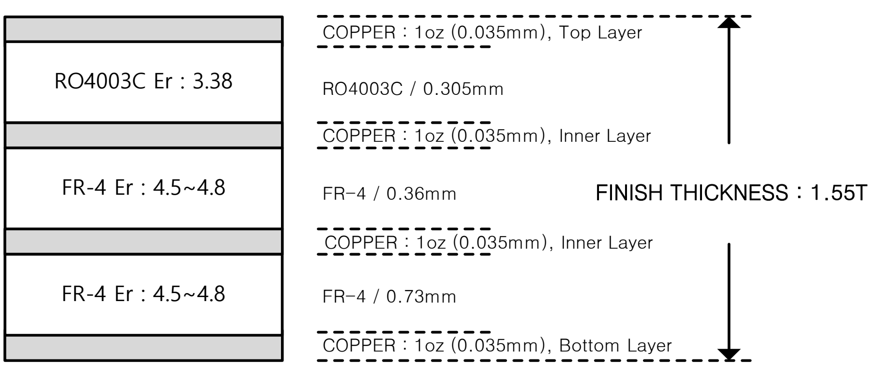


Figure 44. Suggested PCB Land Pattern and PAD Layout

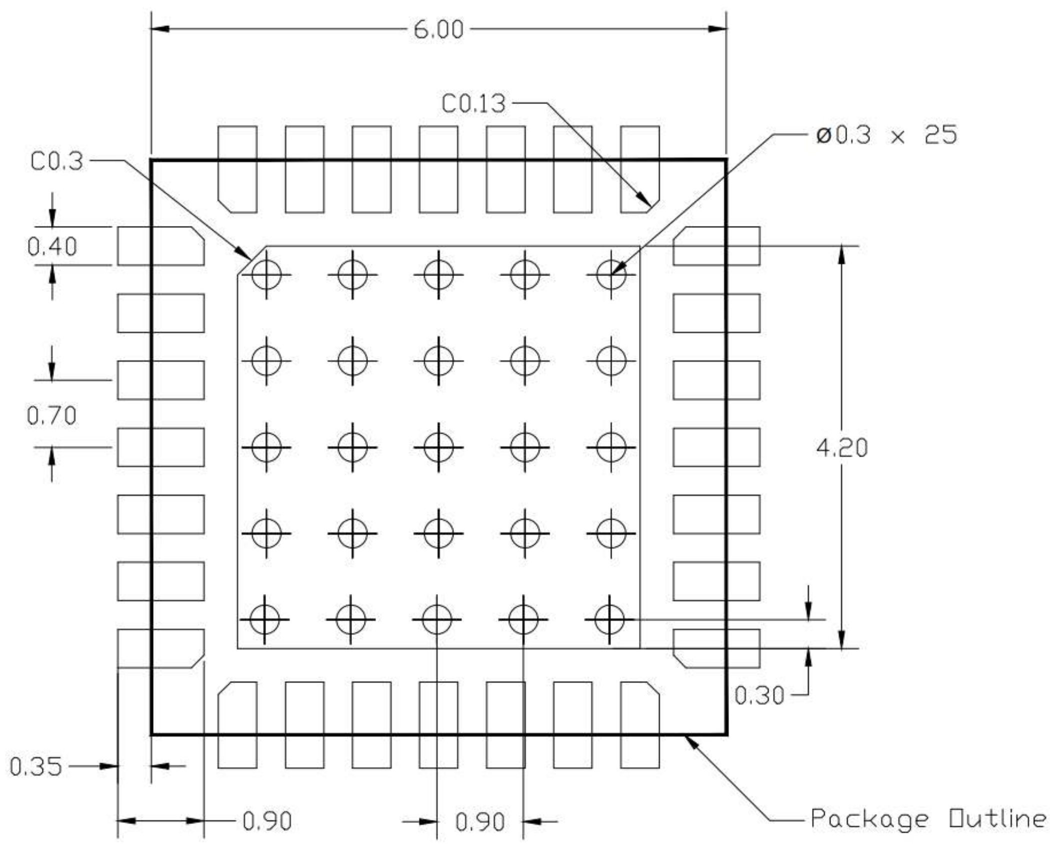
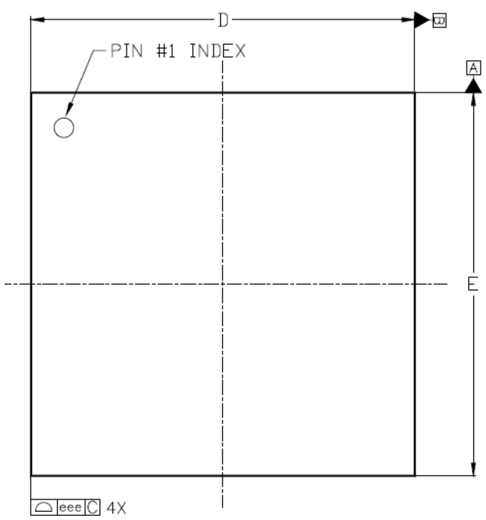
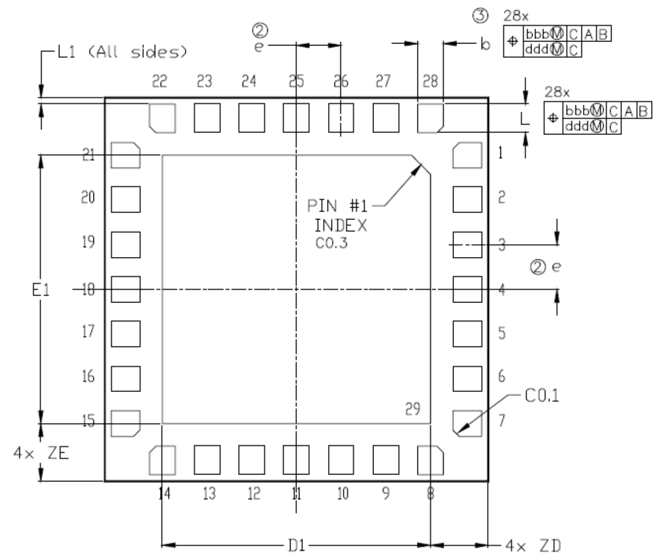


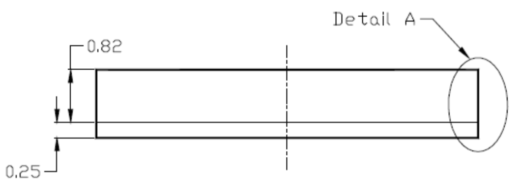
Figure 45. Package Outline Dimension



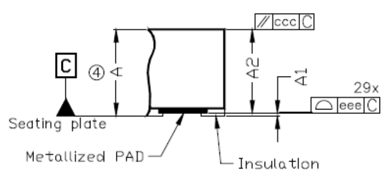
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Detail A

Dimension Table				
Symbol Thickness	Min	Nominal	Max	Note
A	1.01	1.07	1.13	
A1	—	—	0.03	
A2	—	—	1.10	
b		0.40		
L		0.45		
L1	0.00	0.10	0.20	
D	5.90	6.00	6.10	
E	5.90	6.00	6.10	
D1		4.20 BSC		
ZD		0.90 BSC		
E1		4.20 BSC		
ZE		0.90 BSC		
aaa		0.10		
bbb		0.10		
ccc		0.10		
ddd		0.08		
eee		0.08		

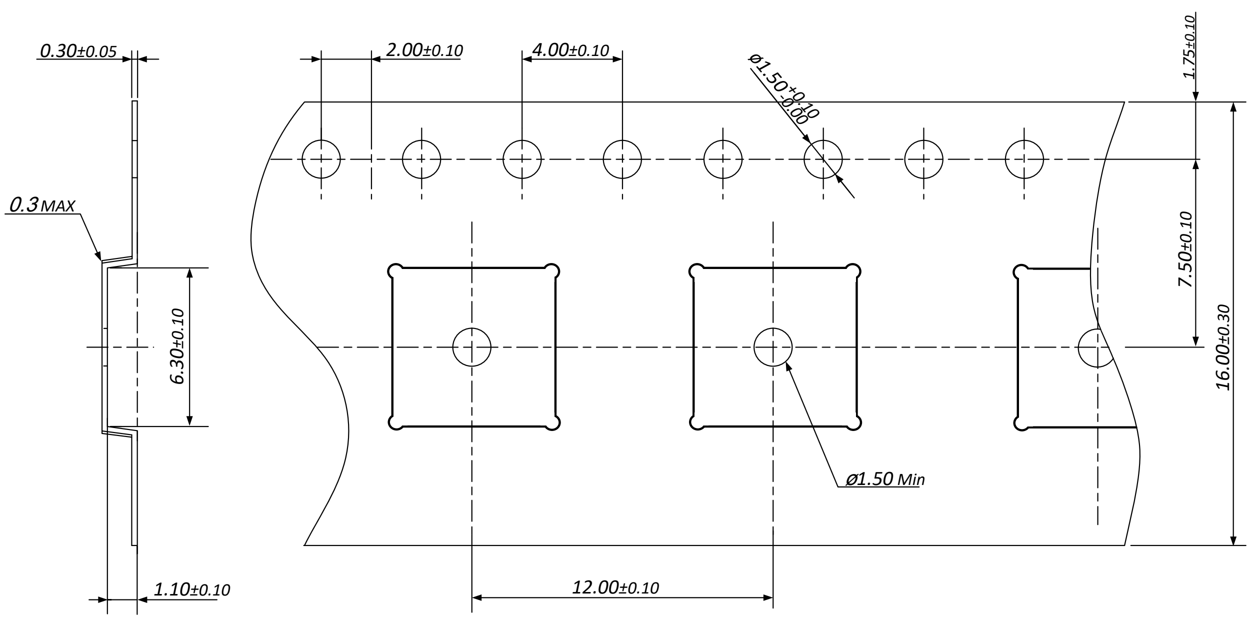
NOTES:

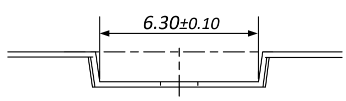
1. All dimensions are in millimeters.
2. 'e1, e2' represents the basic terminal pitch. Specifies the true geometric position of the terminal axis.
3. Dimension 'b' applies to metallized terminal and is measured between 0.00mm and 0.25mm from terminal tip.
4. Diemstion 'A' inclueds package warpage.
5. Exposed metallized pads are cu pads with surface finish protection.
6. Package dimensions take reference to JEDEC MO-208 REV.C.

Figure 46. Package Marking Information

YY = Year
WW = Working Week
XXX = Wafer Lot Number

Figure 47. Tape and Reel





Package information :
Tape Width : 16mm / Reel Size : 7 inches
Device Cavity Pitch : 12mm / Devices Per Reel : 1,000 EA

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating : Class 1C
Value : ±1000V
Test : Human Body Model (HBM)
Standard : JEDEC Standard JS-001-2017

ESD Rating : Class C3
Value : ±1000V
Test : Charged Device Model (CDM)
Standard : JEDEC Standard JS-002-2018

MSL Rating : MSL3 at +260°C convection reflow
Standard : JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F