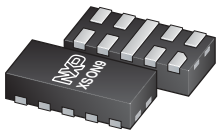


IP4285CZ9-TBB

ESD protection for high-speed interfaces

Rev. 2 — 12 July 2012 Product data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as High-Definition Multimedia Interface (HDMI), DisplayPort, USB, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes high-level ESD protection diodes for high-speed signal lines in a 4-channel 0.4 mm pitch DFN2110-9 (SOT1178-1/XSON9) package. The extremely small package dimensions make this product ideally suitable for portable devices. The pinout is designed for convenient flow-through routing of high-speed signal lines.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of 0.85 pF maximum. These diodes provide protection to downstream components from ESD voltages up to ±12 kV contact according to IEC 61000-4-2, level 4.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- System ESD protection for USB 2.0, HDMI 1.3 and HDMI 1.4, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±12 kV according to IEC 61000-4-2, level 4
- Matched 0.4 mm trace spacing
- Line capacitance of 0.85 pF maximum for each channel
- 4-channel, DFN2110-9 (SOT1178-1/XSON9) Pb-free package
- Design-friendly 'flow-through' signal routing

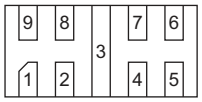
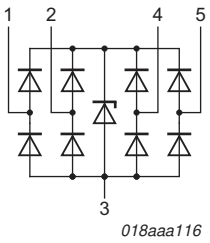
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- Portable devices
- Mobile handsets
- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 Transparent top view	 018aaa116
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	n.c.	not connected		
9	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4285CZ9-TBB	DFN2110-9	plastic extremely thin small outline package; no leads; 9 terminals; body 1 × 2.1 × 0.5 mm	SOT1178-1

4. Marking

Table 3. Marking codes

Type number	Marking code
IP4285CZ9-TBB	85

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage		−0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	pins 1, 2, 4, 5 to ground; IEC 61000-4-2, level 4			
		contact discharge	-	±12	kV
T_{amb}	ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

6. Characteristics

Table 5. Characteristics

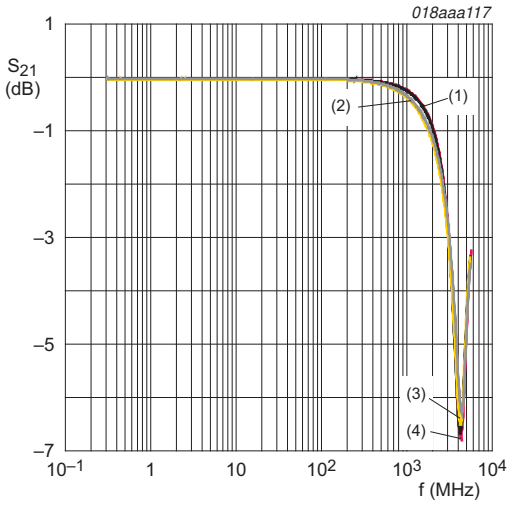
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_{test} = 1 mA		6	-	9	V
I_{RM}	reverse leakage current	per channel; V_I = 5.0 V		-	-	1	μA
V_F	forward voltage			-	0.7	-	V
C_{ch}	channel capacitance	f = 1 MHz	[1]				
		V_{bias} = 0 V		-	-	0.85	pF
		V_{bias} = 2.5 V		-	-	0.75	pF
ΔC_{ch}	channel capacitance difference	f = 1 MHz; V_{bias} = 2.5 V	[1]	-	-	0.1	pF
R_{dyn}	dynamic resistance	TLP	[3]				
		positive transient		-	0.42	-	Ω
		negative transient		-	0.33	-	Ω
		surge	[2]				
		positive transient		-	0.42	-	Ω
		negative transient		-	0.33	-	Ω
$V_{CL(trt)}$	transient clamping voltage	I_{PP} = 4 A	[2]				
		positive transient		-	4.2	-	V
		negative transient		-	−1.9	-	V

[1] This parameter is guaranteed by design.

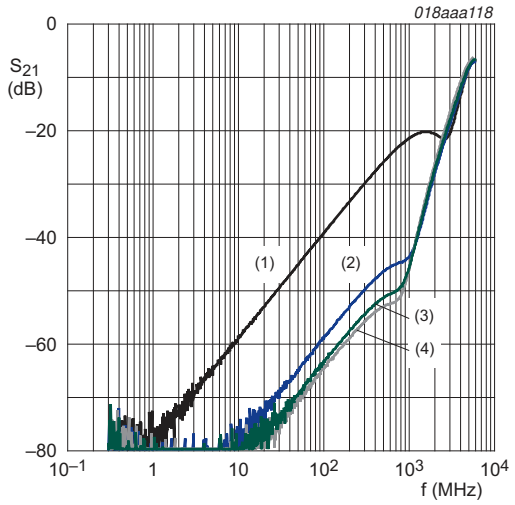
[2] According to IEC 61000-4-5.

[3] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.



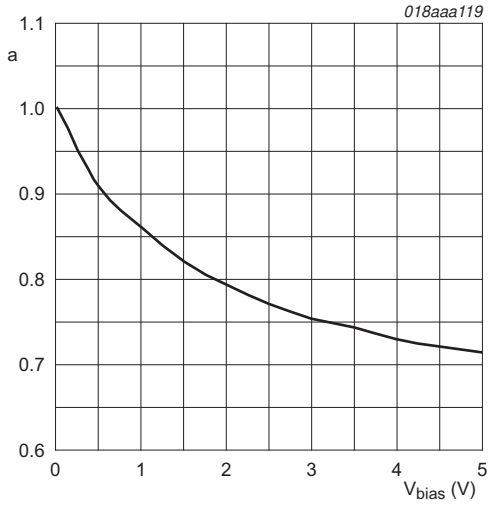
(1) Pin 1
(2) Pin 2
(3) Pin 4
(4) Pin 5

Fig 1. Insertion loss



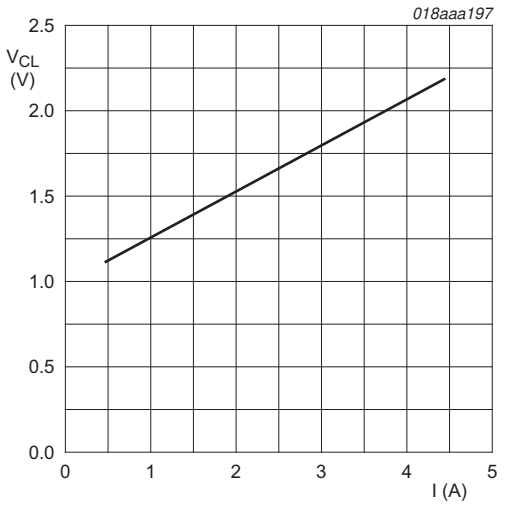
(1) Pin 1 to 2
(2) Pin 2 to 4
(3) Pin 2 to 5
(4) Pin 1 to 5

Fig 2. Crosstalk



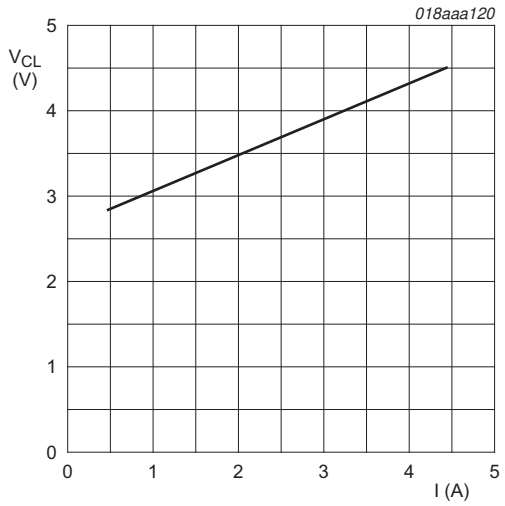
$$a = \frac{C_{ch(TMDS)}}{C_{ch(TMDS)(0V_{bias})}}$$

Fig 3. Relative channel capacitance as a function of bias voltage; typical values



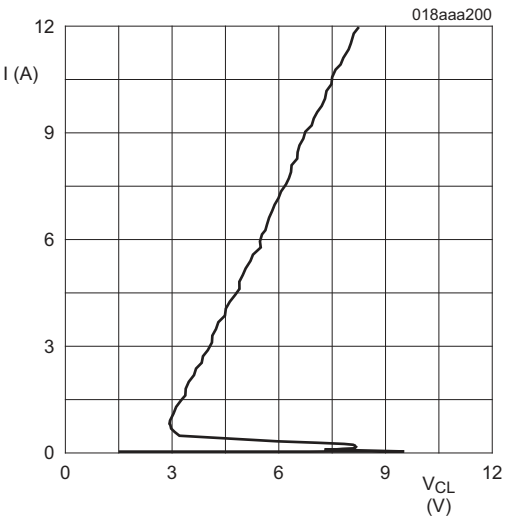
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 4. Dynamic resistance with positive clamping



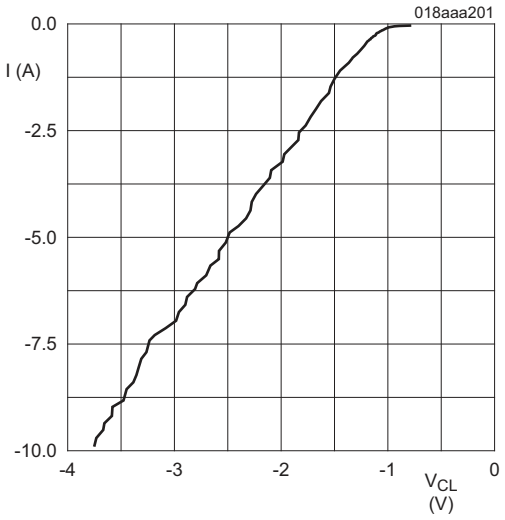
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 5. Dynamic resistance with negative clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

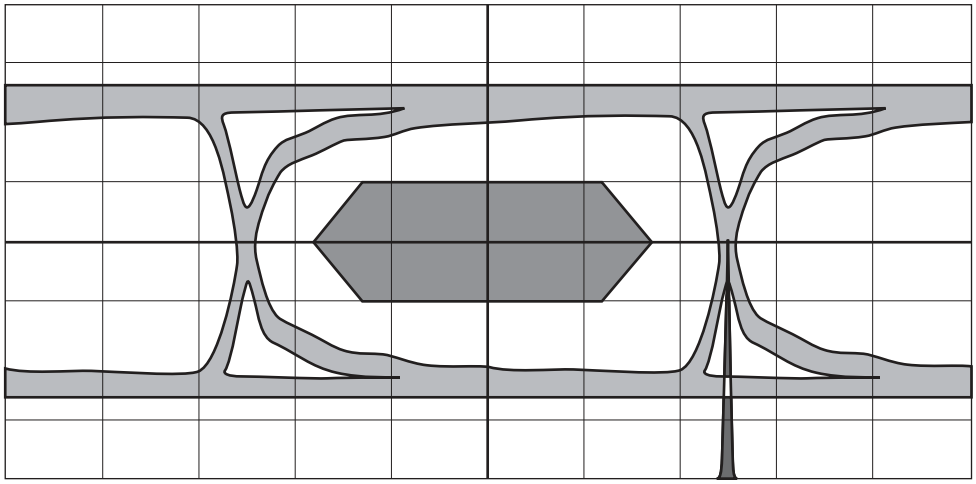
Fig 6. Dynamic resistance with positive clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with negative clamping

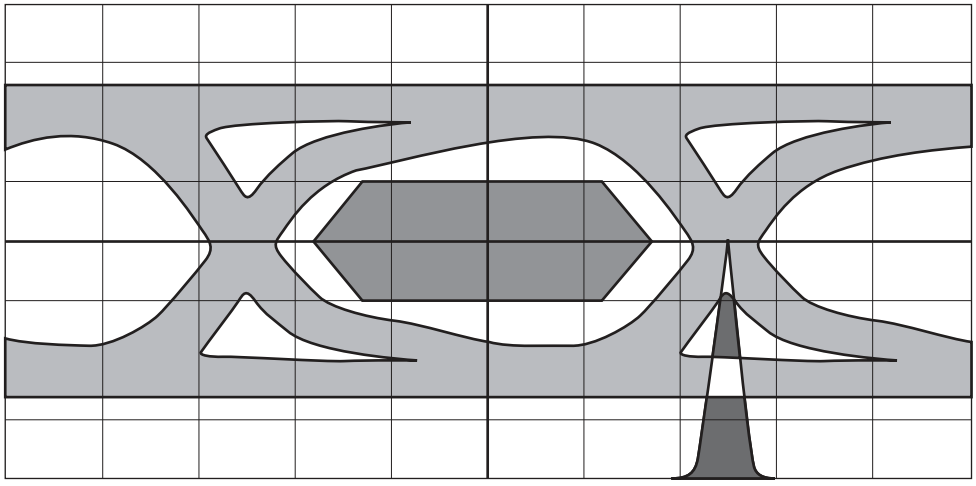
The device uses an advanced clamping structure, which shows a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).



001aao035

HDMI input signal 1280 × 720p; pixel clock = 74.25 MHz
Vertical scale = 200 mV/div
Horizontal scale = 270 ps/div

Fig 8. HDMI eye diagram with IP4285CZ9-TBB (720p)



001aao034

HDMI input signal 1920 × 1080p; pixel clock = 222.75 MHz
Vertical scale = 200 mV/div
Horizontal scale = 90 ps/div

Fig 9. HDMI eye diagram with IP4285CZ9-TBB (1080p)

7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), careful consideration should be given to basic high-speed routing guidelines, impedance matching, and signal coupling. Signal pins 1 and 2 (4 and 5) can be laid out through not connected pins 9 and 8 (6 and 7) respectively to avoid the need for vias and stubs.

Basic application diagrams for the ESD protection of an HDMI interface are shown in Figure 10.

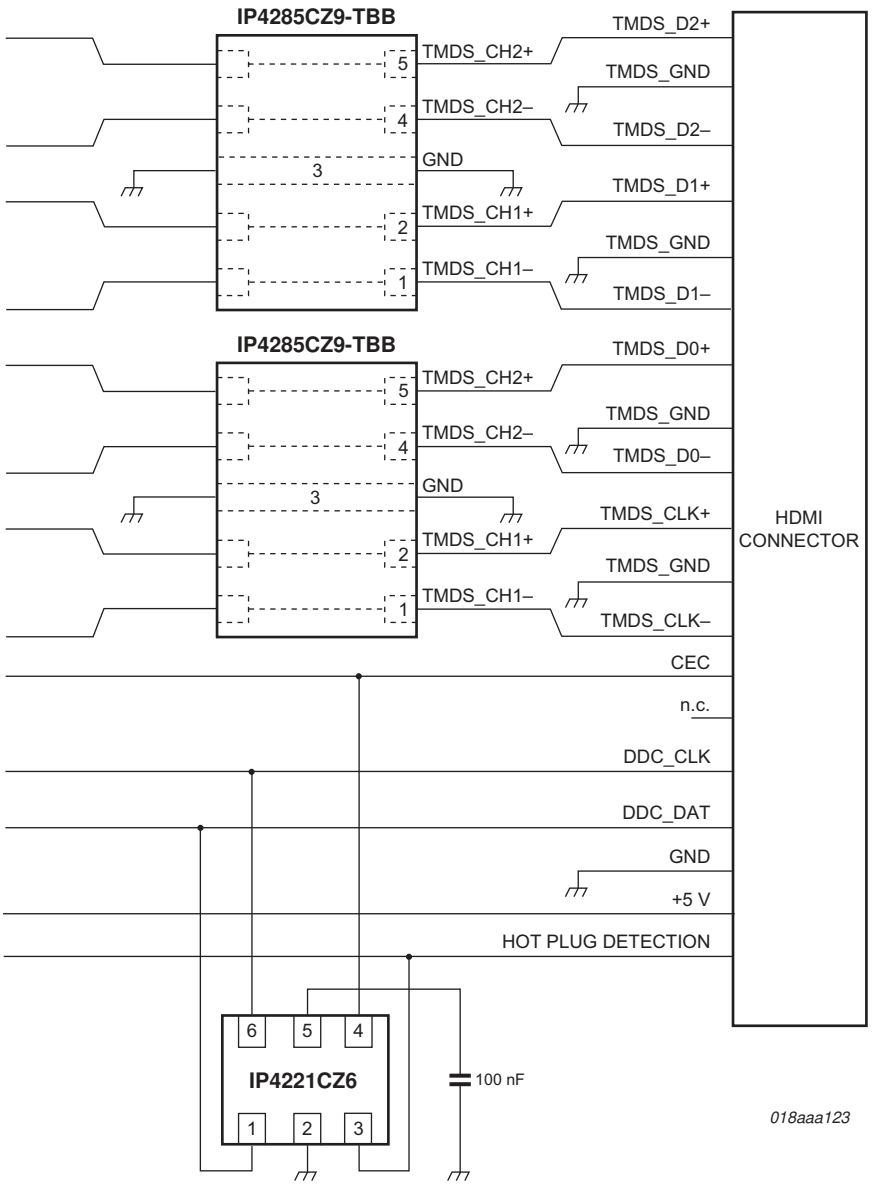


Fig 10. Application diagram of HDMI ESD protection using IP4285CZ9-TBB

8. Package outline

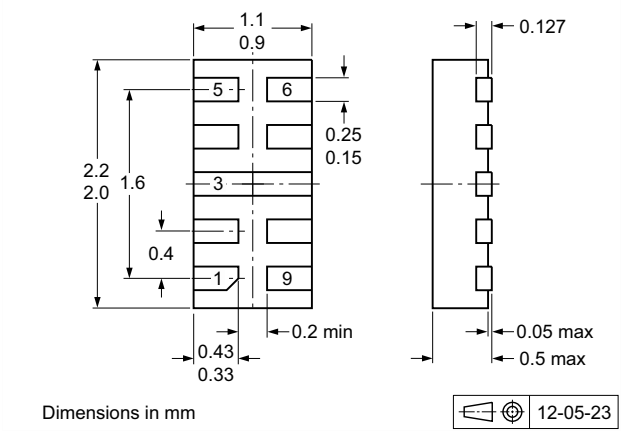
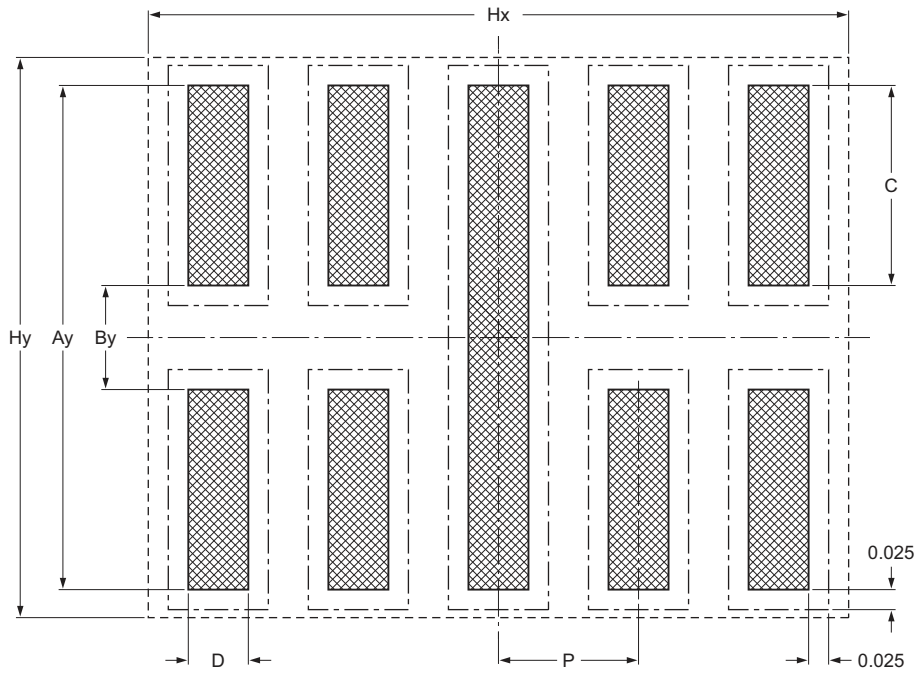


Fig 11. Package outline DFN2110-9 (SOT1178-1/XSON9)

9. Soldering

Footprint information for reflow soldering of XSON9 package **SOT1178-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

DIMENSIONS in mm

P	Ay	By	C	D	Hx	Hy
0.4	1.35	0.25	0.55	0.22	2.05	1.6

Issue date ~~11-06-27~~ 11-07-06

sot1178-1_fr

Fig 12. Reflow soldering footprint DFN2110-9 (SOT1178-1/XSON9)

10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4285CZ9-TBB v.2	20120712	Product data sheet	-	IP4285CZ9-TBB v.1
Modifications:	• Section 1 “Product profile”: updated • Section 4 “Marking”: added • Table 4 “Limiting values”: updated • Section 6 “Characteristics”: redesigned in order to specify in detail ESD protection behaviour • Section 8 “Package outline”: drawing replaced with minimized package outline drawing			
IP4285CZ9-TBB v.1	20110527	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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