ANALOG DEVICES

Wideband Voltage Feedback Amplifier

AD9622*

FEATURES
220 MHz Small Signal Bandwidth
160 MHz Large Signal BW (4 V p-p)
High Slew Rate: 1500 V/μs
Low Distortion: –66 dB @ 20 MHz
Fast Settling: 14 ns to 0.01%
3.5 nV/√Hz Spectral Noise Density
±3 V Supply Operation

APPLICATIONS
ADC Input Signal Amplifier
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Active Filters/Integrators/Log Amps

CONNECTION DIAGRAM

Pin		Pin	
NC #	1	8	NC #
–INPUT	2	7	+V$_S$
+INPUT	3	6	OUTPUT
–V$_S$	4	5	NC

AD9622

 # OPTIONAL CAPACITOR CB CONNECTED HERE
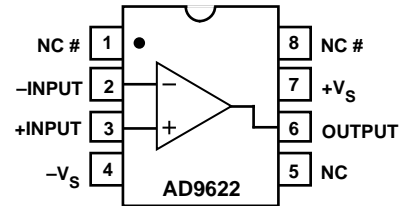**DECREASES SETTLING TIME (SEE TEXT).**

GENERAL DESCRIPTION
The AD9622 is one of a family of very high speed and wide-bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, low distortion, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9622 exhibits extraordinarily accurate and fast pulse response characteristics (8 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9622 offers performance not previously available in a monolithic operational amplifier.

*Protected by U.S. Patent 5,150,074 and others pending.

Other members of the AD962X amplifier family are the AD9621 (G = +1), AD9623 (G = +4), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9622 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS
1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Low Distortion
5. Output Short-Circuit Protected
6. Low Intermodulation Distortion of High Frequencies

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	–52	–66	–64	–66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/μs
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz – 200 MHz)	80	49	36	32	μV rms

REV. 0

AD9622–SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5$ V, $R_{LOAD} = 100$ Ω; $A_V = 2$, $R_F = 270$ Ω unless otherwise noted)

Parameter	Conditions	Temp	Test Level	AD9622AN/AQ/AR Min	Typ	Max	AD9622SQ Min	Typ	Max	Units
DC SPECIFICATIONS[1]										
Input Offset Voltage		+25°C	I	–10	±2	+10	–10	±2	+10	mV
		Full	VI	–12		+12	–12		+12	mV
Input Bias Current		+25°C	I		7	14		7	14	µA
		Full	VI			18			18	µA
Bias Current TC		Full	V		35			35		nA/°C
Input Offset Current		+25°C	I	–2	±0.3	+2	–2	±0.3	+2	µA
		Full	VI	–3		+3	–3		+3	µA
Offset Current TC		Full	V		2.5			2.5		nA/°C
Input Resistance		+25°C	V		500			500		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	$\Delta V_{CM} = 1$ V	+25°C	I	47	57		47	57		dB
Open-Loop Gain	$V_{OUT} = \pm 2$ V p-p	+25°C	V		60			60		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (–3 dB)										
Small Signal	$V_{OUT} \leq 0.4$ V p-p	Full	II	160	220		160	220		MHz
Large Signal[2]	$V_{OUT} \leq 4$ V p-p	+25°C	V		160			160		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.2	1.2		0.2	1.2	dB
Amplitude of Roll-off	DC to 100 MHz	Full	II		0	0.8		0	0.8	dB
Phase Nonlinearity	0.3 to 100 MHz	+25°C	V		1.3			1.3		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		–66	–56		–66	–56	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		–68	–56		–68	–56	dBc
Common-Mode Rejection Ratio	@ 20 MHz	+25°C	V		+23			+23		dB
Spectral Input Noise Voltage	1 to 200 MHz	+25°C	V		3.5			3.5		nV/√Hz
Spectral Input Noise Current	1 to 200 MHz	+25°C	V		3.2			3.2		pA/√Hz
Average Equivalent Integrated										
Input Noise Voltage	0.1 to 200 MHz	+25°C	V		49			49		µV rms
TIME DOMAIN										
Slew Rate	$V_{OUT} = 5$ V Step	Full	IV	1150	1500		1150	1500		V/µs
Rise/Fall Time	$V_{OUT} = 0.5$ V Step	+25°C	V		1.7			1.7		ns
	$V_{OUT} = 5$ V Step	Full	IV		3.1	4.2		3.1	4.2	ns
Overshoot	$V_{OUT} = 2$ V Step	Full	IV		3	15		3	15	%
Settling Time										
To 0.1%	$V_{OUT} = 2$ V Step	+25°C	V		8			8		ns
To 0.01%	$V_{OUT} = 2$ V Step	Full	IV		14	19		14	19	ns
To 0.1%[3]	$V_{OUT} = 4$ V Step	+25°C	V		10			10		ns
To 0.01%[3]	$V_{OUT} = 4$ V Step	+25°C	V		17			17		ns
Overdrive Recovery	2× to ±2 mV	+25°C	V		150			150		ns
Differential Gain (4.3 MHz)	$R_L = 150$ Ω	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	$R_L = 150$ Ω	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS[1]										
Supply Voltage ($\pm V_S$)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
$+I_S$	$+V_S = +5$ V	Full	VI		23	29		23	29	mA
$-I_S$	$-V_S = -5$ V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	$\Delta V_S = 0.5$ V	+25°C	I	54	63		54	63		dB

NOTES

[1]Measured at $A_V = 21$.

[2]Effective large signal bandwidth; the device should not be stressed above 250 V × MHz (V_{OUT} p-p × Frequency) to ensure long term reliability.

[3]Measured with a 0.001 µF C_B capacitor connected across Pins 1 and 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . ± 6 V
Common-Mode Input Voltage . . . . $\pm V_S$
Voltage Swing × Bandwidth Product . . . . 250 V × MHz
Differential Input Voltage . . . . .6 V
Continuous Output Current[2] . . . . 90 mA
Operating Temperature Ranges
    AN, AQ, AR . . . . –40°C to +85°C
    SQ . . . . –55°C to +125°C
Storage Temperature
    Ceramic . . . . –65°C to +150°C
    Plastic . . . . –65°C to +125°C
Junction Temperature
    Ceramic[3] . . . . +175°C
    Plastic[3] . . . . +150°C
Lead Soldering Temperature (1 minute)[4] . . . . +220°C
NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.
[3]Typical thermal impedances (part soldered onto board; no air flow):
    Ceramic DIP: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W
    Plastic SOIC: θ_{JA} = 125°C/W; θ_{JC} = 45°C/W
    Plastic DIP: θ_{JA} = 90°C/W; θ_{JC} = 45°C/W
[4]Temperature shown is for surface mount devices, mounted by vapor phase soldering. Throughhole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9622AN	–40°C to +85°C	8-Pin Plastic DIP	N-8
AD9622AQ	–40°C to +85°C	8-Pin Cerdip	Q-8
AD9622AR	–40°C to +85°C	8-Pin SOIC	R-8
AD9622SQ	–55°C to +125°C	8-Pin Cerdip	Q-8

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of "A" grade devices done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Chip Layout
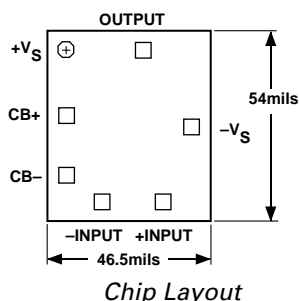
THEORY OF OPERATION

The AD9622 is a wide bandwidth voltage feedback amplifier that is guaranteed for minimum gain stability of +2. Since its open-loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9622 typically maintains a 60 degree unity loop gain phase margin with $R_F \cong 270\ \Omega$. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice
At minimum stable gain (+2), the AD9622 provides optimum dynamic performance with R_F = 270 Ω. When using this value and following the high speed layout guidelines, a shunt capacitor (C_F) should not be required. This value for R_F provides the best combination of wide bandwidth, low peaking, and distortion.

However, if improved gain flatness is desired, a shunt capacitor (C_F) will provide extra phase margin. This reduces both overshoot and peaking with only a slight reduction of bandwidth.

As an example, if the amplifier exhibits (worst case) peaking of 1 dB with $R_G \| R_F$ = 135 Ω (A_V = 2), then using a C_F of ≈ 1.5 pF across R_F will reduce this peaking to 0 dB. In addition, overshoot, noise, and settling time (0.01%) will also improve. This comes at the expense of slightly decreased closed-loop bandwidth due to the $R_F \times C_F$ time constant created.

If the equivalent input capacitance greatly exceeds 2 pF (due to source drive or long input traces to the amplifier), then added shunt capacitance (C_F) will be necessary to maintain stability. Likewise, if larger R_G/R_F minimum-gain setting resistors are used, C_F will be necessary. As a rule of thumb, if the product of $R_F \| R_G \times C_I \leq 270 \times 10^{-12}$ seconds, then C_F is not required (for maximum bandwidth applications) and the amplifier's phase margin will maintain about 60°.

For $R_F \| R_G$ >150 Ω, use a C_F equal to $C_I \times R_G/R_F$. As the value of $R_F \| R_G$ increases, the bandwidth of the amplifier will begin to be controlled by the $R_F \times C_F$ time constant. Increasing C_F much beyond these guidelines will also cause amplifier instability.

Pulse Response
Unlike a traditional voltage feedback amplifier in which slew speed is usually dictated by its front end dc quiescent current and gain bandwidth product, the AD9622 provides "on demand" transconductance current that increases proportionally to the input "step" signal amplitude. This results in slew speeds (1500 V/µs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (3.2 pA/√Hz), gives the AD9622 the best attributes of both voltage and current feedback amplifiers.

Bootstrap Capacitor (C_B)
In most applications, the C_B capacitor should not be required. Under certain conditions, it can be used to further enhance settling time performance.
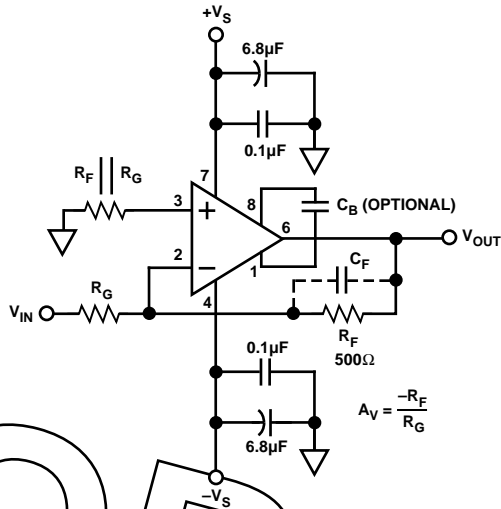
AD9622

Figure 1. Inverting Gain Connection Diagram

$$A_V = \frac{-R_F}{R_G}$$

Figure 2. Noninverting Gain Connection Diagram

$$A_V = 1 + \frac{R_F}{R_G}$$

The C_B capacitor (0.001 µF) connects to the internal high impedance nodes of the amplifier. Using this capacitor will reduce the large signal (4 V) step output settling time by 3 ns to 5 ns for 0.05% or greater accuracy. For settling accuracy less than 0.05% or for smaller step sizes, its effect will be less apparent.

Under heavy slew conditions, this capacitor forces the internal signal (initial step) amplitude to be controlled by the "on" (slewed) transistor, preventing its complement from completely turning off. This allows for faster settling time of these internal nodes and also the output.

In the frequency domain, total (high frequency) distortion will be approximately the same with or without C_B. Typically, the 3rd harmonic will be greater than the 2nd without C_B. This will be reversed with C_B in place.

APPLICATIONS

The AD9622 is a voltage feedback amplifier and is well suited for such applications as active filters, and log amplifiers. The device's wide bandwidth (230 MHz), phase margin (55°), low noise current (3.2 pA /$\sqrt{Hz}$), and slew rate (1500 V/µs) give higher performance capabilities to these applications over previous voltage feedback designs.

With a settling time of 15 ns to 0.01% and 8 ns to 0.1%, the device is an excellent choice for DAC I/V conversion. The same characteristics along with low harmonic distortion make it a good choice for ADC buffering/ amplification. With its superb linearity at relatively high signal frequencies, it is an ideal driver for ADCs up to 14 bits.

Layout Considerations

As with all wide bandwidth components, printed circuit layout is critical to obtain best dynamic performance with the AD9622. The ground plane in the area of the amplifier and its associated components should cover as much of the component side of the board as possible (or first interior layer of a multilayer surface mount board).

The ground plane should be removed in the area of the inputs and R_F and R_G to minimize stray capacitance at the input. The same precaution should be used for C_F, if used. Each power supply trace should be decoupled close to the package with a 0.1 µF ceramic capacitor, plus a 6.8 µF tantalum nearby.

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Microstrip techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if at all possible because of their high series inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray reactance than molded socket assemblies.

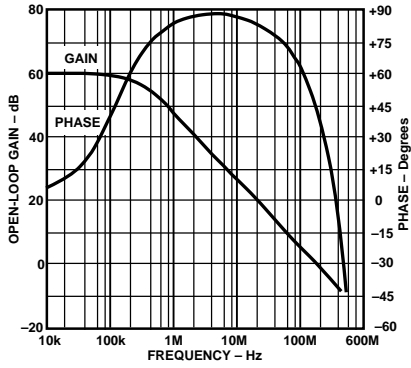An evaluation board is available from Analog Devices for a nominal charge.
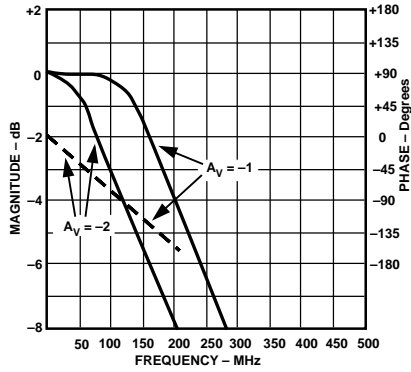
Figure 3. Open-Loop Gain and Phase

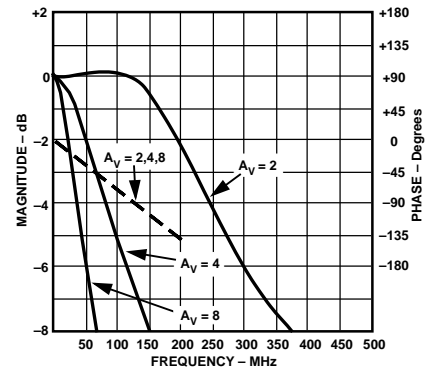Figure 4. Inverting Frequency Response
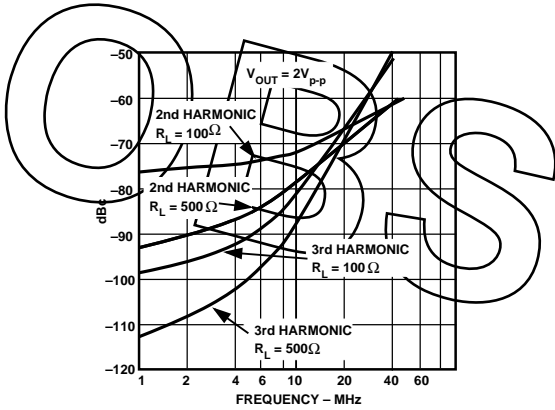

Figure 5. Noninverting Frequency Response

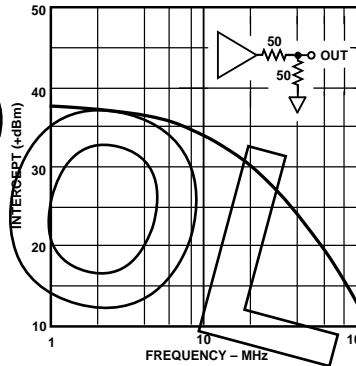Figure 6. Harmonic Distortion vs. Frequency
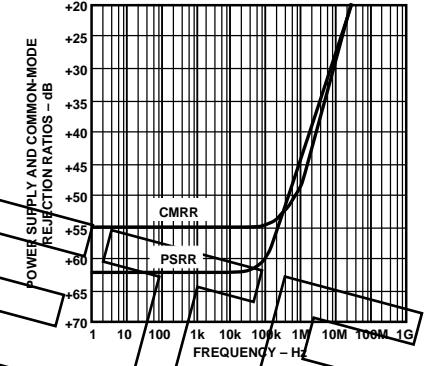

Figure 7. Third Order Intercept
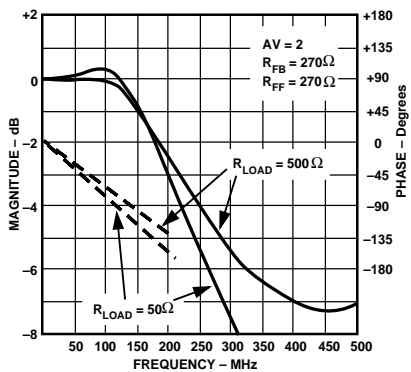

Figure 8. CMRR and PSRR vs. Frequency

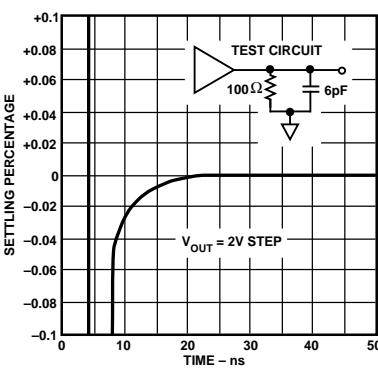Figure 9. Frequency Response vs. R_{LOAD}
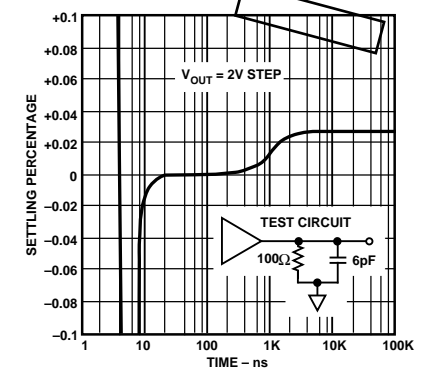

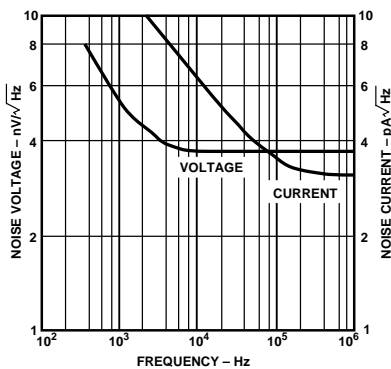Figure 10. Short-Term Settling Time

Figure 11. Long-Term Settling Time
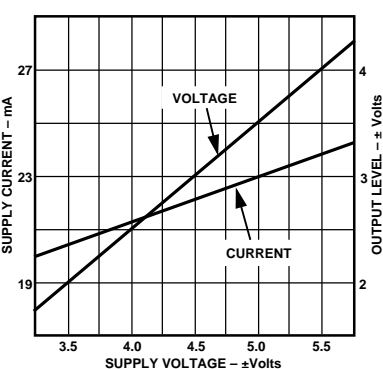

Figure 12. Input Spectral Noise Density
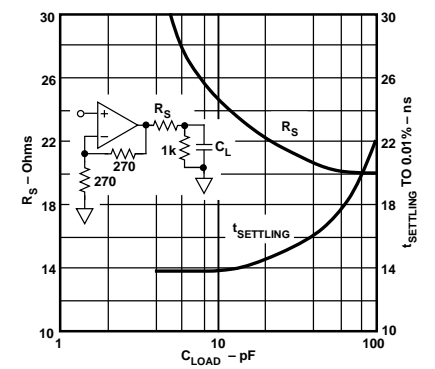

Figure 13. Output Level and Supply Current vs. Supply Voltage

Figure 14. Settling Time vs. Capacitive Load

AD9622
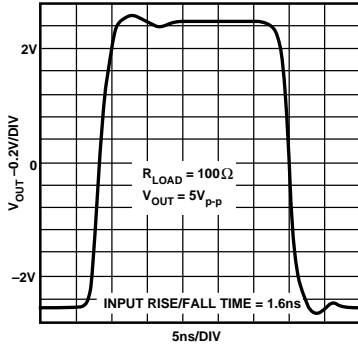
Figure 15. Large Signal Pulse Response
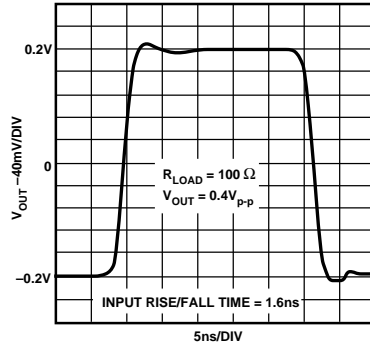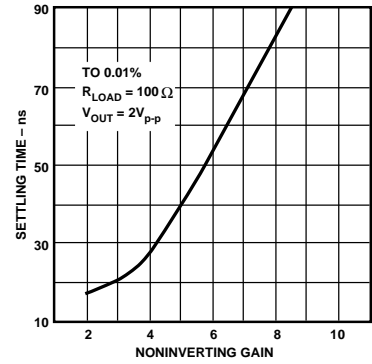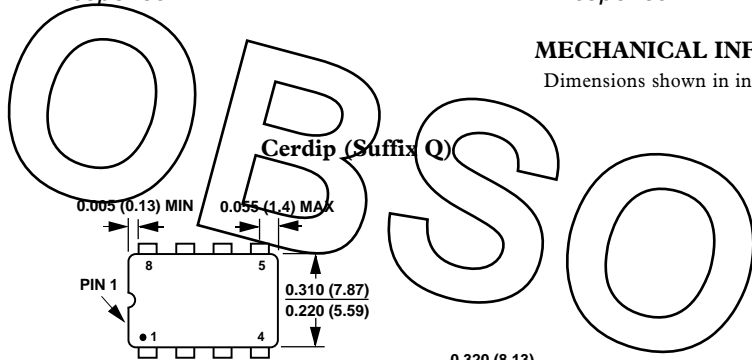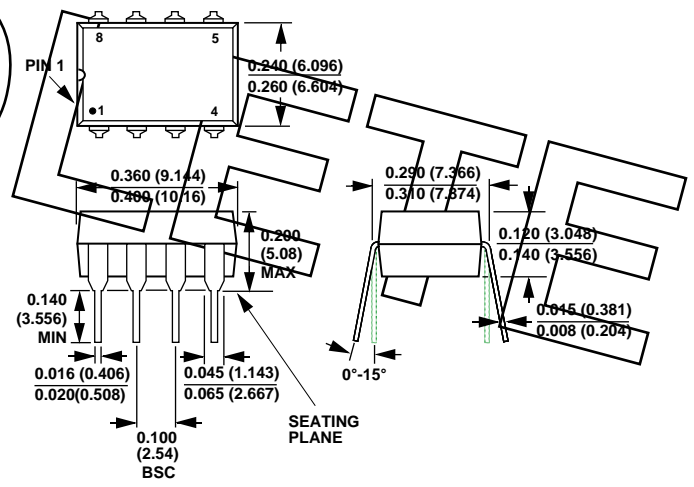

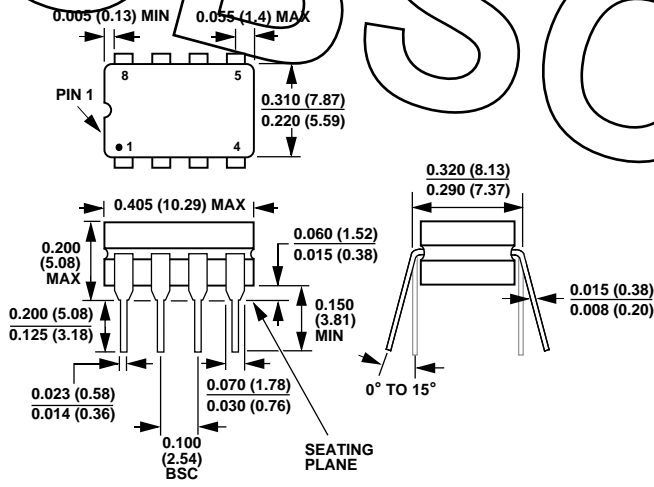Figure 16. Small Signal Pulse Response

Figure 17. Settling Time vs. Noninverting Gain

MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

Cerdip (Suffix Q)

Plastic DIP (Suffix N)

Plastic SOIC (Suffix R)

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