TS3A4751 0.9-Ω Low-voltage, single-supply, 4-channel spst analog switch

1 Features

- Low ON-State Resistance (R_{ON})
  - 0.9 Ω Max (3-V Supply)
  - 1.5 Ω Max (1.8-V Supply)
- R_{ON} Flatness: 0.4 Ω Max (3-V)
- R_{ON} Channel Matching
  - 0.05 Ω Max (3-V Supply)
  - 0.15 Ω Max (1.8-V Supply)
- 1.6-V to 3.6-V Single-Supply Operation
- 1.8-V CMOS Logic Compatible (3-V Supply)
- High Current-Handling Capacity (100 mA Continuous)
- Fast Switching: t_{ON} = 5 ns, t_{OFF} = 4 ns
- Supports Both Digital and Analog Applications
- ESD Protection Exceeds JESD-22
  - ±4000-V Human Body Model (A114-A)
  - 300-V Machine Model (A115-A)
  - ±1000-V Charged-Device Model (C101)

2 Applications

- Power Routing
- Battery-Powered Systems
- Audio and Video Signal Routing
- Low-Voltage Data-Acquisition Systems
- Communications Circuits
- PCMCIA Cards
- Cellular Phones
- Modems
- Hard Drives

3 Description

The TS3A4751 device is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

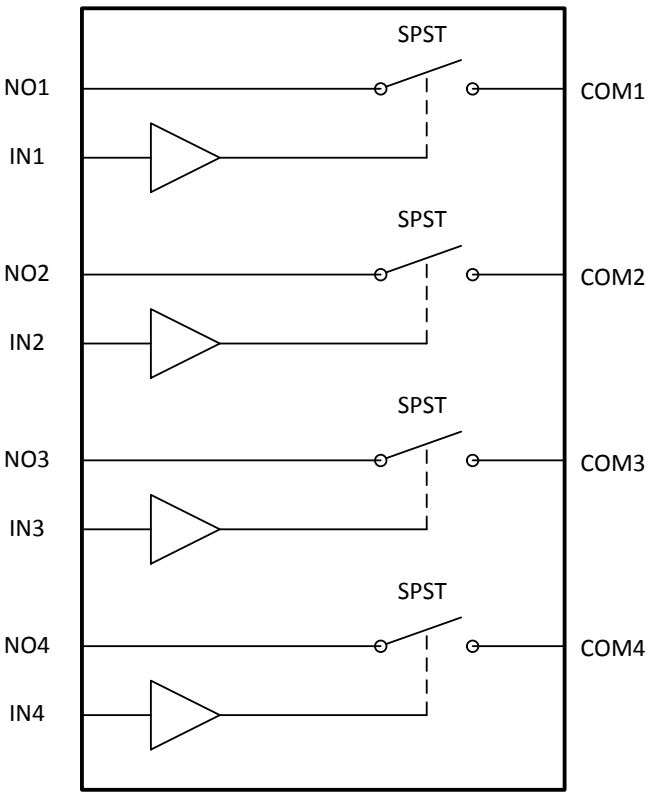
The TS3A4751 device has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3A4751	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm
	X2QFN (14)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision E (January 2015) to Revision F **Page**

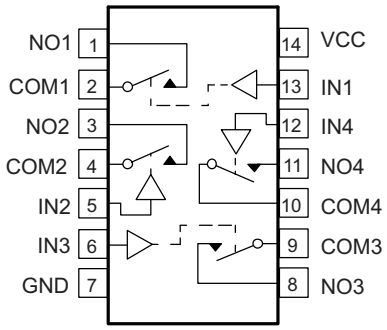
- Changed Supply Voltage from: 3.3 V to: 3.6 V in the *Recommended Operating Conditions* ... 5

Changes from Revision D (July 2008) to Revision E **Page**

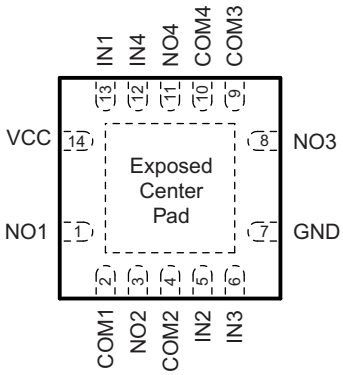
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

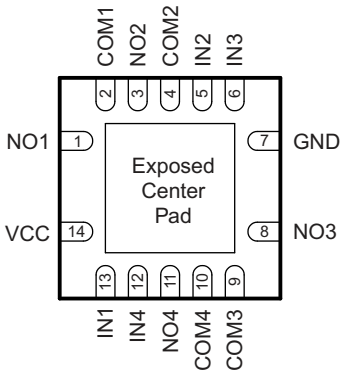
PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)

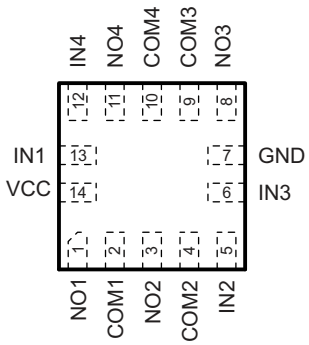


RGY PACKAGE
(BOTTOM VIEW)

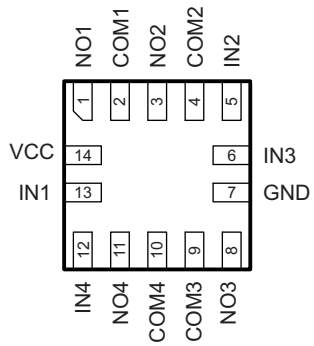


If the exposed center pad is used, it must be connected as a secondary ground or left electrically open.

RUC PACKAGE
(TOP VIEW)



RUC PACKAGE
(BOTTOM VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO1	I/O	Normally open signal path
2	COM1	I/O	Common signal path
3	NO2	I/O	Normally open signal path
4	COM2	I/O	Common signal path
5	IN2	I	Logic control input
6	IN3	I	Logic control input
7	GND	—	Ground
8	NO3	I/O	Normally open signal path
9	COM3	I/O	Common signal path
10	COM4	I/O	Common signal path
11	NO4	I/O	Normally open signal path
12	IN4	I	Logic control input
13	IN1	I	Logic control input
14	V_{CC}	I	Positive supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage referenced to GND(2)		–0.3	4	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage		–0.3	V_{CC} + 0.3	V
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–100	100	mA
I_{CC} I_{GND}	Continuous current through V_{CC} or GND			±100	mA
V	Peak current pulsed at 1 ms, 10% duty cycle	COM, $V_{I/O}$		±200	mA
T_A	Operating temperature		–40	85	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Signals on COM or NO exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to maximum current rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1000	
		Machine Model	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply Voltage	1.65	3.6	V
V_{NO} V_{COM} V_{IN}	Analog and digital voltage range	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC(1)		TS3A4751			UNIT
		PW	RGY	RUC	
		14 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.3	68.5	196.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.6	83.1	73.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	74.2	44.6	130.7	
ψ_{JT}	Junction-to-top characterization parameter	11.2	7.8	2.1	
ψ_{JB}	Junction-to-board characterization parameter	73.6	44.7	130.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	24.6	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C, V_{IH} = 1 V, V_{IL} = 0.4 V (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(3)	MAX	UNIT
ANALOG SWITCH								
V_{COM}, V_{NO}	Analog signal range				0		V_{CC}	V
R_{on}	ON-state resistance	V_{CC} = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		1	1.5	Ω
				Full			2	
ΔR_{on}	ON-state resistance match between channels(4)	V_{CC} = 1.8 V, I_{COM} = –10 mA, V_{NO} = 0.9 V		25°C		0.09	0.15	Ω
				Full			0.25	
$R_{on(flat)}$	ON-state resistance flatness(5)	V_{CC} = 1.8 V, I_{COM} = –10 mA, 0 ≤ V_{NO} ≤ V_{CC}		25°C		0.7	0.9	Ω
				Full			1.5	
$I_{NO(OFF)}$	NO OFF leakage current(6)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.8 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
$I_{COM(OFF)}$	COM OFF leakage current(6)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 1.65 V, 0.15 V		25°C	–1	0.5	1	nA
				Full	–10		10	
$I_{COM(ON)}$	COM ON leakage current(6)	V_{CC} = 1.95 V, V_{COM} = 0.15 V, 1.65 V, V_{NO} = 0.15 V, 1.65 V, or floating		25°C	–1	0.01	1	nA
				Full	–3		3	
DYNAMIC								
t_{ON}	Turn-on time	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 1		25°C		6	18	ns
				Full			20	
t_{OFF}	Turn-off time	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 1		25°C		5	10	ns
				Full			12	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 5		25°C		3.2		pC
$C_{NO(OFF)}$	NO OFF capacitance	f = 1 MHz, See Figure 2		25°C		23		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 2		25°C		20		pF
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 2		25°C		43		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON		25°C		123		MHz
O_{ISO}	OFF isolation(7)	R_L = 50 Ω, C_L = 5 pF, See Figure 3	f = 1 MHz	25°C		–61		dB
			f = 10 MHz			–36		
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF, See Figure 3	f = 10 MHz	25°C		–95		dB
			f = 100 MHz			–73		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.14%		
			R_L = 600 Ω			0.013%		
DIGITAL CONTROL INPUTS (IN1–IN4)								
V_{IH}	Input logic high			Full	1			V
V_{IL}	Input logic low			Full			0.4	V
I_{IN}	Input leakage current	V_I = 0 or V_{CC}		25°C		0.1	5	nA
				Full	–10		10	
SUPPLY								
V_{CC}	Power-supply range				1.6		3.6	V
I_{CC}	Positive-supply current	V_I = 0 or V_{CC}		25°C			0.05	µA
				Full			0.5	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

6.6 Electrical Characteristics for 3-V Supply

V_{CC} = 2.7 V to 3.6 V, T_A = –40°C to 85°C, V_{IH} = 1.4 V, V_{IL} = 0.5 V (unless otherwise noted).(1) (2)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(3)	MAX	UNIT
ANALOG SWITCH								
V_{COM}, V_{NO}	Analog signal range				0		V_{CC}	V
R_{on}	ON-state resistance	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.7	0.9	Ω
				Full			1.1	
ΔR_{on}	ON-state resistance match between channels(4)	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1.5 V		25°C		0.03	0.05	Ω
				Full			0.15	
$R_{on(flat)}$	ON-state resistance flatness(5)	V_{CC} = 2.7 V, I_{COM} = –100 mA, V_{NO} = 1 V, 1.5 V, 2 V		25°C		0.23	0.4	Ω
				Full			0.5	
$I_{NO(OFF)}$	NO OFF leakage current(6)	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
$I_{COM(OFF)}$	COM OFF leakage current(6)	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 3 V, 0.3 V		25°C	–2	1	2	nA
				Full	–18		18	
$I_{COM(ON)}$	COM ON leakage current(6)	V_{CC} = 3.6 V, V_{COM} = 0.3 V, 3 V, V_{NO} = 0.3 V, 3 V, or floating		25°C	–2.5	0.01	2.5	nA
				Full	–5		5	
DYNAMIC								
t_{ON}	Turn-on time	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 1		25°C		5	14	ns
				Full			15	
t_{OFF}	Turn-off time	V_{NO} = 1.5 V, R_L = 50 Ω, C_L = 35 pF, See Figure 1		25°C		4	9	ns
				Full			10	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 1 nF, See Figure 5		25°C		3		pC
$C_{NO(OFF)}$	NO OFF capacitance	f = 1 MHz, See Figure 2		25°C		23		pF
$C_{COM(OFF)}$	COM OFF capacitance	f = 1 MHz, See Figure 2		25°C		20		pF
$C_{COM(ON)}$	COM ON capacitance	f = 1 MHz, See Figure 2		25°C		43		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON		25°C		125		MHz
O_{ISO}	OFF isolation(7)	R_L = 50 Ω, C_L = 5 pF, See Figure 3	f = 10 MHz	25°C		–40		dB
			f = 1 MHz			–62		
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF, See Figure 3	f = 10 MHz	25°C		–73		dB
			f = 1 MHz			–95		
THD	Total harmonic distortion	f = 20 Hz to 20 kHz, V_{COM} = 2 V_{P-P}	R_L = 32 Ω	25°C		0.04%		
			R_L = 600 Ω			0.003%		
DIGITAL CONTROL INPUTS (IN1–IN4)								
V_{IH}	Input logic high			Full	1.4			V
V_{IL}	Input logic low			Full			0.5	V
I_{IN}	Input leakage current	V_I = 0 or V_{CC}		25°C		0.5	1	nA
				Full	–20		20	
SUPPLY								
V_{CC}	Power-supply range				1.6		3.6	V
I_{CC}	Positive-supply current	V_{CC} = 3.6 V, V_{IN} = 0 or V_{CC}		25°C			0.075	μA
				Full			0.75	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(2) Parts are tested at 85°C and specified by design and correlation over the full temperature range.
(3) Typical values are at V_{CC} = 3 V, T_A = 25°C.
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$
(5) Flatness is defined as the difference between the maximum and minimum value of r_{on} as measured over the specified analog signal ranges.
(6) Leakage parameters are 100% tested at the maximum-rated hot operating temperature and specified by correlation at T_A = 25°C.
(7) OFF isolation = $20_{log}10$ (V_{COM}/V_{NO}), V_{COM} = output, V_{NO} = input to OFF switch

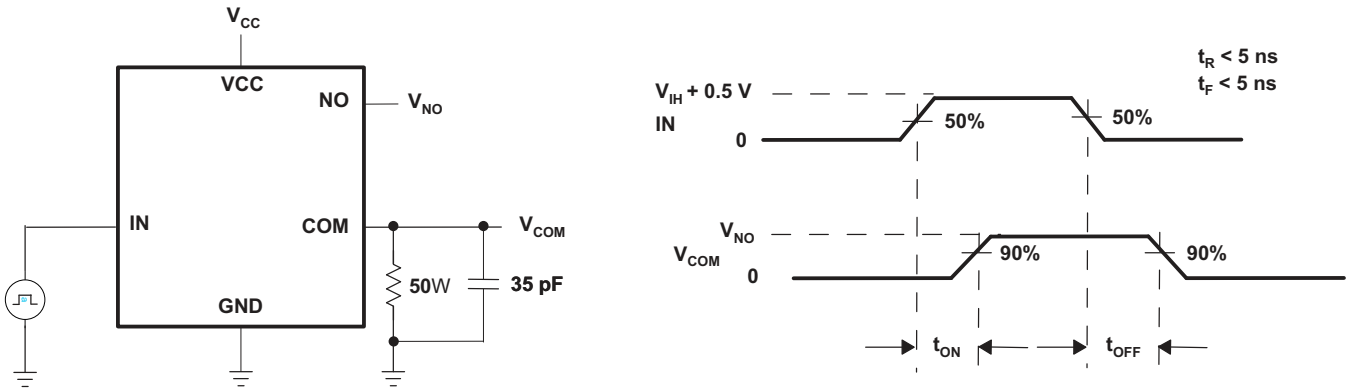


Figure 1. Switching Times

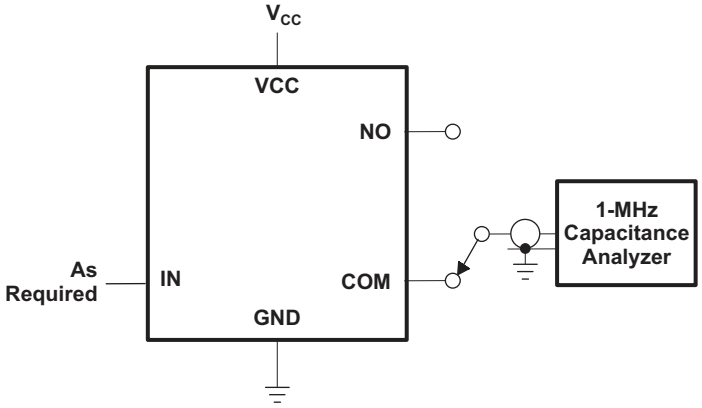
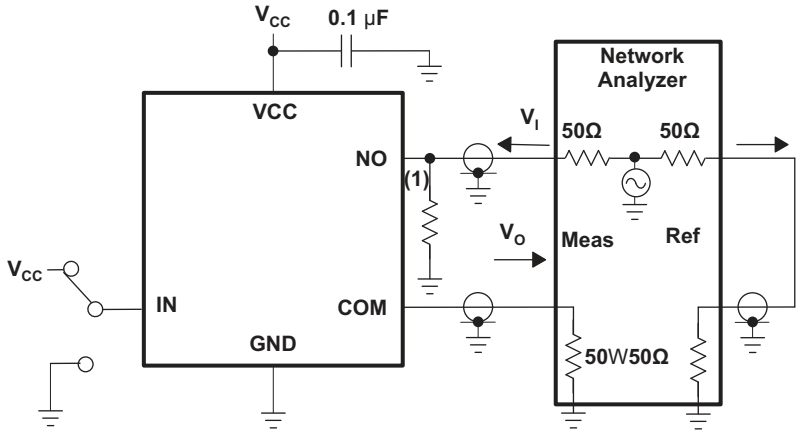


Figure 2. NO and COM Capacitance



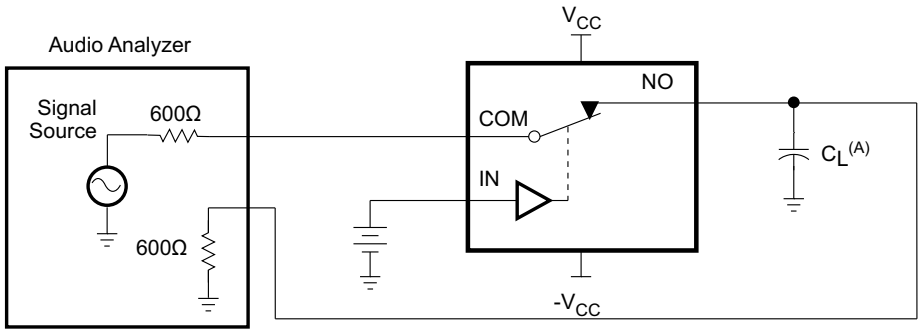
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. Bandwidth is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

OFF isolation = 20 log V_O/V_I

(1) Add 50-Ω termination for OFF isolation

Figure 3. OFF Isolation, Bandwidth, and Crosstalk

Channel ON: COM to NO	$V_I = V_{CC}$	C_L = 50 pF
$V_{SOURCE} = V_{CC}$ P-P	f_{SOURCE} = 20 Hz to 20 kHz	R_L = 600Ω



A. C_L includes probe and jig capacitance.

Figure 4. Total Harmonic Distortion (THD)

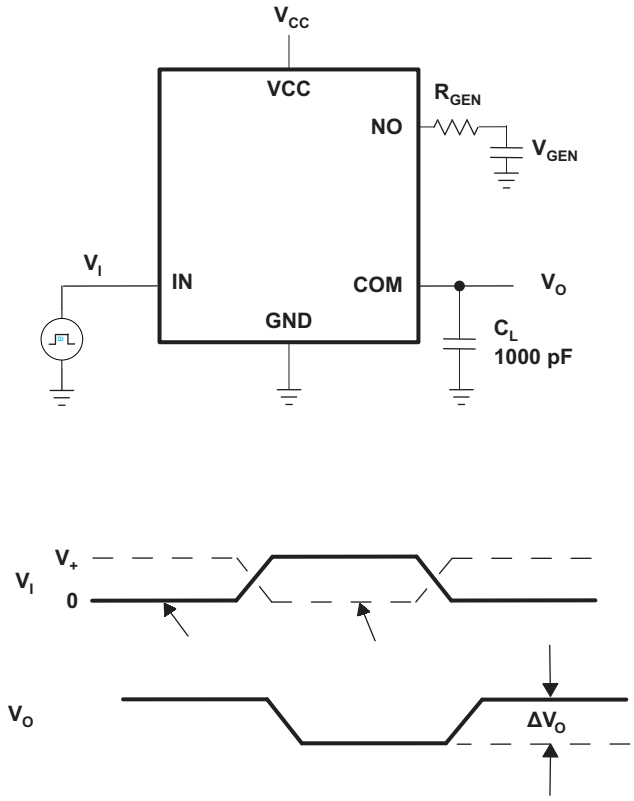


Figure 5. Charge Injection (Q_C)

6.7 Typical Characteristics

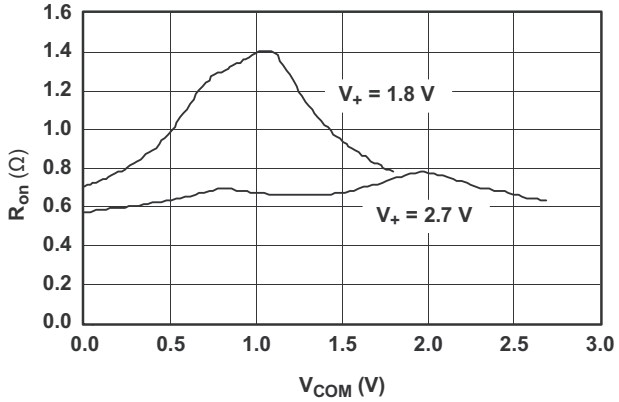


Figure 6. R_{on} vs V_{COM}

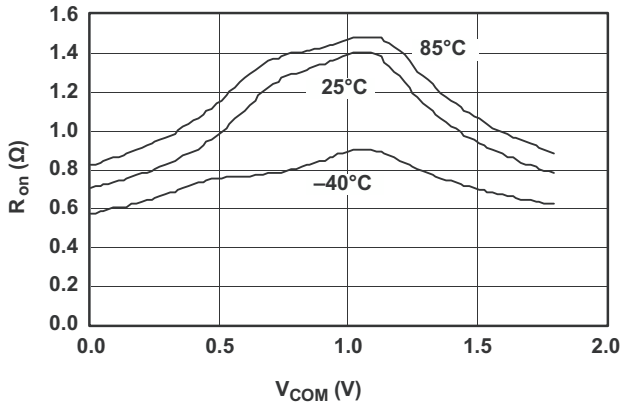


Figure 7. R_{on} vs V_{COM} (V_{CC} = 1.8 V)

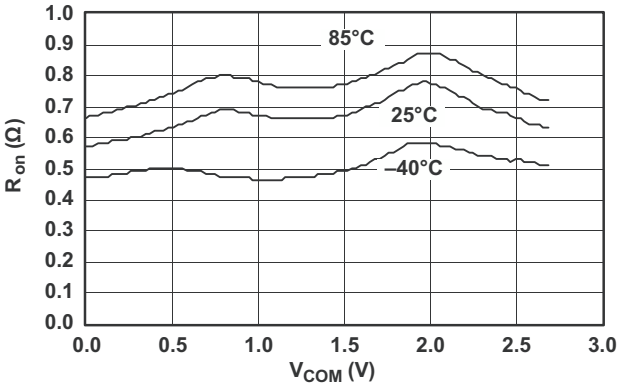


Figure 8. R_{on} vs V_{COM} (V_{CC} = 2.7 V)

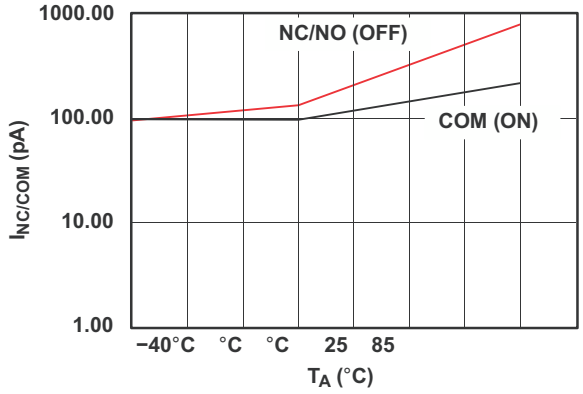


Figure 9. I_{ON} and I_{OFF} vs Temperature (V_{CC} = 3.6 V)

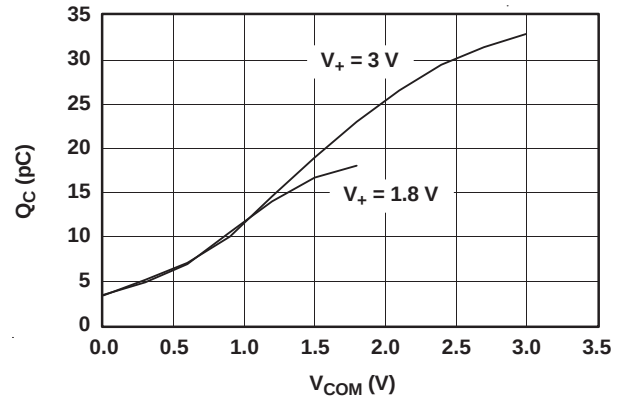


Figure 10. Q_C vs V_{COM}

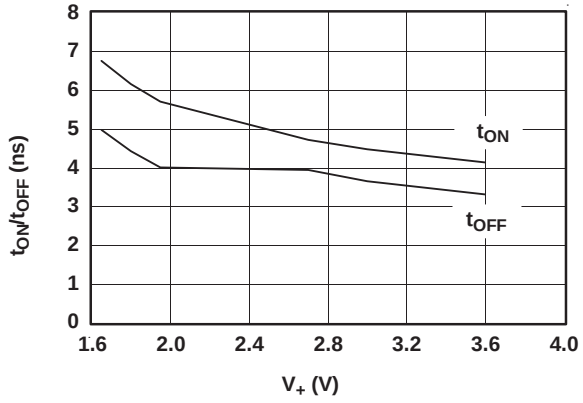


Figure 11. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

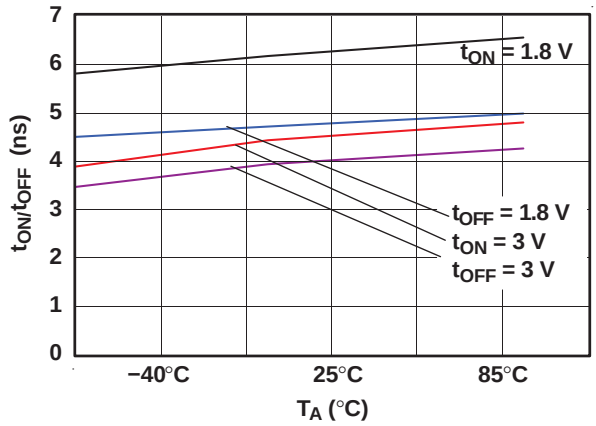


Figure 12. t_{ON} and t_{OFF} vs Temperature

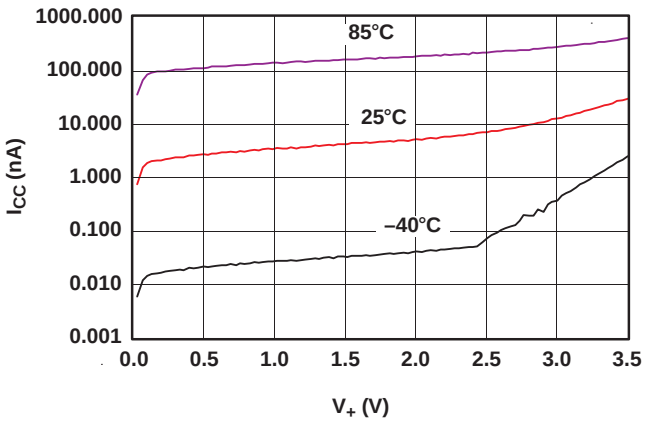


Figure 13. I_{CC} vs V_{CC}

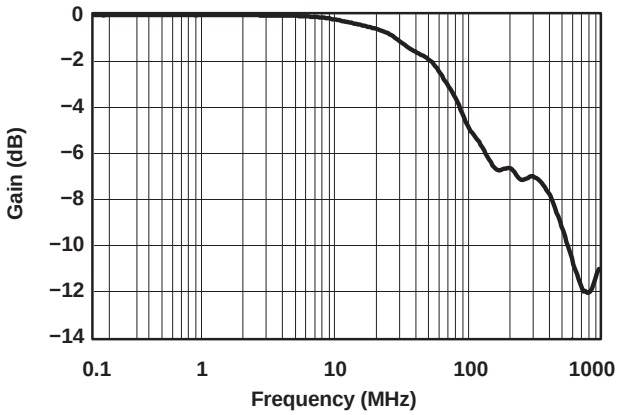


Figure 14. Gain vs Frequency (V_{CC} = 3 V)

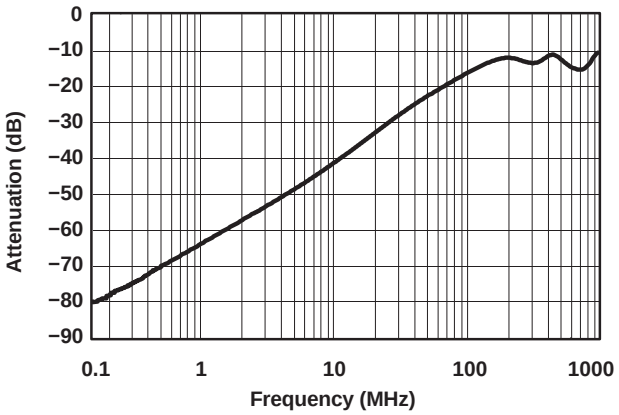


Figure 15. OFF Isolation vs Frequency (V_{CC} = 3 V)

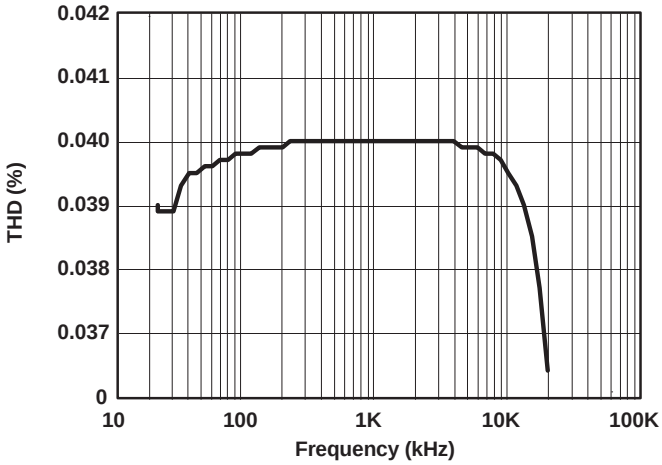


Figure 16. Total Harmonic Distortion vs Frequency (R_L = 32 Ω)

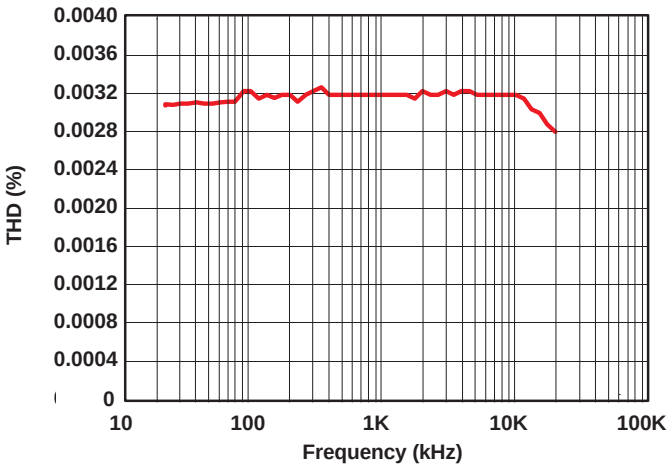


Figure 17. Total Harmonic Distortion vs Frequency (R_L = 600 Ω)

Typical Characteristics (continued)

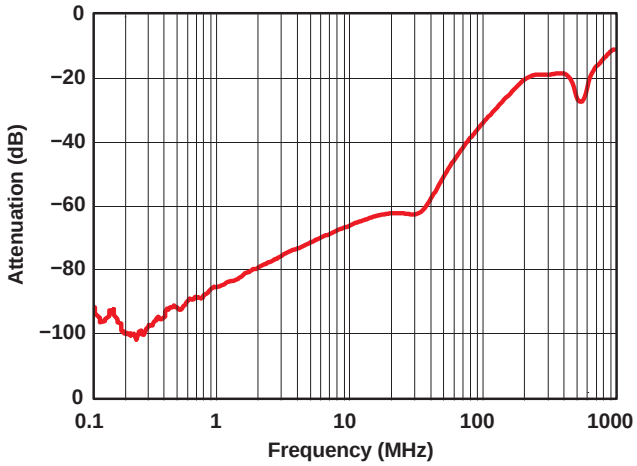


Figure 18. Crosstalk vs Frequency (V_{CC} = 3 V)

7 Detailed Description

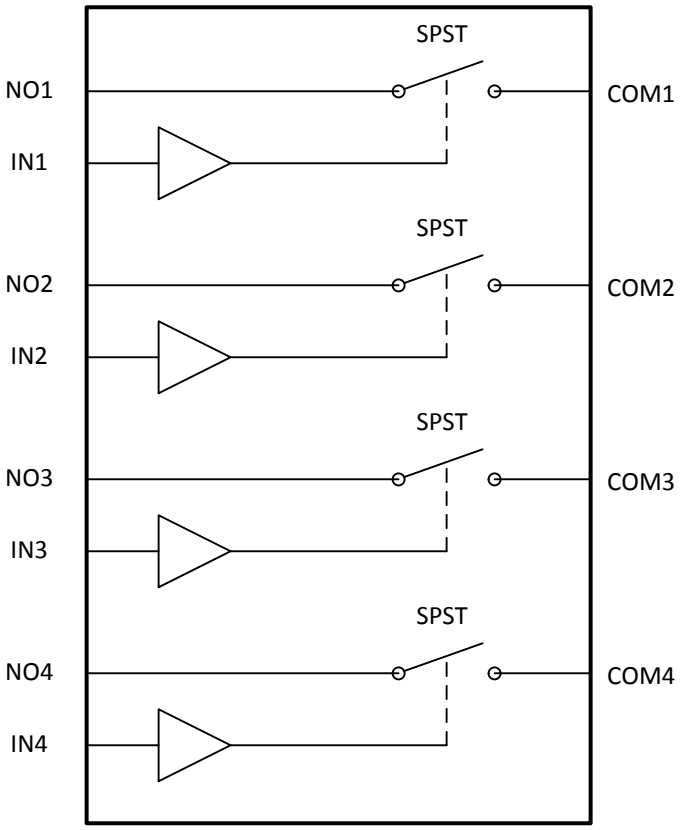
7.1 Overview

The TS3A4751 is a bidirectional, 4-channel, normally open (NO) single-pole single-throw (SPST) analog switch that operates from a single 1.6-V to 3.6-V supply. This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V CMOS compatible when using a 3-V supply.

The TS3A4751 has four normally open (NO) switches. The TS3A4751 is available in a 14-pin thin shrink small-outline package (TSSOP) and in space-saving 14-pin VQFN (RGY) and micro X2QFN (RUC) packages.

7.2 Functional Block Diagram



7.3 Feature Description

This device has fast switching speeds, handles rail-to-rail analog signals, and consumes very low quiescent power.

The digital input is 1.8-V TTL/CMOS compatible when using a 3-V supply.

7.4 Device Functional Modes

Table 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Logic Inputs

The TS3A4751 logic inputs can be driven up to 3.6 V, regardless of the supply voltage. For example, with a 1.8-V supply, IN may be driven low to GND and high to 3.6 V. Driving IN rail to rail minimizes power consumption.

8.1.2 Analog Signal Levels

Analog signals that range over the entire supply voltage (V_{CC} to GND) can be passed with very little change in R_{on} (see *Typical Characteristics*). The switches are bidirectional, so NO and COM can be used as either inputs or outputs.

8.2 Typical Application

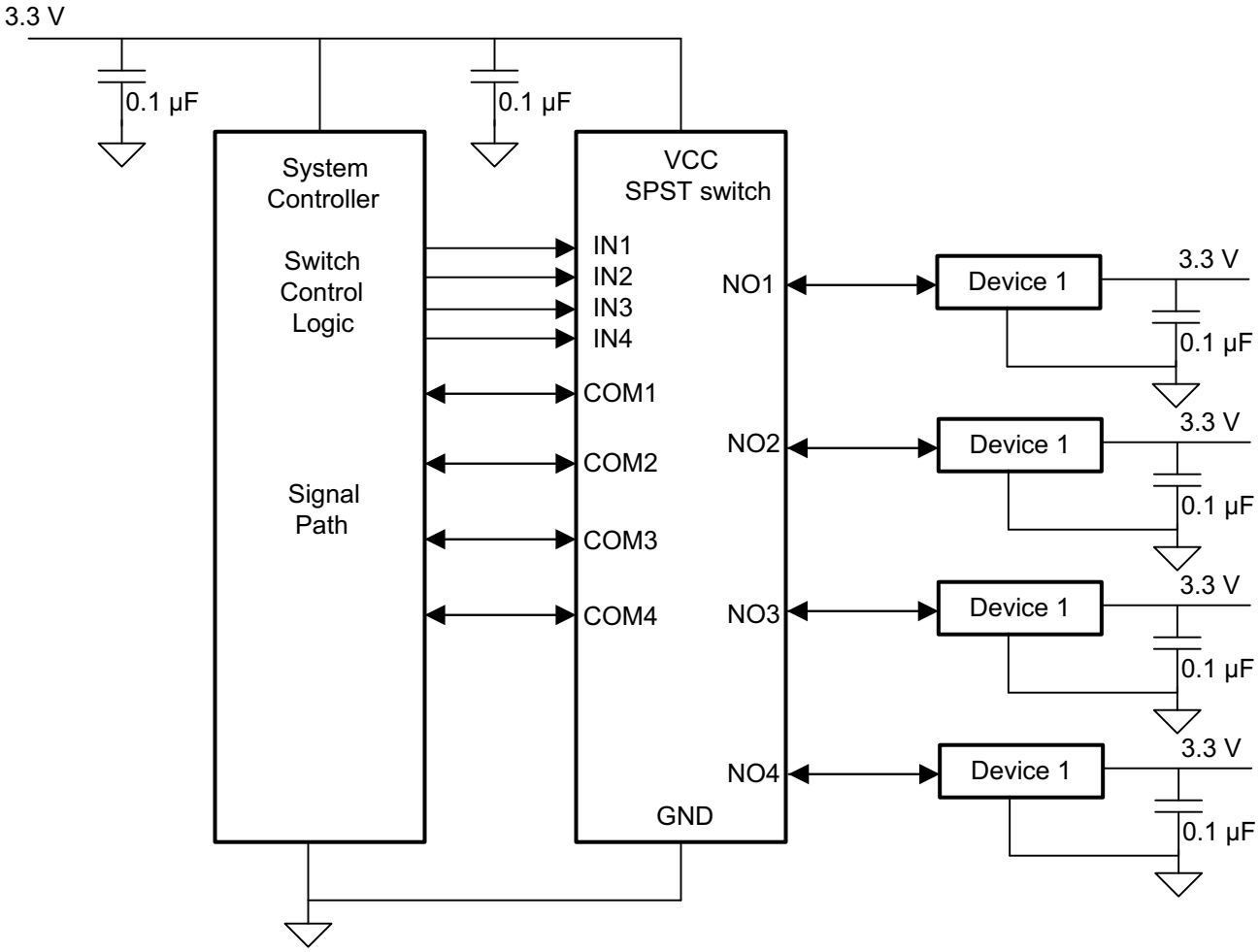


Figure 19. Typical Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

Ensure that all of the signals passing through the switch are with in the specified ranges to ensure proper performance.

8.2.2 Detailed Design Procedure

The TS3A4751 and can be properly operated without any external components. However, it is recommended that unused pins should be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device. It is also recommneded that the digital control pins (INX) be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

8.2.3 Application Curve

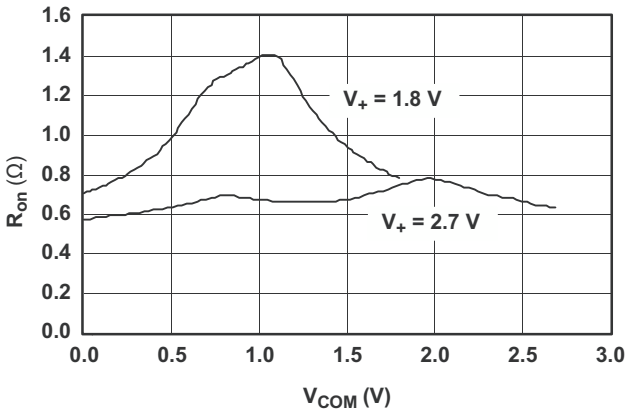


Figure 20. R_{on} vs V_{COM}

9 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V_{CC} on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-μF capacitor, connected from V_{CC} to GND, is adequate for most applications.

10 Layout

10.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance.

Reduce stray inductance and capacitance by keeping traces short and wide.

Ensure that bypass capacitors are as close to the device as possible.

Use large ground planes where possible.

10.2 Layout Example

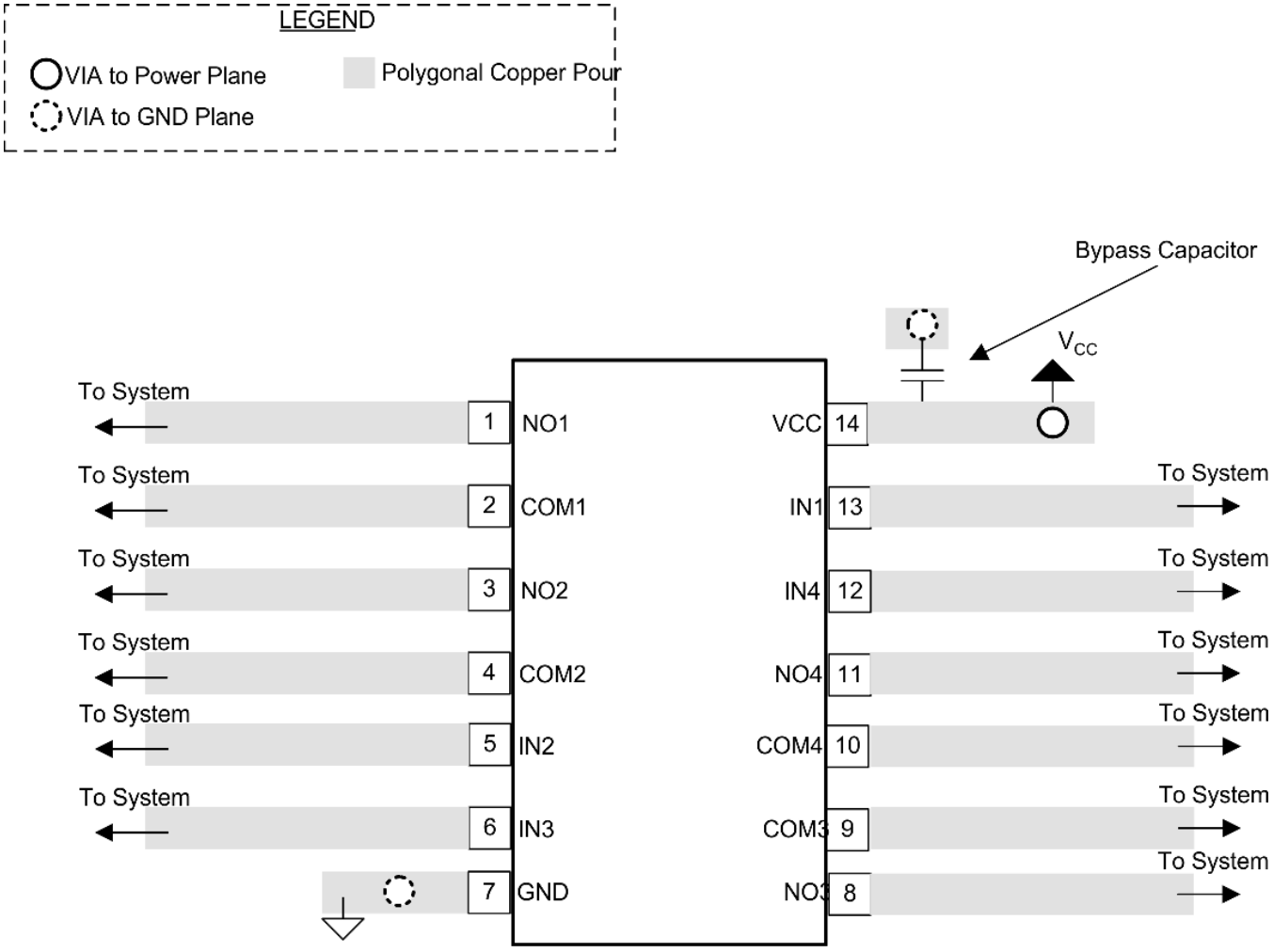


Figure 21. Layout Schematic

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A4751PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	YC751	Samples
TS3A4751RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	YC751	Samples
TS3A4751RUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3MO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

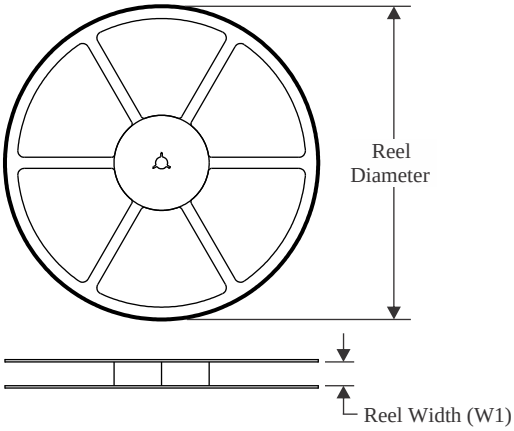
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

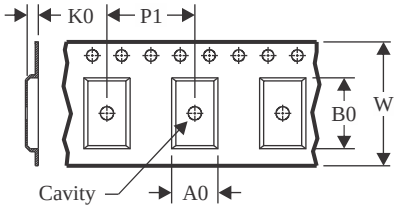
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

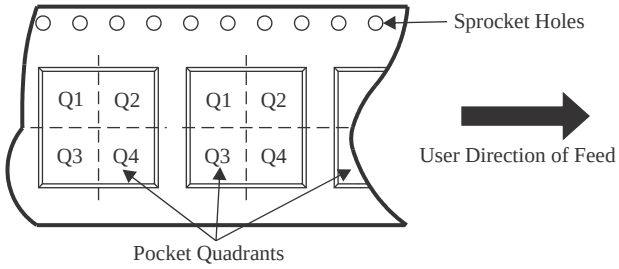


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

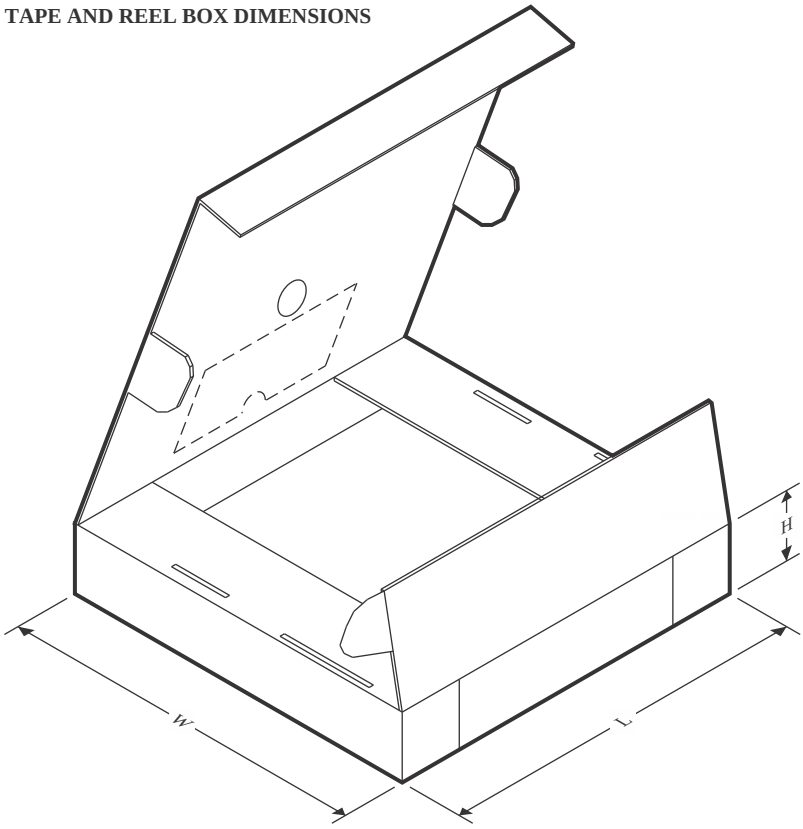
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A4751PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3A4751RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TS3A4751RUCR	QFN	RUC	14	3000	180.0	9.5	2.2	2.2	0.5	4.0	8.0	Q2
TS3A4751RUCR	QFN	RUC	14	3000	179.0	8.4	2.25	2.25	0.55	4.0	8.0	Q2

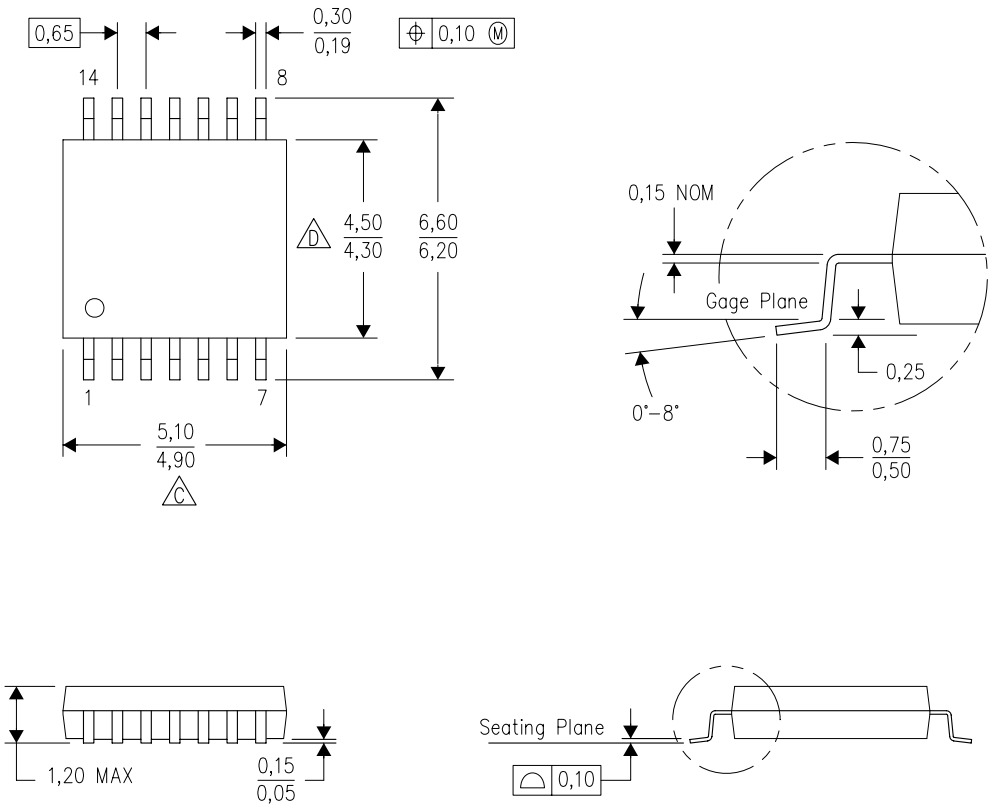
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A4751PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TS3A4751RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0
TS3A4751RUCR	QFN	RUC	14	3000	189.0	185.0	36.0
TS3A4751RUCR	QFN	RUC	14	3000	200.0	183.0	25.0

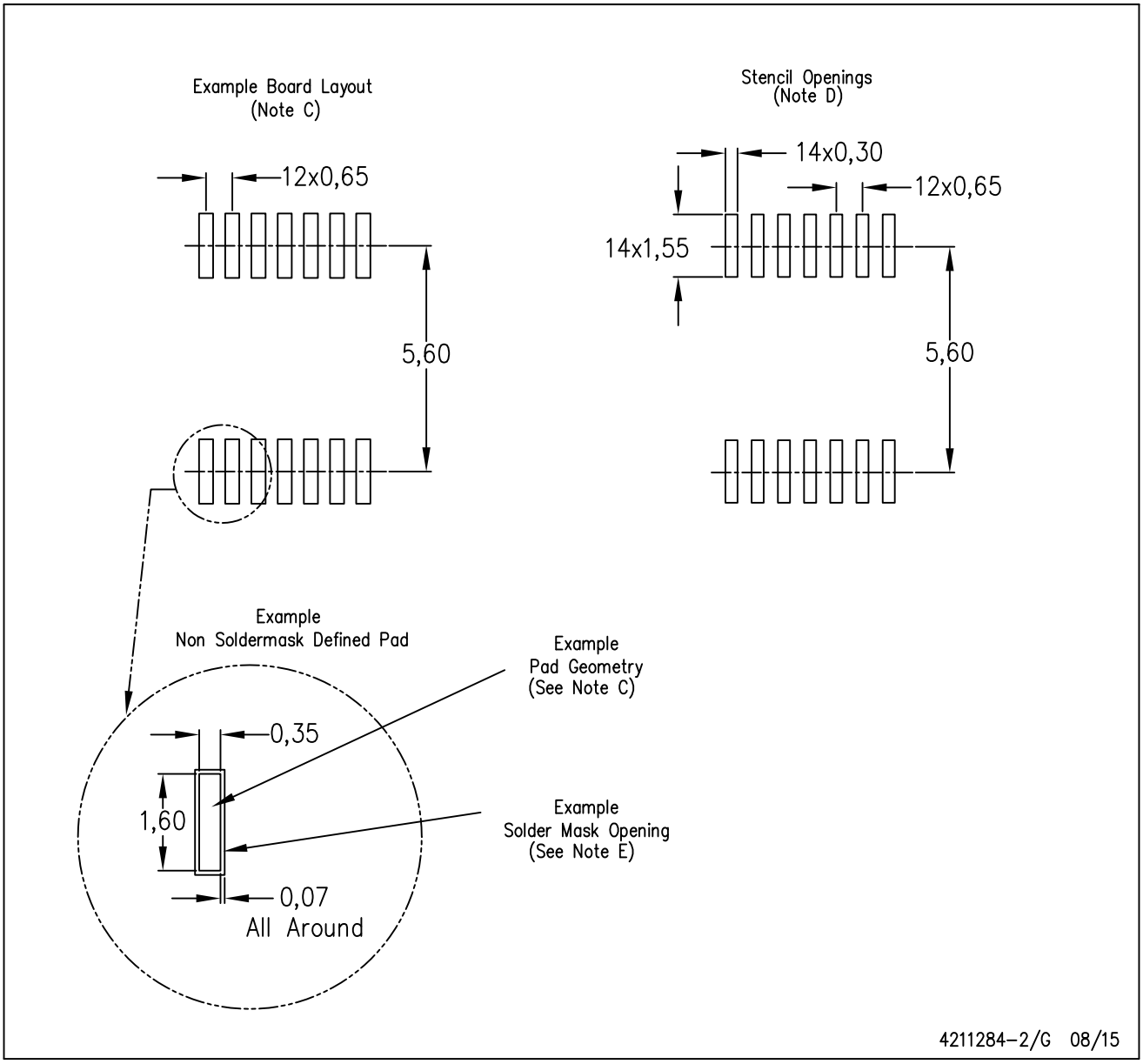
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



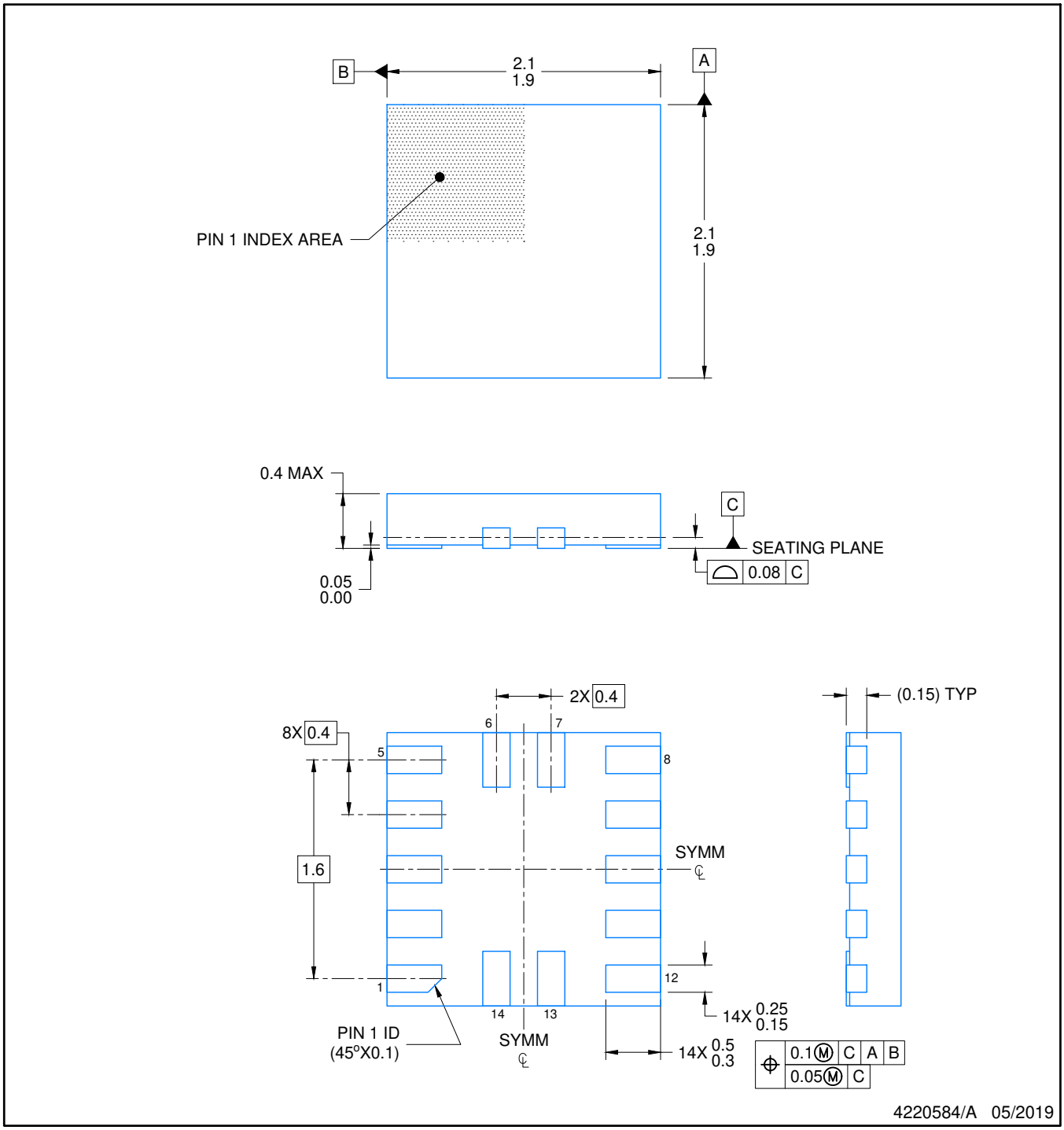
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

RUC0014A

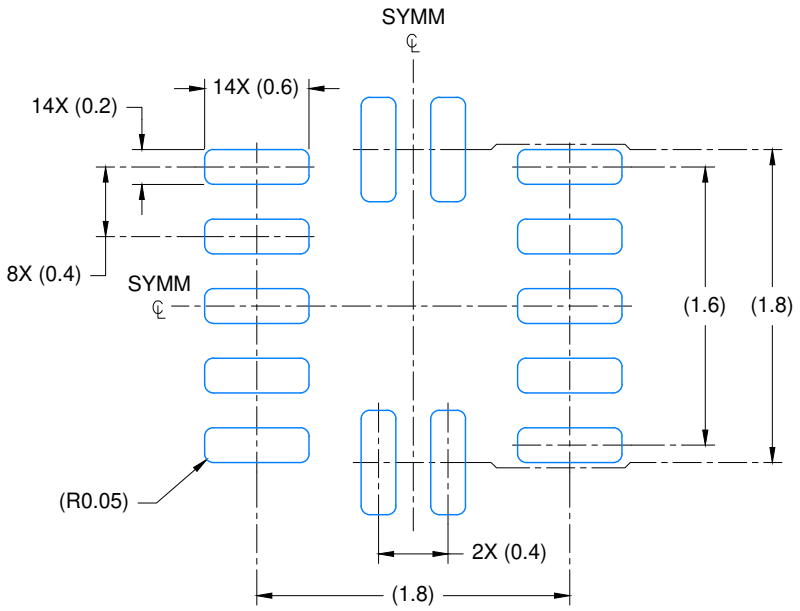
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

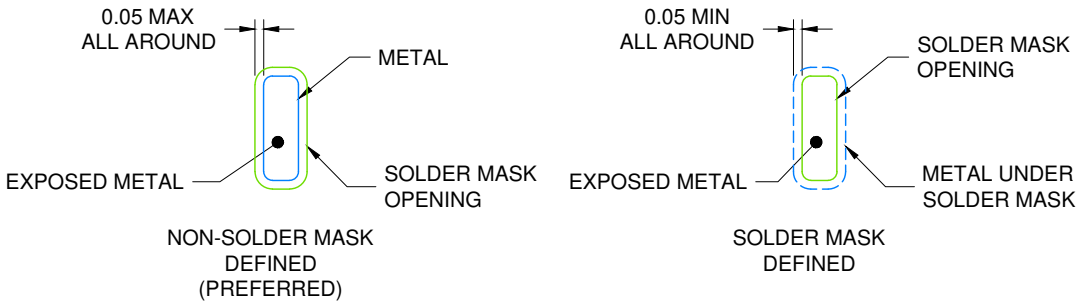


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

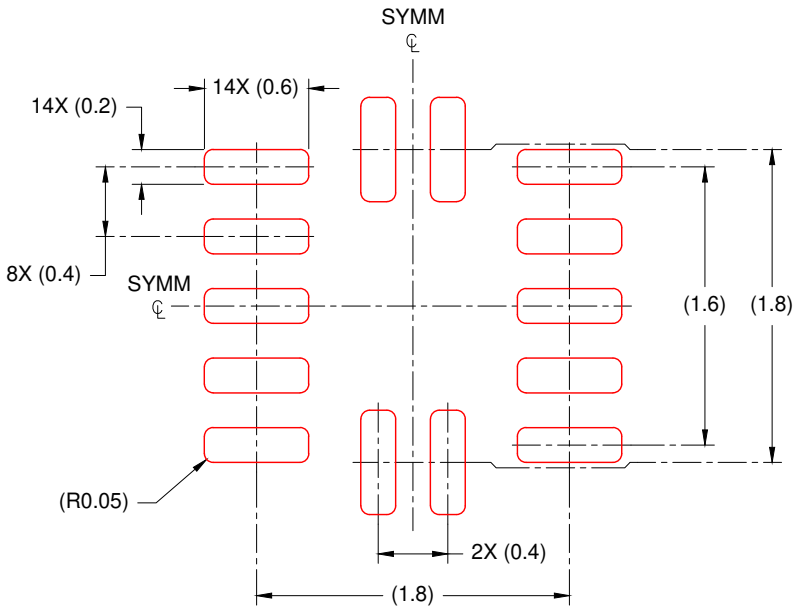


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



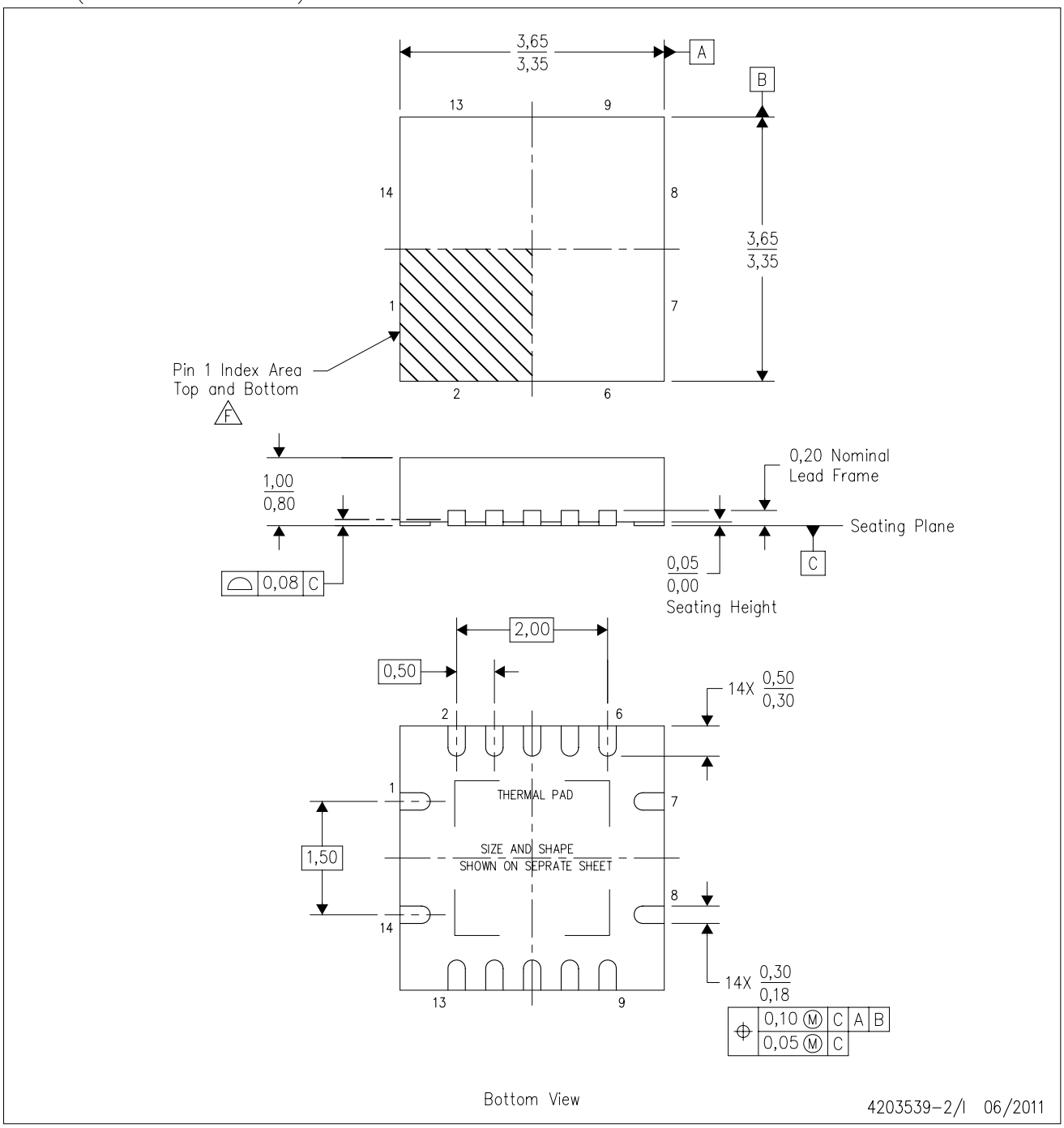
SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

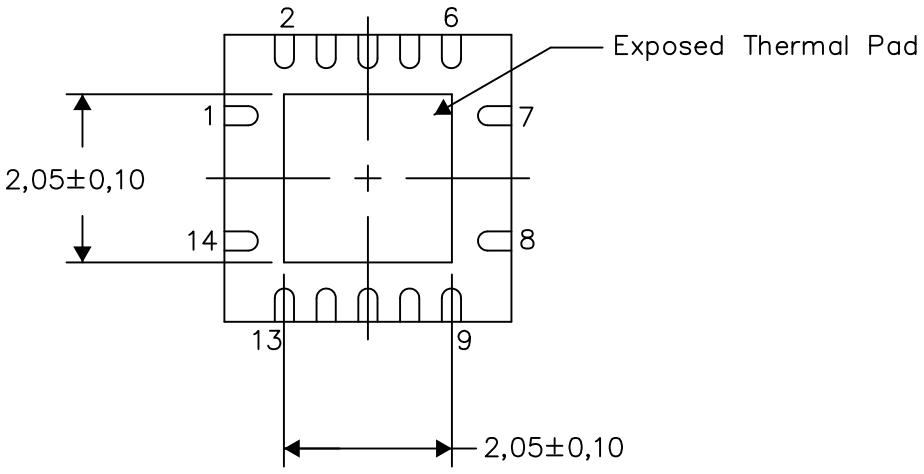
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



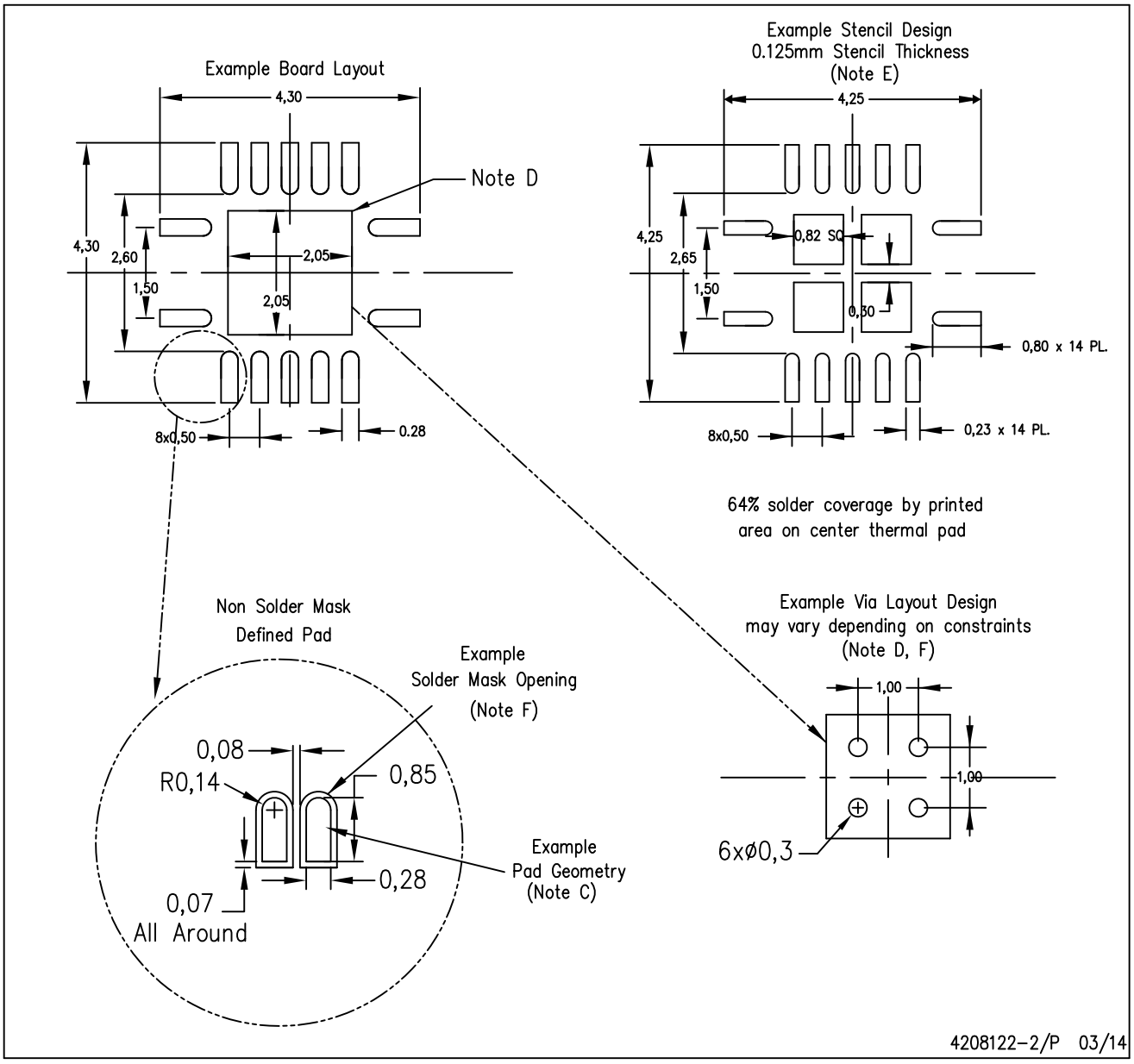
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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