

Description

The ICS502 LOCO™ is the most cost effective way to generate a high-quality, high-frequency clock output and a reference from a lower frequency crystal or clock input. The name LOCO stands for Low Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 160 MHz.

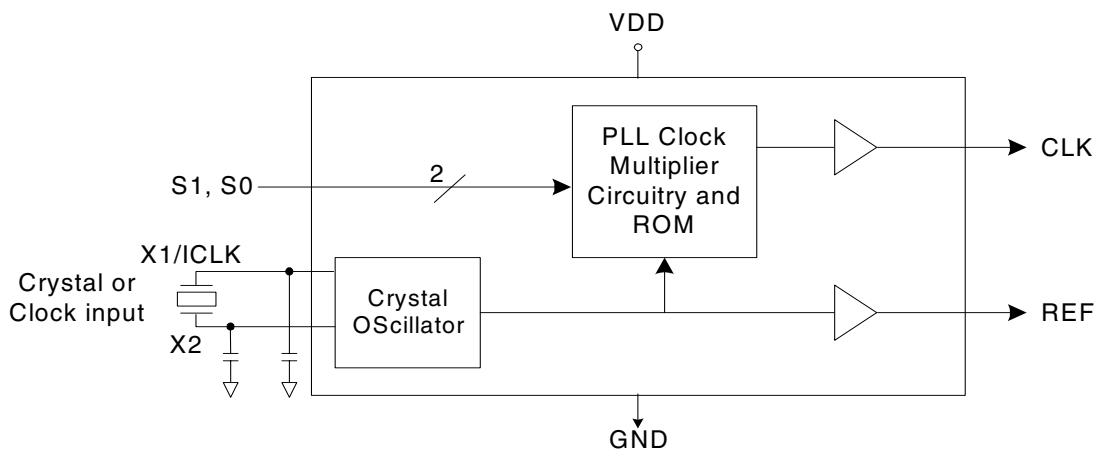
Stored in the chip's ROM is the ability to generate six different multiplication factors, allowing one chip to output many common frequencies (see table on page 2).

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined or guaranteed. For applications which require defined input to output skew, use the ICS570B.

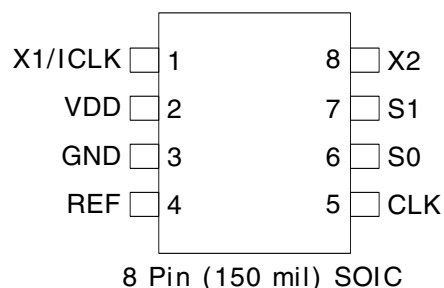
Features

- Packaged as 8-pin SOIC or die
- Pb (lead) free package
- IDT's lowest cost PLL clock
- Zero ppm multiplication error
- Easy to cascade with ICS5xx series
- Input crystal frequency of 5 – 27 MHz
- Input clock frequency of 2 – 50 MHz
- Output clock frequencies up to 190 MHz
- Low jitter – 50 ps one sigma
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 160 MHz
- Operating voltages of 3.0 to 5.5 V
- 25 mA drive capability at TTL levels
- Industrial temperature version available
- Advanced, low-power CMOS process

Block Diagram



Pin Assignment



Clock Decoding Table (MHz)

| S1 | S0 | CLK |
|----|----|-------|
| 0 | 0 | x2 |
| 0 | 1 | x5 |
| M | 0 | x3 |
| M | 1 | x3.33 |
| 1 | 0 | x4 |
| 1 | 1 | x2.5 |

Minimum input frequency for all selections is per table on page 3.

0 = connect directly to ground

1 = connect directly to VDD

M = leave unconnected (floating)

Common Output Frequency Examples (MHz)

| | | | | | | | | | | | |
|---------------------------|-----------|--------------|-----------|-----------|--------------|-------------|-----------|------------|------------|------------|------------|
| Output | 20 | 25 | 30 | 32 | 33.33 | 37.5 | 40 | 48 | 50 | 54 | 60 |
| Input | 10 | 10 | 10 | 16 | 10 | 15 | 20 | 16 | 20 | 13.5 | 20 |
| Selection (S1, S0) | 0, 0 | 1, 1 | M, 0 | 0, 0 | M, 1 | 1, 1 | 0, 0 | M, 0 | 1, 1 | 1, 0 | M, 0 |
| Output | 64 | 66.66 | 72 | 75 | 80 | 81 | 90 | 100 | 108 | 120 | 135 |
| Input | 16 | 20 | 24 | 15 | 20 | 27 | 27 | 20 | 27 | 24 | 27 |
| Selection (S1, S0) | 1, 0 | M, 1 | M, 0 | 0, 1 | 1, 0 | M, 0 | M, 1 | 0, 1 | 1, 0 | 0, 1 | 0, 1 |

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | XI/ICLK | Input | Crystal connection or clock input. |
| 2 | VDD | Power | Connect to +3.3 V or +5 V. |
| 3 | GND | Power | Connect to ground. |
| 4 | REF | Output | Buffered crystal oscillator output clock. |
| 5 | CLK | Output | Clock output per table above. |
| 6 | S0 | Input | Select 0 for output clock. Connect to GND or VDD. |
| 7 | S1 | Input | Select 1 for output clock. Connect to GND or VDD or float. |
| 8 | X2 | Input | Crystal connection. Leave unconnected for clock input. |

External Components

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS502 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01 μ F must be connected between VDD and GND. It must be connected close to the ICS502 to minimize lead inductance. No external power supply filtering is required for the ICS502.

Series Termination Resistor

A 33 Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal $(C_L - 12 \text{ pF}) \times 2$. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF $[(16 - 12) \times 2] = 8$.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS502. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (industrial) | -40 to +85° C |
| Ambient Operating Temperature (commercial) | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Soldering Temperature | 260° C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|------|------|------|-------|
| Ambient Operating Temperature (commercial) | 0 | – | +70 | °C |
| Ambient Operating Temperature (industrial) | -40 | – | +85 | °C |
| Power Supply Voltage (measured in respect to GND) | +3 | | +5.5 | V |

DC Electrical Characteristics

VDD=5.0 V ±5% , Ambient temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------|--------------------------|-----------|-------|-----------|-------|
| Operating Voltage | VDD | | 3 | | 5.5 | V |
| Input High Voltage, ICLK only | V _{IH} | ICLK (pin 1) | (VDD/2)+1 | | | V |
| Input Low Voltage, ICLK only | V _{IL} | ICLK (pin 1) | | | (VDD/2)-1 | V |
| Input High Voltage | V _{IH} | OE (pin 7) | 2 | | | V |
| Input Low Voltage | V _{IL} | OE (pin 7) | | | 0.8 | V |
| Input High Voltage | V _{IH} | S0, S1 | VDD-0.5 | | | V |
| Input Mid Voltage | V _{IM} | S1 | | VDD/2 | | V |
| Input Low Voltage | V _{IL} | S0, S1 | | | 0.5 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.4 | V |
| IDD Operating Supply Current, 20 MHz crystal | | No load, 100 MHz | | 20 | | mA |
| Short Circuit Current | | CLK output | | ±70 | | mA |
| On-Chip Pull-up Resistor | | Pin 7 | | 270 | | kΩ |
| Input Capacitance, S1, S0, and OE | | Pins 4, 6, 7 | | 4 | | pF |

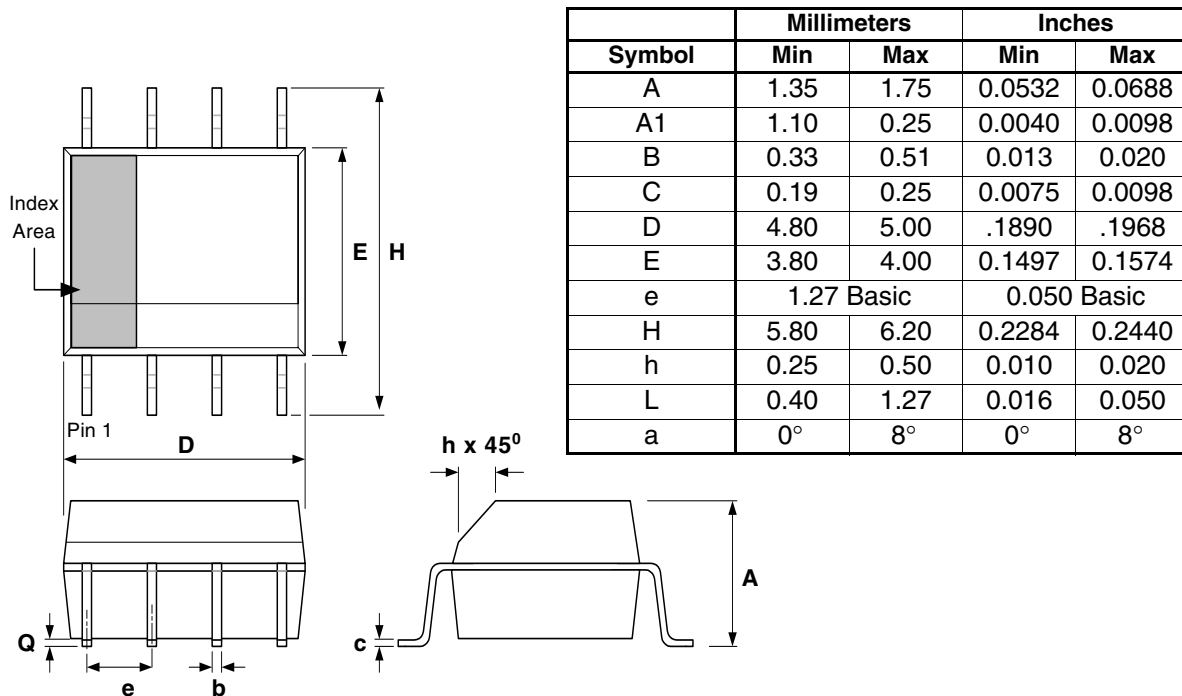
AC Electrical Characteristics

VDD = 5.0 V ±5%, Ambient Temperature -40 to +85° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|------------------|---------------------|------|-------|------|-------|
| Input Frequency, crystal input | F _{IN} | | 5 | | 27 | MHz |
| Input Frequency, clock input | F _{IN} | | 2 | | 50 | MHz |
| Output Frequency, VDD = 4.5 to 5.5V | F _{OUT} | 0 to +70° C | 14 | | 160 | MHz |
| Output Frequency, VDD = 3.0 to 3.6V | | -40 to +85° C | 14 | | 120 | MHz |
| Output Frequency, VDD = 4.5 to 5.5V | F _{OUT} | +25° C | 14 | | 190 | MHz |
| Output Frequency, VDD = 3.0 to 3.6V | | +25° C | 14 | | 140 | MHz |
| Output Clock Rise Time | t _{OR} | 0.8 to 2.0 V | | 1 | | ns |
| Output Clock Fall Time | t _{OF} | 2.0 to 8.0V | | 1 | | ns |
| Output Clock Duty Cycle | t _{OD} | 1.5V, up to 160 MHz | 45 | 49-51 | 55 | % |
| PLL Bandwidth | | | 10 | | | kHz |
| Output Enable Time, OE high to output on | | | | 50 | | ns |
| Output Disable Time, OE low to tri-state | | | | 50 | | ns |
| Absolute Clock Period Jitter | t _{ja} | Deviation from mean | | ±70 | | ps |
| One Sigma Clock Period Jitter | t _{js} | | | 25 | | ps |

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------|-----------------------------|------------|---------------|
| 502MLF | 502MLF | Tubes | 8-pin SOIC | 0 to +70° C |
| 502MLFT | 502MLF | Tape and Reel | 8-pin SOIC | 0 to +70° C |
| 502MILF | 502MILF | Tubes | 8-pin SOIC | -40 to +85° C |
| 502MILFT | 502MILF | Tape and Reel | 8-pin SOIC | -40 to +85° C |
| 502-DWF | - | Die on uncut, probed wafers | | 0 to +70° C |
| 502-DPK | - | Tested die in waffle pack | | 0 to +70° C |

Parts that are ordered with an “LF” suffix to the part number are the Pb-free configuration and are RoHS compliant.

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