



Le79114 VoiceEdge™ Control Processor II Ve790 Series

APPLICATIONS DESCRIPTION Cost effective voice solution for long or short loops The Le79114 VoiceEdge™ Control Processor II (VCP II) is a providing POTS and integrated test capabilities second generation platform that delivers enhanced call control. self-test and line test capabilities. This latest processor works Applications include: IVD, DLC, CO, Voice-enabled with Zarlink Ve790 devices using its SPI interface(s), PCM DSLAM, PBX/KTS, MSAP, MSAN port(s), and GPIO. The Le79114 VCP II device provides the same integrated line-testing and feature-set as the Le79112 VCP device, plus additional capabilities such as 32 channels of **FEATURES** simultaneous DTMF detection and 64 channels of improved POTS control. Aggregated call control lowers demand on host micro-This product enables the design of a low-cost, highprocessor performance, fully software programmable line interface for 64 channels of call control multiple country applications. All AC, DC, signaling parameters Provides expanded line and circuit testing in and data are fully programmable. The integrated test capability conjunction with Zarlink's Ve790 Series chipsets is crucial for remote applications where dedicated test Provides 32 channels of simultaneous DTMF hardware is not cost-effective. Provides 4 channels of simultaneous line testing The Le79114 device is provided with extensive software and ■ Software interface using VoicePath[™] API-II support, through the LineCare[™] software suite, enabling the designer to develop a fully programmable solution in the least Software downloadable, field upgradeable, expandable amount of time. Serial and parallel host controller interface options Complete control of up to 16 Quad ISLAC devices RELATED LITERATURE Two master SPI ports 081130 Le79232 SLIC Device Data Sheet — 32 General Purpose I/Os 081185 Le79252 SLIC Device Data Sheet 16 configured as chip selects ■ 081256 Le79228 Quad ISLAC[™] Device Data Sheet 16 configured for interrupts ■ 081190 Le792288 Octal ISLACTM Device Data Sheet Two slave PCM highway ports — Single or dual PCM highways capable of operating 081507 MPI and PCM Signal Integrity Application Note up to 16.384 MHz ■ 081572 Le79114-SW VCP Software Package Data Sheet Separate test highway option ■ VoicePath[™] API II Reference Guide Internal PLL and hardware network timing recovery for creating analog sampling clocks ■ 3.3 V compliant I/O; Internal 3.3 V to 1.8 V linear **BLOCK DIAGRAM** regulator for the core logic

ORDERING INFORMATION

Device	Package (Green) ¹	Packing ²
Le79114KVC	128-pin TQFP	Tray

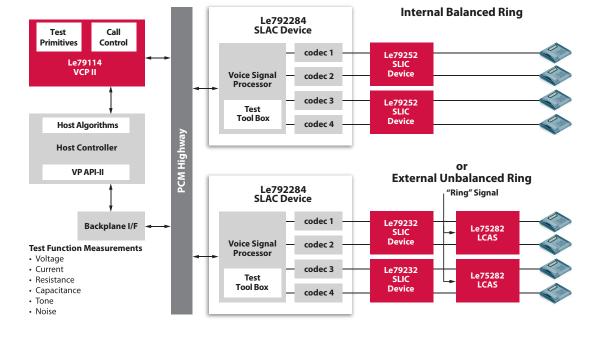
1. The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.

2. For delivery using a tape and reel packing system, add a "T" suffix to the OPN (Ordering Part Number) when placing an order.

PCM High Master PCM PLL PCM b or Secondary Slave Clock Generator BST Slave PCM A/B Interrupt Controller INT DSP Con and Memory SPI1 To SLAC To Host нві SPI/GPI Host Bus źı SPI2 CONF or Zarlink ebug use only JTAG UART GPIO Linear 1.8V Regulator VDD18CTRL

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Please see the LineCare™ Line-Test with Le79114 VCP II Product Preview for more information on Zarlink's line testing solutions.

*Contact your Zarlink Sales Representative to obtain the data sheet.

Packaging and Availability

See Ordering Information on first page.

For More Information:

To find the Zarlink Sales Office nearest you or for technical support, visit our website at: www.zarlink.com