

TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type

## SSM3K15CT

High-Speed Switching Applications  
Analog Switch Applications

- Optimum for high-density mounting in small packages
- Low ON-resistance
  - :  $R_{on} = 4.0 \Omega$  (max) (@ $V_{GS} = 4 V$ )
  - :  $R_{on} = 7.0 \Omega$  (max) (@ $V_{GS} = 2.5 V$ )

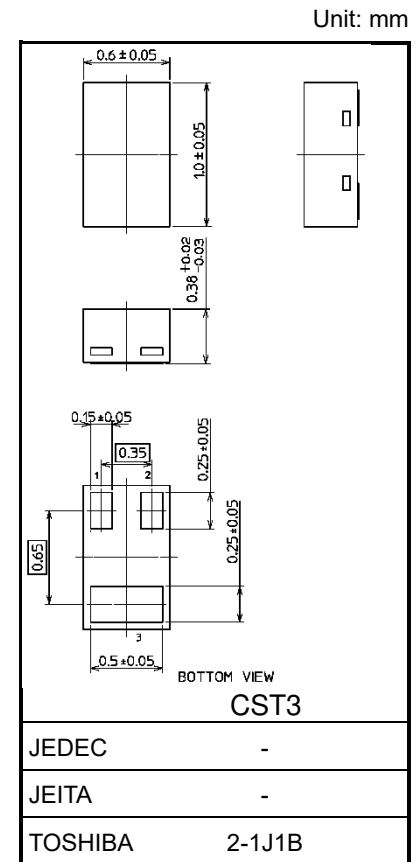
### Absolute Maximum Ratings ( $T_a = 25^\circ C$ )

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DS}$	30	V
Gate-source voltage		$V_{GS}$	$\pm 20$	V
Drain current	DC	$I_D$	100	mA
	Pulse	$I_{DP}$	200	
Drain power dissipation ( $T_a = 25^\circ C$ )		$P_D$ (Note 1)	100	mW
Channel temperature		$T_{ch}$	150	$^\circ C$
Storage temperature		$T_{stg}$	-55 to 150	$^\circ C$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

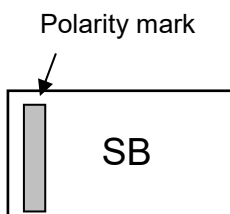
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board  
(10 mm × 10 mm × 1.0 t, Cu Pad: 100 mm<sup>2</sup>)

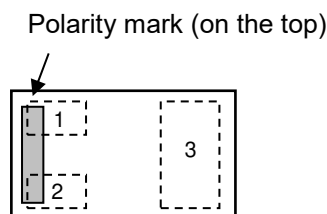


Weight: 0.75 mg (typ.)

### Marking (Top View)

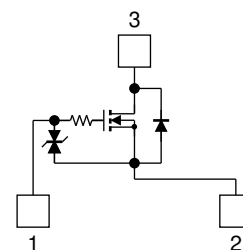


### Pin Condition (Top View)



1. Gate
  2. Source
  3. Drain
- \* Electrodes: On the bottom

### Equivalent Circuit



### Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, ensure that the environment is protected against electrostatic discharge. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

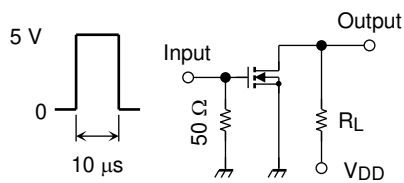
Start of commercial production  
2004-08

## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	IGSS	VGS = ±16 V, VDS = 0 V	—	—	±1	μA
Drain-source breakdown voltage	V (BR) DSS	ID = 0.1 mA, VGS = 0 V	30	—	—	V
Drain cut-off current	IDSS	VDS = 30 V, VGS = 0 V	—	—	1	μA
Gate threshold voltage	Vth	VDS = 3 V, ID = 0.1 mA	0.8	—	1.5	V
Forward transfer admittance	Yfs	VDS = 3 V, ID = 10 mA	25	—	—	mS
Drain-Source ON-resistance	RDS (ON)	ID = 10 mA, VGS = 4 V	—	2.2	4.0	Ω
		ID = 10 mA, VGS = 2.5 V	—	4.0	7.0	
Input capacitance	Ciss	VDS = 3 V, VGS = 0 V, f = 1 MHz	—	7.8	—	pF
Reverse transfer capacitance	Crss	VDS = 3 V, VGS = 0 V, f = 1 MHz	—	3.6	—	pF
Output capacitance	Coss	VDS = 3 V, VGS = 0 V, f = 1 MHz	—	8.8	—	pF
Switching time	Turn-on time	VDD = 5 V, ID = 10 mA, VGS = 0 to 5 V	—	50	—	ns
	Turn-off time		—	180	—	

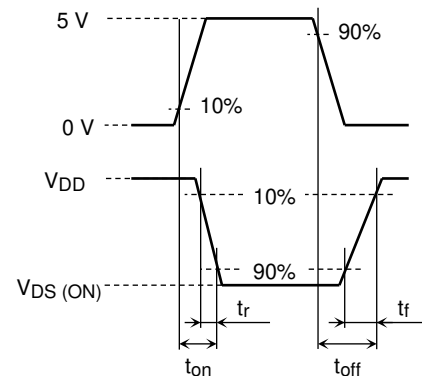
## Switching Time Test Circuit

### (a) Test circuit



$V_{DD} = 5\text{ V}$   
 Duty  $\leq 1\%$   
 Input:  $t_r, t_f < 5\text{ ns}$   
 $(Z_{out} = 50\ \Omega)$   
 Common Source  
 $T_a = 25^\circ\text{C}$

### (b) VIN



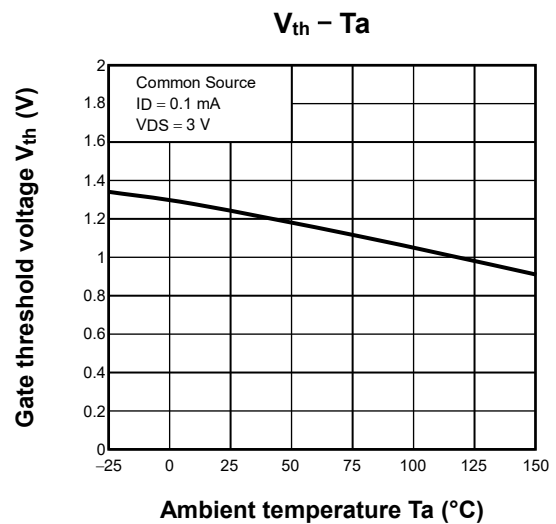
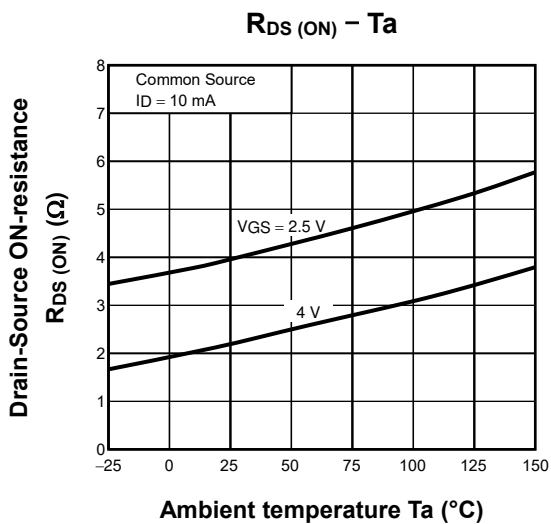
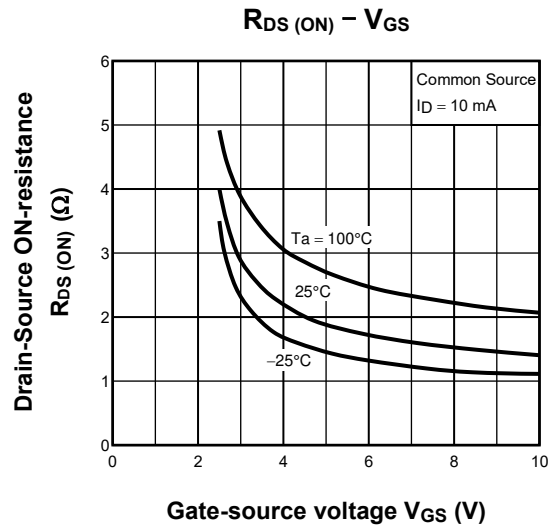
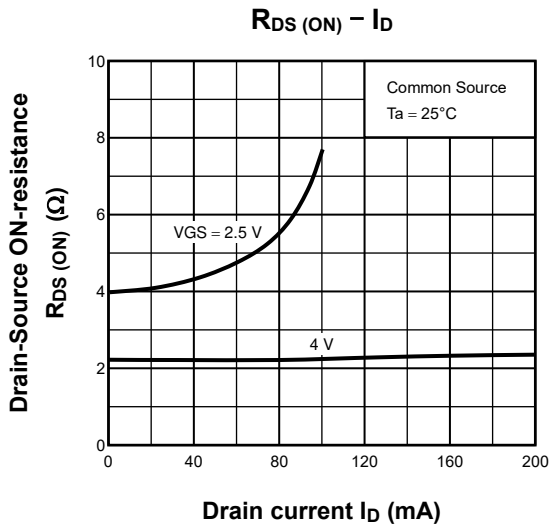
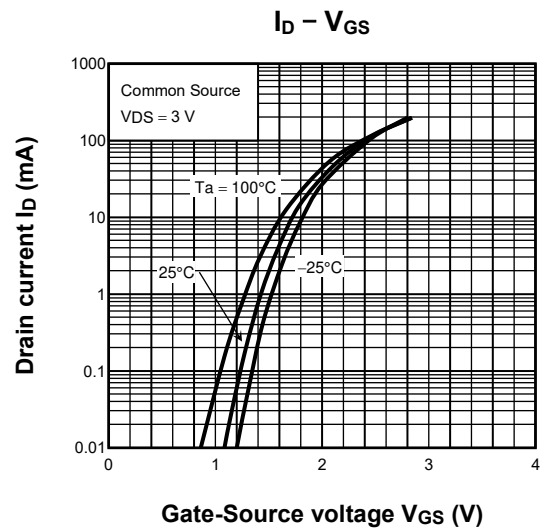
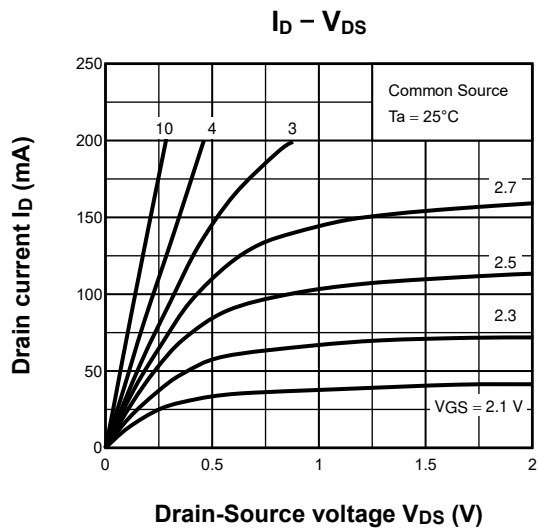
### (c) VOUT

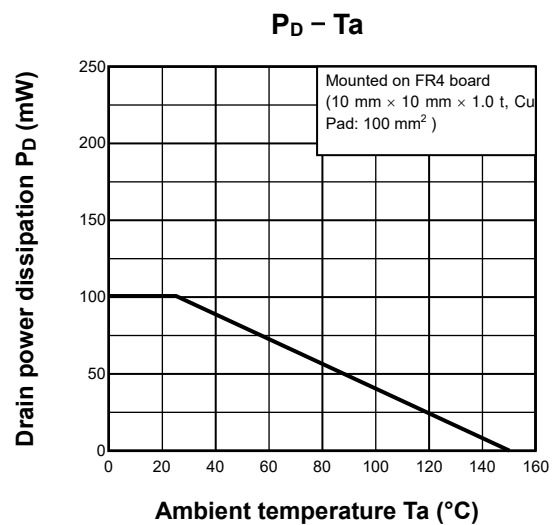
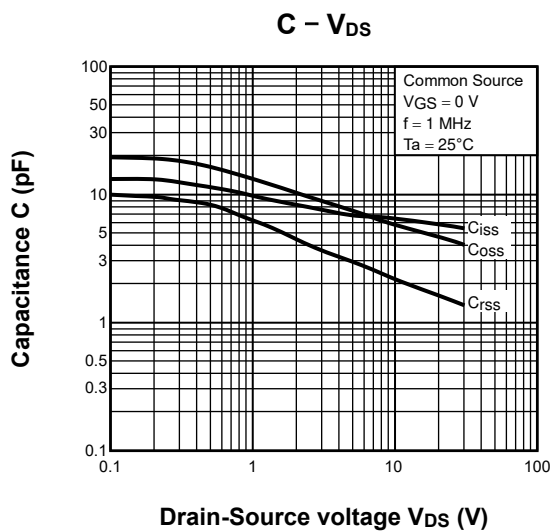
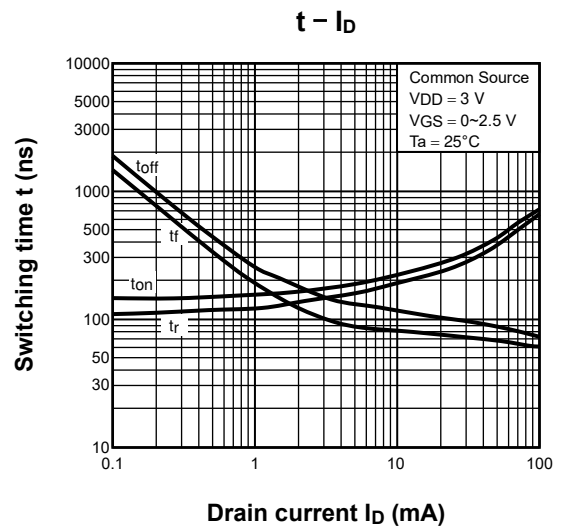
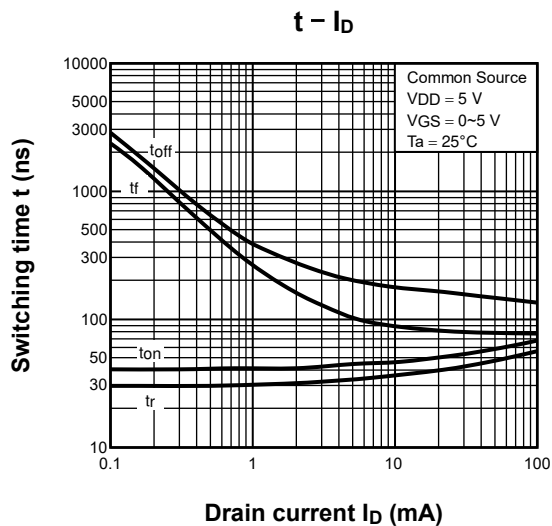
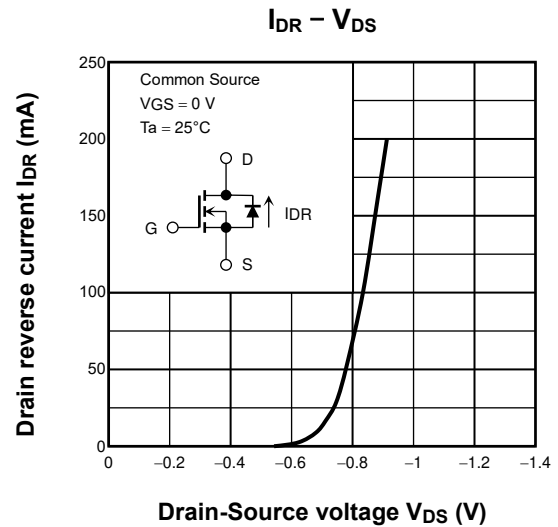
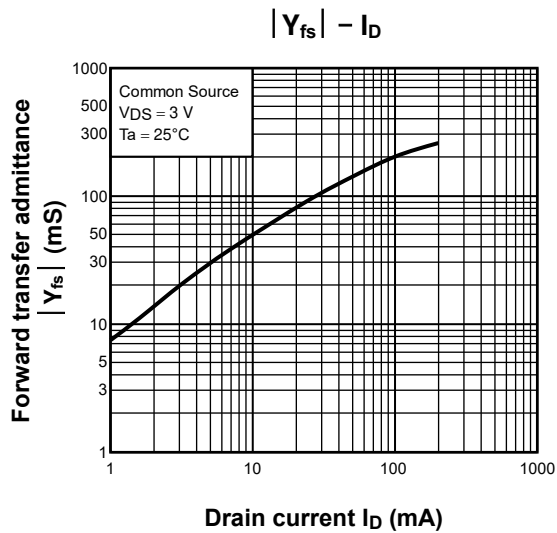
## Precaution

$V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D = 100\ \mu\text{A}$  for this product. For normal switching operation,  $V_{GS (on)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS (off)}$  requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS (off)} < V_{th} < V_{GS (on)}$ .)

Take this into consideration when using the device.

### Characteristics Curves (Note)





Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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