A5G26H110N

Airfast RF Power GaN Transistor

Rev. 2 — May 2023

Data Sheet: Technical Data

This 15 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2496 to 2690 MHz.

This part is characterized and performance is guaranteed for applications operating in the 2496 to 2690 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

2600 MHz

- Typical Doherty Single−Carrier W−CDMA Reference Circuit Performance: V_{DD} = 48 Vdc, I_{DQA} = 46 mA, V_{GSB} = –4.45 Vdc, P_{out} = 15 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2496 MHz	16.2	58.5	8.6	–29.2
2595 MHz	17.0	57.1	8.7	–33.4
2690 MHz	16.7	58.2	8.2	–34.6

1. All data measured in reference circuit with device soldered to printed circuit board.

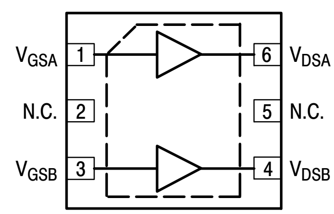
Features

- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

A5G26H110N

2496–2690 MHz, 15 W Avg., 48 V AIRFAST RF POWER GaN TRANSISTOR

DFN 7 × 6.5 PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

NXP reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	125	Vdc
Gate–Source Voltage	V_{GS}	–16, 0	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum Forward Gate Current, $I_{G\ (A+B)}$, @ T_C = 25°C	I_{GMAX}	13.3	mA
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–55 to +150	°C
Maximum Channel Temperature	T_{CH}	225	°C

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	48	Vdc

Table 3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case Case Temperature 115°C, P_D = 14.7 W	$R_{\theta JC}$ (IR)	1.8 (1)	°C/W
Thermal Resistance by Finite Element Analysis, Channel–to–Case Case Temperature 115°C, P_D = 14.7 W	$R_{\theta CHC}$ (FEA)	6.2 (2)	°C/W

Table 4. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS–001–2017)	1A
Charge Device Model (per JS–002–2014)	C3

Table 5. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	°C

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (3)					
Off–State Drain Leakage (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Carrier (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc) Peaking	$I_{D(BR)}$	— —	— —	2.1 3.9	mAdc
Off–State Gate Leakage (V_{DS} = 48 Vdc, V_{GS} = –8 Vdc) Carrier (V_{DS} = 48 Vdc, V_{GS} = –8 Vdc) Peaking	I_{GLK}	–1.0 –1.0	— —	— —	mAdc
On Characteristics — Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 4.6 mAdc)	$V_{GS(th)}$	–4.6	–3.0	–1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 35 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	–3.0	–2.5	–2.0	Vdc
Gate–Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	I_{GSS}	–2.1	—	—	mAdc
On Characteristics — Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 8.7 mAdc)	$V_{GS(th)}$	–4.6	–3.0	–1.9	Vdc
Gate–Source Leakage Current (V_{DS} = 150 Vdc, V_{GS} = –8 Vdc)	I_{GSS}	–3.9	—	—	mAdc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where *T* is the channel temperature in degrees Celsius, *A* = –11.6 and *B* = 9129.
3. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Doherty Production Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 35 mA, V_{GSB} = (V_t – 2.2) Vdc, P_{out} = 15 W Avg., f = 2600 MHz, 1–tone CW.					
Power Gain	G_{ps}	15.0	17.7	21.0	dB
Drain Efficiency	η_D	45.5	51.7	—	%
P_{out} @ 6 dB Compression Point	P6dB	45.5	47.9	—	dBm
Wideband Ruggedness (2) (In NXP Doherty Reference Circuit, 50 ohm system) I_{DQA} = 50 mA, V_{GSB} = –4.30 Vdc, f = 2595 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 15 W Avg. Modulated Output Power (3 dB Input Overdrive from 15 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance (2) (In NXP Doherty Reference Circuit, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 46 mA, V_{GSB} = –4.45 Vdc, 2496–2690 MHz Bandwidth					
Fast CW, 27 ms Sweep					
P_{out} @ 6 dB Compression Point	P6dB	—	112	—	W
AM/PM (Maximum value measured at the P6dB compression point across the 2496–2690 MHz bandwidth)	Φ	—	–11	—	°
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.025	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP6dB	—	0.008	—	dB/°C
Single–Carrier W–CDMA, Unclipped					
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 15 W Avg.	G_F	—	0.8	—	dB
2–Tone CW					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	200	—	MHz

Table 7. Ordering Information

Device	Tape and Reel Information	Package
A5G26H110NT4	T4 Suffix = 2,500 Units, 16 mm Tape Width, 13–inch Reel	DFN 7 × 6.5

1. Part internally input matched.
2. All data measured in reference circuit with device soldered to printed circuit board.

Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

Bias ON the device

1. Set gate voltage V_{GSA} and V_{GSB} to –5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

Bias OFF the device

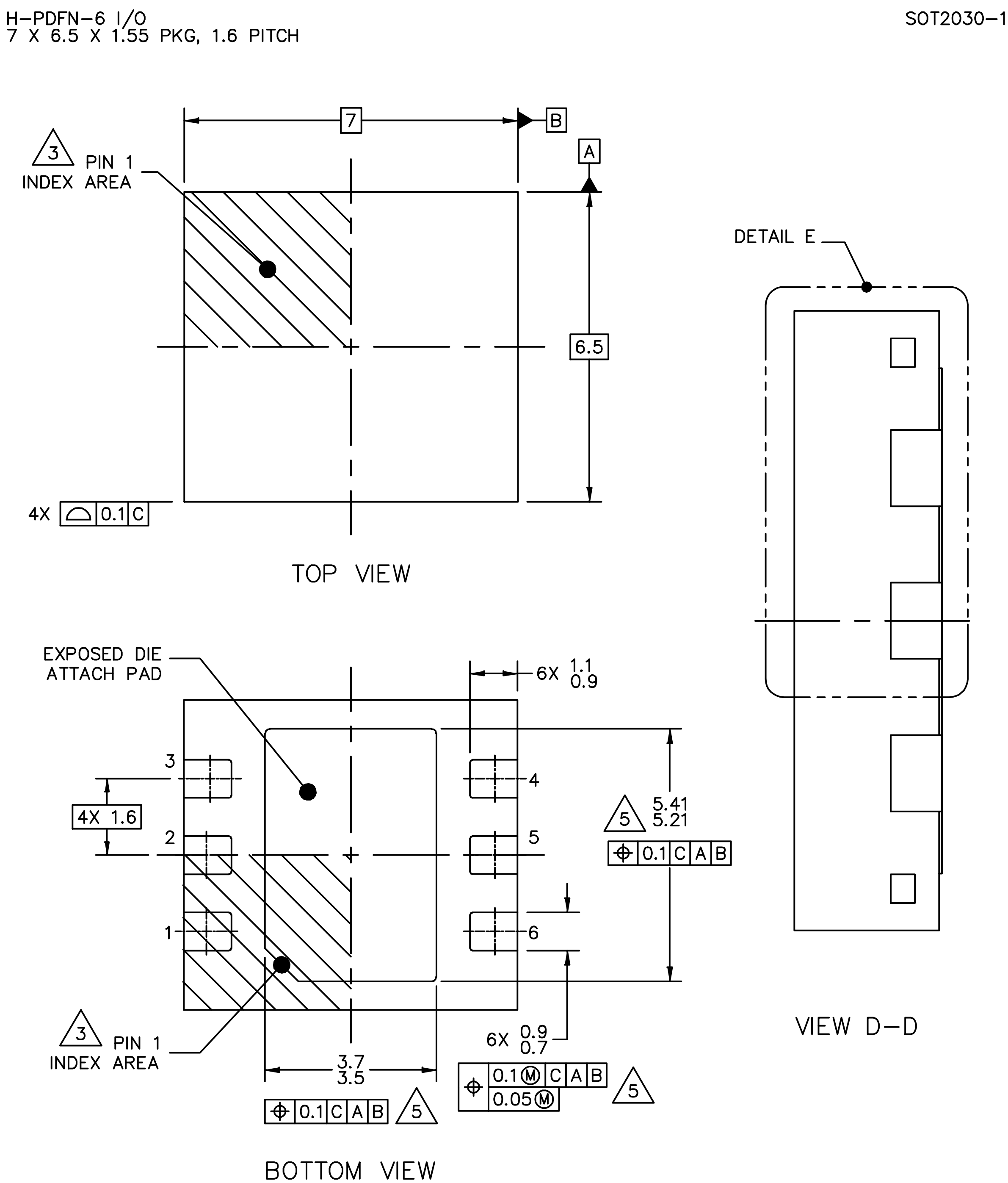
1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to –5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB}.

Figure 2. Product Marking

Table 8. Product Marking Trace Code

Identifier	Description
A	Assembly location
WL	Wafer lot indicator
YYWW	Date code
Z	Assembly lot

Package Information

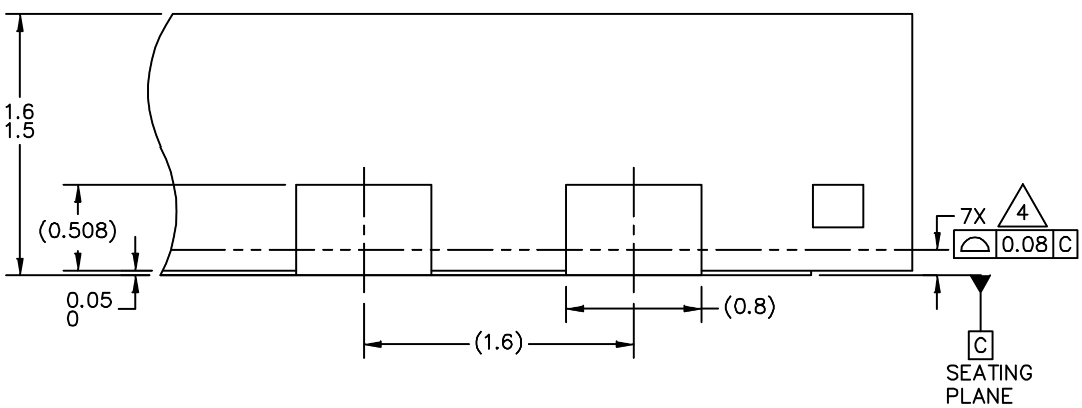


DATE: 02 APR 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD:	DRAWING NUMBER:	REVISION:	PAGE:
	NON JEDEC	98ASA01485D	A	1 OF 6

H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1



DETAIL E
VIEW ROTATED 90°CW

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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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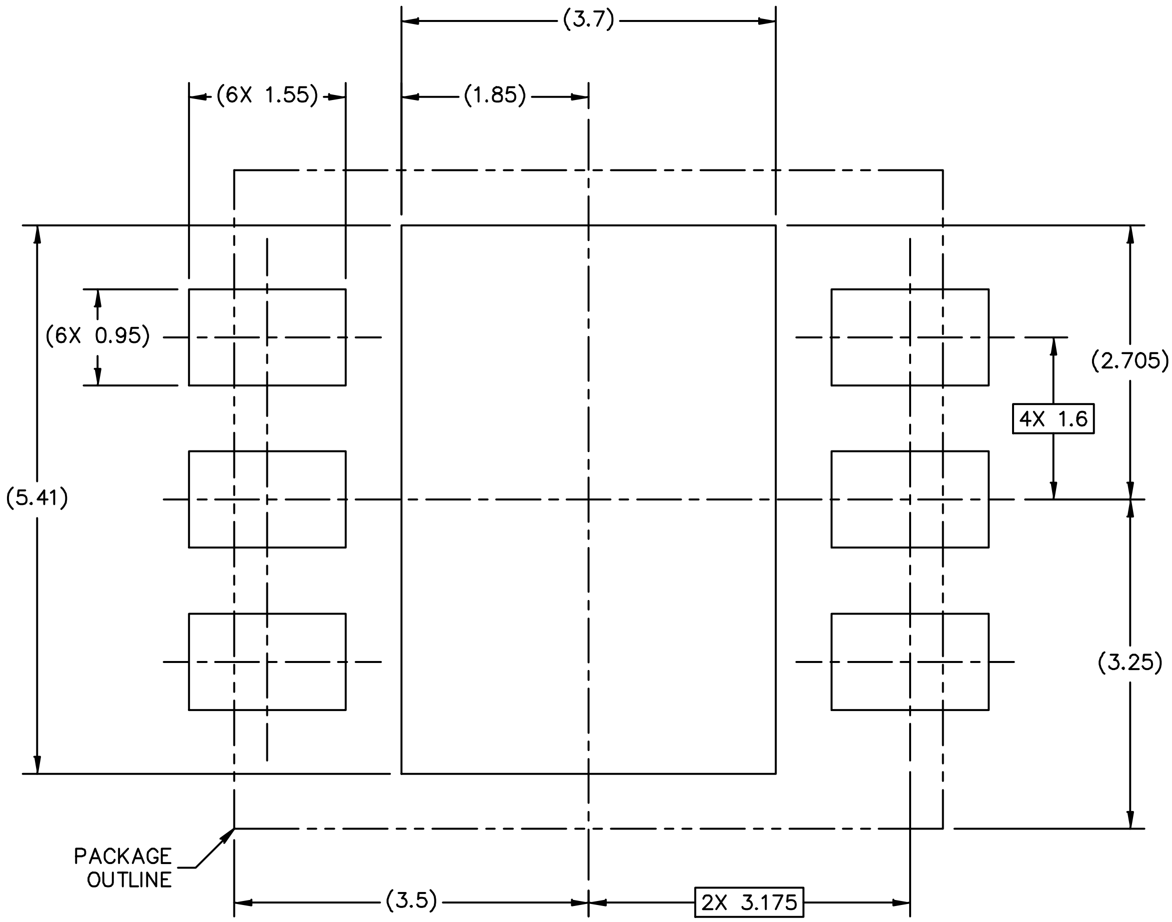

PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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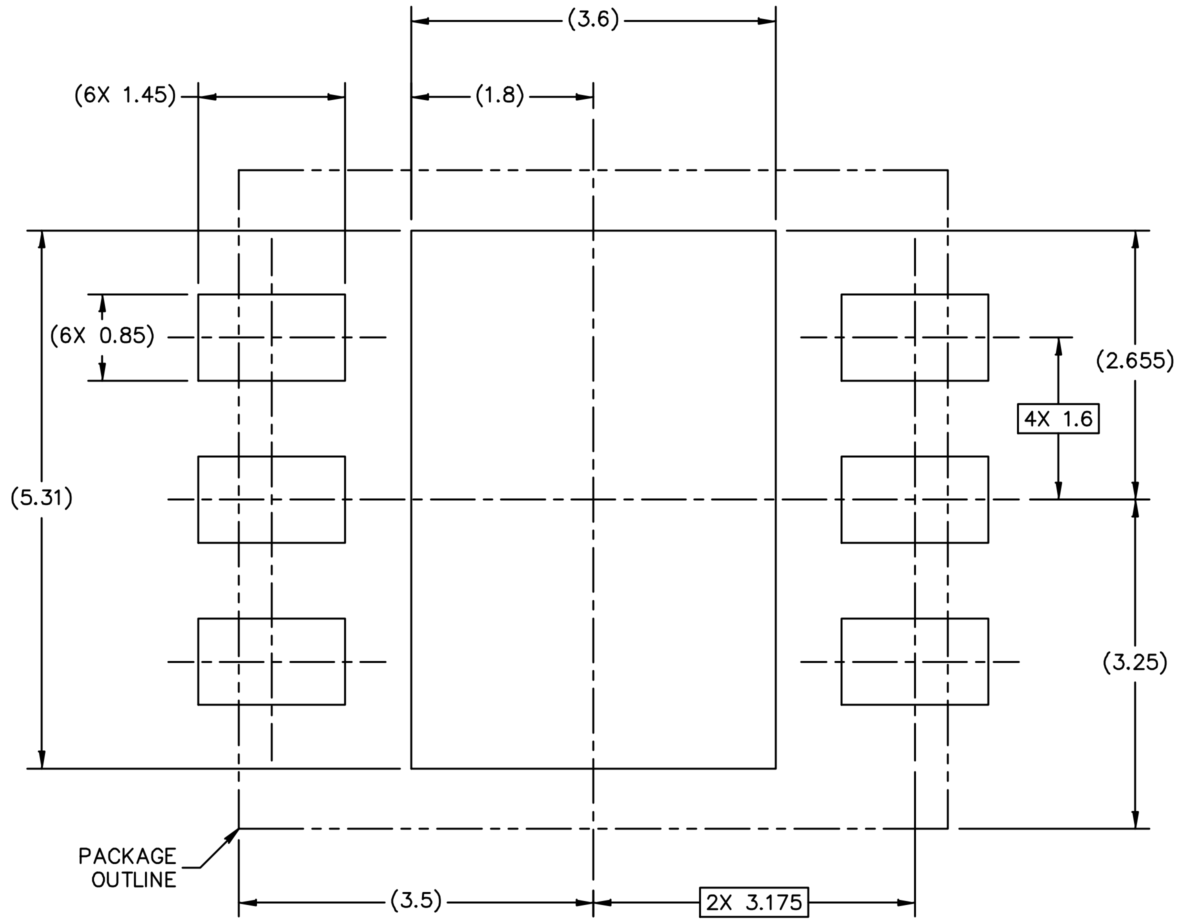

PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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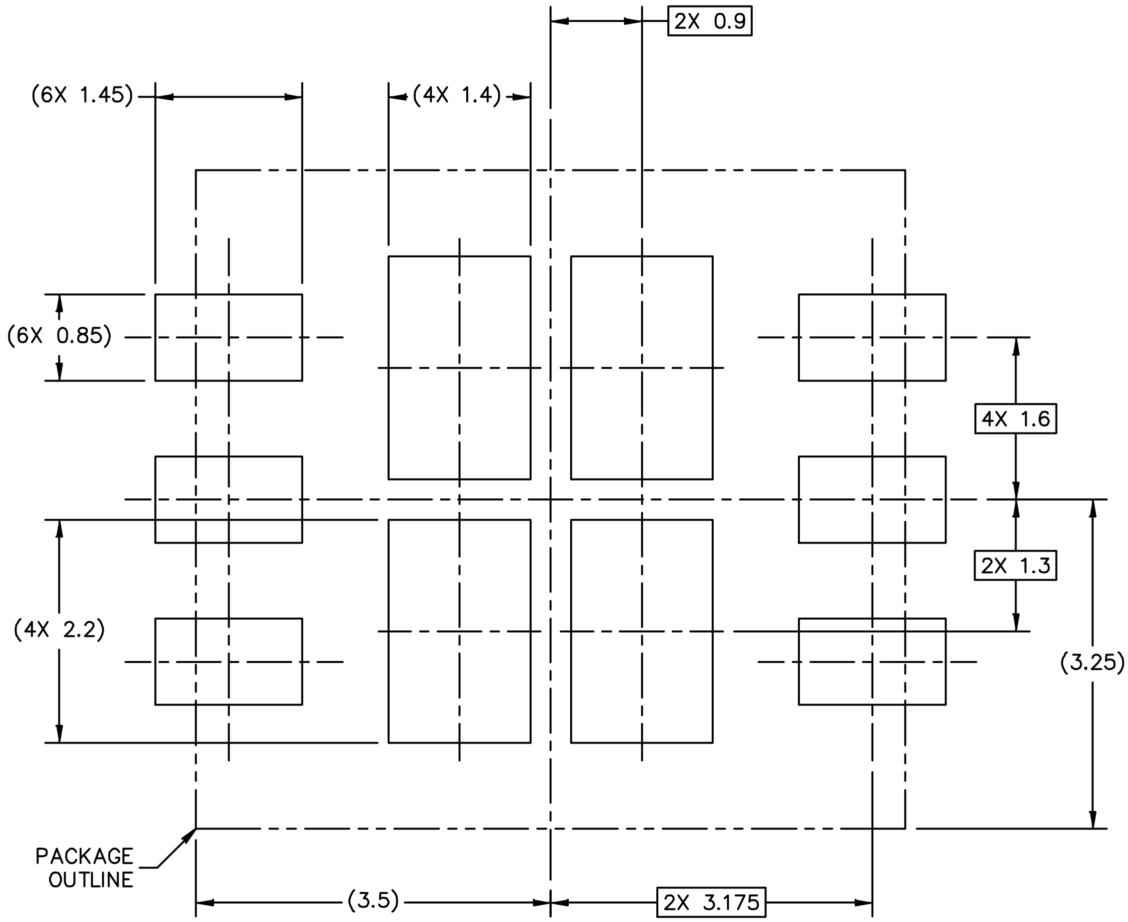

STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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H–PDFN–6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

SOT2030–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. RADIUS ON LEAD AND DIE ATTACH FLAG IS OPTIONAL.

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	NON JEDEC	98ASA01485D	A	6

Product Documentation and Software

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2022	• Initial release of data sheet
1	Nov. 2022	• Table 1, Maximum Ratings: Gate–Source Voltage: updated –8, 0 to –16, 0 Vdc, p. 2 • Table 4, ESD Protection Characteristics, Human Body Model: updated to reflect test data, p. 2 • Table 6, Electrical Characteristics, Off Characteristics: added Off–State Gate Leakage, p. 2 • General updates made to align data sheet to current standard
2	May 2023	• Table 6, Functional Tests: Min efficiency value updated to match production test value, p. 3 • Figure 2, Product Marking: added, p. 4 • Table 8, Product Marking Trace Code: added, p. 4 • General updates made to align data sheet to current standard

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