0.5 Ω, CMOS, 1.8 V to 5.5 V, 2:1 Mux/SPDT Switch

Data Sheet **ADG819**

FEATURES

Low on resistance: 0.8 Ω maximum at 125°C
0.25 Ω maximum on resistance flatness
1.8 V to 5.5 V single supply
200 mA current carrying capability
Automotive temperature range: −40°C to +125°C
Rail-to-rail operation
6-lead SOT-23, 8-lead MSOP, and 6-ball WLCSP packages
Fast switching times
Typical power consumption (<0.01 µW)
TTL-/CMOS-compatible inputs
Pin compatible with the ADG719

APPLICATIONS

Power routing
Battery-powered systems
Communication systems
Data acquisition systems
Cellular phones
Modems
PCMCIA cards
Hard drives
Relay replacement

GENERAL DESCRIPTION

The ADG819 is a monolithic, CMOS, single-pole, double-throw (SPDT) switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

Low power consumption and an operating supply range of 1.8 V to 5.5 V make the ADG819 ideal for battery-powered, portable instruments.

Each switch of the ADG819 conducts equally well in both directions when on. The ADG819 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG819 is available in a 6-lead SOT-23 package, an 8-lead MSOP package, and in a 6-ball WLCSP package. This chip occupies only a 1.14 mm × 2.18 mm area, making it the ideal candidate for space-constrained applications.

FUNCTIONAL BLOCK DIAGRAM

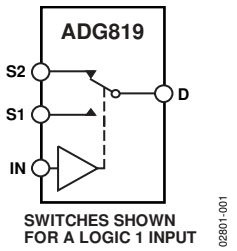

Figure 1.

PRODUCT HIGHLIGHTS

1. Very low on resistance, 0.5 Ω typical.
2. 1.8 V to 5.5 V single-supply operation.
3. High current carrying capability.
4. Tiny 6-lead SOT-23, 8-lead MSOP, and 6-ball, 1.14 mm × 2.18 mm WLCSP packages.

Rev. A

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REVISION HISTORY

5/12—Rev. 0 to Rev. A

Updated Format ..... Universal
Deleted ADG820 ..... Universal
Changes to General Description 1
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Change to WLCSP θ_{JA} Thermal Impedance Parameter, Table 3 5
Added Table 5 and Table 6; Renumbered Sequentially 6
Deleted Test Circuit 6; Renumbered Sequentially 8
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5/02—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}[1]	0.5			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA; see Figure 16
	0.6	0.7	0.8	Ω max	
On Resistance Match Between Channels, ΔR_{ON}[1]	0.06			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA
	0.08	0.1	0.12	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$[1]	0.1			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA
	0.17	0.2	0.25	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V; see Figure 17
	±0.25	±3	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V, or V_S = V_D = 4.5 V; see Figure 18
	±0.25	±3	±25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	35			ns typ	R_L = 50 Ω, C_L = 35 pF, V_S = 3 V; see Figure 19
	45	50	55	ns max	
t_{OFF}	10			ns typ	R_L = 50 Ω, C_L = 35 pF, V_S = 3 V; see Figure 19
	16	18	21	ns max	
Break-Before-Make Time Delay, t_{BBM}	5			ns typ	R_L = 50 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 3 V; see Figure 20
			1	ns min	
Charge Injection	20			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 21
Off Isolation	−71			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 22
Channel-to-Channel Crosstalk	−72			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 24
Bandwidth, −3 dB	17			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 23
C_S (Off)	80			pF typ	f = 1 MHz
C_D, C_S (On)	300			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V, digital inputs = 0 V or 5.5 V
I_{DD}	0.001			μA typ	
		1.0	2.0	μA max	

[1] On resistance parameters tested with I_S = 10 mA.
[2] Guaranteed by design; not subject to production test.

V_{DD} = 2.7 V to 3.6 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}[1]	0.7			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA; see Figure 16
	1.4	1.5	1.6	Ω max	
On Resistance Match Between Channels, ΔR_{ON}[1]	0.06			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA
		0.13	0.13	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$[1]	0.25			Ω typ	V_S = 0 V to V_{DD}, I_S = 100 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 3.3 V/1 V, V_D = 1 V/3.3 V; see Figure 17
	±0.25	±3	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01			nA typ	V_S = V_D = 1 V, or V_S = V_D = 3.3 V; see Figure 18
	±0.25	±3	±25	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	40			ns typ	R_L = 50 Ω, C_L = 35 pF, V_S = 1.5 V; see Figure 19
	60	65	70	ns max	
t_{OFF}	10			ns typ	R_L = 50 Ω, C_L = 35 pF, V_S = 1.5 V; see Figure 19
	16	18	21	ns max	
Break-Before-Make Time Delay, t_{BBM}	40			ns typ	R_L = 50 Ω, C_L = 35 pF, V_{S1} = V_{S2} = 1.5 V; see Figure 20
			1	ns min	
Charge Injection	10			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 21
Off Isolation	−71			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 22
Channel-to-Channel Crosstalk	−72			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 24
Bandwidth, −3 dB	17			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 23
C_S (Off)	80			pF typ	f = 1 MHz
C_D, C_S (On)	300			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V, digital Inputs = 0 V or 3.6 V
I_{DD}	0.001			μA typ	
		1.0	2.0	μA max	

[1] On resistance parameters tested with I_S = 10 mA.
[2] Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or D	400 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or D	200 mA
Operating Temperature Range	
Industrial	−40°C to +85°C
Automotive	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
SOT-23 (4-Layer Board)	
θ_{JA} Thermal Impedance	119°C/W
WLCSP (4-Layer Board)	
θ_{JA} Thermal Impedance	80°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

[1] Overvoltages at IN, Sx, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

Table 4. Truth Table for the ADG819

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

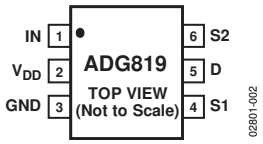


Figure 2. 6-Lead SOT-23 Pin Configuration

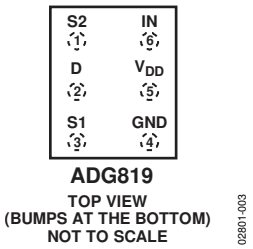


Figure 3. 6-Ball WLCSP Pin Configuration

Table 5. 6-Lead SOT-23 and 6-Ball WLCSP Pin Function Descriptions

Pin No.			
SOT-23	**WLCSP**	**Mnemonic**	**Description**
1	6	IN	Logic Control Input.
2	5	V_{DD}	Most Positive Power Supply Potential.
3	4	GND	Ground (0 V) Reference.
4	3	S1	Source Terminal. Can be an input or output.
5	2	D	Drain Terminal. Can be an input or output.
6	1	S2	Source Terminal. Can be an input or output.

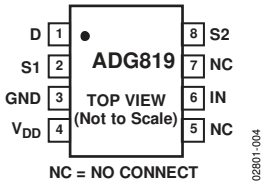


Figure 4. 8-Lead MSOP Pin Configuration

Table 6. 8-Lead MSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. Can be an input or output.
2	S1	Source Terminal. Can be an input or output.
3	GND	Ground (0 V) Reference.
4	V_{DD}	Most Positive Power Supply Potential.
5	NC	No Connect. Do not connect to this pin.
6	IN	Logic Control Input.
7	NC	No Connect. Do not connect to this pin.
8	S2	Source Terminal. Can be an input or output.

TYPICAL PERFORMANCE CHARACTERISTICS

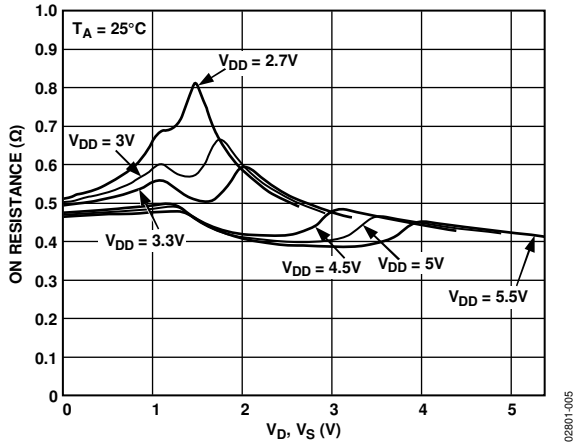


Figure 5. On Resistance vs. V_D, V_S

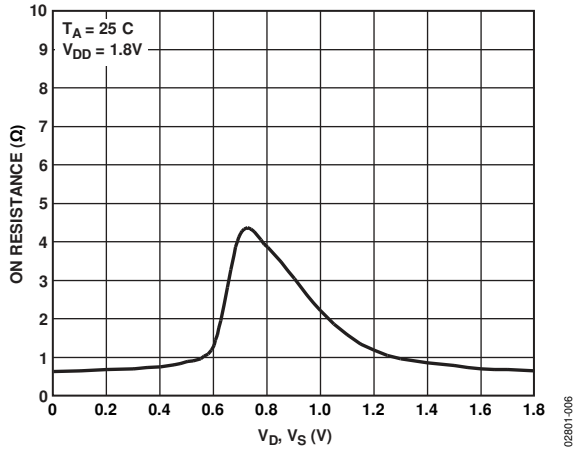


Figure 6. On Resistance vs. V_D, V_S

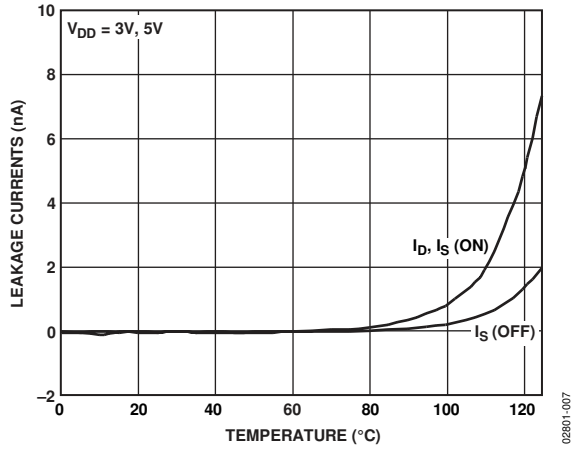


Figure 7. Leakage Currents vs. Temperature

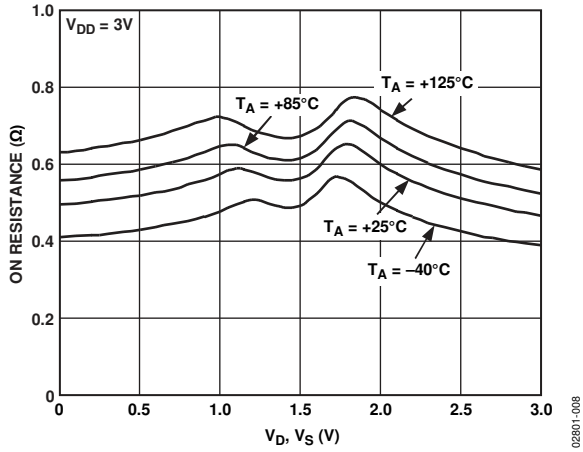


Figure 8. On Resistance vs. V_D, V_S for Different Temperatures

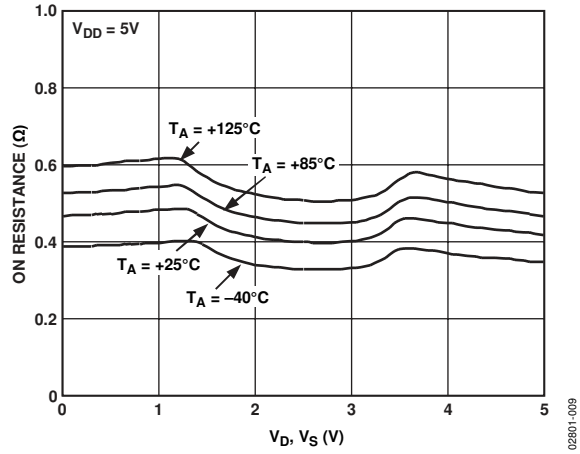


Figure 9. On Resistance vs. V_D, V_S for Different Temperatures

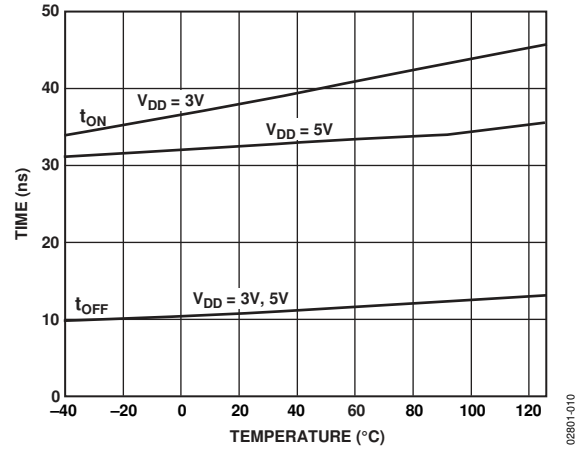


Figure 10. t_{ON}/t_{OFF} Times vs. Temperature

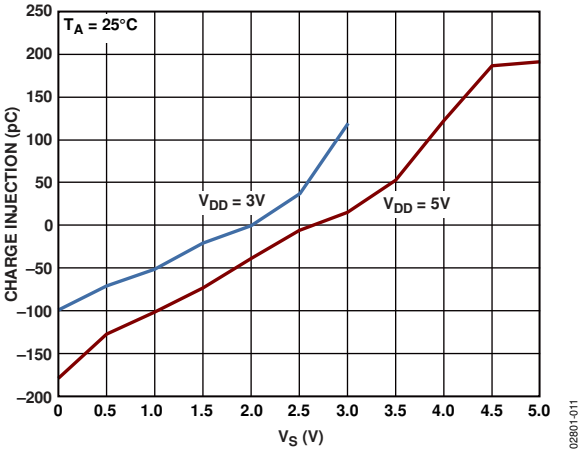


Figure 11. Charge Injection vs. V_S (Source Voltage)

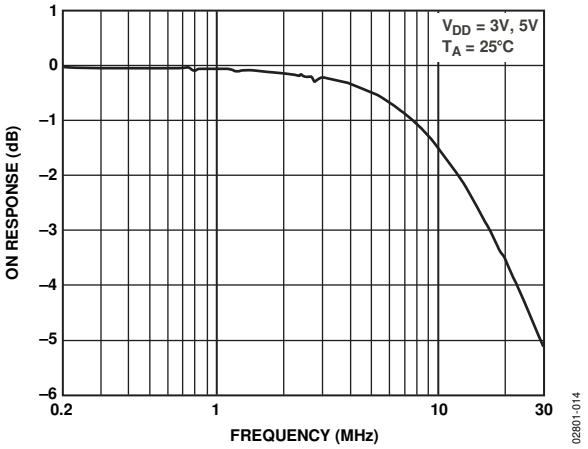


Figure 14. On Response vs. Frequency

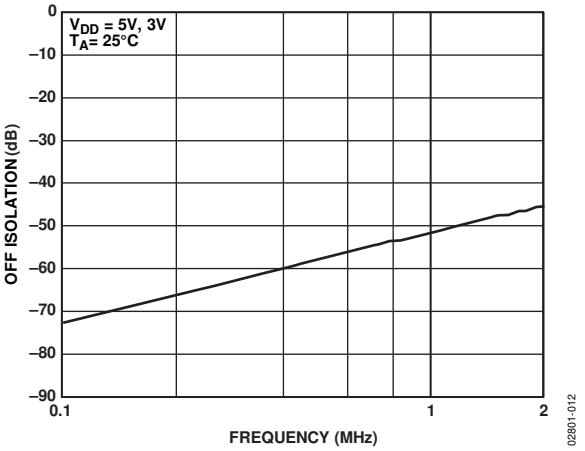


Figure 12. Off Isolation vs. Frequency

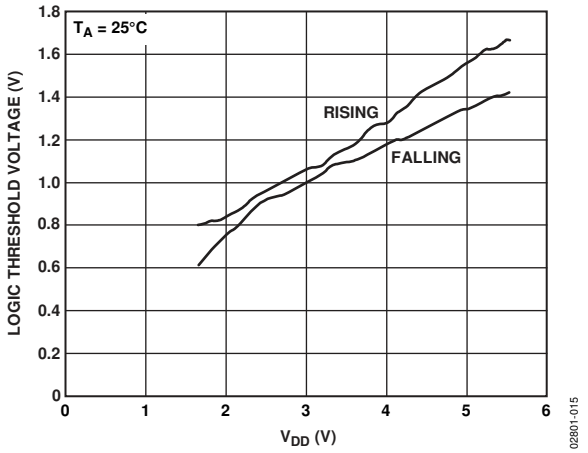


Figure 15. Logic Threshold Voltage vs. Supply Voltage

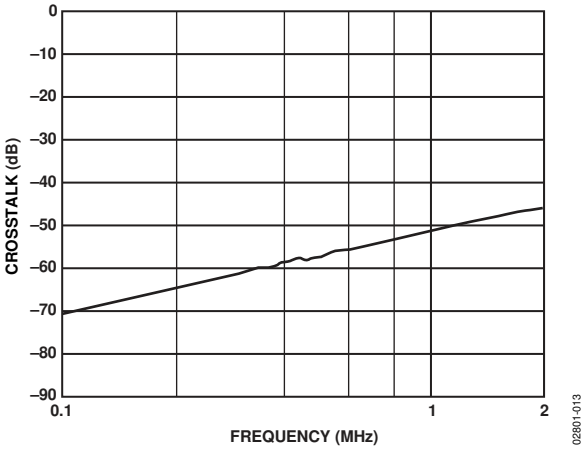


Figure 13. Crosstalk vs. Frequency

TEST CIRCUITS

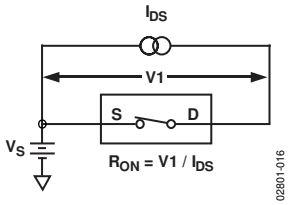


Figure 16. On Resistance

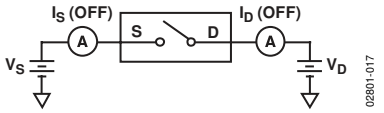


Figure 17. Off Leakage

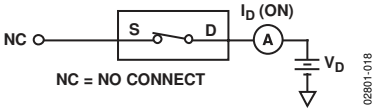


Figure 18. On Leakage

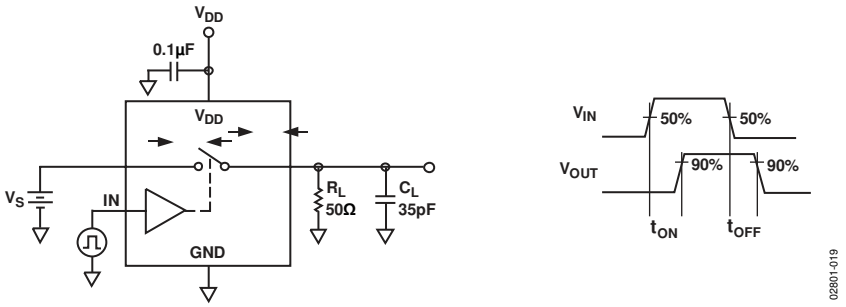


Figure 19. Switching Times

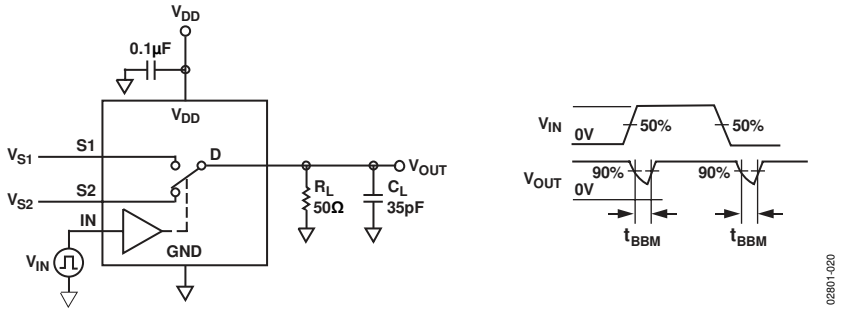


Figure 20. Break-Before-Make Time Delay, t_{BBM}

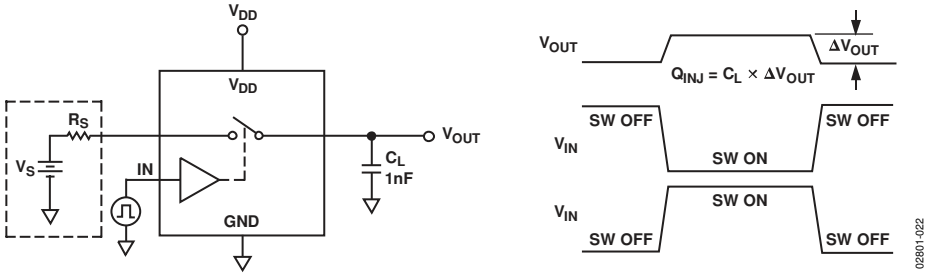


Figure 21. Charge Injection

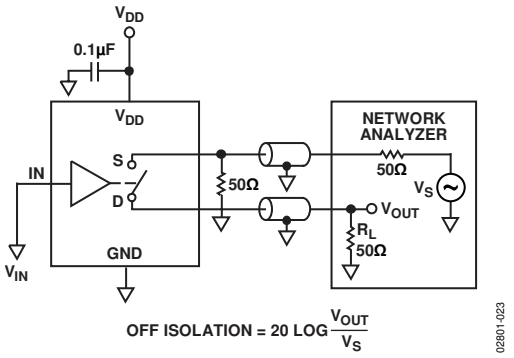


Figure 22. Off Isolation

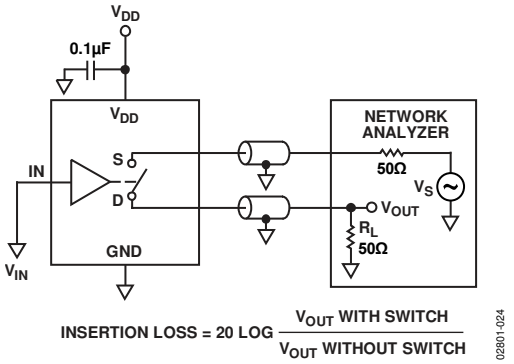


Figure 23. Bandwidth

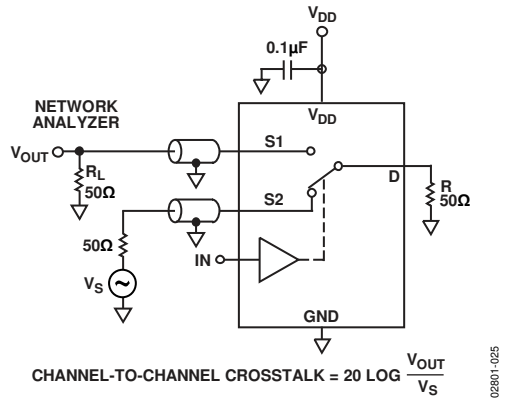


Figure 24. Channel-to-Channel Crosstalk

TERMINOLOGY

R_{ON}
Ohmic resistance between D and Sx.

ΔR_{ON}
On resistance match between any two channels, that is, R_{ON} maximum − R_{ON} minimum.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
Source leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (Off)
Off switch source capacitance.

C_D, C_S (On)
On switch capacitance.

t_{ON}
Delay between applying the digital control input and the output switching on.

t_{OFF}
Delay between applying the digital control input and the output switching off.

t_{BBM}
Off time or on time measured between the 90% points of both switches when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

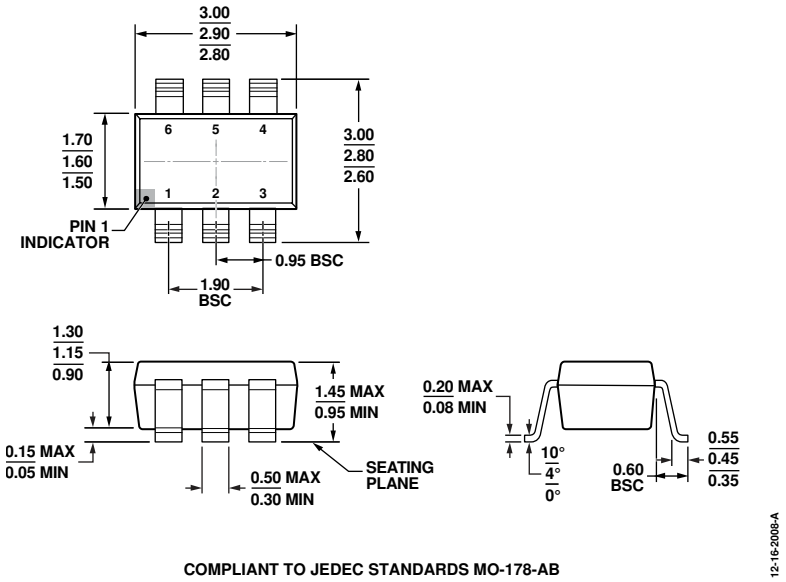
Channel-to-Channel Crosstalk
A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Bandwidth
Frequency at which the output is attenuated by −3 dB.

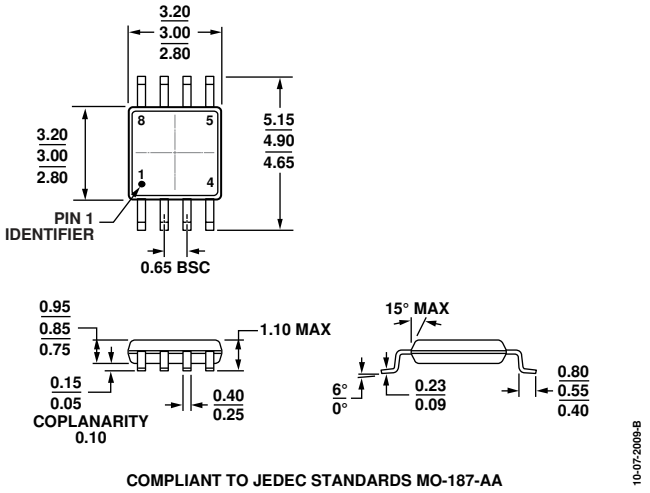
On Response
Frequency response of the on switch.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 25. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 26. 8-Lead mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

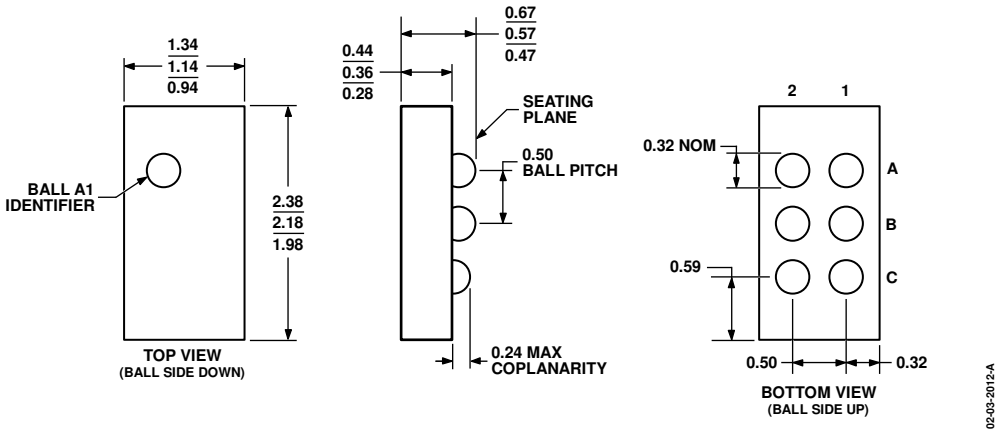


Figure 27. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option	Branding[2]
ADG819BCBZ-REEL	[3]	–40°C to +85°C	6-Ball Wafer Level Chip Package [WLCSP]	CB-6-1	SBC
ADG819BCBZ-REEL7	[3]	–40°C to +85°C	6-Ball Wafer Level Chip Package [WLCSP]	CB-6-1	SBC
ADG819BRM		–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SNB
ADG819BRM-REEL		–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SNB
ADG819BRMZ		–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBC
ADG819BRMZ-REEL7	[3]	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	SBC
ADG819BRT-500RL7	[3]	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SNB
ADG819BRT-REEL7	[3]	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SNB
ADG819BRTZ-500RL7	[3]	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SBC
ADG819BRTZ-REEL	[3]	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SBC
ADG819BRTZ-REEL7	[3]	–40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	SBC

[1] Z = RoHS Compliant Part.
[2] Branding on these packages is limited to three characters due to space constraints.
[3] Contact factory for availability.

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