



MX681EBA156M250

Ultra-low Jitter 156.25MHz LVPECL XO

Confidential Rev0.6 7/7/14

Description

The MX681EBA156M250 is an ultra-low phase jitter and phase noise XO with LVPECL output optimized for high line rate applications.

Applications

- 10/40/100GE
- Telecom, NAS, Networking, Storage

Absolute Maximum Ratings

Supply Voltage (V_{IN})	+4V
Lead Temperature (soldering, 10s)	260°C
Storage Temperature (T_s)	125°C
ESD Rating	2kV

Features

- 156.25MHz LVPECL output
- Ultra-low 46fs output jitter (12kHz to 20MHz)
- ± 50 ppm total stability
- -40°C to $+85^\circ\text{C}$ temperature range
- Industry standard 5x7mm package

Operating Ratings

Supply Voltage (V_{IN})	+2.97V to +3.63V
Ambient Temperature (T_A)	-40°C to $+85^\circ\text{C}$
Junction Thermal Resistance PDIP (θ_{JA})	xx°C/W

Electrical Characteristics

$V_{DD}=3.3\pm 10\%$, -40°C to 85°C , terminated 50Ω to $V_{DD} - 2V^{(1)}$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DD}	Supply Current	Outputs loaded with 50 Ohms to $V_{DD}-2V$			65	mA
F_0	Center Frequency			156.25		MHz
	Stability	Note 2			± 50	PPM
Φ_J	Jitter	Phase jitter (12kHz to 20MHz)		46		fsRMS
		Phase jitter (1.875MHz to 20MHz)		43		
		Phase jitter (50kHz to 80MHz)		100		
		Period jitter.		1.7		ps
t_{START}	Startup Time				20	ms
V_{OH}	Output Voltage High	LVPECL output levels	$V_{DD} - 1.02$			
V_{OL}	Output Voltage Low				$V_{DD} - 1.62$	V
	Duty Cycle		45		55	%
t_R/t_F	Rise/Fall Time		300			ps
V_{IH}	OE input Voltage High	Output disabled when OE is high	$V_{DD} \times 0.7$			V
V_{IL}	OE Input Voltage Low	Outputs enabled when OE is low for floating			$V_{DD} \times 0.3$	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to 85°C .

Ordering Information*

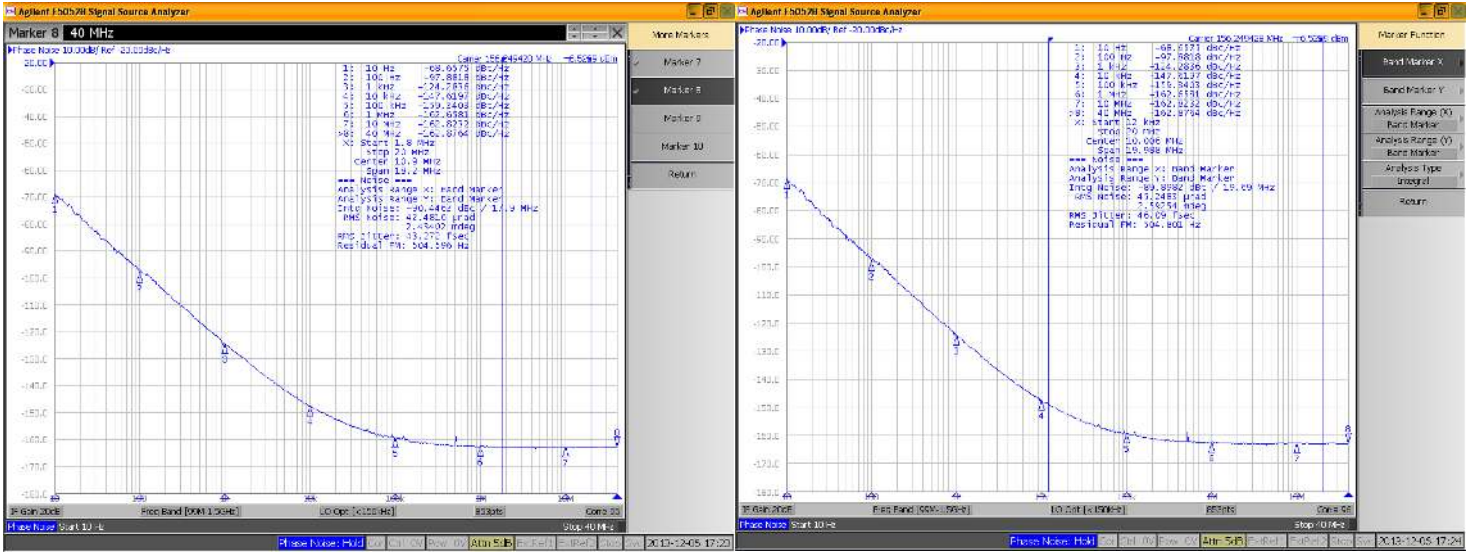
Part Number	Line 1 Marking	Line 2 Marking	Shipping	Temperature Range	Package
MX681EBA156M250	MX681E	BA156M250	Tube	-40°C to 85°C	6-pin 5x7mm
MX681EBA156M250 TR	MX681E	BA156M250	Tape&Reel	-40°C to 85°C	6-pin 5x7mm

*Line 3 marking is datecode information. See figu

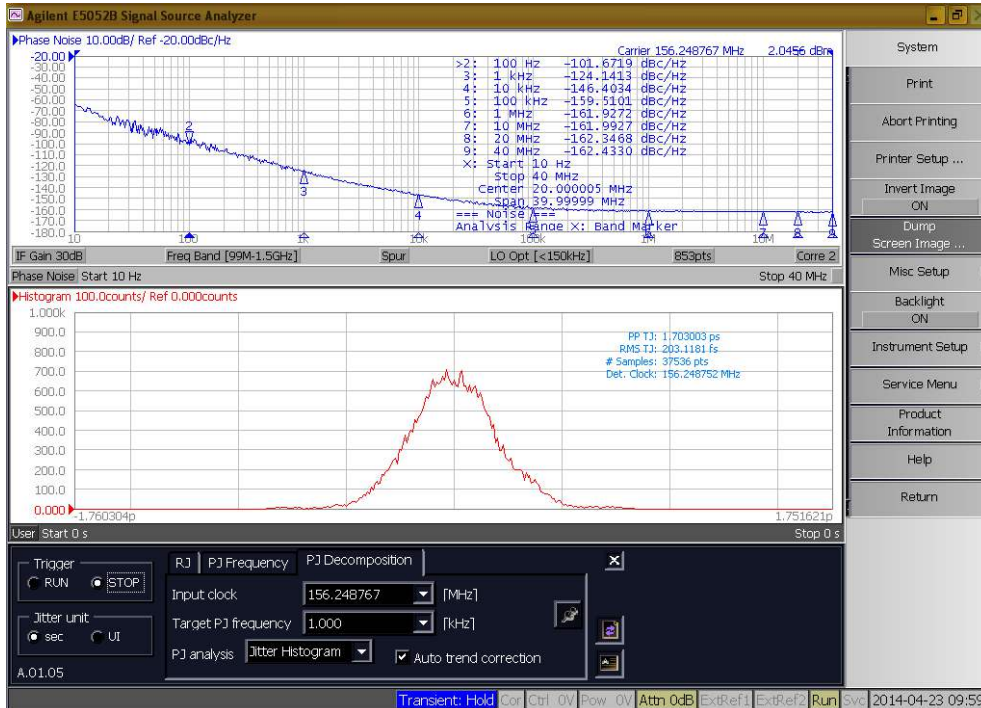
Phase Noise Performance

1.875MHz to 20MHz Integration Range

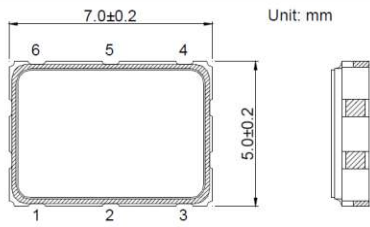
12kHz to 20MHz Integration Range



Period Jitter (37536 samples)

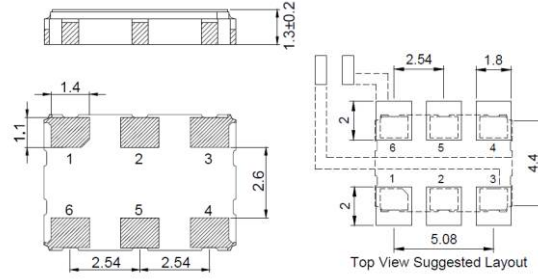


Dimensions, Pin Assignment, Land Pattern



Pin Function:

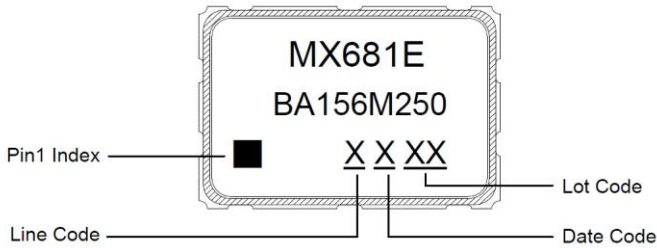
- 1. OE
- 2. NC
- 3. GND
- 4. OUT
- 5. $\overline{\text{OUT}}$
- 6. VDD



※ Pad dimension tolerance ±0.2 mm

※ Power Supply Decoupling Capacitor is Required.

Date Code Information



		MONTH													
YEAR		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC		
2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

* This date code will be cycled every four years.

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