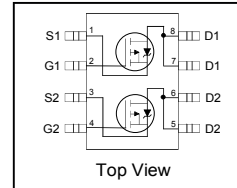


- Generation V Technology
- Ultra Low On-Resistance
- Dual P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

HEXFET® Power MOSFET



$V_{DS}$	<b>-55V</b>
$R_{DS(on)}$ max.	<b>0.105Ω</b>
$I_D$	<b>-3.4A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

### Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SO-8 has been modified through a customized lead frame for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7342PbF	SO-8	Tape and Reel	4000	IRF7342PbF

### Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$V_{DS}$	Drain-Source Voltage	-55	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-3.4	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-2.7	
$I_{DM}$	Pulsed Drain Current ①	-27	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation	2.0	W
$P_D @ T_A = 70^\circ\text{C}$	Maximum Power Dissipation	1.3	
	Linear De rating Factor	0.016	mW/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$V_{GSM}$	Gate-to-Source Voltage Single Pulse $t_p < 10\mu\text{s}$	30	
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	114	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C


### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ④	—	62.5	°C/W

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

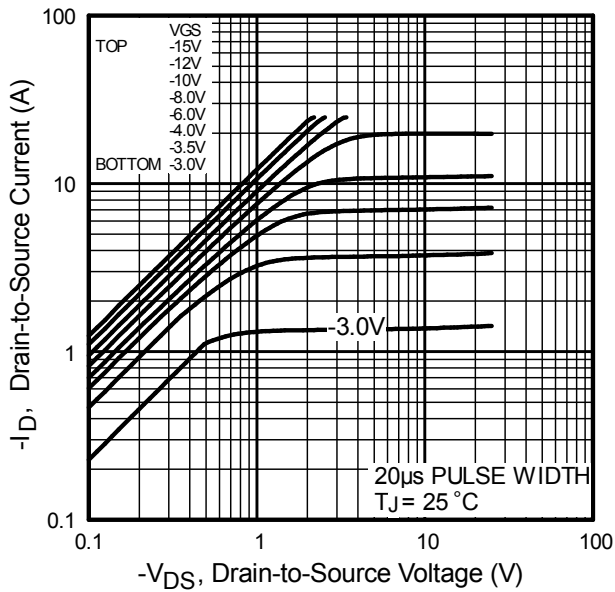
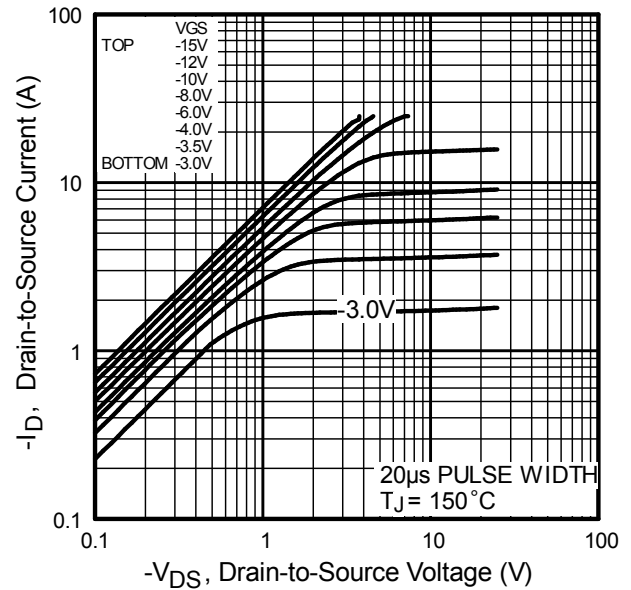
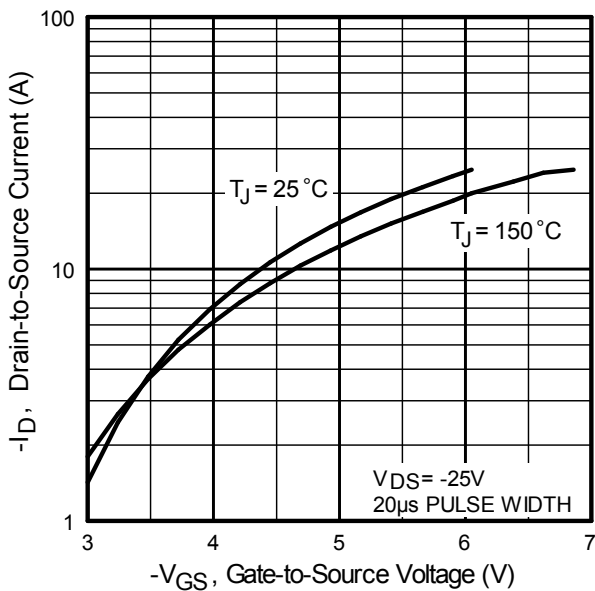
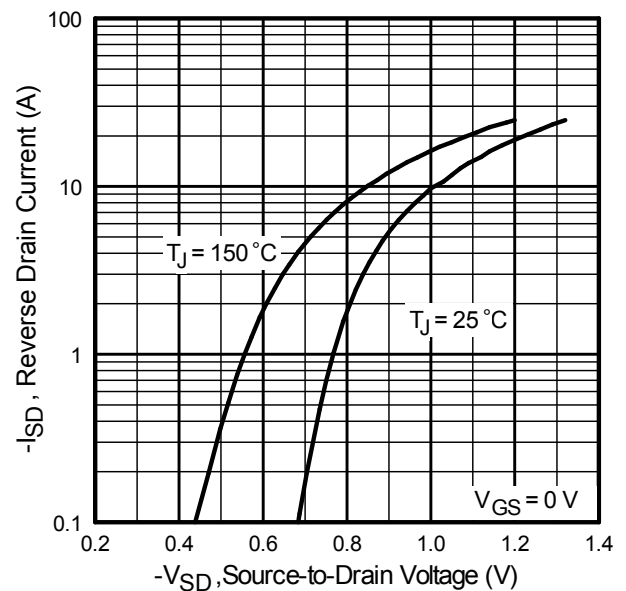
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.054	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.095	0.105	$\Omega$	$V_{GS} = -10V, I_D = -3.4A$ ④
		—	0.150	0.170		$V_{GS} = -4.5V, I_D = -2.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$g_{fs}$	Forward Trans conductance	3.3	—	—	S	$V_{DS} = -10V, I_D = -3.1A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-2.0	$\mu A$	$V_{DS} = -55V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$Q_g$	Total Gate Charge	—	26	38	nC	$I_D = -3.1A$
$Q_{gs}$	Gate-to-Source Charge	—	3.0	4.5		$V_{DS} = -44V$
$Q_{gd}$	Gate-to-Drain ('Miller') Charge	—	8.4	13		$V_{GS} = -10V$ , See Fig.10 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	22	ns	$V_{DD} = -28V$
$t_r$	Rise Time	—	10	15		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	64		$R_G = 6.0\Omega$
$t_f$	Fall Time	—	22	32		$R_D = 16\Omega$ ④
$C_{iss}$	Input Capacitance	—	690	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	210	—		$V_{DS} = -25V$
$C_{riss}$	Reverse Transfer Capacitance	—	86	—		$f = 1.0\text{MHz}$ , See Fig.9

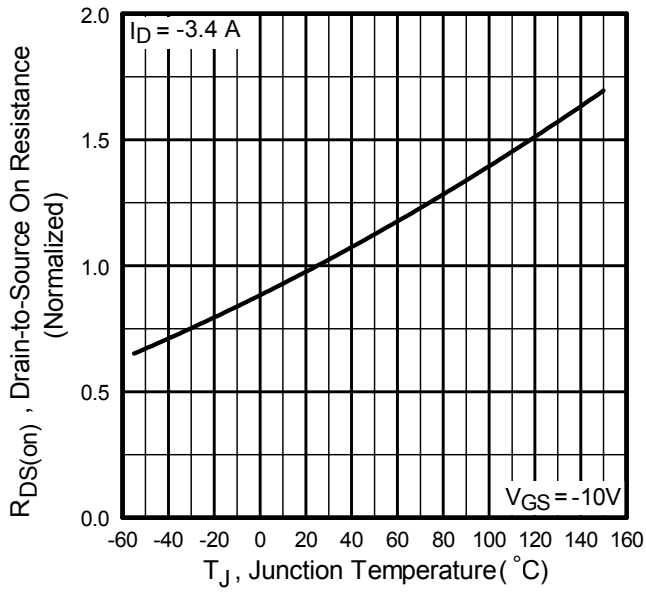
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-27		
$V_{SD}$	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	54	80	ns	$T_J = 25^\circ\text{C}, I_F = -2.0A$ ,
$Q_{rr}$	Reverse Recovery Charge	—	85	130	nC	$di/dt = 100A/\mu s$ ④

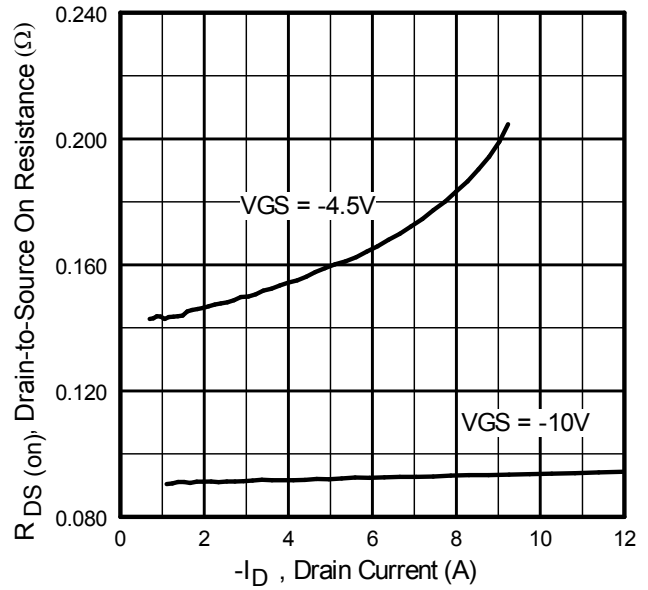
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 20\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = -3.4A$ . (See Fig. 8)
- ③  $I_{SD} \leq -3.4A$ ,  $di/dt \leq 150A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤ When mounted on 1" square copper board,  $t \leq 10\text{sec}$ .

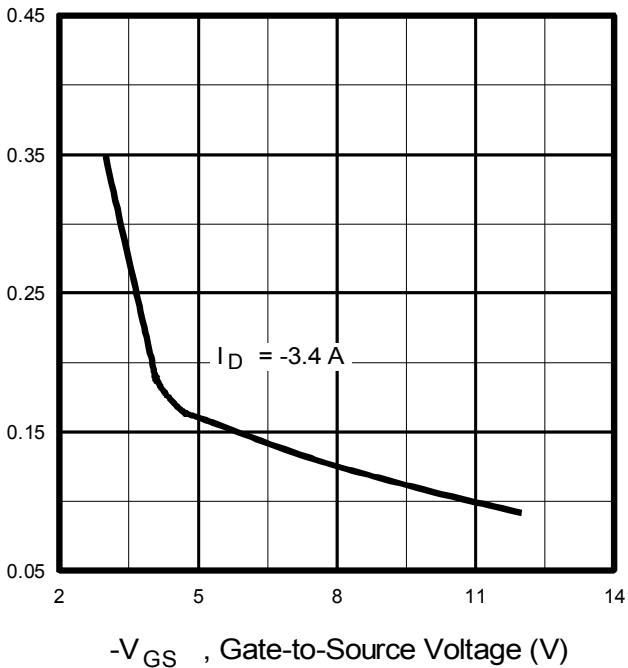

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Source-Drain Diode Forward Voltage



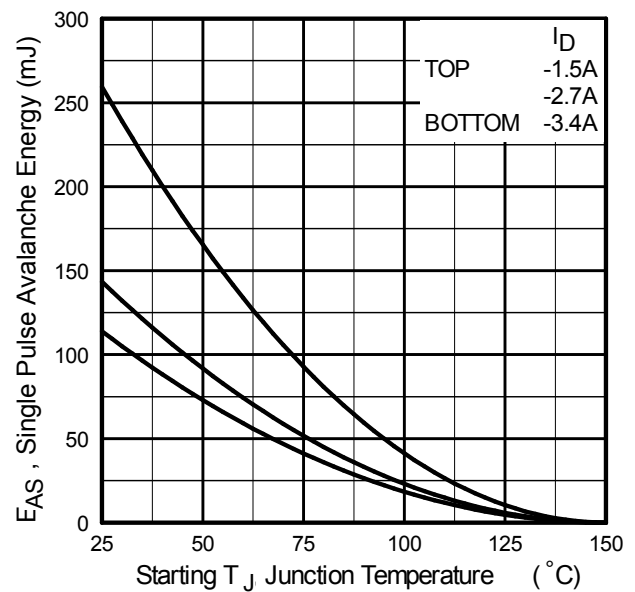
**Fig 5.** Normalized On-Resistance Vs. Temperature



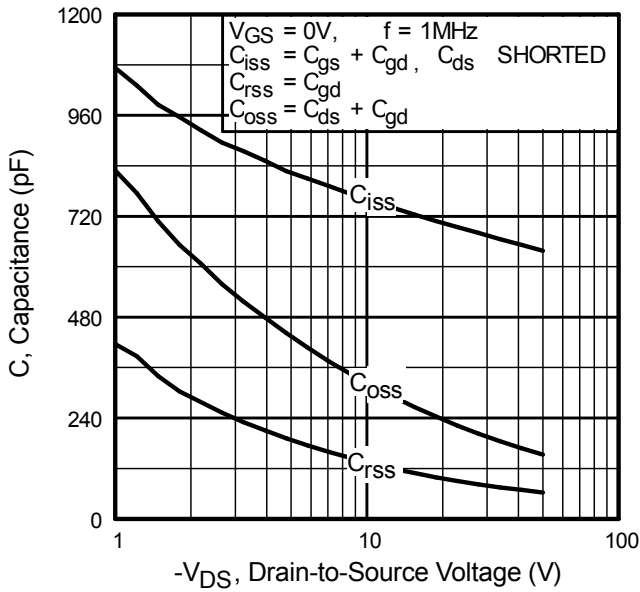
**Fig 6.** Typical On-Resistance Vs. Drain Current



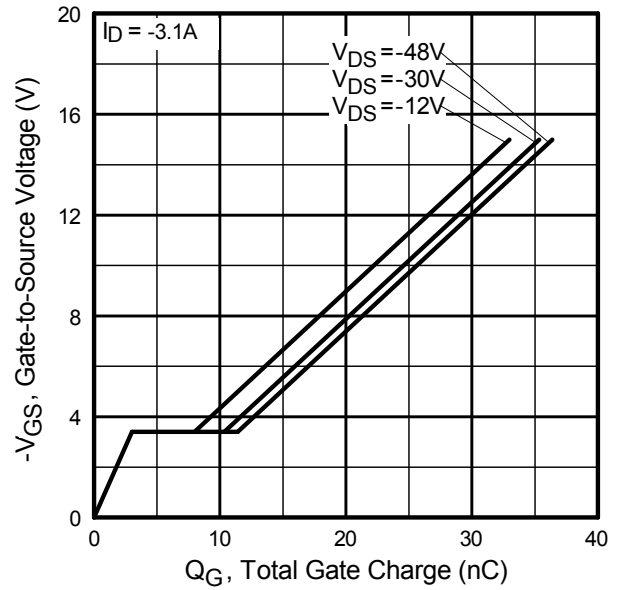
**Fig 7** Typical On-Resistance Vs. Gate Voltage



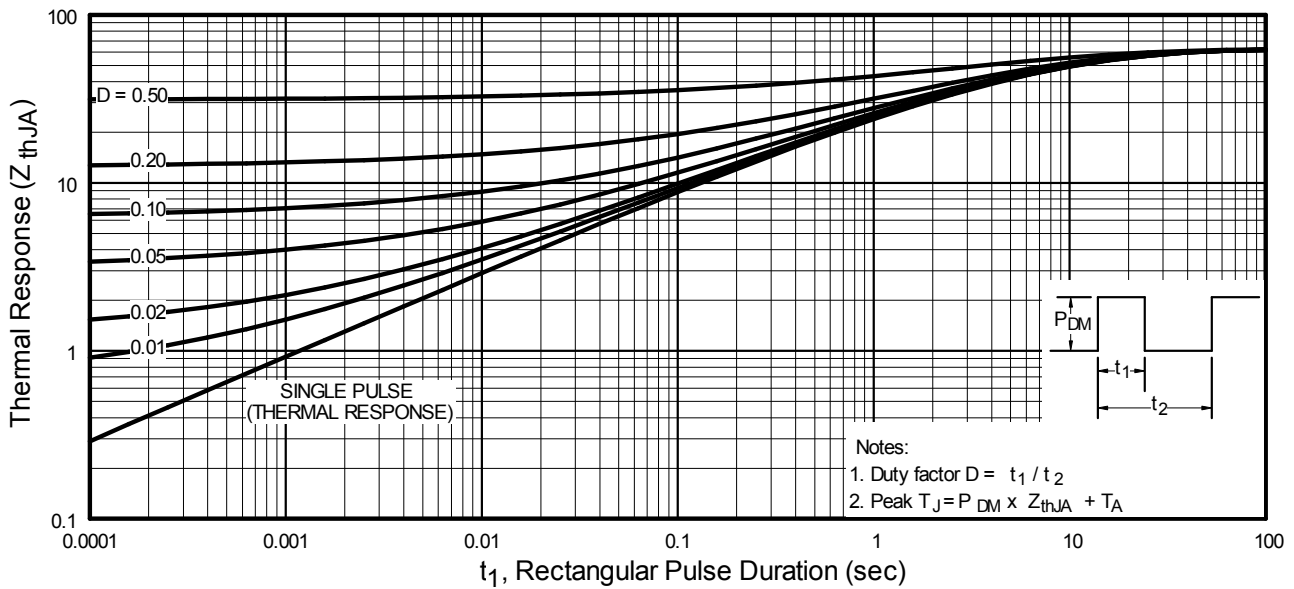
**Fig 8.** Maximum Avalanche Energy



**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage

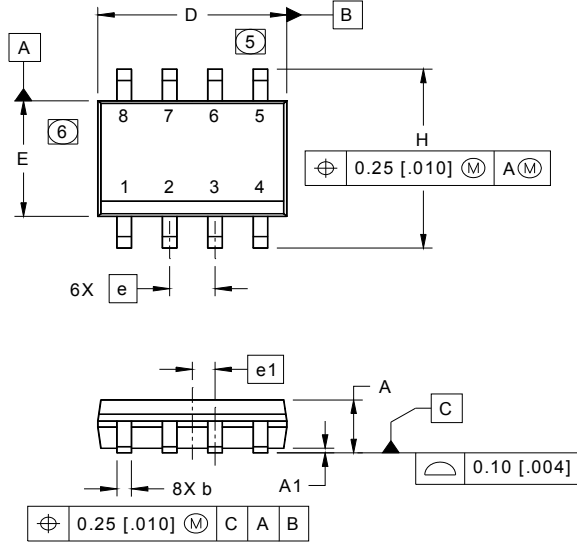


**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage

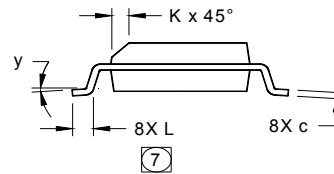


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

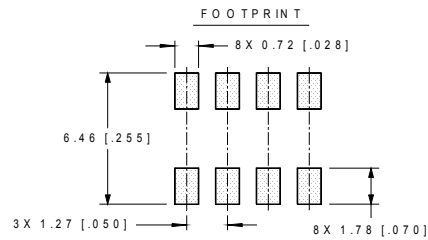
## SO-8 Package Outline (Dimensions are shown in millimeters (inches))



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

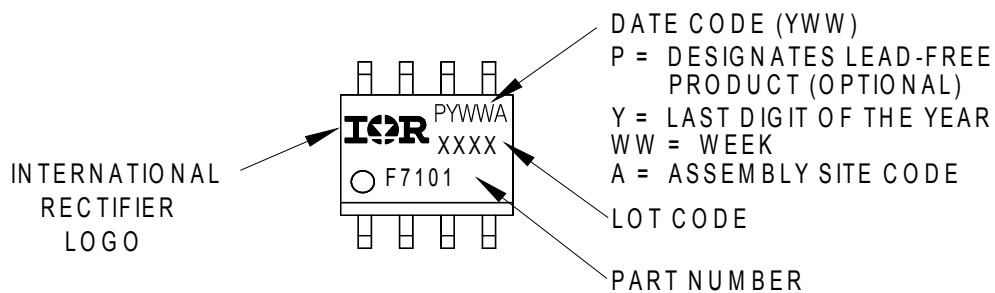


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
  2. CONTROLLING DIMENSION: MILLIMETER
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
  5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
  6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
  7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

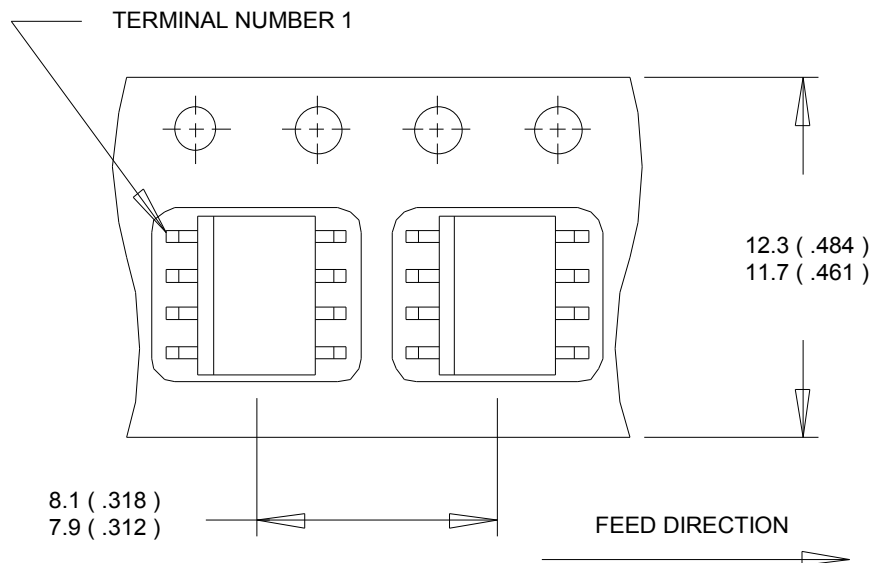


## SO-8 Part Marking Information

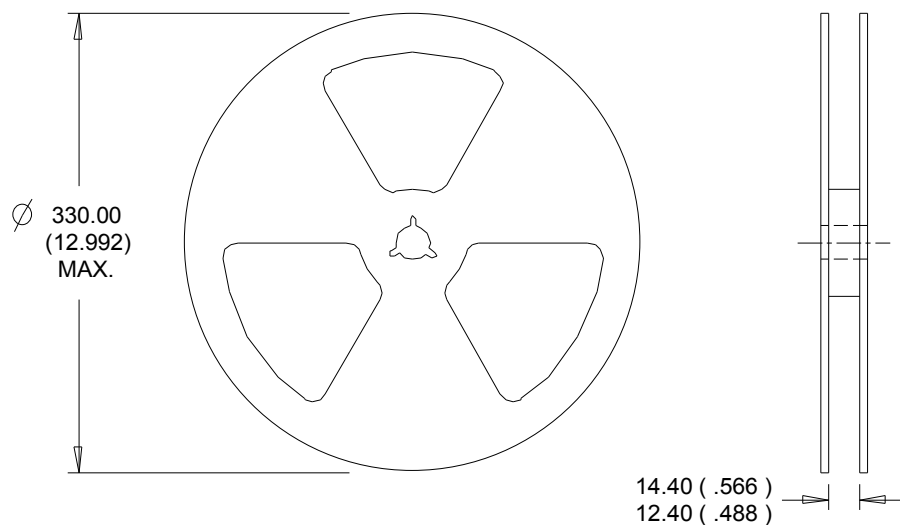
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**SO-8 Tape and Reel** (Dimensions are shown in millimeters (inches))

**NOTES:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**Qualification Information†**

<b>Qualification Level</b>	Consumer	
<b>Moisture Sensitivity Level</b>	SO-8	MSL1 (per JEDEC J-STD-020D) <sup>††</sup>
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at Infineon’s web site [www.infineon.com](http://www.infineon.com)

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
05/26/2016	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Added disclaimer on last page.</li> </ul>

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