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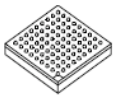
B4860 QorIQ Qonverge Data Sheet



FC-PBGA–1020
33 mm x 33 mm

This B4860 QorIQ Qonverge chip is a NXP high-end heterogeneous multicore SoC based on StarCore, Power Architecture®, CoreNet, MAPLE, and DPAA technologies. The chip targets the emerging broadband wireless infrastructure and builds upon the proven success of NXP's existing multicore DSPs and CPUs. It is designed to bolster the rapidly changing and expanding wireless base station markets, such as 3G-LTE (FDD and TDD), LTE-Advanced, TD-SCDMA, GSM and WCDMA.

This chip can be used for combined control, data path, and application layer processing in base stations and in general-purpose embedded computing systems. Its high level of integration offers performance benefits compared to multiple discrete devices, while also simplifying board design.This chip includes these functions and features:

- Six fully-programmable StarCore SC3900 FVP core subsystems, divided into three clusters—each core runs up to 1.2 GHz, with an architecture highly optimized for wireless base station applications
- Four dual-thread e6500 Power Architecture processors organized in one cluster—each core runs up to 1.6 GHz
- Two 64-bits DDR3/3L controllers for high-speed, industry-standard memory interfaces running up to 1866 MT/s
- MAPLE-B3 hardware acceleration—for forward error correction schemes including Turbo or Viterbi decoding, Turbo encoding and rate matching, MIMO MMSE equalization scheme, matrix operations, CRC insertion and check, DFT/iDFT and FFT/iFFT calculations, PUSCH/PDSCH acceleration, and UMTS chip rate acceleration
- CoreNet fabric supports coherency using MESI protocol between the e6500 cores, SC3900 FVP cores, memories and external interfaces. CoreNet fabric interconnect runs at up to 667 MHz and supports coherent and non-coherent out of order transactions with prioritization and bandwidth allocation amongst CoreNet endpoints.
- Data Path Acceleration Architecture, which includes:
  - Frame Manager (FMan), which supports in-line packet parsing and general classification to enable policing and QoS-based packet distribution
  - Queue Manager (QMan) and Buffer Manager (BMan), which allow offloading of queue management, task management, load distribution, flow ordering, buffer management, and allocation tasks from the cores
  - Security engine (SEC 5.3)—crypto-acceleration for protocols such as IPsec, SSL and 802.16
- Large internal cache memory with snooping and stashing capabilities for bandwidth saving and high utilization of processor elements. The 9856 KB internal memory space includes the following:
  - 32 KB L1 ICache per e6500/SC3900 core
  - 32 KB L1 DCache per e6500/SC3900 core
  - 2048 KB unified L2 cache for each SC3900 FVP cluster
  - 2048 KB unified L2 cache for e6500 cluster
  - Two 512 KB shared L3 CoreNet platform caches (CPC)
- Sixteen 10 Gbps SerDes lanes serving:
  - Two Serial RapidIO controllers each with four lanes running at up to 5 GT/s
  - Eight lanes common public radio interface (CPRI V4.2) controller for glueless antenna connection running at up to 9.8 GT/s
  - Two 10 GT/s Ethernet controllers (10GbE) for network communications
  - Six 1 GT/s/2.5 GT/s Ethernet controllers for network communications
  - Four lanes PCI Express controller running at up to 5 GT/s
  - Eight2.5 GT/s/3.125 GT/s/5 GT/s Debug (Aurora)
- Two OCeaN DMAs
- Various system peripherals
- 118 32-bit timers

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This figure shows the major functional units of the chip.

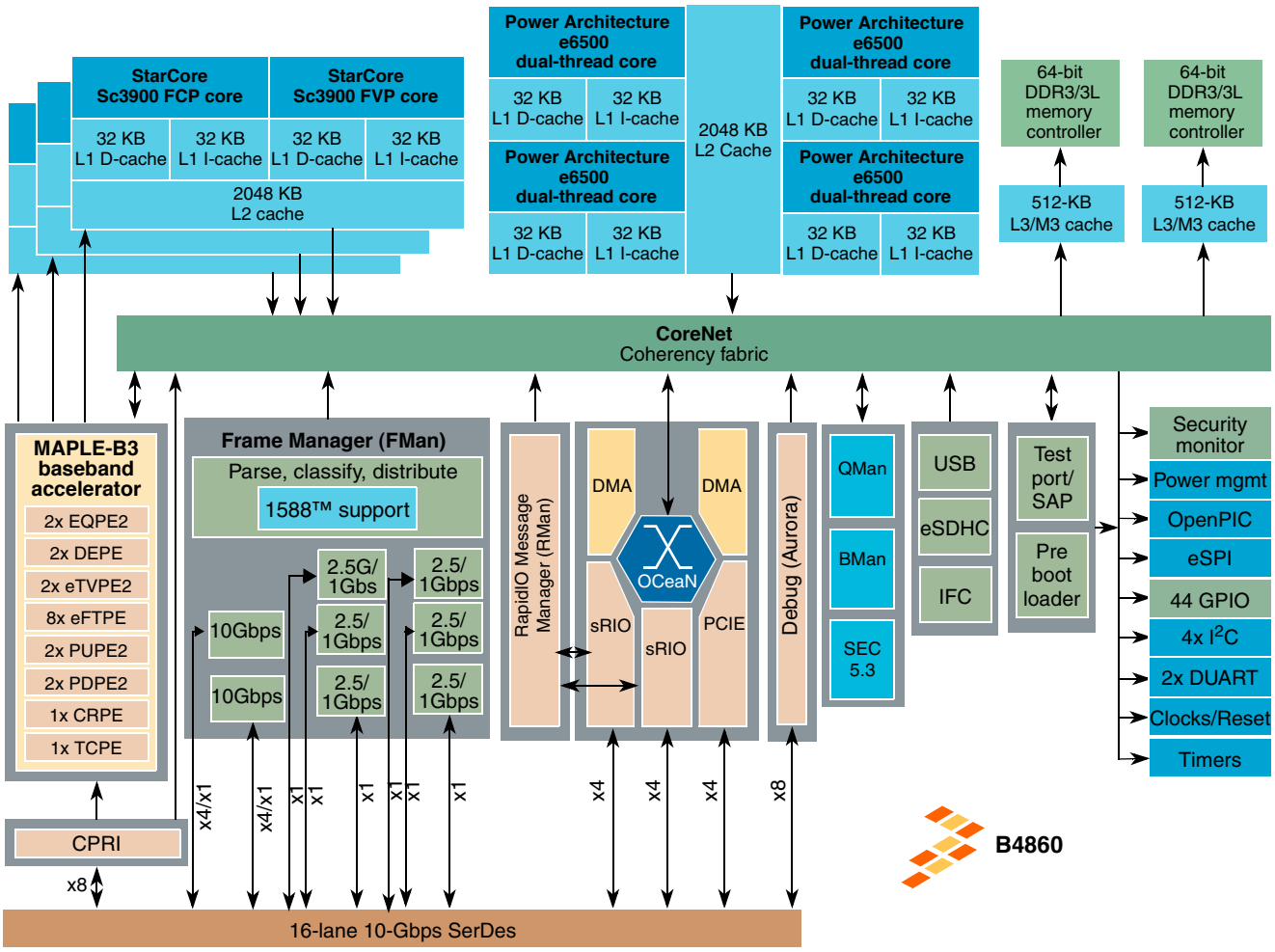


Figure 1. Block diagram

1 Pin assignments

1.1 1020 FC-PBGA ball layout diagrams

These figures show the B4860 FC-PBGA ball map.

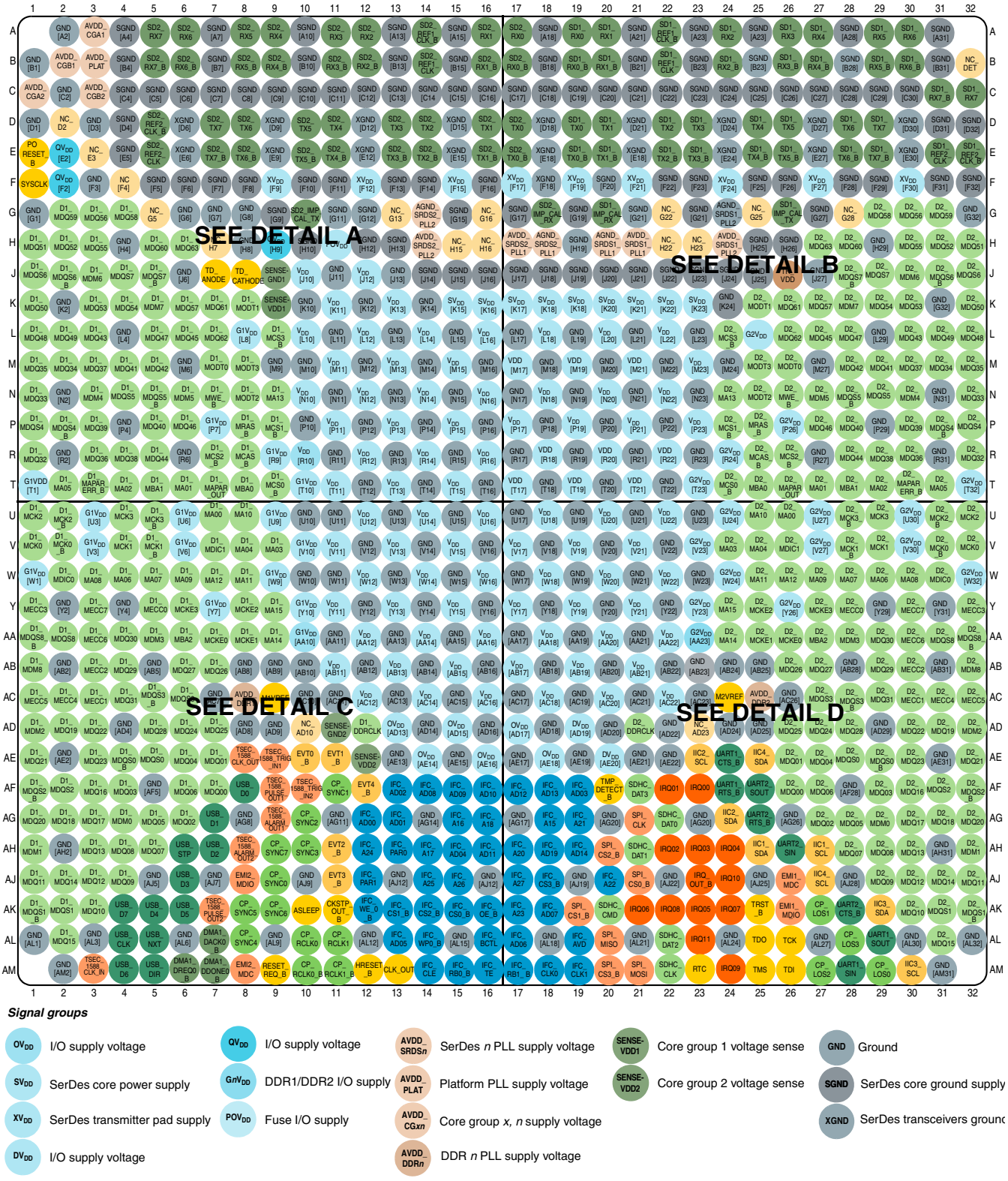


Figure 2. 1020 BGA ball map diagram (top view)

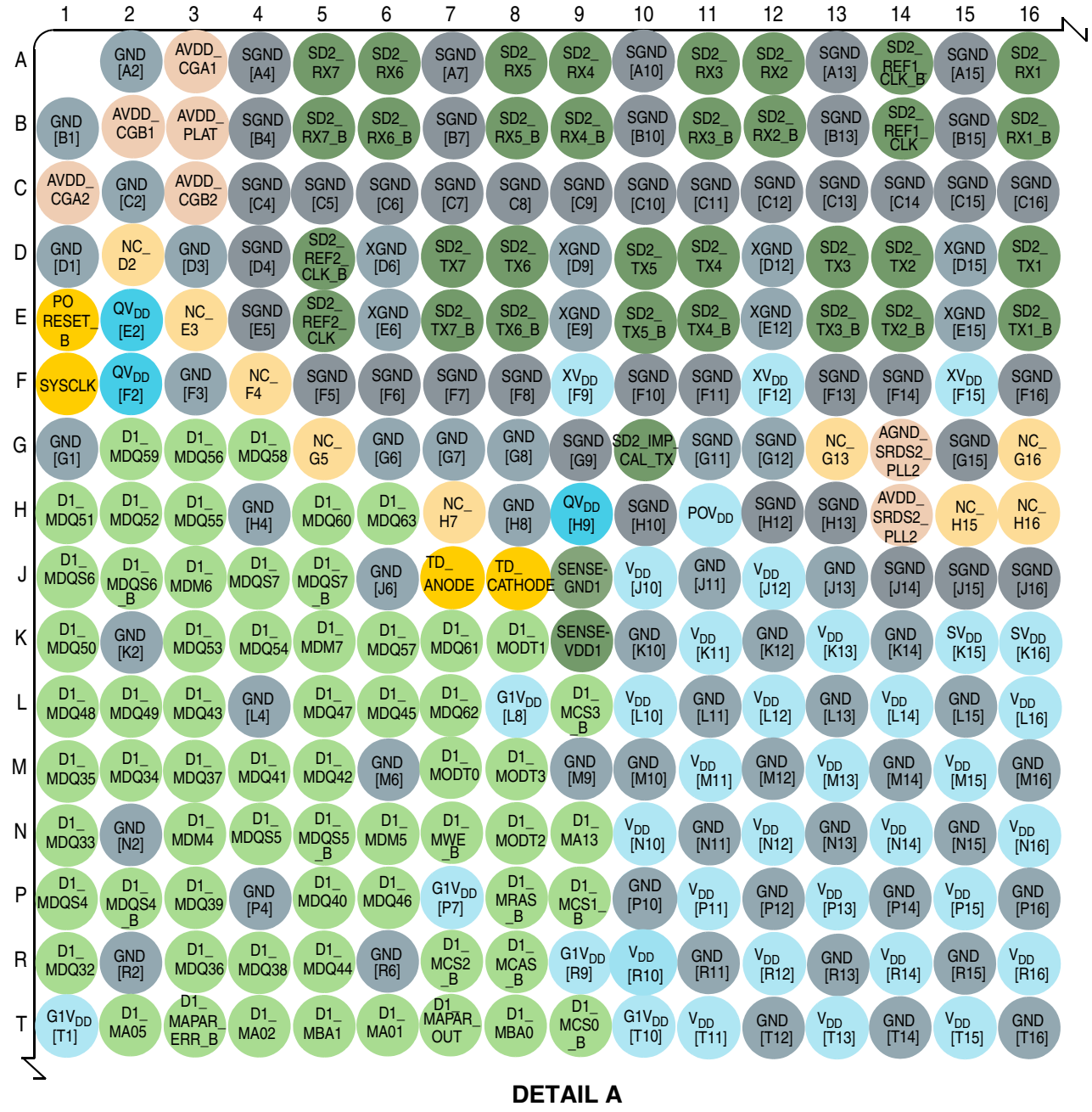
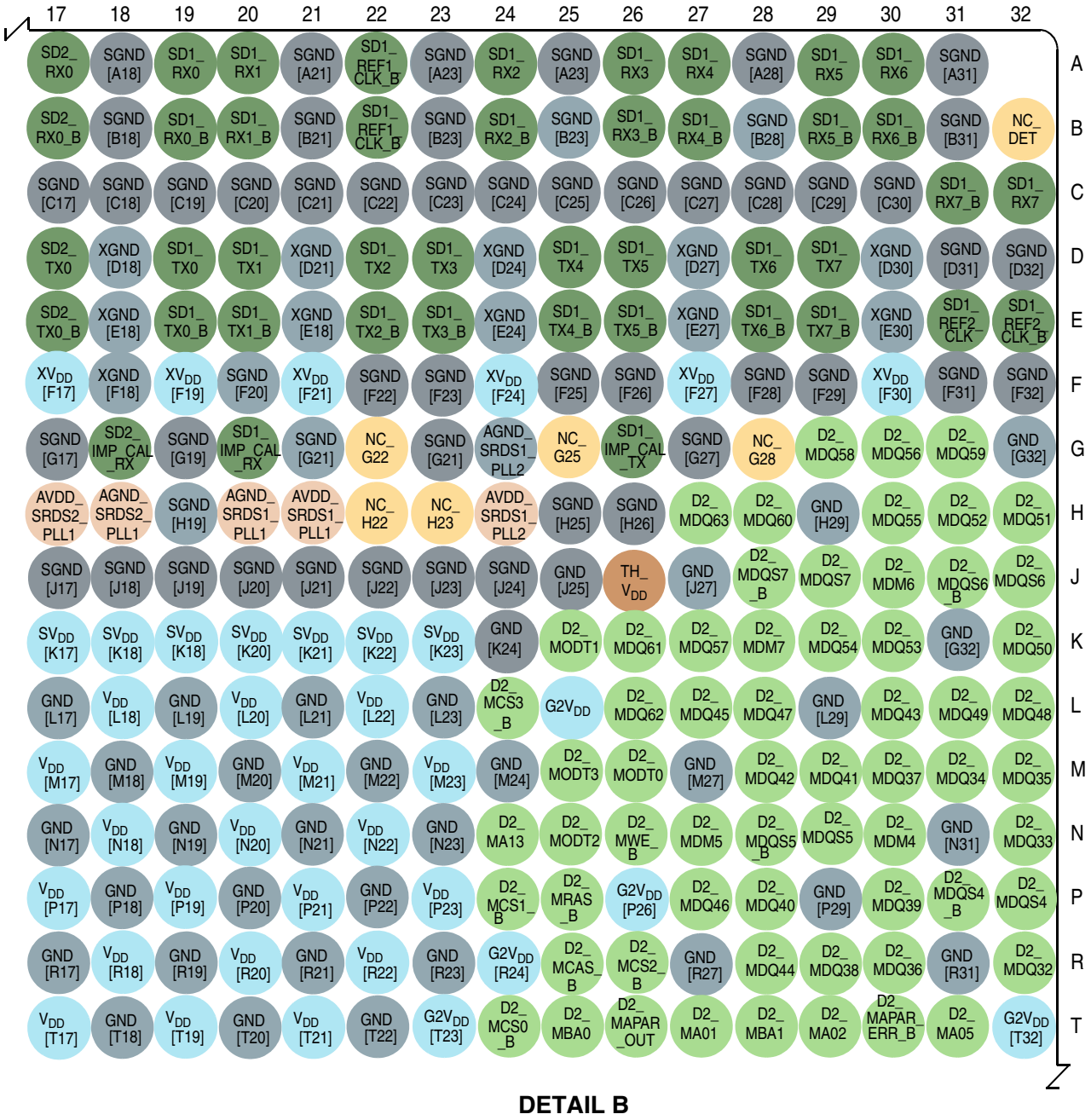


Figure 3. 1020 BGA ball map diagram (detail view A)



DETAIL B

Figure 4. 1020 BGA ball map diagram (detail view B)

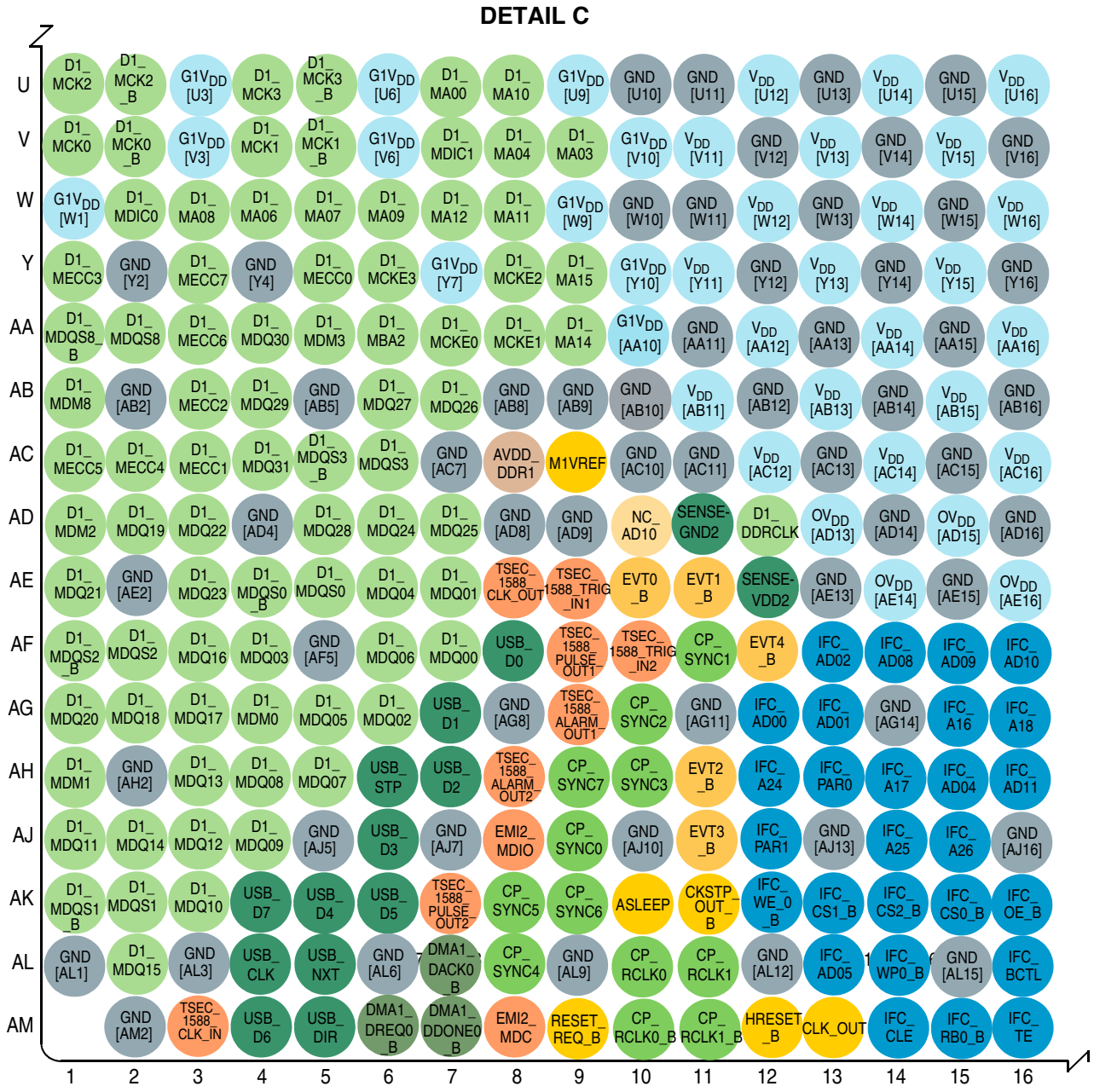


Figure 5. 1020 BGA ball map diagram (detail view C)

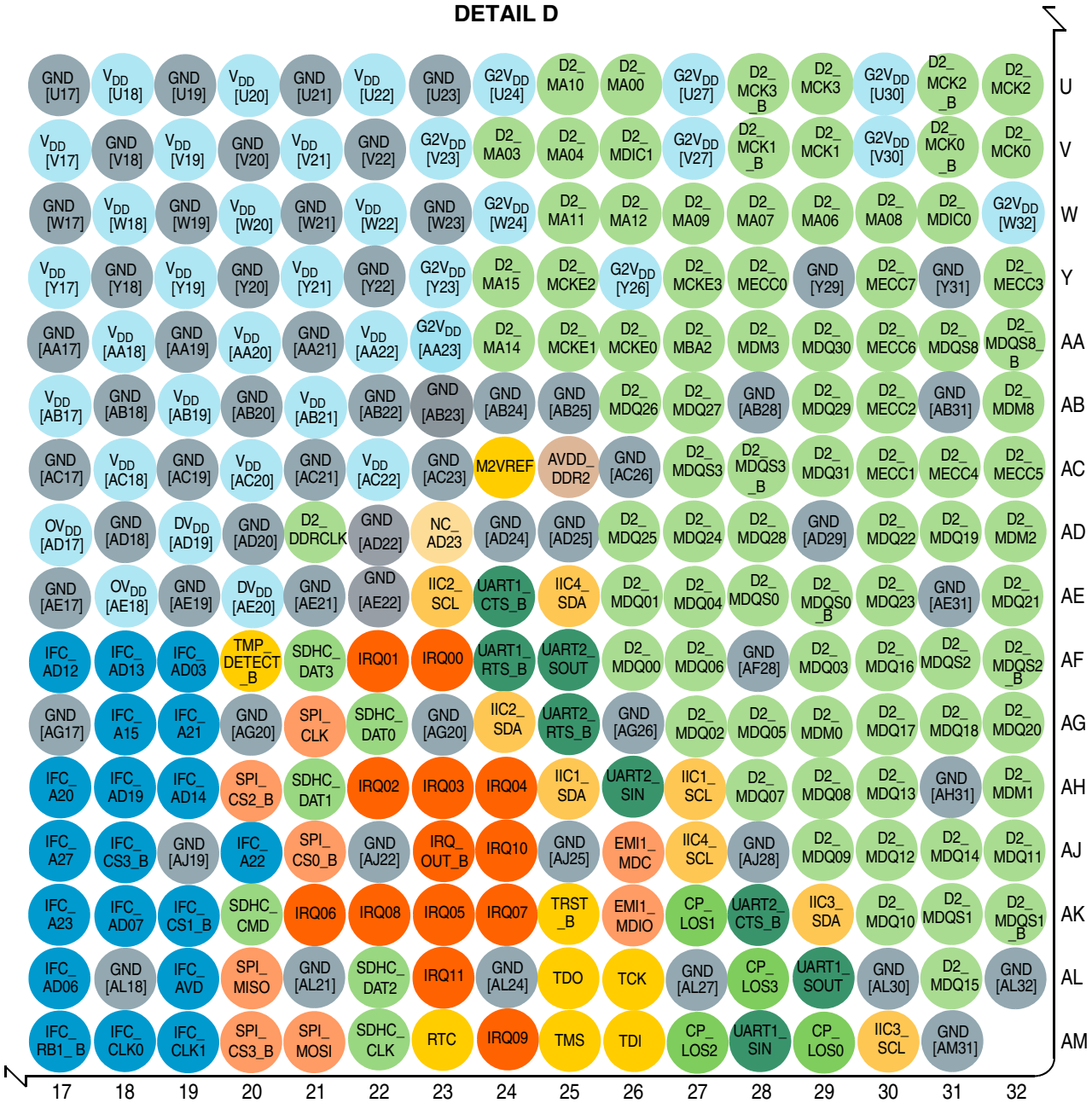


Figure 6. 1020 BGA ball map diagram (detail view D)

1.2 Pinout list by bus

This table provides the pinout list for the chip sorted by bus.

Table 1. Pinout list by bus

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
DDR SDRAM memory Interface 1					
D1_MDQ00	Data	AF7	IO	$G1V_{DD}$	—
D1_MDQ01	Data	AE7	IO	$G1V_{DD}$	—
D1_MDQ02	Data	AG6	IO	$G1V_{DD}$	—
D1_MDQ03	Data	AF4	IO	$G1V_{DD}$	—
D1_MDQ04	Data	AE6	IO	$G1V_{DD}$	—
D1_MDQ05	Data	AG5	IO	$G1V_{DD}$	—
D1_MDQ06	Data	AF6	IO	$G1V_{DD}$	—
D1_MDQ07	Data	AH5	IO	$G1V_{DD}$	—
D1_MDQ08	Data	AH4	IO	$G1V_{DD}$	—
D1_MDQ09	Data	AJ4	IO	$G1V_{DD}$	—
D1_MDQ10	Data	AK3	IO	$G1V_{DD}$	—
D1_MDQ11	Data	AJ1	IO	$G1V_{DD}$	—
D1_MDQ12	Data	AJ3	IO	$G1V_{DD}$	—
D1_MDQ13	Data	AH3	IO	$G1V_{DD}$	—
D1_MDQ14	Data	AJ2	IO	$G1V_{DD}$	—
D1_MDQ15	Data	AL2	IO	$G1V_{DD}$	—
D1_MDQ16	Data	AF3	IO	$G1V_{DD}$	—
D1_MDQ17	Data	AG3	IO	$G1V_{DD}$	—
D1_MDQ18	Data	AG2	IO	$G1V_{DD}$	—
D1_MDQ19	Data	AD2	IO	$G1V_{DD}$	—
D1_MDQ20	Data	AG1	IO	$G1V_{DD}$	—
D1_MDQ21	Data	AE1	IO	$G1V_{DD}$	—
D1_MDQ22	Data	AD3	IO	$G1V_{DD}$	—
D1_MDQ23	Data	AE3	IO	$G1V_{DD}$	—
D1_MDQ24	Data	AD6	IO	$G1V_{DD}$	—
D1_MDQ25	Data	AD7	IO	$G1V_{DD}$	—
D1_MDQ26	Data	AB7	IO	$G1V_{DD}$	—
D1_MDQ27	Data	AB6	IO	$G1V_{DD}$	—
D1_MDQ28	Data	AD5	IO	$G1V_{DD}$	—
D1_MDQ29	Data	AB4	IO	$G1V_{DD}$	—
D1_MDQ30	Data	AA4	IO	$G1V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D1_MDQ31	Data	AC4	IO	$G1V_{DD}$	—
D1_MDQ32	Data	R1	IO	$G1V_{DD}$	—
D1_MDQ33	Data	N1	IO	$G1V_{DD}$	—
D1_MDQ34	Data	M2	IO	$G1V_{DD}$	—
D1_MDQ35	Data	M1	IO	$G1V_{DD}$	—
D1_MDQ36	Data	R3	IO	$G1V_{DD}$	—
D1_MDQ37	Data	M3	IO	$G1V_{DD}$	—
D1_MDQ38	Data	R4	IO	$G1V_{DD}$	—
D1_MDQ39	Data	P3	IO	$G1V_{DD}$	—
D1_MDQ40	Data	P5	IO	$G1V_{DD}$	—
D1_MDQ41	Data	M4	IO	$G1V_{DD}$	—
D1_MDQ42	Data	M5	IO	$G1V_{DD}$	—
D1_MDQ43	Data	L3	IO	$G1V_{DD}$	—
D1_MDQ44	Data	R5	IO	$G1V_{DD}$	—
D1_MDQ45	Data	L6	IO	$G1V_{DD}$	—
D1_MDQ46	Data	P6	IO	$G1V_{DD}$	—
D1_MDQ47	Data	L5	IO	$G1V_{DD}$	—
D1_MDQ48	Data	L1	IO	$G1V_{DD}$	—
D1_MDQ49	Data	L2	IO	$G1V_{DD}$	—
D1_MDQ50	Data	K1	IO	$G1V_{DD}$	—
D1_MDQ51	Data	H1	IO	$G1V_{DD}$	—
D1_MDQ52	Data	H2	IO	$G1V_{DD}$	—
D1_MDQ53	Data	K3	IO	$G1V_{DD}$	—
D1_MDQ54	Data	K4	IO	$G1V_{DD}$	—
D1_MDQ55	Data	H3	IO	$G1V_{DD}$	—
D1_MDQ56	Data	G3	IO	$G1V_{DD}$	—
D1_MDQ57	Data	K6	IO	$G1V_{DD}$	—
D1_MDQ58	Data	G4	IO	$G1V_{DD}$	—
D1_MDQ59	Data	G2	IO	$G1V_{DD}$	—
D1_MDQ60	Data	H5	IO	$G1V_{DD}$	—
D1_MDQ61	Data	K7	IO	$G1V_{DD}$	—
D1_MDQ62	Data	L7	IO	$G1V_{DD}$	—
D1_MDQ63	Data	H6	IO	$G1V_{DD}$	—
D1_MECC0	Error Correcting Code	Y5	IO	$G1V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D1_MECC1	Error Correcting Code	AC3	IO	$G1V_{DD}$	—
D1_MECC2	Error Correcting Code	AB3	IO	$G1V_{DD}$	—
D1_MECC3	Error Correcting Code	Y1	IO	$G1V_{DD}$	—
D1_MECC4	Error Correcting Code	AC2	IO	$G1V_{DD}$	—
D1_MECC5	Error Correcting Code	AC1	IO	$G1V_{DD}$	—
D1_MECC6	Error Correcting Code	AA3	IO	$G1V_{DD}$	—
D1_MECC7	Error Correcting Code	Y3	IO	$G1V_{DD}$	—
D1_MAPAR_ERR_B	Address Parity Error	T3	I	$G1V_{DD}$	2, 26
D1_MAPAR_OUT	Address Parity Out	T7	O	$G1V_{DD}$	—
D1_MDM0	Data Mask	AG4	O	$G1V_{DD}$	2
D1_MDM1	Data Mask	AH1	O	$G1V_{DD}$	2
D1_MDM2	Data Mask	AD1	O	$G1V_{DD}$	2
D1_MDM3	Data Mask	AA5	O	$G1V_{DD}$	2
D1_MDM4	Data Mask	N3	O	$G1V_{DD}$	2
D1_MDM5	Data Mask	N6	O	$G1V_{DD}$	2
D1_MDM6	Data Mask	J3	O	$G1V_{DD}$	2
D1_MDM7	Data Mask	K5	O	$G1V_{DD}$	2
D1_MDM8	Data Mask	AB1	O	$G1V_{DD}$	2
D1_MDQS0	Data Strobe	AE5	IO	$G1V_{DD}$	—
D1_MDQS1	Data Strobe	AK2	IO	$G1V_{DD}$	—
D1_MDQS2	Data Strobe	AF2	IO	$G1V_{DD}$	—
D1_MDQS3	Data Strobe	AC6	IO	$G1V_{DD}$	—
D1_MDQS4	Data Strobe	P1	IO	$G1V_{DD}$	—
D1_MDQS5	Data Strobe	N4	IO	$G1V_{DD}$	—
D1_MDQS6	Data Strobe	J1	IO	$G1V_{DD}$	—
D1_MDQS7	Data Strobe	J4	IO	$G1V_{DD}$	—
D1_MDQS8	Data Strobe	AA2	IO	$G1V_{DD}$	—
D1_MDQS0_B	Data Strobe	AE4	IO	$G1V_{DD}$	—
D1_MDQS1_B	Data Strobe	AK1	IO	$G1V_{DD}$	—
D1_MDQS2_B	Data Strobe	AF1	IO	$G1V_{DD}$	—
D1_MDQS3_B	Data Strobe	AC5	IO	$G1V_{DD}$	—
D1_MDQS4_B	Data Strobe	P2	IO	$G1V_{DD}$	—
D1_MDQS5_B	Data Strobe	N5	IO	$G1V_{DD}$	—
D1_MDQS6_B	Data Strobe	J2	IO	$G1V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D1_MDQS7_B	Data Strobe	J5	IO	$G1V_{DD}$	—
D1_MDQS8_B	Data Strobe	AA1	IO	$G1V_{DD}$	—
D1_MBA0	Bank Select	T8	O	$G1V_{DD}$	—
D1_MBA1	Bank Select	T5	O	$G1V_{DD}$	—
D1_MBA2	Bank Select	AA6	O	$G1V_{DD}$	—
D1_MA00	Address	U7	O	$G1V_{DD}$	—
D1_MA01	Address	T6	O	$G1V_{DD}$	—
D1_MA02	Address	T4	O	$G1V_{DD}$	—
D1_MA03	Address	V9	O	$G1V_{DD}$	—
D1_MA04	Address	V8	O	$G1V_{DD}$	—
D1_MA05	Address	T2	O	$G1V_{DD}$	—
D1_MA06	Address	W4	O	$G1V_{DD}$	—
D1_MA07	Address	W5	O	$G1V_{DD}$	—
D1_MA08	Address	W3	O	$G1V_{DD}$	—
D1_MA09	Address	W6	O	$G1V_{DD}$	—
D1_MA10	Address	U8	O	$G1V_{DD}$	—
D1_MA11	Address	W8	O	$G1V_{DD}$	—
D1_MA12	Address	W7	O	$G1V_{DD}$	—
D1_MA13	Address	N9	O	$G1V_{DD}$	—
D1_MA14	Address	AA9	O	$G1V_{DD}$	—
D1_MA15	Address	Y9	O	$G1V_{DD}$	—
D1_MWE_B	Write Enable	N7	O	$G1V_{DD}$	—
D1_MRAS_B	Row Address Strobe	P8	O	$G1V_{DD}$	—
D1_MCAS_B	Column Address Strobe	R8	O	$G1V_{DD}$	—
D1_MCS0_B	Chip Select	T9	O	$G1V_{DD}$	—
D1_MCS1_B	Chip Select	P9	O	$G1V_{DD}$	—
D1_MCS2_B	Chip Select	R7	O	$G1V_{DD}$	—
D1_MCS3_B	Chip Select	L9	O	$G1V_{DD}$	—
D1_MCKE0	Clock Enable	AA7	O	$G1V_{DD}$	10
D1_MCKE1	Clock Enable	AA8	O	$G1V_{DD}$	10
D1_MCKE2	Clock Enable	Y8	O	$G1V_{DD}$	10
D1_MCKE3	Clock Enable	Y6	O	$G1V_{DD}$	10
D1_MCK0	Clock	V1	O	$G1V_{DD}$	—
D1_MCK1	Clock	V4	O	$G1V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D1_MCK2	Clock	U1	O	$G1V_{DD}$	—
D1_MCK3	Clock	U4	O	$G1V_{DD}$	—
D1_MCK0_B	Clock Complements	V2	O	$G1V_{DD}$	—
D1_MCK1_B	Clock Complements	V5	O	$G1V_{DD}$	—
D1_MCK2_B	Clock Complements	U2	O	$G1V_{DD}$	—
D1_MCK3_B	Clock Complements	U5	O	$G1V_{DD}$	—
D1_DDRCLK	DDR Clock - Controller 1	AD12	I	OV_{DD}	—
D1_MODT0	On Die Termination	M7	O	$G1V_{DD}$	10
D1_MODT1	On Die Termination	K8	O	$G1V_{DD}$	10
D1_MODT2	On Die Termination	N8	O	$G1V_{DD}$	10
D1_MODT3	On Die Termination	M8	O	$G1V_{DD}$	10
D1_MDIC0	Driver Impedance Calibration	W2	IO	$G1V_{DD}$	1
D1_MDIC1	Driver Impedance Calibration	V7	IO	$G1V_{DD}$	1
DDR SDRAM memory Interface 2					
D2_MDQ00	Data	AF26	IO	$G2V_{DD}$	—
D2_MDQ01	Data	AE26	IO	$G2V_{DD}$	—
D2_MDQ02	Data	AG27	IO	$G2V_{DD}$	—
D2_MDQ03	Data	AF29	IO	$G2V_{DD}$	—
D2_MDQ04	Data	AE27	IO	$G2V_{DD}$	—
D2_MDQ05	Data	AG28	IO	$G2V_{DD}$	—
D2_MDQ06	Data	AF27	IO	$G2V_{DD}$	—
D2_MDQ07	Data	AH28	IO	$G2V_{DD}$	—
D2_MDQ08	Data	AH29	IO	$G2V_{DD}$	—
D2_MDQ09	Data	AJ29	IO	$G2V_{DD}$	—
D2_MDQ10	Data	AK30	IO	$G2V_{DD}$	—
D2_MDQ11	Data	AJ32	IO	$G2V_{DD}$	—
D2_MDQ12	Data	AJ30	IO	$G2V_{DD}$	—
D2_MDQ13	Data	AH30	IO	$G2V_{DD}$	—
D2_MDQ14	Data	AJ31	IO	$G2V_{DD}$	—
D2_MDQ15	Data	AL31	IO	$G2V_{DD}$	—
D2_MDQ16	Data	AF30	IO	$G2V_{DD}$	—
D2_MDQ17	Data	AG30	IO	$G2V_{DD}$	—
D2_MDQ18	Data	AG31	IO	$G2V_{DD}$	—
D2_MDQ19	Data	AD31	IO	$G2V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D2_MDQ20	Data	AG32	IO	$G2V_{DD}$	—
D2_MDQ21	Data	AE32	IO	$G2V_{DD}$	—
D2_MDQ22	Data	AD30	IO	$G2V_{DD}$	—
D2_MDQ23	Data	AE30	IO	$G2V_{DD}$	—
D2_MDQ24	Data	AD27	IO	$G2V_{DD}$	—
D2_MDQ25	Data	AD26	IO	$G2V_{DD}$	—
D2_MDQ26	Data	AB26	IO	$G2V_{DD}$	—
D2_MDQ27	Data	AB27	IO	$G2V_{DD}$	—
D2_MDQ28	Data	AD28	IO	$G2V_{DD}$	—
D2_MDQ29	Data	AB29	IO	$G2V_{DD}$	—
D2_MDQ30	Data	AA29	IO	$G2V_{DD}$	—
D2_MDQ31	Data	AC29	IO	$G2V_{DD}$	—
D2_MDQ32	Data	R32	IO	$G2V_{DD}$	—
D2_MDQ33	Data	N32	IO	$G2V_{DD}$	—
D2_MDQ34	Data	M31	IO	$G2V_{DD}$	—
D2_MDQ35	Data	M32	IO	$G2V_{DD}$	—
D2_MDQ36	Data	R30	IO	$G2V_{DD}$	—
D2_MDQ37	Data	M30	IO	$G2V_{DD}$	—
D2_MDQ38	Data	R29	IO	$G2V_{DD}$	—
D2_MDQ39	Data	P30	IO	$G2V_{DD}$	—
D2_MDQ40	Data	P28	IO	$G2V_{DD}$	—
D2_MDQ41	Data	M29	IO	$G2V_{DD}$	—
D2_MDQ42	Data	M28	IO	$G2V_{DD}$	—
D2_MDQ43	Data	L30	IO	$G2V_{DD}$	—
D2_MDQ44	Data	R28	IO	$G2V_{DD}$	—
D2_MDQ45	Data	L27	IO	$G2V_{DD}$	—
D2_MDQ46	Data	P27	IO	$G2V_{DD}$	—
D2_MDQ47	Data	L28	IO	$G2V_{DD}$	—
D2_MDQ48	Data	L32	IO	$G2V_{DD}$	—
D2_MDQ49	Data	L31	IO	$G2V_{DD}$	—
D2_MDQ50	Data	K32	IO	$G2V_{DD}$	—
D2_MDQ51	Data	H32	IO	$G2V_{DD}$	—
D2_MDQ52	Data	H31	IO	$G2V_{DD}$	—
D2_MDQ53	Data	K30	IO	$G2V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D2_MDQ54	Data	K29	IO	$G2V_{DD}$	—
D2_MDQ55	Data	H30	IO	$G2V_{DD}$	—
D2_MDQ56	Data	G30	IO	$G2V_{DD}$	—
D2_MDQ57	Data	K27	IO	$G2V_{DD}$	—
D2_MDQ58	Data	G29	IO	$G2V_{DD}$	—
D2_MDQ59	Data	G31	IO	$G2V_{DD}$	—
D2_MDQ60	Data	H28	IO	$G2V_{DD}$	—
D2_MDQ61	Data	K26	IO	$G2V_{DD}$	—
D2_MDQ62	Data	L26	IO	$G2V_{DD}$	—
D2_MDQ63	Data	H27	IO	$G2V_{DD}$	—
D2_MECC0	Error Correcting Code	Y28	IO	$G2V_{DD}$	—
D2_MECC1	Error Correcting Code	AC30	IO	$G2V_{DD}$	—
D2_MECC2	Error Correcting Code	AB30	IO	$G2V_{DD}$	—
D2_MECC3	Error Correcting Code	Y32	IO	$G2V_{DD}$	—
D2_MECC4	Error Correcting Code	AC31	IO	$G2V_{DD}$	—
D2_MECC5	Error Correcting Code	AC32	IO	$G2V_{DD}$	—
D2_MECC6	Error Correcting Code	AA30	IO	$G2V_{DD}$	—
D2_MECC7	Error Correcting Code	Y30	IO	$G2V_{DD}$	—
D2_MAPAR_ERR_B	Address Parity Error	T30	I	$G2V_{DD}$	26
D2_MAPAR_OUT	Address Parity Out	T26	O	$G2V_{DD}$	2
D2_MDM0	Data Mask	AG29	O	$G2V_{DD}$	2
D2_MDM1	Data Mask	AH32	O	$G2V_{DD}$	2
D2_MDM2	Data Mask	AD32	O	$G2V_{DD}$	2
D2_MDM3	Data Mask	AA28	O	$G2V_{DD}$	2
D2_MDM4	Data Mask	N30	O	$G2V_{DD}$	2
D2_MDM5	Data Mask	N27	O	$G2V_{DD}$	2
D2_MDM6	Data Mask	J30	O	$G2V_{DD}$	2
D2_MDM7	Data Mask	K28	O	$G2V_{DD}$	2
D2_MDM8	Data Mask	AB32	O	$G2V_{DD}$	2
D2_MDQS0	Data Strobe	AE28	IO	$G2V_{DD}$	—
D2_MDQS1	Data Strobe	AK31	IO	$G2V_{DD}$	—
D2_MDQS2	Data Strobe	AF31	IO	$G2V_{DD}$	—
D2_MDQS3	Data Strobe	AC27	IO	$G2V_{DD}$	—
D2_MDQS4	Data Strobe	P32	IO	$G2V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D2_MDQS5	Data Strobe	N29	IO	$G2V_{DD}$	—
D2_MDQS6	Data Strobe	J32	IO	$G2V_{DD}$	—
D2_MDQS7	Data Strobe	J29	IO	$G2V_{DD}$	—
D2_MDQS8	Data Strobe	AA31	IO	$G2V_{DD}$	—
D2_MDQS0_B	Data Strobe	AE29	IO	$G2V_{DD}$	—
D2_MDQS1_B	Data Strobe	AK32	IO	$G2V_{DD}$	—
D2_MDQS2_B	Data Strobe	AF32	IO	$G2V_{DD}$	—
D2_MDQS3_B	Data Strobe	AC28	IO	$G2V_{DD}$	—
D2_MDQS4_B	Data Strobe	P31	IO	$G2V_{DD}$	—
D2_MDQS5_B	Data Strobe	N28	IO	$G2V_{DD}$	—
D2_MDQS6_B	Data Strobe	J31	IO	$G2V_{DD}$	—
D2_MDQS7_B	Data Strobe	J28	IO	$G2V_{DD}$	—
D2_MDQS8_B	Data Strobe	AA32	IO	$G2V_{DD}$	—
D2_MBA0	Bank Select	T25	O	$G2V_{DD}$	—
D2_MBA1	Bank Select	T28	O	$G2V_{DD}$	—
D2_MBA2	Bank Select	AA27	O	$G2V_{DD}$	—
D2_MA00	Address	U26	O	$G2V_{DD}$	—
D2_MA01	Address	T27	O	$G2V_{DD}$	—
D2_MA02	Address	T29	O	$G2V_{DD}$	—
D2_MA03	Address	V24	O	$G2V_{DD}$	—
D2_MA04	Address	V25	O	$G2V_{DD}$	—
D2_MA05	Address	T31	O	$G2V_{DD}$	—
D2_MA06	Address	W29	O	$G2V_{DD}$	—
D2_MA07	Address	W28	O	$G2V_{DD}$	—
D2_MA08	Address	W30	O	$G2V_{DD}$	—
D2_MA09	Address	W27	O	$G2V_{DD}$	—
D2_MA10	Address	U25	O	$G2V_{DD}$	—
D2_MA11	Address	W25	O	$G2V_{DD}$	—
D2_MA12	Address	W26	O	$G2V_{DD}$	—
D2_MA13	Address	N24	O	$G2V_{DD}$	—
D2_MA14	Address	AA24	O	$G2V_{DD}$	—
D2_MA15	Address	Y24	O	$G2V_{DD}$	—
D2_MWE_B	Write Enable	N26	O	$G2V_{DD}$	—
D2_MRAS_B	Row Address Strobe	P25	O	$G2V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
D2_MCAS_B	Column Address Strobe	R25	O	$G2V_{DD}$	—
D2_MCS0_B	Chip Select	T24	O	$G2V_{DD}$	—
D2_MCS1_B	Chip Select	P24	O	$G2V_{DD}$	—
D2_MCS2_B	Chip Select	R26	O	$G2V_{DD}$	—
D2_MCS3_B	Chip Select	L24	O	$G2V_{DD}$	—
D2_MCKE0	Clock Enable	AA26	O	$G2V_{DD}$	10
D2_MCKE1	Clock Enable	AA25	O	$G2V_{DD}$	10
D2_MCKE2	Clock Enable	Y25	O	$G2V_{DD}$	10
D2_MCKE3	Clock Enable	Y27	O	$G2V_{DD}$	10
D2_MCK0	Clock	V32	O	$G2V_{DD}$	—
D2_MCK1	Clock	V29	O	$G2V_{DD}$	—
D2_MCK2	Clock	U32	O	$G2V_{DD}$	—
D2_MCK3	Clock	U29	O	$G2V_{DD}$	—
D2_MCK0_B	Clock Complements	V31	O	$G2V_{DD}$	—
D2_MCK1_B	Clock Complements	V28	O	$G2V_{DD}$	—
D2_MCK2_B	Clock Complements	U31	O	$G2V_{DD}$	—
D2_MCK3_B	Clock Complements	U28	O	$G2V_{DD}$	—
D2_DDRCLK	DDR Clock–Controller 2	AD21	I	OV_{DD}	—
D2_MODT0	On Die Termination	M26	O	$G2V_{DD}$	10
D2_MODT1	On Die Termination	K25	O	$G2V_{DD}$	10
D2_MODT2	On Die Termination	N25	O	$G2V_{DD}$	10
D2_MODT3	On Die Termination	M25	O	$G2V_{DD}$	10
D2_MDIC0	Driver Impedance Calibration	W31	IO	$G2V_{DD}$	1
D2_MDIC1	Driver Impedance Calibration	V26	IO	$G2V_{DD}$	1
Integrated Flash Controller Interface					
IFC_AD00/CFG_GPINPUT0	Muxed Data/Address	AG12	IO	OV_{DD}	22
IFC_AD01/CFG_GPINPUT1	Muxed Data/Address	AG13	IO	OV_{DD}	22
IFC_AD02/CFG_GPINPUT2	Muxed Data/Address	AF13	IO	OV_{DD}	22
IFC_AD03/CFG_GPINPUT3	Muxed Data/Address	AF19	IO	OV_{DD}	22
IFC_AD04/CFG_GPINPUT4	Muxed Data/Address	AH15	IO	OV_{DD}	22
IFC_AD05/CFG_GPINPUT5	Muxed Data/Address	AL13	IO	OV_{DD}	22
IFC_AD06/CFG_GPINPUT6	Muxed Data/Address	AL17	IO	OV_{DD}	22
IFC_AD07/CFG_GPINPUT7	Muxed Data/Address	AK18	IO	OV_{DD}	22
IFC_AD08/CFG_RCW_SRC0	Muxed Data/Address	AF14	IO	OV_{DD}	22

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
IFC_AD09/CFG_RCW_SRC1	Muxed Data/Address	AF15	IO	OV_{DD}	22
IFC_AD10/CFG_RCW_SRC2	Muxed Data/Address	AF16	IO	OV_{DD}	22
IFC_AD11/CFG_RCW_SRC3	Muxed Data/Address	AH16	IO	OV_{DD}	22
IFC_AD12/CFG_RCW_SRC4	Muxed Data/Address	AF17	IO	OV_{DD}	22
IFC_AD13/CFG_RCW_SRC5	Muxed Data/Address	AF18	IO	OV_{DD}	22
IFC_AD14/CFG_RCW_SRC6	Muxed Data/Address	AH19	IO	OV_{DD}	22
IFC_AD15/CFG_RCW_SRC7	Muxed Data/Address	AG18	IO	OV_{DD}	22
IFC_A16	Address	AG15	O	OV_{DD}	2, 8
IFC_A17	Address	AH14	O	OV_{DD}	2, 8
IFC_A18	Address	AG16	O	OV_{DD}	2, 8
IFC_A19	Address	AH18	O	OV_{DD}	2, 8
IFC_A20	Address	AH17	O	OV_{DD}	2, 8
IFC_A21/CFG_DRAM_TYPE	Address	AG19	O	OV_{DD}	2, 22, 23
IFC_A22/IFC_WP1_B	Address	AJ20	O	OV_{DD}	2,
IFC_A23/IFC_WP2_B	Address	AK17	O	OV_{DD}	2,
IFC_A24/IFC_WP3_B	Address	AH12	O	OV_{DD}	2,
IFC_A25/GPIO2[25]/ IFC_RB2_B/IFC_FCTA2	Address	AJ14	O	OV_{DD}	2
IFC_A26/GPIO2[26]/ IFC_RB3_B/IFC_FCTA3	Address	AJ15	O	OV_{DD}	2
IFC_A27/GPIO2[27]	Address	AJ17	O	OV_{DD}	2
IFC_PAR0/GPIO2[13]	Data Parity / Address and Data Parity for byte 0	AH13	IO	OV_{DD}	—
IFC_PAR1/GPIO2[14]	Data Parity / Address and Data Parity for byte 1	AJ12	IO	OV_{DD}	—
IFC_CS0_B	Chip Select	AK15	O	OV_{DD}	2, 27
IFC_CS1_B/GPIO2[10]	Chip Select	AK13	O	OV_{DD}	2, 27
IFC_CS2_B/GPIO2[11]	Chip Select	AK14	O	OV_{DD}	2, 27
IFC_CS3_B/GPIO2[12]	Chip Select	AJ18	O	OV_{DD}	2, 27
IFC_WE_B/IFC_WBE0	Write Enable (NAND/NOR)	AK12	IO	OV_{DD}	2, 8
IFC_WE_B/**IFC_WBE0**	Write byte 0 enable (GPCM)	AK12	IO	OV_{DD}	2, 8
IFC_CLE/**IFC_WBE1**/ CFG_RCW_SRC8	Write byte 1 enable (GPCM)	AM14	IO	OV_{DD}	22
IFC_BCTL	External Buffer control	AL16	O	OV_{DD}	2
IFC_TE/CFG_IFC_TE	External Transceiver Enable	AM16	O	OV_{DD}	2, 22, 25

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
IFC_AVD/**IFC_ALE**/ CFG_RSP_DIS	Address Latch Enable–NAND/NOR & GPCM (NAND)	AL19	IO	OV_{DD}	22, 15
IFC_AVD/IFC_ALE/ CFG_RSP_DIS	Address Valid Data for internal latched based NOR	AL19	IO	OV_{DD}	22, 15
IFC_CLE/IFC_WBE1/ CFG_RCW_SRC8	Command Latch Enable (NAND)	AM14	IO	OV_{DD}	22
IFC_OE_B/IFC_RE_B	Output Enable–NOR & GPCM	AK16	IO	OV_{DD}	8
IFC_OE_B/**IFC_RE_B**	Read Enable–NAND	AK16	IO	OV_{DD}	8
IFC_WP0_B	NAND write protect signal 0	AL14	O	OV_{DD}	8
IFC_A22/**IFC_WP1_B**	NAND write protect signal 1	AJ20	IO	OV_{DD}	—
IFC_A23/**IFC_WP2_B**	NAND write protect signal 2	AK17	IO	OV_{DD}	—
IFC_A24/**IFC_WP3_B**	NAND write protect signal 3	AH12	IO	OV_{DD}	—
IFC_RB0_B/IFC_FCTA0	CS0: NAND/NOR Flash Ready Busy	AM15	I	OV_{DD}	2, 28
IFC_RB1_B/IFC_FCTA1	CS1: NAND/NOR Flash Ready Busy	AM17	I	OV_{DD}	2, 28
IFC_A25/GPIO2[25]/ **IFC_RB2_B**/IFC_FCTA2	CS2: NAND/NOR Flash Ready Busy	AJ14	I	OV_{DD}	2
IFC_A26/GPIO2[26]/ **IFC_RB3_B**/IFC_FCTA3	CS3: NAND/NOR Flash Ready Busy	AJ15	I	OV_{DD}	2
IFC_RB0_B/**IFC_FCTA0**	CS0: GPCM External Access Termination	AM15	I	OV_{DD}	2, 28
IFC_RB1_B/**IFC_FCTA1**	CS1: GPCM External Access Termination	AM17	I	OV_{DD}	2, 28
IFC_A25/GPIO2[25]/ IFC_RB2_B/**IFC_FCTA2**	CS2: GPCM External Access Termination	AJ14	I	OV_{DD}	2
IFC_A26/GPIO2[26]/ IFC_RB3_B/**IFC_FCTA3**	CS3: GPCM External Access Termination	AJ15	I	OV_{DD}	2
IFC_CLK0	Clock	AM18	O	OV_{DD}	2
IFC_CLK1	Clock	AM19	O	OV_{DD}	2
DUART Interface					
UART1_SOUT/GPIO1[15]/ CP_LOS4	Transmit Data	AL29	O	DV_{DD}	2
UART1_SIN/GPIO1[17]/ CP_LOS5	Receive Data	AM28	I	DV_{DD}	2
UART1_RTS_B/GPIO1[19]/ UART3_SOUT/CP_LOS6	Ready to Send	AF24	O	DV_{DD}	2
UART1_CTS_B/GPIO1[21]/ UART3_SIN/CP_LOS7	Clear to Send	AE24	I	DV_{DD}	2

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
UART2_SOUT/GPIO1[16]	Transmit Data	AF25	O	DV_{DD}	2
UART2_SIN/GPIO1[18]	Receive Data	AH26	I	DV_{DD}	2
UART2_RTS_B/GPIO1[20]/ UART4_SOUT	Ready to Send	AG25	O	DV_{DD}	2
UART2_CTS_B/GPIO1[22]/ UART4_SIN	Clear to Send	AK28	I	DV_{DD}	2
UART1_RTS_B/GPIO1[19]/ **UART3_SOUT**/CP_LOS6	Transmit Data	AF24	O	DV_{DD}	2
UART1_CTS_B/GPIO1[21]/ **UART3_SIN**/CP_LOS7	Receive Data	AE24	I	DV_{DD}	2
UART2_RTS_B/GPIO1[20]/ **UART4_SOUT**	Transmit Data	AG25	O	DV_{DD}	2
UART2_CTS_B/GPIO1[22]/ **UART4_SIN**	Receive Data	AK28	I	DV_{DD}	2
I2C Interface					
IIC1_SCL	Serial Clock (supports PBL)	AH27	IO	DV_{DD}	4
IIC1_SDA	Serial Data (supports PBL)	AH25	IO	DV_{DD}	4
IIC2_SCL	Serial Clock	AE23	IO	DV_{DD}	4
IIC2_SDA	Serial Data	AG24	IO	DV_{DD}	4
IIC3_SCL/GPIO3[3]	Serial Clock	AM30	IO	DV_{DD}	4
IIC3_SDA/GPIO3[4]	Serial Data	AK29	IO	DV_{DD}	4
IIC4_SCL/GPIO3[5]/EVT5_B	Serial Clock	AJ27	IO	DV_{DD}	4
IIC4_SDA/GPIO3[6]/EVT6_B/ USB_PWRFAULT	Serial Data	AE25	IO	DV_{DD}	4
eSPI Interface					
SPI_MOSI	Master Out Slave In	AM21	IO	OV_{DD}	—
SPI_MISO	Master In Slave Out	AL20	I	OV_{DD}	—
SPI_CLK	Clock	AG21	O	OV_{DD}	2
SPI_CS0_B/GPIO2[0]/ SDHC_DAT4	Chip Select	AJ21	O	OV_{DD}	2
SPI_CS1_B/GPIO2[1]/ SDHC_DAT5	Chip Select	AK19	O	OV_{DD}	2
SPI_CS2_B/GPIO2[2]/ SDHC_DAT6	Chip Select	AH20	O	OV_{DD}	2
SPI_CS3_B/GPIO2[3]/ SDHC_DAT7	Chip Select	AM20	O	OV_{DD}	2
eSDHC Interface					

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SDHC_CMD/GPIO2[4]	Command/Response	AK20	IO	OV_{DD}	32
SDHC_DAT0/GPIO2[5]	Data	AG22	IO	OV_{DD}	32
SDHC_DAT1/GPIO2[6]	Data	AH21	IO	OV_{DD}	32
SDHC_DAT2/GPIO2[7]	Data	AL22	IO	OV_{DD}	32
SDHC_DAT3/GPIO2[8]	Data	AF21	IO	OV_{DD}	32
SPI_CS0_B/GPIO2[0]/ **SDHC_DAT4**	Data	AJ21	IO	OV_{DD}	32
SPI_CS1_B/GPIO2[1]/ **SDHC_DAT5**	Data	AK19	IO	OV_{DD}	32
SPI_CS2_B/GPIO2[2]/ **SDHC_DAT6**	Data	AH20	IO	OV_{DD}	32
SPI_CS3_B/GPIO2[3]/ **SDHC_DAT7**	Data	AM20	IO	OV_{DD}	32
SDHC_CLK/GPIO2[9]	Host to Card Clock	AM22	O	OV_{DD}	2
Programmable Interrupt Controller Interface					
IRQ00	External Interrupts	AF23	I	OV_{DD}	2
IRQ01	External Interrupts	AF22	I	OV_{DD}	2
IRQ02	External Interrupts	AH22	I	OV_{DD}	2
IRQ03/GPIO1[23]	External Interrupts	AH23	I	OV_{DD}	2
IRQ04/GPIO1[24]	External Interrupts	AH24	I	OV_{DD}	2
IRQ05/GPIO1[25]	External Interrupts	AK23	I	OV_{DD}	2
IRQ06/GPIO1[26]/TMR0	External Interrupts	AK21	I	OV_{DD}	2
IRQ07/GPIO1[27]/TMR1	External Interrupts	AK24	I	OV_{DD}	2
IRQ08/GPIO1[28]/TMR2	External Interrupts	AK22	I	OV_{DD}	2
IRQ09/GPIO1[29]/TMR3	External Interrupts	AM24	I	OV_{DD}	2
IRQ10/GPIO1[30]/TMR4	External Interrupts	AJ24	I	OV_{DD}	2
IRQ11/GPIO1[31]/TMR5	External Interrupts	AL23	I	OV_{DD}	2
IRQ_OUT_B/EVT9_B	Interrupt Output	AJ23	O	OV_{DD}	2, 5
Trust					
TMP_DETECT_B	Tamper Detect	AF20	I	OV_{DD}	2, 6
System Control					
PORESET_B	Power On Reset	E1	I	QV_{DD}	7
HRESET_B	Hard Reset	AM12	IO	OV_{DD}	3
RESET_REQ_B	Reset Request (POR or Hard)	AM9	O	OV_{DD}	2, 8
Power Management					

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
ASLEEP/GPIO1[13]/CFG_XVDD_SEL	Asleep	AK10	O	OV_{DD}	2, 22, 24
Clock Signals					
SYSCLK	System Clock	F1	I	QV_{DD}	7
RTC/GPIO1[14]	Real Time Clock	AM23	I	OV_{DD}	2
Debug Signals					
EVT0_B	Event 0	AE10	I	OV_{DD}	9
EVT1_B	Event 1	AE11	IO	OV_{DD}	—
EVT2_B	Event 2	AH11	IO	OV_{DD}	—
EVT3_B	Event 3	AJ11	IO	OV_{DD}	—
EVT4_B	Event 4	AF12	IO	OV_{DD}	—
IIC4_SCL/GPIO3[5]/**EVT5_B**	Event 5	AJ27	IO	DV_{DD}	—
IIC4_SDA/GPIO3[6]/**EVT6_B**/USB_PWRFAULT	Event 6	AE25	IO	DV_{DD}	—
DMA1_DACK0_B/GPIO3[1]/**EVT7_B**/TMR6	Event 7	AL7	IO	OV_{DD}	—
DMA1_DDONE0_B/GPIO3[2]/**EVT8_B**/TMR7	Event 8	AM7	IO	OV_{DD}	—
IRQ_OUT_B/**EVT9_B**	Event 9	AJ23	IO	OV_{DD}	—
CKSTP_OUT_B	Checkstop Out	AK11	O	OV_{DD}	2, 3
CLK_OUT	Clock Out	AM13	O	OV_{DD}	10
JTAG Signals					
TCK	Test Clock	AL26	I	OV_{DD}	—
TDI	Test Data In	AM26	I	OV_{DD}	9
TDO	Test Data Out	AL25	O	OV_{DD}	10
TMS	Test Mode Select	AM25	I	OV_{DD}	9
TRST_B	Test Reset	AK25	I	OV_{DD}	9
SerDes 1 (x8) CPRI, Aurora, 1GE, 2.5GE					
SD1_TX0	SerDes Tx Data (pos)	D19	O	XV_{DD}	—
SD1_TX1	SerDes Tx Data (pos)	D20	O	XV_{DD}	—
SD1_TX2	SerDes Tx Data (pos)	D22	O	XV_{DD}	—
SD1_TX3	SerDes Tx Data (pos)	D23	O	XV_{DD}	—
SD1_TX4	SerDes Tx Data (pos)	D25	O	XV_{DD}	—
SD1_TX5	SerDes Tx Data (pos)	D26	O	XV_{DD}	—
SD1_TX6	SerDes Tx Data (pos)	D28	O	XV_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SD1_TX7	SerDes Tx Data (pos)	D29	O	XV_{DD}	—
SD1_TX0_B	SerDes Tx Data (neg)	E19	O	XV_{DD}	—
SD1_TX1_B	SerDes Tx Data (neg)	E20	O	XV_{DD}	—
SD1_TX2_B	SerDes Tx Data (neg)	E22	O	XV_{DD}	—
SD1_TX3_B	SerDes Tx Data (neg)	E23	O	XV_{DD}	—
SD1_TX4_B	SerDes Tx Data (neg)	E25	O	XV_{DD}	—
SD1_TX5_B	SerDes Tx Data (neg)	E26	O	XV_{DD}	—
SD1_TX6_B	SerDes Tx Data (neg)	E28	O	XV_{DD}	—
SD1_TX7_B	SerDes Tx Data (neg)	E29	O	XV_{DD}	—
SD1_RX0	SerDes Rx Data (pos)	A19	I	SV_{DD}	—
SD1_RX1	SerDes Rx Data (pos)	A20	I	SV_{DD}	—
SD1_RX2	SerDes Rx Data (pos)	A24	I	SV_{DD}	—
SD1_RX3	SerDes Rx Data (pos)	A26	I	SV_{DD}	—
SD1_RX4	SerDes Rx Data (pos)	A27	I	SV_{DD}	—
SD1_RX5	SerDes Rx Data (pos)	A29	I	SV_{DD}	—
SD1_RX6	SerDes Rx Data (pos)	A30	I	SV_{DD}	—
SD1_RX7	SerDes Rx Data (pos)	C32	I	SV_{DD}	—
SD1_RX0_B	SerDes Rx Data (neg)	B19	I	SV_{DD}	—
SD1_RX1_B	SerDes Rx Data (neg)	B20	I	SV_{DD}	—
SD1_RX2_B	SerDes Rx Data (neg)	B24	I	SV_{DD}	—
SD1_RX3_B	SerDes Rx Data (neg)	B26	I	SV_{DD}	—
SD1_RX4_B	SerDes Rx Data (neg)	B27	I	SV_{DD}	—
SD1_RX5_B	SerDes Rx Data (neg)	B29	I	SV_{DD}	—
SD1_RX6_B	SerDes Rx Data (neg)	B30	I	SV_{DD}	—
SD1_RX7_B	SerDes Rx Data (neg)	C31	I	SV_{DD}	—
SD1_REF1_CLK	SerDes PLL 1 Reference Clock	B22	I	SV_{DD}	—
SD1_REF1_CLK_B	SerDes PLL 1 Reference Clock Complement	A22	I	SV_{DD}	—
SD1_REF2_CLK	SerDes PLL 2 Reference Clock	E31	I	SV_{DD}	—
SD1_REF2_CLK_B	SerDes PLL 2 Reference Clock Complement	E32	I	SV_{DD}	—
SD1_IMP_CAL_TX	SerDes Tx Impedance Calibration	G26	I	XV_{DD}	11

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SD1_IMP_CAL_RX	SerDes Rx Impedance Calibration	G20	I	SV_{DD}	12
SerDes 2 (x8) PCIe, sRIO, Aurora, 10GE, 1GE, 2.5GE					
SD2_TX0	SerDes Tx Data (pos)	D17	O	XV_{DD}	—
SD2_TX1	SerDes Tx Data (pos)	D16	O	XV_{DD}	—
SD2_TX2	SerDes Tx Data (pos)	D14	O	XV_{DD}	—
SD2_TX3	SerDes Tx Data (pos)	D13	O	XV_{DD}	—
SD2_TX4	SerDes Tx Data (pos)	D11	O	XV_{DD}	—
SD2_TX5	SerDes Tx Data (pos)	D10	O	XV_{DD}	—
SD2_TX6	SerDes Tx Data (pos)	D8	O	XV_{DD}	—
SD2_TX7	SerDes Tx Data (pos)	D7	O	XV_{DD}	—
SD2_TX0_B	SerDes Tx Data (neg)	E17	O	XV_{DD}	—
SD2_TX1_B	SerDes Tx Data (neg)	E16	O	XV_{DD}	—
SD2_TX2_B	SerDes Tx Data (neg)	E14	O	XV_{DD}	—
SD2_TX3_B	SerDes Tx Data (neg)	E13	O	XV_{DD}	—
SD2_TX4_B	SerDes Tx Data (neg)	E11	O	XV_{DD}	—
SD2_TX5_B	SerDes Tx Data (neg)	E10	O	XV_{DD}	—
SD2_TX6_B	SerDes Tx Data (neg)	E8	O	XV_{DD}	—
SD2_TX7_B	SerDes Tx Data (neg)	E7	O	XV_{DD}	—
SD2_RX0	SerDes Rx Data (pos)	A17	I	SV_{DD}	—
SD2_RX1	SerDes Rx Data (pos)	A16	I	SV_{DD}	—
SD2_RX2	SerDes Rx Data (pos)	A12	I	SV_{DD}	—
SD2_RX3	SerDes Rx Data (pos)	A11	I	SV_{DD}	—
SD2_RX4	SerDes Rx Data (pos)	A9	I	SV_{DD}	—
SD2_RX5	SerDes Rx Data (pos)	A8	I	SV_{DD}	—
SD2_RX6	SerDes Rx Data (pos)	A6	I	SV_{DD}	—
SD2_RX7	SerDes Rx Data (pos)	A5	I	SV_{DD}	—
SD2_RX0_B	SerDes Rx Data (neg)	B17	I	SV_{DD}	—
SD2_RX1_B	SerDes Rx Data (neg)	B16	I	SV_{DD}	—
SD2_RX2_B	SerDes Rx Data (neg)	B12	I	SV_{DD}	—
SD2_RX3_B	SerDes Rx Data (neg)	B11	I	SV_{DD}	—
SD2_RX4_B	SerDes Rx Data (neg)	B9	I	SV_{DD}	—
SD2_RX5_B	SerDes Rx Data (neg)	B8	I	SV_{DD}	—
SD2_RX6_B	SerDes Rx Data (neg)	B6	I	SV_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SD2_RX7_B	SerDes Rx Data (neg)	B5	I	SV_{DD}	—
SD2_REF1_CLK	SerDes PLL 1 Reference Clock	B14	I	SV_{DD}	—
SD2_REF1_CLK_B	SerDes PLL 1 Reference Clock Complement	A14	I	SV_{DD}	—
SD2_REF2_CLK	SerDes PLL 2 Reference Clock	E5	I	SV_{DD}	—
SD2_REF2_CLK_B	SerDes PLL 2 Reference Clock Complement	D5	I	SV_{DD}	—
SD2_IMP_CAL_TX	SerDes Tx Impedance Calibration	G10	I	XV_{DD}	11
SD2_IMP_CAL_RX	SerDes Rx Impedance Calibration	G18	I	SV_{DD}	12
CPRI Interface					
CP_SYNC0	Sync	AJ9	IO	OV_{DD}	—
CP_SYNC1	Sync	AF11	IO	OV_{DD}	—
CP_SYNC2	Sync	AG10	IO	OV_{DD}	—
CP_SYNC3	Sync	AH10	IO	OV_{DD}	—
CP_SYNC4	Sync	AL8	IO	OV_{DD}	—
CP_SYNC5	Sync	AK8	IO	OV_{DD}	—
CP_SYNC6	Sync	AK9	IO	OV_{DD}	—
CP_SYNC7	Sync	AH9	IO	OV_{DD}	—
CP_RCLK0	Reconstructed Clock	AL10	O	OV_{DD}	2
CP_RCLK1	Reconstructed Clock	AL11	O	OV_{DD}	2
CP_RCLK0_B	Reconstructed Clock Complement	AM10	O	OV_{DD}	2
CP_RCLK1_B	Reconstructed Clock Complement	AM11	O	OV_{DD}	2
CP_LOS0	Loss Of Signal	AM29	I	DV_{DD}	2, 29
CP_LOS1	Loss Of Signal	AK27	I	DV_{DD}	2, 29
CP_LOS2	Loss Of Signal	AM27	I	DV_{DD}	2, 29
CP_LOS3	Loss Of Signal	AL28	I	DV_{DD}	2, 29
UART1_SOUT/GPIO1[15]/ **CP_LOS4**	Loss Of Signal	AL29	I	DV_{DD}	2, 30
UART1_SIN/GPIO1[17]/ **CP_LOS5**	Loss Of Signal	AM28	I	DV_{DD}	2, 30
UART1_RTS_B/GPIO1[19]/ UART3_SOUT/**CP_LOS6**	Loss Of Signal	AF24	I	DV_{DD}	2, 30

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
UART1_CTS_B/GPIO1[21]/ UART3_SIN/**CP_LOS7**	Loss Of Signal	AE24	I	DV_{DD}	2, 30
IEEE 1588 Interface					
TSEC_1588_CLK_IN	Clock In	AM3	I	OV_{DD}	2
TSEC_1588_TRIG_IN1	Trigger In 1	AE9	I	OV_{DD}	2
TSEC_1588_TRIG_IN2	Trigger In 2	AF10	I	OV_{DD}	2
TSEC_1588_ALARM_OUT1	Alarm Out 1	AG9	O	OV_{DD}	2
TSEC_1588_ALARM_OUT2	Alarm Out 2	AH8	O	OV_{DD}	2
TSEC_1588_CLK_OUT	Clock Out	AE8	O	OV_{DD}	2
TSEC_1588_PULSE_OUT1	Pulse Out 1	AF9	O	OV_{DD}	2
TSEC_1588_PULSE_OUT2	Pulse Out 2	AK7	O	OV_{DD}	2
Ethernet MII Management Interface 1					
EMI1_MDC	Management Data Clock	AJ26	O	DV_{DD}	2
EMI1_MDIO	Management Data In/Out	AK26	IO	DV_{DD}	27
Ethernet MII Management Interface 2					
EMI2_MDC	Management Data Clock	AM8	O	OV_{DD}	13, 14
EMI2_MDIO	Management Data In/Out	AJ8	IO	OV_{DD}	13, 14
USB ULPI Interface					
USB_D7	Data	AK4	IO	OV_{DD}	—
USB_D6	Data	AM4	IO	OV_{DD}	—
USB_D5	Data	AK6	IO	OV_{DD}	—
USB_D4	Data	AK5	IO	OV_{DD}	—
USB_D3	Data	AJ6	IO	OV_{DD}	—
USB_D2	Data	AH7	IO	OV_{DD}	—
USB_D1	Data	AG7	IO	OV_{DD}	—
USB_D0	Data	AF8	IO	OV_{DD}	—
USB_STP	Stop Data	AH6	O	OV_{DD}	2
USB_CLK	Clock	AL4	I	OV_{DD}	2
USB_NXT	Next Data	AL5	I	OV_{DD}	2
USB_DIR	Data Direction	AM5	I	OV_{DD}	2
IIC4_SDA/GPIO3[6]/EVT6_B/ **USB_PWRFAULT**	Overcurrent Status on VBUS line	AE25	I	DV_{DD}	—
DMA Interface					
DMA1_DREQ0_B/GPIO3[0]	DMA1 channel 0 request	AM6	I	OV_{DD}	2

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
DMA1_DACK0_B/GPIO3[1]/ EVT7_B/TMR6	DMA1 channel 0 acknowledge	AL7	O	OV_{DD}	2
DMA1_DDONE0_B/GPIO3[2]/ EVT8_B/TMR7	DMA1 channel 0 done	AM7	O	OV_{DD}	2
GPIO Signals					
ASLEEP/**GPIO1[13]**/ CFG_XVDD_SEL	General Purpose Output	AK10	O	OV_{DD}	2
RTC/**GPIO1[14**]	General Purpose Input / Output	AM23	IO	OV_{DD}	—
UART1_SOUT/**GPIO1[15**]/ CP_LOS4	General Purpose Input / Output	AL29	IO	DV_{DD}	—
UART2_SOUT/**GPIO1[16]**	General Purpose Input / Output	AF25	IO	DV_{DD}	—
UART1_SIN/**GPIO1[17]**/ CP_LOS5	General Purpose Input / Output	AM28	IO	DV_{DD}	—
UART2_SIN/**GPIO1[18]**	General Purpose Input / Output	AH26	IO	DV_{DD}	—
UART1_RTS_B/**GPIO1[19]**/ UART3_SOUT/CP_LOS6	General Purpose Input / Output	AF24	IO	DV_{DD}	—
UART2_RTS_B/**GPIO1[20]**/ UART4_SOUT	General Purpose Input / Output	AG25	IO	DV_{DD}	—
UART1_CTS_B/**GPIO1[21]**/ UART3_SIN/CP_LOS7	General Purpose Input / Output	AE24	IO	DV_{DD}	—
UART2_CTS_B/**GPIO1[22]**/ UART4_SIN	General Purpose Input / Output	AK28	IO	DV_{DD}	—
IRQ03/**GPIO1[23]**	General Purpose Input / Output	AH23	IO	OV_{DD}	—
IRQ04/**GPIO1[24]**	General Purpose Input / Output	AH24	IO	OV_{DD}	—
IRQ05/**GPIO1[25]**	General Purpose Input / Output	AK23	IO	OV_{DD}	—
IRQ06/**GPIO1[26]**/TMR0	General Purpose Input / Output	AK21	IO	OV_{DD}	—
IRQ07/**GPIO1[27]**/TMR1	General Purpose Input / Output	AK24	IO	OV_{DD}	—
IRQ08/**GPIO1[28]**/TMR2	General Purpose Input / Output	AK22	IO	OV_{DD}	—
IRQ09/**GPIO1[29]**/TMR3	General Purpose Input / Output	AM24	IO	OV_{DD}	—
IRQ10/**GPIO1[30]**/TMR4	General Purpose Input / Output	AJ24	IO	OV_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
IRQ11/**GPIO1[31]**/TMR5	General Purpose Input / Output	AL23	IO	OV_{DD}	—
SPI_CS0_B/**GPIO2[0]**/ SDHC_DAT4	General Purpose Input / Output	AJ21	IO	OV_{DD}	—
SPI_CS1_B/**GPIO2[1]**/ SDHC_DAT5	General Purpose Input / Output	AK19	IO	OV_{DD}	—
SPI_CS2_B/**GPIO2[2]**/ SDHC_DAT6	General Purpose Input / Output	AH20	IO	OV_{DD}	—
SPI_CS3_B/**GPIO2[3]**/ SDHC_DAT7	General Purpose Input / Output	AM20	IO	OV_{DD}	—
SDHC_CMD/**GPIO2[4]**	General Purpose Input / Output	AK20	IO	OV_{DD}	—
SDHC_DAT0/**GPIO2[5]**	General Purpose Input / Output	AG22	IO	OV_{DD}	—
SDHC_DAT1**/GPIO2[6]**	General Purpose Input / Output	AH21	IO	OV_{DD}	—
SDHC_DAT2/**GPIO2[7]**	General Purpose Input / Output	AL22	IO	OV_{DD}	—
SDHC_DAT3/**GPIO2[8]**	General Purpose Input / Output	AF21	IO	OV_{DD}	—
SDHC_CLK/**GPIO2[9]**	General Purpose Input / Output	AM22	IO	OV_{DD}	—
IFC_CS1_B/**GPIO2[10]**	General Purpose Input / Output	AK13	IO	OV_{DD}	—
IFC_CS2_B/**GPIO2[11]**	General Purpose Input / Output	AK14	IO	OV_{DD}	—
IFC_CS3_B/**GPIO2[12]**	General Purpose Input / Output	AJ18	IO	OV_{DD}	—
IFC_PAR0/**GPIO2[13]**	General Purpose Input / Output	AH13	IO	OV_{DD}	—
IFC_PAR1/**GPIO2[14]**	General Purpose Input / Output	AJ12	IO	OV_{DD}	—
IFC_A25/**GPIO2[25]**/ IFC_RB2_B/IFC_FCTA2	General Purpose Input / Output	AJ14	IO	OV_{DD}	—
IFC_A26/**GPIO2[26]**/ IFC_RB3_B/IFC_FCTA3	General Purpose Input / Output	AJ15	IO	OV_{DD}	—
IFC_A27/**GPIO2[27**]	General Purpose Input / Output	AJ17	IO	OV_{DD}	—
DMA1_DREQ0_B/**GPIO3[0]**	General Purpose Input / Output	AM6	IO	OV_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
DMA1_DACK0_B/**GPIO3[1]**/ EVT7_B/TMR6	General Purpose Input / Output	AL7	IO	OV_{DD}	—
DMA1_DDONE0_B/**GPIO3[2]**/ EVT8_B/TMR7	General Purpose Input / Output	AM7	IO	OV_{DD}	—
IIC3_SCL/**GPIO3[3]**	General Purpose Input / Output	AM30	IO	DV_{DD}	—
IIC3_SDA/**GPIO3[4]**	General Purpose Input / Output	AK29	IO	DV_{DD}	—
IIC4_SCL/**GPIO3[5]**/EVT5_B	General Purpose Input / Output	AJ27	IO	DV_{DD}	—
IIC4_SDA/**GPIO3[6]**/EVT6_B/ USB_PWRFAULT	General Purpose Input / Output	AE25	IO	DV_{DD}	—
Timer Signals					
IRQ06/GPIO1[26]/**TMR0**	Timer Input / Output	AK21	IO	OV_{DD}	—
IRQ07/GPIO1[27]/**TMR1**	Timer Input / Output	AK24	IO	OV_{DD}	—
IRQ08/GPIO1[28]/**TMR2**	Timer Input / Output	AK22	IO	OV_{DD}	—
IRQ09/GPIO1[29]/**TMR3**	Timer Input / Output	AM24	IO	OV_{DD}	—
IRQ10/GPIO1[30]/**TMR4**	Timer Input / Output	AJ24	IO	OV_{DD}	—
IRQ11/GPIO1[31]/**TMR5**	Timer Input / Output	AL23	IO	OV_{DD}	—
DMA1_DACK0_B/GPIO3[1]/ EVT7_B/**TMR6**	Timer Input / Output	AL7	IO	OV_{DD}	—
DMA1_DDONE0_B/GPIO3[2]/ EVT8_B/**TMR7**	Timer Input / Output	AM7	IO	OV_{DD}	—
Analog Signals					
TD_ANODE	Thermal diode anode	J7	—	Internal diode	31
TD_CATHODE	Thermal diode cathode	J8	—	Internal diode	31
M1VREF	SSTL 1.35/1.5 Reference Voltage	AC9	—	$G1V_{DD}/2$	—
M2VREF	SSTL 1.35/1.5 Reference Voltage	AC24	—	$G2V_{DD}/2$	—
POVDD	Fuse Programming Override Supply	H11	—	POV_{DD}	16
Power-on-Reset Configuration Signals					
IFC_AD00/**CFG_GPINPUT0**	General-Purpose Input, application defined	AG12	I	OV_{DD}	22
IFC_AD01/**CFG_GPINPUT1**	General-Purpose Input, application defined	AG13	I	OV_{DD}	22

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
IFC_AD02/**CFG_GPINPUT2**	General-Purpose Input, application defined	AF13	I	OV_{DD}	22
IFC_AD03/**CFG_GPINPUT3**	General-Purpose Input, application defined	AF19	I	OV_{DD}	22
IFC_AD04/**CFG_GPINPUT4**	General-Purpose Input, application defined	AH15	I	OV_{DD}	22
IFC_AD05/**CFG_GPINPUT5**	General-Purpose Input, application defined	AL13	I	OV_{DD}	22
IFC_AD06/**CFG_GPINPUT6**	General-Purpose Input, application defined	AL17	I	OV_{DD}	22
IFC_AD07/**CFG_GPINPUT7**	General-Purpose Input, application defined	AK18	I	OV_{DD}	22
IFC_AD08/**CFG_RCW_SRC0**	RCW Source	AF14	I	OV_{DD}	22
IFC_AD09/**CFG_RCW_SRC1**	RCW Source	AF15	I	OV_{DD}	22
IFC_AD10/**CFG_RCW_SRC2**	RCW Source	AF16	I	OV_{DD}	22
IFC_AD11/**CFG_RCW_SRC3**	RCW Source	AH16	I	OV_{DD}	22
IFC_AD12/**CFG_RCW_SRC4**	RCW Source	AF17	I	OV_{DD}	22
IFC_AD13/**CFG_RCW_SRC5**	RCW Source	AF18	I	OV_{DD}	22
IFC_AD14/**CFG_RCW_SRC6**	RCW Source	AH19	I	OV_{DD}	22
IFC_AD15/**CFG_RCW_SRC7**	RCW Source	AG18	I	OV_{DD}	22
IFC_CLE/IFC_WBE1/ **CFG_RCW_SRC8**	RCW Source	AM14	I	OV_{DD}	22
IFC_AVD/IFC_ALE/ **CFG_RSP_DIS**	Reset Sequence Pause Disable	AL19	I	OV_{DD}	22, 15
IFC_A21/**CFG_DRAM_TYPE**	DRAM Type Select	AG19	I	OV_{DD}	22, 23
ASLEEP/GPIO1[13]/ **CFG_XVDD_SEL**	XVDD Voltage Select	AK10	I	OV_{DD}	2, 22, 24
IFC_TE/**CFG_IFC_TE**	IFC External Transceiver Enable Pin Polarity Select	AM16	I	OV_{DD}	22, 25
Power and Ground Signals					
AVDD_CGA1	Cluster Group A PLL1 supply	A3	—	AV_{DD}_CGA1	—
AVDD_CGA2	Cluster Group A PLL2 supply	C1	—	AV_{DD}_CGA2	—
AVDD_CGB1	Cluster Group B PLL1 supply	B2	—	AV_{DD}_CGB1	—
AVDD_CGB2	Cluster Group B PLL2 supply	C3	—	AV_{DD}_CGB2	—
AVDD_PLAT	Platform PLL supply	B3	—	AV_{DD}_PLAT	—
AVDD_DDR1	DDR1 PLL supply	AC8	—	AV_{DD}_DDR1	—
AVDD_DDR2	DDR2 PLL supply	AC25	—	AV_{DD}_DDR2	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
AVDD_SRDS1_PLL1	SerDes1 PLL 1 supply	H21	—	AV_{DD}_SRDS1_PLL1	—
AVDD_SRDS1_PLL2	SerDes1 PLL 2 supply	H24	—	AV_{DD}_SRDS1_PLL2	—
AVDD_SRDS2_PLL1	SerDes2 PLL 1 supply	H17	—	AV_{DD}_SRDS2_PLL1	—
AVDD_SRDS2_PLL2	SerDes2 PLL 2 supply	H14	—	AV_{DD}_SRDS2_PLL2	—
SENSEVDD1	V_{DD} sense pin 1	K9	—	—	17
SENSEVDD2	V_{DD} sense pin 2	AE12	—	—	17
AGND_SRDS1_PLL1	SerDes1 PLL 1 GND	H20	—	—	—
AGND_SRDS1_PLL2	SerDes1 PLL 2 GND	G24	—	—	—
AGND_SRDS2_PLL1	SerDes2 PLL 1 GND	H18	—	—	—
AGND_SRDS2_PLL2	SerDes2 PLL 2 GND	G14	—	—	—
SENSEGND1	Vss sense pin 1	J9	—	—	17
SENSEGND2	Vss sense pin 2	AD11	—	—	17
OVDD	General I/O supply	AD13	—	OV_{DD}	—
OVDD	General I/O supply	AD15	—	OV_{DD}	—
OVDD	General I/O supply	AD17	—	OV_{DD}	—
OVDD	General I/O supply	AE14	—	OV_{DD}	—
OVDD	General I/O supply	AE16	—	OV_{DD}	—
OVDD	General I/O supply	AE18	—	OV_{DD}	—
DVDD	UART/I2C/CPRI_LOS I/O supply	AD19	—	DV_{DD}	—
DVDD	UART/I2C/CPRI_LOS I/O supply	AE20	—	DV_{DD}	—
G1VDD	DDR supply for port 1	L8	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	P7	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	R9	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	T1	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	T10	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	U3	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	U6	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	U9	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	V3	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	V6	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	V10	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	W1	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	W9	—	$G1V_{DD}$	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
G1VDD	DDR supply for port 1	Y7	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	Y10	—	$G1V_{DD}$	—
G1VDD	DDR supply for port 1	AA10	—	$G1V_{DD}$	—
G2VDD	DDR supply for port 2	L25	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	P26	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	R24	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	T23	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	T32	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	U24	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	U27	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	U30	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	V23	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	V27	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	V30	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	W24	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	W32	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	Y23	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	Y26	—	$G2V_{DD}$	—
G2VDD	DDR supply for port 2	AA23	—	$G2V_{DD}$	—
SVDD	SerDes core logic supply	K15	—	SV_{DD}	—
SVDD	SerDes core logic supply	K16	—	SV_{DD}	—
SVDD	SerDes core logic supply	K17	—	SV_{DD}	—
SVDD	SerDes core logic supply	K18	—	SV_{DD}	—
SVDD	SerDes core logic supply	K19	—	SV_{DD}	—
SVDD	SerDes core logic supply	K20	—	SV_{DD}	—
SVDD	SerDes core logic supply	K21	—	SV_{DD}	—
SVDD	SerDes core logic supply	K22	—	SV_{DD}	—
SVDD	SerDes core logic supply	K23	—	SV_{DD}	—
TH_VDD	Thermal Monitor Unit supply	J26	—	THV_{DD}	21
XVDD	SerDes transceiver supply	F9	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F12	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F15	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F17	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F19	—	XV_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
XVDD	SerDes transceiver supply	F21	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F24	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F27	—	XV_{DD}	—
XVDD	SerDes transceiver supply	F30	—	XV_{DD}	—
QVDD	Quiet I/O supply	E2	—	QV_{DD}	19
QVDD	Quiet I/O supply	F2	—	QV_{DD}	19
QVDD	Quiet I/O supply	H9	—	QV_{DD}	7
VDD	Core and Platform supply	J10	—	V_{DD}	—
VDD	Core and Platform supply	J12	—	V_{DD}	—
VDD	Core and Platform supply	K11	—	V_{DD}	—
VDD	Core and Platform supply	K13	—	V_{DD}	—
VDD	Core and Platform supply	L10	—	V_{DD}	—
VDD	Core and Platform supply	L12	—	V_{DD}	—
VDD	Core and Platform supply	L14	—	V_{DD}	—
VDD	Core and Platform supply	L16	—	V_{DD}	—
VDD	Core and Platform supply	L18	—	V_{DD}	—
VDD	Core and Platform supply	L20	—	V_{DD}	—
VDD	Core and Platform supply	L22	—	V_{DD}	—
VDD	Core and Platform supply	M11	—	V_{DD}	—
VDD	Core and Platform supply	M13	—	V_{DD}	—
VDD	Core and Platform supply	M15	—	V_{DD}	—
VDD	Core and Platform supply	M17	—	V_{DD}	—
VDD	Core and Platform supply	M19	—	V_{DD}	—
VDD	Core and Platform supply	M21	—	V_{DD}	—
VDD	Core and Platform supply	M23	—	V_{DD}	—
VDD	Core and Platform supply	N10	—	V_{DD}	—
VDD	Core and Platform supply	N12	—	V_{DD}	—
VDD	Core and Platform supply	N14	—	V_{DD}	—
VDD	Core and Platform supply	N16	—	V_{DD}	—
VDD	Core and Platform supply	N18	—	V_{DD}	—
VDD	Core and Platform supply	N20	—	V_{DD}	—
VDD	Core and Platform supply	N22	—	V_{DD}	—
VDD	Core and Platform supply	P11	—	V_{DD}	—
VDD	Core and Platform supply	P13	—	V_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
VDD	Core and Platform supply	P15	—	V_{DD}	—
VDD	Core and Platform supply	P17	—	V_{DD}	—
VDD	Core and Platform supply	P19	—	V_{DD}	—
VDD	Core and Platform supply	P21	—	V_{DD}	—
VDD	Core and Platform supply	P23	—	V_{DD}	—
VDD	Core and Platform supply	R10	—	V_{DD}	—
VDD	Core and Platform supply	R12	—	V_{DD}	—
VDD	Core and Platform supply	R14	—	V_{DD}	—
VDD	Core and Platform supply	R16	—	V_{DD}	—
VDD	Core and Platform supply	R18	—	V_{DD}	—
VDD	Core and Platform supply	R20	—	V_{DD}	—
VDD	Core and Platform supply	R22	—	V_{DD}	—
VDD	Core and Platform supply	T11	—	V_{DD}	—
VDD	Core and Platform supply	T13	—	V_{DD}	—
VDD	Core and Platform supply	T15	—	V_{DD}	—
VDD	Core and Platform supply	T17	—	V_{DD}	—
VDD	Core and Platform supply	T19	—	V_{DD}	—
VDD	Core and Platform supply	T21	—	V_{DD}	—
VDD	Core and Platform supply	U12	—	V_{DD}	—
VDD	Core and Platform supply	U14	—	V_{DD}	—
VDD	Core and Platform supply	U16	—	V_{DD}	—
VDD	Core and Platform supply	U18	—	V_{DD}	—
VDD	Core and Platform supply	U20	—	V_{DD}	—
VDD	Core and Platform supply	U22	—	V_{DD}	—
VDD	Core and Platform supply	V11	—	V_{DD}	—
VDD	Core and Platform supply	V13	—	V_{DD}	—
VDD	Core and Platform supply	V15	—	V_{DD}	—
VDD	Core and Platform supply	V17	—	V_{DD}	—
VDD	Core and Platform supply	V19	—	V_{DD}	—
VDD	Core and Platform supply	V21	—	V_{DD}	—
VDD	Core and Platform supply	W12	—	V_{DD}	—
VDD	Core and Platform supply	W14	—	V_{DD}	—
VDD	Core and Platform supply	W16	—	V_{DD}	—
VDD	Core and Platform supply	W18	—	V_{DD}	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
VDD	Core and Platform supply	W20	—	V_{DD}	—
VDD	Core and Platform supply	W22	—	V_{DD}	—
VDD	Core and Platform supply	Y11	—	V_{DD}	—
VDD	Core and Platform supply	Y13	—	V_{DD}	—
VDD	Core and Platform supply	Y15	—	V_{DD}	—
VDD	Core and Platform supply	Y17	—	V_{DD}	—
VDD	Core and Platform supply	Y19	—	V_{DD}	—
VDD	Core and Platform supply	Y21	—	V_{DD}	—
VDD	Core and Platform supply	AA12	—	V_{DD}	—
VDD	Core and Platform supply	AA14	—	V_{DD}	—
VDD	Core and Platform supply	AA16	—	V_{DD}	—
VDD	Core and Platform supply	AA18	—	V_{DD}	—
VDD	Core and Platform supply	AA20	—	V_{DD}	—
VDD	Core and Platform supply	AA22	—	V_{DD}	—
VDD	Core and Platform supply	AB11	—	V_{DD}	—
VDD	Core and Platform supply	AB13	—	V_{DD}	—
VDD	Core and Platform supply	AB15	—	V_{DD}	—
VDD	Core and Platform supply	AB17	—	V_{DD}	—
VDD	Core and Platform supply	AB19	—	V_{DD}	—
VDD	Core and Platform supply	AB21	—	V_{DD}	—
VDD	Core and Platform supply	AC12	—	V_{DD}	—
VDD	Core and Platform supply	AC14	—	V_{DD}	—
VDD	Core and Platform supply	AC16	—	V_{DD}	—
VDD	Core and Platform supply	AC18	—	V_{DD}	—
VDD	Core and Platform supply	AC20	—	V_{DD}	—
VDD	Core and Platform supply	AC22	—	V_{DD}	—
GND	GND	A2	—	—	—
GND	GND	B1	—	—	—
GND	GND	C2	—	—	—
GND	GND	D1	—	—	—
GND	GND	D3	—	—	—
GND	GND	F3	—	—	—
GND	GND	G1	—	—	—
GND	GND	G6	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	G7	—	—	20
GND	GND	G8	—	—	20
GND	GND	G32	—	—	—
GND	GND	H4	—	—	—
GND	GND	H8	—	—	20
GND	GND	H29	—	—	—
GND	GND	J6	—	—	—
GND	GND	J11	—	—	—
GND	GND	J13	—	—	—
GND	GND	J25	—	—	—
GND	GND	J27	—	—	—
GND	GND	K2	—	—	—
GND	GND	K10	—	—	—
GND	GND	K12	—	—	—
GND	GND	K14	—	—	—
GND	GND	K24	—	—	20
GND	GND	K31	—	—	—
GND	GND	L4	—	—	—
GND	GND	L11	—	—	—
GND	GND	L13	—	—	—
GND	GND	L15	—	—	—
GND	GND	L17	—	—	—
GND	GND	L19	—	—	—
GND	GND	L21	—	—	—
GND	GND	L23	—	—	—
GND	GND	L29	—	—	—
GND	GND	M6	—	—	—
GND	GND	M9	—	—	—
GND	GND	M10	—	—	—
GND	GND	M12	—	—	—
GND	GND	M14	—	—	—
GND	GND	M16	—	—	—
GND	GND	M18	—	—	—
GND	GND	M20	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	M22	—	—	—
GND	GND	M24	—	—	—
GND	GND	M27	—	—	—
GND	GND	N2	—	—	—
GND	GND	N11	—	—	—
GND	GND	N13	—	—	—
GND	GND	N15	—	—	—
GND	GND	N17	—	—	—
GND	GND	N19	—	—	—
GND	GND	N21	—	—	—
GND	GND	N23	—	—	—
GND	GND	N31	—	—	—
GND	GND	P4	—	—	—
GND	GND	P10	—	—	—
GND	GND	P12	—	—	—
GND	GND	P14	—	—	—
GND	GND	P16	—	—	—
GND	GND	P18	—	—	—
GND	GND	P20	—	—	—
GND	GND	P22	—	—	—
GND	GND	P29	—	—	—
GND	GND	R2	—	—	—
GND	GND	R6	—	—	—
GND	GND	R11	—	—	—
GND	GND	R13	—	—	—
GND	GND	R15	—	—	—
GND	GND	R17	—	—	—
GND	GND	R19	—	—	—
GND	GND	R21	—	—	—
GND	GND	R23	—	—	—
GND	GND	R27	—	—	—
GND	GND	R31	—	—	—
GND	GND	T12	—	—	—
GND	GND	T14	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	T16	—	—	—
GND	GND	T18	—	—	—
GND	GND	T20	—	—	—
GND	GND	T22	—	—	—
GND	GND	U10	—	—	—
GND	GND	U11	—	—	—
GND	GND	U13	—	—	—
GND	GND	U15	—	—	—
GND	GND	U17	—	—	—
GND	GND	U19	—	—	—
GND	GND	U21	—	—	—
GND	GND	U23	—	—	—
GND	GND	V12	—	—	—
GND	GND	V14	—	—	—
GND	GND	V16	—	—	—
GND	GND	V18	—	—	—
GND	GND	V20	—	—	—
GND	GND	V22	—	—	—
GND	GND	W10	—	—	—
GND	GND	W11	—	—	—
GND	GND	W13	—	—	—
GND	GND	W15	—	—	—
GND	GND	W17	—	—	—
GND	GND	W19	—	—	—
GND	GND	W21	—	—	—
GND	GND	W23	—	—	—
GND	GND	Y2	—	—	—
GND	GND	Y4	—	—	—
GND	GND	Y12	—	—	—
GND	GND	Y14	—	—	—
GND	GND	Y16	—	—	—
GND	GND	Y18	—	—	—
GND	GND	Y20	—	—	—
GND	GND	Y22	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	Y29	—	—	—
GND	GND	Y31	—	—	—
GND	GND	AA11	—	—	—
GND	GND	AA13	—	—	—
GND	GND	AA15	—	—	—
GND	GND	AA17	—	—	—
GND	GND	AA19	—	—	—
GND	GND	AA21	—	—	—
GND	GND	AB2	—	—	—
GND	GND	AB5	—	—	—
GND	GND	AB8	—	—	—
GND	GND	AB9	—	—	—
GND	GND	AB10	—	—	—
GND	GND	AB12	—	—	—
GND	GND	AB14	—	—	—
GND	GND	AB16	—	—	—
GND	GND	AB18	—	—	—
GND	GND	AB20	—	—	—
GND	GND	AB22	—	—	—
GND	GND	AB23	—	—	—
GND	GND	AB24	—	—	—
GND	GND	AB25	—	—	—
GND	GND	AB28	—	—	—
GND	GND	AB31	—	—	—
GND	GND	AC7	—	—	—
GND	GND	AC10	—	—	—
GND	GND	AC11	—	—	—
GND	GND	AC13	—	—	—
GND	GND	AC15	—	—	—
GND	GND	AC17	—	—	—
GND	GND	AC19	—	—	—
GND	GND	AC21	—	—	—
GND	GND	AC23	—	—	—
GND	GND	AC26	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	AD4	—	—	—
GND	GND	AD8	—	—	—
GND	GND	AD9	—	—	—
GND	GND	AD14	—	—	—
GND	GND	AD16	—	—	—
GND	GND	AD18	—	—	—
GND	GND	AD20	—	—	—
GND	GND	AD22	—	—	—
GND	GND	AD24	—	—	—
GND	GND	AD25	—	—	—
GND	GND	AD29	—	—	—
GND	GND	AE2	—	—	—
GND	GND	AE13	—	—	—
GND	GND	AE15	—	—	—
GND	GND	AE17	—	—	—
GND	GND	AE19	—	—	—
GND	GND	AE21	—	—	—
GND	GND	AE22	—	—	—
GND	GND	AE31	—	—	—
GND	GND	AF5	—	—	—
GND	GND	AF28	—	—	—
GND	GND	AG8	—	—	—
GND	GND	AG11	—	—	—
GND	GND	AG14	—	—	—
GND	GND	AG17	—	—	—
GND	GND	AG20	—	—	—
GND	GND	AG23	—	—	—
GND	GND	AG26	—	—	—
GND	GND	AH2	—	—	—
GND	GND	AH31	—	—	—
GND	GND	AJ5	—	—	—
GND	GND	AJ7	—	—	—
GND	GND	AJ10	—	—	—
GND	GND	AJ13	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
GND	GND	AJ16	—	—	—
GND	GND	AJ19	—	—	—
GND	GND	AJ22	—	—	—
GND	GND	AJ25	—	—	—
GND	GND	AJ28	—	—	—
GND	GND	AL1	—	—	—
GND	GND	AL3	—	—	—
GND	GND	AL6	—	—	—
GND	GND	AL9	—	—	—
GND	GND	AL12	—	—	—
GND	GND	AL15	—	—	—
GND	GND	AL18	—	—	—
GND	GND	AL21	—	—	—
GND	GND	AL24	—	—	—
GND	GND	AL27	—	—	—
GND	GND	AL30	—	—	—
GND	GND	AL32	—	—	—
GND	GND	AM2	—	—	—
GND	GND	AM31	—	—	—
XGND	SerDes transceiver GND	D6	—	—	—
XGND	SerDes transceiver GND	D9	—	—	—
XGND	SerDes transceiver GND	D12	—	—	—
XGND	SerDes transceiver GND	D15	—	—	—
XGND	SerDes transceiver GND	D18	—	—	—
XGND	SerDes transceiver GND	D21	—	—	—
XGND	SerDes transceiver GND	D24	—	—	—
XGND	SerDes transceiver GND	D27	—	—	—
XGND	SerDes transceiver GND	D30	—	—	—
XGND	SerDes transceiver GND	E6	—	—	—
XGND	SerDes transceiver GND	E9	—	—	—
XGND	SerDes transceiver GND	E12	—	—	—
XGND	SerDes transceiver GND	E15	—	—	—
XGND	SerDes transceiver GND	E18	—	—	—
XGND	SerDes transceiver GND	E21	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
XGND	SerDes transceiver GND	E24	—	—	—
XGND	SerDes transceiver GND	E27	—	—	—
XGND	SerDes transceiver GND	E30	—	—	—
XGND	SerDes transceiver GND	F18	—	—	—
SGND	SerDes core logic GND	A4	—	—	—
SGND	SerDes core logic GND	A7	—	—	—
SGND	SerDes core logic GND	A10	—	—	—
SGND	SerDes core logic GND	A13	—	—	—
SGND	SerDes core logic GND	A15	—	—	—
SGND	SerDes core logic GND	A18	—	—	—
SGND	SerDes core logic GND	A21	—	—	—
SGND	SerDes core logic GND	A23	—	—	—
SGND	SerDes core logic GND	A25	—	—	—
SGND	SerDes core logic GND	A28	—	—	—
SGND	SerDes core logic GND	A31	—	—	—
SGND	SerDes core logic GND	B4	—	—	—
SGND	SerDes core logic GND	B7	—	—	—
SGND	SerDes core logic GND	B10	—	—	—
SGND	SerDes core logic GND	B13	—	—	—
SGND	SerDes core logic GND	B15	—	—	—
SGND	SerDes core logic GND	B18	—	—	—
SGND	SerDes core logic GND	B21	—	—	—
SGND	SerDes core logic GND	B23	—	—	—
SGND	SerDes core logic GND	B25	—	—	—
SGND	SerDes core logic GND	B28	—	—	—
SGND	SerDes core logic GND	B31	—	—	—
SGND	SerDes core logic GND	C4	—	—	—
SGND	SerDes core logic GND	C5	—	—	—
SGND	SerDes core logic GND	C6	—	—	—
SGND	SerDes core logic GND	C7	—	—	—
SGND	SerDes core logic GND	C8	—	—	—
SGND	SerDes core logic GND	C9	—	—	—
SGND	SerDes core logic GND	C10	—	—	—
SGND	SerDes core logic GND	C11	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SGND	SerDes core logic GND	C12	—	—	—
SGND	SerDes core logic GND	C13	—	—	—
SGND	SerDes core logic GND	C14	—	—	—
SGND	SerDes core logic GND	C15	—	—	—
SGND	SerDes core logic GND	C16	—	—	—
SGND	SerDes core logic GND	C17	—	—	—
SGND	SerDes core logic GND	C18	—	—	—
SGND	SerDes core logic GND	C19	—	—	—
SGND	SerDes core logic GND	C20	—	—	—
SGND	SerDes core logic GND	C21	—	—	—
SGND	SerDes core logic GND	C22	—	—	—
SGND	SerDes core logic GND	C23	—	—	—
SGND	SerDes core logic GND	C24	—	—	—
SGND	SerDes core logic GND	C25	—	—	—
SGND	SerDes core logic GND	C26	—	—	—
SGND	SerDes core logic GND	C27	—	—	—
SGND	SerDes core logic GND	C28	—	—	—
SGND	SerDes core logic GND	C29	—	—	—
SGND	SerDes core logic GND	C30	—	—	—
SGND	SerDes core logic GND	D4	—	—	—
SGND	SerDes core logic GND	D31	—	—	—
SGND	SerDes core logic GND	D32	—	—	—
SGND	SerDes core logic GND	E4	—	—	—
SGND	SerDes core logic GND	F5	—	—	—
SGND	SerDes core logic GND	F6	—	—	—
SGND	SerDes core logic GND	F7	—	—	—
SGND	SerDes core logic GND	F8	—	—	—
SGND	SerDes core logic GND	F10	—	—	—
SGND	SerDes core logic GND	F11	—	—	—
SGND	SerDes core logic GND	F13	—	—	—
SGND	SerDes core logic GND	F14	—	—	—
SGND	SerDes core logic GND	F16	—	—	—
SGND	SerDes core logic GND	F20	—	—	—
SGND	SerDes core logic GND	F22	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
SGND	SerDes core logic GND	F23	—	—	—
SGND	SerDes core logic GND	F25	—	—	—
SGND	SerDes core logic GND	F26	—	—	—
SGND	SerDes core logic GND	F28	—	—	—
SGND	SerDes core logic GND	F29	—	—	—
SGND	SerDes core logic GND	F31	—	—	—
SGND	SerDes core logic GND	F32	—	—	—
SGND	SerDes core logic GND	G9	—	—	—
SGND	SerDes core logic GND	G11	—	—	—
SGND	SerDes core logic GND	G12	—	—	—
SGND	SerDes core logic GND	G15	—	—	—
SGND	SerDes core logic GND	G17	—	—	—
SGND	SerDes core logic GND	G19	—	—	—
SGND	SerDes core logic GND	G21	—	—	—
SGND	SerDes core logic GND	G23	—	—	—
SGND	SerDes core logic GND	G27	—	—	—
SGND	SerDes core logic GND	H10	—	—	—
SGND	SerDes core logic GND	H12	—	—	—
SGND	SerDes core logic GND	H13	—	—	—
SGND	SerDes core logic GND	H19	—	—	—
SGND	SerDes core logic GND	H25	—	—	—
SGND	SerDes core logic GND	H26	—	—	—
SGND	SerDes core logic GND	J14	—	—	—
SGND	SerDes core logic GND	J15	—	—	—
SGND	SerDes core logic GND	J16	—	—	—
SGND	SerDes core logic GND	J17	—	—	—
SGND	SerDes core logic GND	J18	—	—	—
SGND	SerDes core logic GND	J19	—	—	—
SGND	SerDes core logic GND	J20	—	—	—
SGND	SerDes core logic GND	J21	—	—	—
SGND	SerDes core logic GND	J22	—	—	—
SGND	SerDes core logic GND	J23	—	—	—
SGND	SerDes core logic GND	J24	—	—	—

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes
No connection pins					
NC_D2	No Connection	D2	—	—	18
NC_E3	No Connection	E3	—	—	18
NC_F4	No Connection	F4	—	—	18
NC_G5	No Connection	G5	—	—	18
NC_G13	No Connection	G13	—	—	18
NC_G16	No Connection	G16	—	—	18
NC_G22	No Connection	G22	—	—	18
NC_G25	No Connection	G25	—	—	18
NC_G28	No Connection	G28	—	—	18
NC_H7	No Connection	H7	—	—	18
NC_H15	No Connection	H15	—	—	18
NC_H16	No Connection	H16	—	—	18
NC_H22	No Connection	H22	—	—	18
NC_H23	No Connection	H23	—	—	18
NC_AD10	No Connection	AD10	—	—	18
NC_AD23	No Connection	AD23	—	—	18
NC_DET	Orientation Detect	B32	—	—	18

Table 1. Pinout list by bus (continued)

Signal	Signal Description	Package Pin	Pin Type	Power Supply	Notes

1. MDIC[0] is grounded through a 237 Ω for B4860 Rev. 1 and 187 Ω for B4860 Rev. 2 precision 1% resistor and MDIC[1] is connected to GnV$_{DD}$ through a 237 Ω for B4860 Rev. 1 and 187 Ω for B4860 Rev. 2 precision 1% resistor. For either full or half driver strength calibration of DDR IOs, use the same MDIC resistor value of 237 Ω for B4860 Rev. 1 and 187 Ω for B4860 Rev. 2. The memory controller register setting can be used to determine automatic calibration is done to full or half-drive strength. These pins are used for automatic calibration of the DDR3/DDR3L IOs.
2. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or it has other manufacturing test functions. Thus, this pin is described as an I/O for boundary scan.
3. This pin is an open drain signal. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV$_{DD}$.
4. When used as an I2C interface, this pin functions as an open drain I/O. Recommend that a pull-up resistor (1 kΩ) be placed on this pin to DV$_{DD}$.
5. When used as an IRQ_OUT_B pin, this pin functions as an open drain I/O. Recommend that a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV$_{DD}$.
6. See Section 3.5, “Connection recommendations for unused pins,” for additional details on this signal.
7. QVDD is an internal IO quiet power domain. Externally, it should be connected to the OV$_{DD}$ supply.
8. Pin must NOT be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, external pull-up is required to drive this pin to a safe state during reset.
9. Pin has a weak (~20 kΩ) internal pull-up P-FET, which is always enabled.
10. This output is actively driven during reset rather than being tristated during reset.
11. This pin requires a 698 Ω (1% accuracy) pull-up to XV$_{DD}$.
12. This pin requires a 200 Ω (1% accuracy) pull-up to SV$_{DD}$.
13. These pins should be pulled up to 1.2 V through a 180 Ω (1% accuracy) resistor for EMI2_MDC and 330 Ω (1% accuracy) resistor for EMI2_MDIO.
14. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. OV$_{DD}$ must be powered to use this interface.
15. CFG_RSP_DIS configuration pin allows the B4860 to enter debug mode immediately after reset. The board should be configured (by some FPGA/dip-switch) to drive the CFG_RSP_DIS pin during PORESET sequence to logic 0 or logic 1, with a default level of logic 1, and with the timing as defined for all other CFG pins. After POR completion, the pin is used as IFC_AVD function.
16. See Section 2.2, “Power sequencing,” and Section 5, “Security fuse processor,” for additional details on this signal.
17. These pins are connected to the same global power and ground (VDD and GND) nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.
18. Do not connect. These pins should be left floating.
19. The QV$_{DD}$ supply to these pins is not an actual supply pin, but a functional pin requires the QV$_{DD}$ supply connectivity. Pin must be connected with a pull up resistor of 10 kΩ.
20. The GND supply to these pins is not an actual supply pin, but a functional pin requires the GND supply connectivity. Pin must be connected with a pull down resistor of 10 kΩ.
21. The Thermal Monitoring Unit (TMU) is defeatured on this device. TH_VDD should be connected to an OV$_{DD}$ supply.
22. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, when the signal is intended to be high after reset, and when there is a device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.
23. CFG_DRAM_TYPE configuration pin selects the DRAM type: “0”—DDR3 (IO is 1.5 V), “1”—DDR3L (IO is 1.35 V)
24. CFG_XVDD_SEL configuration pin selects the XV$_{DD}$ voltage: “0”—XV$_{DD}$ is 1.5 V, “1”—XV$_{DD}$ is 1.35 V.
25. CFG_IFC_TE configuration pin selects the IFC External Transceiver Enable Pin Polarity: “0”—Default value of IFC’s CSPR0[TE] is logic 1, “1”—Default value of IFC’s CSPR0[TE] is logic 0.
26. Recommend that a weak pull-up resistor (4.7-kΩ) be placed on this pin to the respective power supply.
27. Recommend that a weak pull-up resistor (2-10 kΩ) be placed on this pin to the respective power supply.
28. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.
29. Must be pulled down externally (for any active CPRI lane that is not connected to an SFP).
30. When configured as DUART (using RCW[UART_EXT] bits), pins are internally pulled down. When the pins are configured as CP_LOSi, they should be pulled down externally for any active CPRI lane that is not connected to an SFP.
31. When the thermal diode is not used, its pins (anode, cathode) should be connected to GND.
32. If used as an SDHC signal, pull-up 10 to 100 kΩ. to the respective IO supply.

WARNING

See Section 3.5, "Connection recommendations for unused pins," for additional details on properly connecting these pins for specific applications.

1.3 Pinout list by package pin number

This table provides the pinout list for the chip sorted by package pin number.

Table 2. Pinout by package pin number

Package pin number	Package pin name	Package pin number	Package Pin Name
A1	—	B1	GND
A2	GND	B2	AVDD_CGB1
A3	AVDD_CGA1	B3	AVDD_PLAT
A4	SGND	B4	SGND
A5	SD2_RX7	B5	SD2_RX7_B
A6	SD2_RX6	B6	SD2_RX6_B
A7	SGND	B7	SGND
A8	SD2_RX5	B8	SD2_RX5_B
A9	SD2_RX4	B9	SD2_RX4_B
A10	SGND	B10	SGND
A11	SD2_RX3	B11	SD2_RX3_B
A12	SD2_RX2	B12	SD2_RX2_B
A13	SGND	B13	SGND
A14	SD2_REF1_CLK_B	B14	SD2_REF1_CLK
A15	SGND	B15	SGND
A16	SD2_RX1	B16	SD2_RX1_B
A17	SD2_RX0	B17	SD2_RX0_B
A18	SGND	B18	SGND
A19	SD1_RX0	B19	SD1_RX0_B
A20	SD1_RX1	B20	SD1_RX1_B
A21	SGND	B21	SGND
A22	SD1_REF1_CLK_B	B22	SD1_REF1_CLK
A23	SGND	B23	SGND
A24	SD1_RX2	B24	SD1_RX2_B
A25	SGND	B25	SGND
A26	SD1_RX3	B26	SD1_RX3_B
A27	SD1_RX4	B27	SD1_RX4_B

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
A28	SGND
A29	SD1_RX5
A30	SD1_RX6
A31	SGND
A32	—
C1	AVDD_CGA2
C2	GND
C3	AVDD_CGB2
C4	SGND
C5	SGND
C6	SGND
C7	SGND
C8	SGND
C9	SGND
C10	SGND
C11	SGND
C12	SGND
C13	SGND
C14	SGND
C15	SGND
C16	SGND
C17	SGND
C18	SGND
C19	SGND
C20	SGND
C21	SGND
C22	SGND
C23	SGND
C24	SGND
C25	SGND
C26	SGND
C27	SGND
C28	SGND
C29	SGND

Package pin number	Package Pin Name
B28	SGND
B29	SD1_RX5_B
B30	SD1_RX6_B
B31	SGND
B32	NC_DET
D1	GND
D2	NC_D2
D3	GND
D4	SGND
D5	SD2_REF2_CLK_B
D6	XGND
D7	SD2_TX7
D8	SD2_TX6
D9	XGND
D10	SD2_TX5
D11	SD2_TX4
D12	XGND
D13	SD2_TX3
D14	SD2_TX2
D15	XGND
D16	SD2_TX1
D17	SD2_TX0
D18	XGND
D19	SD1_TX0
D20	SD1_TX1
D21	XGND
D22	SD1_TX2
D23	SD1_TX3
D24	XGND
D25	SD1_TX4
D26	SD1_TX5
D27	XGND
D28	SD1_TX6
D29	SD1_TX7

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
C30	SGND
C31	SD1_RX7_B
C32	SD1_RX7
E1	PORESET_B
E2	QV_{DD}
E3	NC_E3
E4	SGND
E5	SD2_REF2_CLK
E6	XGND
E7	SD2_TX7_B
E8	SD2_TX6_B
E9	XGND
E10	SD2_TX5_B
E11	SD2_TX4_B
E12	XGND
E13	SD2_TX3_B
E14	SD2_TX2_B
E15	XGND
E16	SD2_TX1_B
E17	SD2_TX0_B
E18	XGND
E19	SD1_TX0_B
E20	SD1_TX1_B
E21	XGND
E22	SD1_TX2_B
E23	SD1_TX3_B
E24	XGND
E25	SD1_TX4_B
E26	SD1_TX5_B
E27	XGND
E28	SD1_TX6_B
E29	SD1_TX7_B
E30	XGND
E31	SD1_REF2_CLK

Package pin number	Package Pin Name
D30	XGND
D31	SGND
D32	SGND
F1	SYSCLK
F2	QV_{DD}
F3	GND
F4	NC_F4
F5	SGND
F6	SGND
F7	SGND
F8	SGND
F9	XV_{DD}
F10	SGND
F11	SGND
F12	XV_{DD}
F13	SGND
F14	SGND
F15	XV_{DD}
F16	SGND
F17	XV_{DD}
F18	XGND
F19	XV_{DD}
F20	SGND
F21	XV_{DD}
F22	SGND
F23	SGND
F24	XV_{DD}
F25	SGND
F26	SGND
F27	XV_{DD}
F28	SGND
F29	SGND
F30	XV_{DD}
F31	SGND

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
E32	SD1_REF2_CLK_B
G1	GND
G2	D1_MDQ59
G3	D1_MDQ56
G4	D1_MDQ58
G5	NC_G5
G6	GND
G7	GND
G8	GND
G9	SGND
G10	SD2_IMP_CAL_TX
G11	SGND
G12	SGND
G13	NC_G13
G14	AGND_SRDS2_PLL2
G15	SGND
G16	NC_G16
G17	SGND
G18	SD2_IMP_CAL_RX
G19	SGND
G20	SD1_IMP_CAL_RX
G21	SGND
G22	NC_G22
G23	SGND
G24	AGND_SRDS1_PLL2
G25	NC_G25
G26	SD1_IMP_CAL_TX
G27	SGND
G28	NC_G28
G29	D2_MDQ58
G30	D2_MDQ56
G31	D2_MDQ59
G32	GND
J1	D1_MDQS6

Package pin number	Package Pin Name
F32	SGND
H1	D1_MDQ51
H2	D1_MDQ52
H3	D1_MDQ55
H4	GND
H5	D1_MDQ60
H6	D1_MDQ63
H7	NC_H7
H8	GND
H9	QV_{DD}
H10	SGND
H11	POV_{DD}
H12	SGND
H13	SGND
H14	AVDD_SRDS2_PLL2
H15	NC_H15
H16	NC_H16
H17	AVDD_SRDS2_PLL1
H18	AGND_SRDS2_PLL1
H19	SGND
H20	AGND_SRDS1_PLL1
H21	AVDD_SRDS1_PLL1
H22	NC_H22
H23	NC_H23
H24	AVDD_SRDS1_PLL2
H25	SGND
H26	SGND
H27	D2_MDQ63
H28	D2_MDQ60
H29	GND
H30	D2_MDQ55
H31	D2_MDQ52
H32	D2_MDQ51
K1	D1_MDQ50

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
J2	D1_MDQS6_B
J3	D1_MDM6
J4	D1_MDQS7
J5	D1_MDQS7_B
J6	GND
J7	TD_ANODE
J8	TD_CATHODE
J9	SENSEGND1
J10	V_{DD}
J11	GND
J12	V_{DD}
J13	GND
J14	SGND
J15	SGND
J16	SGND
J17	SGND
J18	SGND
J19	SGND
J20	SGND
J21	SGND
J22	SGND
J23	SGND
J24	SGND
J25	GND
J26	TH_V_{DD}
J27	GND
J28	D2_MDQS7_B
J29	D2_MDQS7
J30	D2_MDM6
J31	D2_MDQS6_B
J32	D2_MDQS6
L1	D1_MDQ48
L2	D1_MDQ49
L3	D1_MDQ43

Package pin number	Package Pin Name
K2	GND
K3	D1_MDQ53
K4	D1_MDQ54
K5	D1_MDM7
K6	D1_MDQ57
K7	D1_MDQ61
K8	D1_MODT1
K9	SENSEVDD1
K10	GND
K11	V_{DD}
K12	GND
K13	V_{DD}
K14	GND
K15	SV_{DD}
K16	SV_{DD}
K17	SV_{DD}
K18	SV_{DD}
K19	SV_{DD}
K20	SV_{DD}
K21	SV_{DD}
K22	SV_{DD}
K23	SV_{DD}
K24	GND
K25	D2_MODT1
K26	D2_MDQ61
K27	D2_MDQ57
K28	D2_MDM7
K29	D2_MDQ54
K30	D2_MDQ53
K31	GND
K32	D2_MDQ50
M1	D1_MDQ35
M2	D1_MDQ34
M3	D1_MDQ37

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
L4	GND
L5	D1_MDQ47
L6	D1_MDQ45
L7	D1_MDQ62
L8	$G1V_{DD}$
L9	D1_MCS3_B
L10	V_{DD}
L11	GND
L12	V_{DD}
L13	GND
L14	V_{DD}
L15	GND
L16	V_{DD}
L17	GND
L18	V_{DD}
L19	GND
L20	V_{DD}
L21	GND
L22	V_{DD}
L23	GND
L24	D2_MCS3_B
L25	$G2V_{DD}$
L26	D2_MDQ62
L27	D2_MDQ45
L28	D2_MDQ47
L29	GND
L30	D2_MDQ43
L31	D2_MDQ49
L32	D2_MDQ48
N1	D1_MDQ33
N2	GND
N3	D1_MDM4
N4	D1_MDQS5
N5	D1_MDQS5_B

Package pin number	Package Pin Name
M4	D1_MDQ41
M5	D1_MDQ42
M6	GND
M7	D1_MODT0
M8	D1_MODT3
M9	GND
M10	GND
M11	V_{DD}
M12	GND
M13	V_{DD}
M14	GND
M15	V_{DD}
M16	GND
M17	V_{DD}
M18	GND
M19	V_{DD}
M20	GND
M21	V_{DD}
M22	GND
M23	V_{DD}
M24	GND
M25	D2_MODT3
M26	D2_MODT0
M27	GND
M28	D2_MDQ42
M29	D2_MDQ41
M30	D2_MDQ37
M31	D2_MDQ34
M32	D2_MDQ35
P1	D1_MDQS4
P2	D1_MDQS4_B
P3	D1_MDQ39
P4	GND
P5	D1_MDQ40

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
N6	D1_MDM5
N7	D1_MWE_B
N8	D1_MODT2
N9	D1_MA13
N10	V_{DD}
N11	GND
N12	V_{DD}
N13	GND
N14	V_{DD}
N15	GND
N16	V_{DD}
N17	GND
N18	V_{DD}
N19	GND
N20	V_{DD}
N21	GND
N22	V_{DD}
N23	GND
N24	D2_MA13
N25	D2_MODT2
N26	D2_MWE_B
N27	D2_MDM5
N28	D2_MDQS5_B
N29	D2_MDQS5
N30	D2_MDM4
N31	GND
N32	D2_MDQ33
R1	D1_MDQ32
R2	GND
R3	D1_MDQ36
R4	D1_MDQ38
R5	D1_MDQ44
R6	GND
R7	D1_MCS2_B

Package pin number	Package Pin Name
P6	D1_MDQ46
P7	$G1V_{DD}$
P8	D1_MRAS_B
P9	D1_MCS1_B
P10	GND
P11	V_{DD}
P12	GND
P13	V_{DD}
P14	GND
P15	V_{DD}
P16	GND
P17	V_{DD}
P18	GND
P19	V_{DD}
P20	GND
P21	V_{DD}
P22	GND
P23	V_{DD}
P24	D2_MCS1_B
P25	D2_MRAS_B
P26	$G2V_{DD}$
P27	D2_MDQ46
P28	D2_MDQ40
P29	GND
P30	D2_MDQ39
P31	D2_MDQS4_B
P32	D2_MDQS4
T1	$G1V_{DD}$
T2	D1_MA05
T3	D1_MAPAR_ERR_B
T4	D1_MA02
T5	D1_MBA1
T6	D1_MA01
T7	D1_MAPAR_OUT

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
R8	D1_MCAS_B
R9	$G1V_{DD}$
R10	V_{DD}
R11	GND
R12	V_{DD}
R13	GND
R14	V_{DD}
R15	GND
R16	V_{DD}
R17	GND
R18	V_{DD}
R19	GND
R20	V_{DD}
R21	GND
R22	V_{DD}
R23	GND
R24	$G2V_{DD}$
R25	D2_MCAS_B
R26	D2_MCS2_B
R27	GND
R28	D2_MDQ44
R29	D2_MDQ38
R30	D2_MDQ36
R31	GND
R32	D2_MDQ32
U1	D1_MCK2
U2	D1_MCK2_B
U3	$G1V_{DD}$
U4	D1_MCK3
U5	D1_MCK3_B
U6	$G1V_{DD}$
U7	D1_MA00
U8	D1_MA10
U9	$G1V_{DD}$

Package pin number	Package Pin Name
T8	D1_MBA0
T9	D1_MCS0_B
T10	$G1V_{DD}$
T11	V_{DD}
T12	GND
T13	V_{DD}
T14	GND
T15	V_{DD}
T16	GND
T17	V_{DD}
T18	GND
T19	V_{DD}
T20	GND
T21	V_{DD}
T22	GND
T23	$G2V_{DD}$
T24	D2_MCS0_B
T25	D2_MBA0
T26	D2_MAPAR_OUT
T27	D2_MA01
T28	D2_MBA1
T29	D2_MA02
T30	D2_MAPAR_ERR_B
T31	D2_MA05
T32	$G2V_{DD}$
V1	D1_MCK0
V2	D1_MCK0_B
V3	$G1V_{DD}$
V4	D1_MCK1
V5	D1_MCK1_B
V6	$G1V_{DD}$
V7	D1_MDIC1
V8	D1_MA04
V9	D1_MA03

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
U10	GND
U11	GND
U12	V_{DD}
U13	GND
U14	V_{DD}
U15	GND
U16	V_{DD}
U17	GND
U18	V_{DD}
U19	GND
U20	V_{DD}
U21	GND
U22	V_{DD}
U23	GND
U24	$G2V_{DD}$
U25	D2_MA10
U26	D2_MA00
U27	$G2V_{DD}$
U28	D2_MCK3_B
U29	D2_MCK3
U30	$G2V_{DD}$
U31	D2_MCK2_B
U32	D2_MCK2
W1	$G1V_{DD}$
W2	D1_MDIC0
W3	D1_MA08
W4	D1_MA06
W5	D1_MA07
W6	D1_MA09
W7	D1_MA12
W8	D1_MA11
W9	$G1V_{DD}$
W10	GND
W11	GND

Package pin number	Package Pin Name
V10	$G1V_{DD}$
V11	V_{DD}
V12	GND
V13	V_{DD}
V14	GND
V15	V_{DD}
V16	GND
V17	V_{DD}
V18	GND
V19	V_{DD}
V20	GND
V21	V_{DD}
V22	GND
V23	$G2V_{DD}$
V24	D2_MA03
V25	D2_MA04
V26	D2_MDIC1
V27	$G2V_{DD}$
V28	D2_MCK1_B
V29	D2_MCK1
V30	$G2V_{DD}$
V31	D2_MCK0_B
V32	D2_MCK0
Y1	D1_MECC3
Y2	GND
Y3	D1_MECC7
Y4	GND
Y5	D1_MECC0
Y6	D1_MCKE3
Y7	$G1V_{DD}$
Y8	D1_MCKE2
Y9	D1_MA15
Y10	$G1V_{DD}$
Y11	V_{DD}

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
W12	V_{DD}
W13	GND
W14	V_{DD}
W15	GND
W16	V_{DD}
W17	GND
W18	V_{DD}
W19	GND
W20	V_{DD}
W21	GND
W22	V_{DD}
W23	GND
W24	$G2V_{DD}$
W25	D2_MA11
W26	D2_MA12
W27	D2_MA09
W28	D2_MA07
W29	D2_MA06
W30	D2_MA08
W31	D2_MDIC0
W32	$G2V_{DD}$
AA1	D1_MDQS8_B
AA2	D1_MDQS8
AA3	D1_MECC6
AA4	D1_MDQ30
AA5	D1_MDM3
AA6	D1_MBA2
AA7	D1_MCKE0
AA8	D1_MCKE1
AA9	D1_MA14
AA10	$G1V_{DD}$
AA11	GND
AA12	V_{DD}
AA13	GND

Package pin number	Package Pin Name
Y12	GND
Y13	VDD
Y14	GND
Y15	V_{DD}
Y16	GND
Y17	V_{DD}
Y18	GND
Y19	V_{DD}
Y20	GND
Y21	V_{DD}
Y22	GND
Y23	$G2V_{DD}$
Y24	D2_MA15
Y25	D2_MCKE2
Y26	$G2V_{DD}$
Y27	D2_MCKE3
Y28	D2_MECC0
Y29	GND
Y30	D2_MECC7
Y31	GND
Y32	D2_MECC3
AB1	D1_MDM8
AB2	GND
AB3	D1_MECC2
AB4	D1_MDQ29
AB5	GND
AB6	D1_MDQ27
AB7	D1_MDQ26
AB8	GND
AB9	GND
AB10	GND
AB11	V_{DD}
AB12	GND
AB13	V_{DD}

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AA14	V_{DD}
AA15	GND
AA16	V_{DD}
AA17	GND
AA18	V_{DD}
AA19	GND
AA20	V_{DD}
AA21	GND
AA22	V_{DD}
AA23	$G2V_{DD}$
AA24	D2_MA14
AA25	D2_MCKE1
AA26	D2_MCKE0
AA27	D2_MBA2
AA28	D2_MDM3
AA29	D2_MDQ30
AA30	D2_MECC6
AA31	D2_MDQS8
AA32	D2_MDQS8_B
AC1	D1_MECC5
AC2	D1_MECC4
AC3	D1_MECC1
AC4	D1_MDQ31
AC5	D1_MDQS3_B
AC6	D1_MDQS3
AC7	GND
AC8	AVDD_DDR1
AC9	M1VREF
AC10	GND
AC11	GND
AC12	V_{DD}
AC13	GND
AC14	V_{DD}
AC15	GND

Package pin number	Package Pin Name
AB14	GND
AB15	V_{DD}
AB16	GND
AB17	V_{DD}
AB18	GND
AB19	V_{DD}
AB20	GND
AB21	V_{DD}
AB22	GND
AB23	GND
AB24	GND
AB25	GND
AB26	D2_MDQ26
AB27	D2_MDQ27
AB28	GND
AB29	D2_MDQ29
AB30	D2_MECC2
AB31	GND
AB32	D2_MDM8
AD1	D1_MDM2
AD2	D1_MDQ19
AD3	D1_MDQ22
AD4	GND
AD5	D1_MDQ28
AD6	D1_MDQ24
AD7	D1_MDQ25
AD8	GND
AD9	GND
AD10	NC_AD10
AD11	SENSEGND2
AD12	D1_DDRCLK
AD13	OV_{DD}
AD14	GND
AD15	OV_{DD}

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AC16	V_{DD}
AC17	GND
AC18	V_{DD}
AC19	GND
AC20	V_{DD}
AC21	GND
AC22	V_{DD}
AC23	GND
AC24	M2VREF
AC25	AVDD_DDR2
AC26	GND
AC27	D2_MDQS3
AC28	D2_MDQS3_B
AC29	D2_MDQ31
AC30	D2_MECC1
AC31	D2_MECC4
AC32	D2_MECC5
AE1	D1_MDQ21
AE2	GND
AE3	D1_MDQ23
AE4	D1_MDQS0_B
AE5	D1_MDQS0
AE6	D1_MDQ04
AE7	D1_MDQ01
AE8	TSEC_1588_CLK_OUT
AE9	TSEC_1588_TRIG_IN1
AE10	EVT0_B
AE11	EVT1_B
AE12	SENSEVDD2
AE13	GND
AE14	OV_{DD}
AE15	GND
AE16	OV_{DD}
AE17	GND

Package pin number	Package Pin Name
AD16	GND
AD17	OV_{DD}
AD18	GND
AD19	DV_{DD}
AD20	GND
AD21	D2_DDRCLK
AD22	GND
AD23	NC_AD23
AD24	GND
AD25	GND
AD26	D2_MDQ25
AD27	D2_MDQ24
AD28	D2_MDQ28
AD29	GND
AD30	D2_MDQ22
AD31	D2_MDQ19
AD32	D2_MDM2
AF1	D1_MDQS2_B
AF2	D1_MDQS2
AF3	D1_MDQ16
AF4	D1_MDQ03
AF5	GND
AF6	D1_MDQ06
AF7	D1_MDQ00
AF8	USB_D0
AF9	TSEC_1588_PULSE_OUT1
AF10	TSEC_1588_TRIG_IN2
AF11	CP_SYNC1
AF12	EVT4_B
AF13	IFC_AD02/CFG_GPINPUT2
AF14	IFC_AD08/CFG_RCW_SRC0
AF15	IFC_AD09/CFG_RCW_SRC1
AF16	IFC_AD10/CFG_RCW_SRC2
AF17	IFC_AD12/CFG_RCW_SRC4

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AE18	OV_{DD}
AE19	GND
AE20	DV_{DD}
AE21	GND
AE22	GND
AE23	IIC2_SCL
AE24	UART1_CTS_B/GPIO1[21]/UART3_SIN/ CP_LOS7
AE25	IIC4_SDA/GPIO3[6]/EVT6_B/ USB_PWRFAULT
AE26	D2_MDQ01
AE27	D2_MDQ04
AE28	D2_MDQS0
AE29	D2_MDQS0_B
AE30	D2_MDQ23
AE31	GND
AE32	D2_MDQ21
AG1	D1_MDQ20
AG2	D1_MDQ18
AG3	D1_MDQ17
AG4	D1_MDM0
AG5	D1_MDQ05
AG6	D1_MDQ02
AG7	USB_D1
AG8	GND
AG9	TSEC_1588_ALARM_OUT1
AG10	CP_SYNC2
AG11	GND
AG12	IFC_AD00/CFG_GPINPUT0
AG13	IFC_AD01/CFG_GPINPUT1
AG14	GND
AG15	IFC_A16
AG16	IFC_A18
AG17	GND
AG18	IFC_AD15/CFG_RCW_SRC7

Package pin number	Package Pin Name
AF18	IFC_AD13/CFG_RCW_SRC5
AF19	IFC_AD03/CFG_GPINPUT3
AF20	TMP_DETECT_B
AF21	SDHC_DAT3/GPIO2[8]
AF22	IRQ01
AF23	IRQ00
AF24	UART1_RTS_B/GPIO1[19]/UART3_SOUT/ CP_LOS6
AF25	UART2_SOUT/GPIO1[16]
AF26	D2_MDQ00
AF27	D2_MDQ06
AF28	GND
AF29	D2_MDQ03
AF30	D2_MDQ16
AF31	D2_MDQS2
AF32	D2_MDQS2_B
AH1	D1_MDM1
AH2	GND
AH3	D1_MDQ13
AH4	D1_MDQ08
AH5	D1_MDQ07
AH6	USB_STP
AH7	USB_D2
AH8	TSEC_1588_ALARM_OUT2
AH9	CP_SYNC7
AH10	CP_SYNC3
AH11	EVT2_B
AH12	IFC_A24/IFC_WP3_B
AH13	IFC_PAR0/GPIO2[13]
AH14	IFC_A17
AH15	IFC_AD04/CFG_GPINPUT4
AH16	IFC_AD11/CFG_RCW_SRC3
AH17	IFC_A20
AH18	IFC_A19

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AG19	IFC_A21/CFG_DRAM_TYPE
AG20	GND
AG21	SPI_CLK
AG22	SDHC_DAT0/GPIO2[5]
AG23	GND
AG24	IIC2_SDA
AG25	UART2_RTS_B/GPIO1[20]/UART4_SOUT
AG26	GND
AG27	D2_MDQ02
AG28	D2_MDQ05
AG29	D2_MDM0
AG30	D2_MDQ17
AG31	D2_MDQ18
AG32	D2_MDQ20
AJ1	D1_MDQ11
AJ2	D1_MDQ14
AJ3	D1_MDQ12
AJ4	D1_MDQ09
AJ5	GND
AJ6	USB_D3
AJ7	GND
AJ8	EMI2_MDIO
AJ9	CP_SYNC0
AJ10	GND
AJ11	EVT3_B
AJ12	IFC_PAR1/GPIO2[14]
AJ13	GND
AJ14	IFC_A25/GPIO2[25]/IFC_RB2_B/ IFC_FCTA2
AJ15	IFC_A26/GPIO2[26]/IFC_RB3_B/ IFC_FCTA3
AJ16	GND
AJ17	IFC_A27/GPIO2[27]
AJ18	IFC_CS3_B/GPIO2[12]
AJ19	GND

Package pin number	Package Pin Name
AH19	IFC_AD14/CFG_RCW_SRC6
AH20	SPI_CS2_B/GPIO2[2]/SDHC_DAT6
AH21	SDHC_DAT1/GPIO2[6]
AH22	IRQ02
AH23	IRQ03/GPIO1[23]
AH24	IRQ04/GPIO1[24]
AH25	IIC1_SDA
AH26	UART2_SIN/GPIO1[18]
AH27	IIC1_SCL
AH28	D2_MDQ07
AH29	D2_MDQ08
AH30	D2_MDQ13
AH31	GND
AH32	D2_MDM1
AK1	D1_MDQS1_B
AK2	D1_MDQS1
AK3	D1_MDQ10
AK4	USB_D7
AK5	USB_D4
AK6	USB_D5
AK7	TSEC_1588_PULSE_OUT2
AK8	CP_SYNC5
AK9	CP_SYNC6
AK10	ASLEEP/GPIO1[13]/CFG_XVDD_SEL
AK11	CKSTP_OUT_B
AK12	IFC_WE_B/IFC_WBE0
AK13	IFC_CS1_B/GPIO2[10]
AK14	IFC_CS2_B/GPIO2[11]
AK15	IFC_CS0_B
AK16	IFC_OE_B/IFC_RE_B
AK17	IFC_A23/IFC_WP2_B
AK18	IFC_AD07/CFG_GPINPUT7
AK19	SPI_CS1_B/GPIO2[1]/SDHC_DAT5

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AJ20	IFC_A22/IFC_WP1_B
AJ21	SPI_CS0_B/GPIO2[0]/SDHC_DAT4
AJ22	GND
AJ23	IRQ_OUT_B/EVT9_B
AJ24	IRQ10/GPIO1[30]/TMR4
AJ25	GND
AJ26	EMI1_MDC
AJ27	IIC4_SCL/GPIO3[5]/EVT5_B
AJ28	GND
AJ29	D2_MDQ09
AJ30	D2_MDQ12
AJ31	D2_MDQ14
AJ32	D2_MDQ11
AL1	GND
AL2	D1_MDQ15
AL3	GND
AL4	USB_CLK
AL5	USB_NXT
AL6	GND
AL7	DMA1_DACK0_B/GPIO3[1]/EVT7_B/TMR6
AL8	CP_SYNC4
AL9	GND
AL10	CP_RCLK0
AL11	CP_RCLK1
AL12	GND
AL13	IFC_AD05/CFG_GPINPUT5
AL14	IFC_WP0_B
AL15	GND
AL16	IFC_BCTL
AL17	IFC_AD06/CFG_GPINPUT6
AL18	GND
AL19	IFC_AVD/IFC_ALE/CFG_RSP_DIS
AL20	SPI_MISO

Package pin number	Package Pin Name
AK20	SDHC_CMD/GPIO2[4]
AK21	IRQ06/GPIO1[26]/TMR0
AK22	IRQ08/GPIO1[28]/TMR2
AK23	IRQ05/GPIO1[25]
AK24	IRQ07/GPIO1[27]/TMR1
AK25	TRST_B
AK26	EMI1_MDIO
AK27	CP_LOS1
AK28	UART2_CTS_B/GPIO1[22]/UART4_SIN
AK29	IIC3_SDA/GPIO3[4]
AK30	D2_MDQ10
AK31	D2_MDQS1
AK32	D2_MDQS1_B
AM1	—
AM2	GND
AM3	TSEC_1588_CLK_IN
AM4	USB_D6
AM5	USB_DIR
AM6	DMA1_DREQ0_B/GPIO3[0]
AM7	DMA1_DDONE0_B/GPIO3[2]/EVT8_B/TMR7
AM8	EMI2_MDC
AM9	RESET_REQ_B
AM10	CP_RCLK0_B
AM11	CP_RCLK1_B
AM12	HRESET_B
AM13	CLK_OUT
AM14	IFC_CLE/IFC_WBE1/CFG_RCW_SRC8
AM15	IFC_RB0_B/IFC_FCTA0
AM16	IFC_TE/CFG_IFC_TE
AM17	IFC_RB1_B/IFC_FCTA1
AM18	IFC_CLK0
AM19	IFC_CLK1
AM20	SPI_CS3_B/GPIO2[3]/SDHC_DAT7

Table 2. Pinout by package pin number (continued)

Package pin number	Package pin name
AL21	GND
AL22	SDHC_DAT2/GPIO2[7]
AL23	IRQ11/GPIO1[31]/TMR5
AL24	GND
AL25	TDO
AL26	TCK
AL27	GND
AL28	CP_LOS3
AL29	UART1_SOUT/GPIO1[15]/CP_LOS4
AL30	GND
AL31	D2_MDQ15
AL32	GND

Package pin number	Package Pin Name
AM21	SPI_MOSI
AM22	SDHC_CLK/GPIO2[9]
AM23	RTC/GPIO1[14]
AM24	IRQ09/GPIO1[29]/TMR3
AM25	TMS
AM26	TDI
AM27	CP_LOS2
AM28	UART1_SIN/GPIO1[17]/CP_LOS5
AM29	CP_LOS0
AM30	IIC3_SCL/GPIO3[3]
AM31	GND
AM32	—

2 Electrical characteristics

This section provides the AC and DC electrical specifications for the chip.

2.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

2.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 3. Absolute operating conditions[1]

Parameter	Symbol	Recommended value	Unit	Notes
Platform and cores supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage: • CGA1 PLL • CGA2 PLL • CGB1 PLL • CGB2 PLL • Platform PLL • DDR1 PLL • DDR2 PLL	 AV_{DD}_CGA1 AV_{DD}_CGA2 AV_{DD}_CGB1 AV_{DD}_CGB2 AV_{DD}_PLAT AV_{DD}_DDR1 AV_{DD}_DDR2	–0.3 to 1.9	V	—
PLL supply voltage (SerDes) • SerDes1 PLL1 • SerDes1 PLL2 • SerDes2 PLL1 • SerDes2 PLL2	 AV_{DD}_SRDS1_PLL1 AV_{DD}_SRDS1_PLL2 AV_{DD}_SRDS2_PLL1 AV_{DD}_SRDS2_PLL2	–0.3 to 1.45/1.6	V	—
Fuse programming override supply	POV_{DD}	–0.3 to 1.99	V	—
Thermal monitor unit supply	TH_V_{DD}	–0.3 to 1.90	V	5
UART, I2C, CPRI LOS and GPIO I/O voltage	DV_{DD}	–0.3 to 1.9 V/2.6	V	—
IFC, SPI, (e)SDHC, MPIC, Trust, power management, clocking, debug, JTAG, CPRI SYNC/RCLK, 1588, Ethernet MI, USB ULPI, DMA, GPIO, system control I/O voltage	OV_{DD}	–0.3 to 1.9	V	—
SYSCLK, PORESET_B I/O voltage	QV_{DD}	–0.3 to 1.9	V	—
DDR DRAM I/O voltage • DDR1 • DDR2	 $G1V_{DD}$ $G2V_{DD}$	–0.3 to 1.45/1.6	V	2
Core power supply for SerDes receivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transmitters	XV_{DD}	–0.3 to 1.45/1.6	V	—

Table 3. Absolute operating conditions[1] (continued)

Parameter		Symbol	Recommended value	Unit	Notes
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GnV_{DD} + 0.3)	V	2
	DDR DRAM reference	MnV_{REF}	–0.3 to (GnV_{DD}/2 + 0.3)	V	—
	UART, I2C, Ethernet MI1, CPRI LOS and GPIO signals	QV_{IN}	–0.3 to (DV_{DD} + 0.3)	V	3
	SYSCLK and PORESET_B signals	QV_{IN}	–0.3 to (QV_{DD} + 0.3)	V	4
	IFC, SPI, (e)SDHC, MPIC, Trust, power management, clocking, debug, JTAG, CPRI SYNC/RCLK, 1588, USB ULPI, DMA, GPIO, system signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3
	Ethernet Management Interface (EMI2)	—	–0.3 to 1.98	V	6
	SerDes signals	SV_{IN}	–0.4 to (SV_{DD} + 0.3)	V	—
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

Note:

1. Functional operating conditions are given in Table 4. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GnV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** QV_{IN} must not exceed QV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. The Thermal Monitoring Unit (TMU) supply is defeatured on this device. TH_VDD should be connected to an OV_{DD} supply.
6. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. OV_{DD} must be powered to use this interface.

2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 4. Recommended operating conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	At initial start-up	V_{DD}	1.05 V ± 30 mV	V	4, 5, 6
	During normal operation		VID ± 30 mV	V	1, 4, 5
PLL supply voltage (core, platform, DDR)		AV_{DD}_CGAn AV_{DD}_CGBn AV_{DD}_PLAT AV_{DD}_DDRn	1.8 V ± 90 mV	V	—

Table 4. Recommended operating conditions (continued)

PLL supply voltage (SerDes, filtered from XnVDD)		AV_{DD}_SDRSn_PLLn	1.5 V ± 75 mV 1.35 V ± 67 mV	V	—
Fuse programming override supply		POV_{DD}	1.8 V ± 90 mV	V	2
IFC, eSPI, eSHDC, MPIC, trust (TMP_DETECT_B), system control (HRESET_B), power management (ASLEEP), DDRCLK, RTC, debug (EVT*, CKSTP_OUT_B, CLK_OUT), JTAG, CPRI SYNC/RCLK, 1588, US ULPI, DMA		OV_{DD}	1.8 V ± 90 mV	V	—
UART, I2C, Ethernet MI1, CPRI LOS, and GPIO I/O voltage		DV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
SYSCLK and PORESET I/O voltage		QV_{DD}	1.8 V ± 90mV	V	7
DDR DRAM I/O voltage	DDR3	GnV_{DD}	1.5 V ± 75 mV	V	—
	DDR3L		1.35 V ± 67 mV		—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SV_{DD}	1.0 V +50mV/-30mV	V	—
Pad power supply for SerDes transmitters		XV_{DD}	1.5 V ± 75 mV 1.35 V ± 67 mV	V	—
Ethernet management interface 2 (EMI2) I/O voltage		—	1.2 V ± 60 mV	V	8
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GnV_{DD}	V	—
	DDR3 and DDR3L DRAM reference	Dn_MV_{REF}	GnV_{DD}/2 ± 1%	V	—
	UART, I^2C, Ethernet MI1, CPRI LOS and GPIO signals	DV_{IN}	GND to DV_{DD}	V	—
	eSHDC, eSPI, DMA, MPIC, GPIO, system control and power management, clocking, debug, IFC, Dn_DDRCLK supply, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
	SYSCLK, PORESET signals	QV_{IN}	GND to QV_{DD}	V	—
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	—
	Ethernet management interface 2 (EMI2) signals	—	GND to 1.2 V	V	3

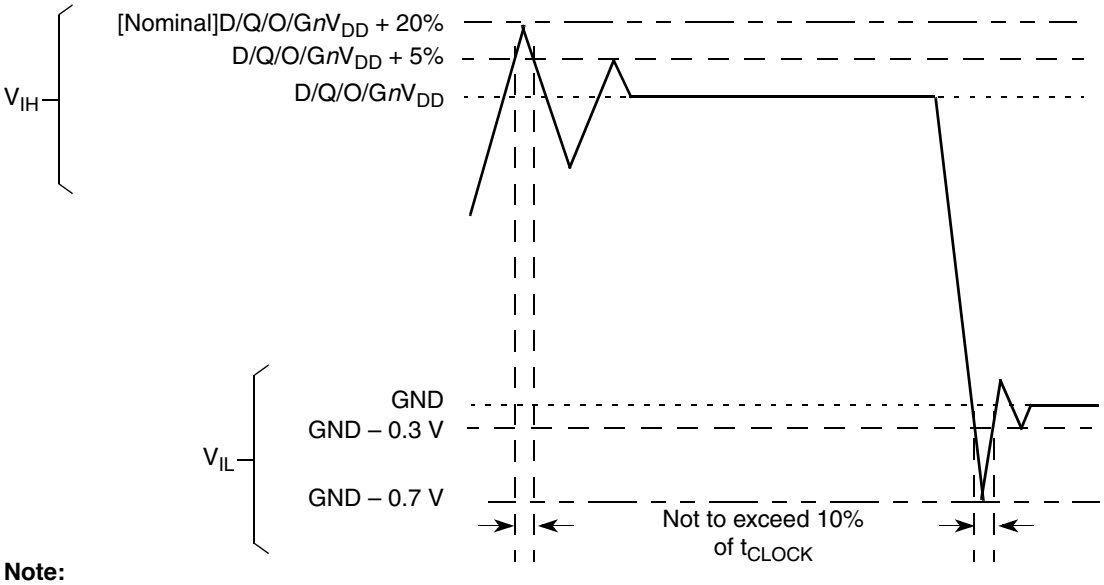
Table 4. Recommended operating conditions (continued)

Operating temperature range	Normal operation	TA, TJ	TA = 0 (min) to TJ = 105 (max)	°C	—
	Extended Temperature	TA, TJ	TA = -40 (min) to TJ = 105 (max)	°C	—
	Secure boot fuse programming	TA, TJ	TA = 0 (min) to TJ = 70 (max)	°C	2

Note:

1. The Voltage ID (VID) operating range is between 0.95 V and 1.05 V. Regulator selection should be based on a Vout range of at least 0.9 V to 1.1 V, with resolution of 12.5 mV or better. See Section 3.2.1, "Voltage ID (VID) controllable supply" for more details.
2. POV_{DD} must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only –0 –70°C during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power sequencing."
3. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels.
4. See Section 3.2.2, "Core supply voltage filtering," for additional information.
5. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
6. Operation at 1.05 V is allowable for up to 1 second at initial power on.
7. Add a bypass cap of 0.1uF on this power ball pin.
8. These pins should be pulled up to 1.2 V through a 180 Ω (1% accuracy) resistor for EMI2_MDC and 330 Ω (1% accuracy) resistor for EMI2_MDIO. When Ethernet Management Interface 2 unused, EMI2_MDIO's external pull-up resistor can be tied to OV_{DD}

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:
t_{CLOCK} refers to the clock period associated with the respective interface:
For I2C and JTAG, t_{CLOCK} refers to SYSCLK.
For DDR GnV$_{DD}$, t_{CLOCK} refers to Dn_DDRCLK.
For SPI OV$_{DD}$, t_{CLOCK} refers to SPI_CLK.
For SerDes XV$_{DD}$, t_{CLOCK} refers to SD_REF_CLK.

Figure 7. Overshoot/Undershoot voltage for DV$_{DD}$/QV$_{DD}$/OV$_D$D/GnV$_{DD}$

See Table 4 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 4. The input voltage threshold scales with respect to the associated I/O supply voltage. DVDD, QVDD, and OVDD-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied MnVREF signal (nominally set to GnVDD/2) as is appropriate for the SSTL_1.35/SSTL_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths. These values are preliminary estimates.

Table 5. Output drive capability

Driver type	Output impedance (Ω)	Supply voltage	Notes
DDR3 signal	18 (full-strength mode) 27 (half-strength mode)	GnV$_{DD}$= 1.5 V	1

Table 5. Output drive capability (continued)

Driver type	Output impedance (Ω)	Supply voltage	Notes
DDR3L signal	18 (full-strength mode) 27 (half-strength mode)	G*n*V_{DD} = 1.35 V	1
IFC, eSPI, eSDHC, MPIC, Trust, power management, clocking, debug, JTAG, CPRI SYNC/RCLK, 1588, USB ULPI, DMA, GPIO, system control, Reset	45	OV_{DD} = 1.8 V	—
DUART, I^2C, Ethernet MI, CPRI-LOS, GPIO	45	DV_{DD} = 2.5 V DV_{DD} = 1.8 V	—

Note:

1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at G*n*V_{DD} (min).

2.2 Power sequencing

The chip requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For power up, these requirements are as follows:

1. There are no restrictions on the order of Power supplies bringing up. During power up, drive POV_{DD} = GND.
   — PORESET_B input must be driven asserted and held during this step.
2. Negate PORESET_B input as long as the required assertion/hold time has been met per Table 13.
3. For secure boot fuse programming, use the following steps:
   a) After negation of PORESET_B, drive POV_{DD} = 1.8 V after a required minimum delay per Table 6.
   b) After fuse programming is completed, it is required to return POV_{DD} = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 6. See Section 5, "Security fuse processor," for additional details.

WARNING

No activity other than that required for secure boot fuse programming is permitted while POV_{DD} is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND.

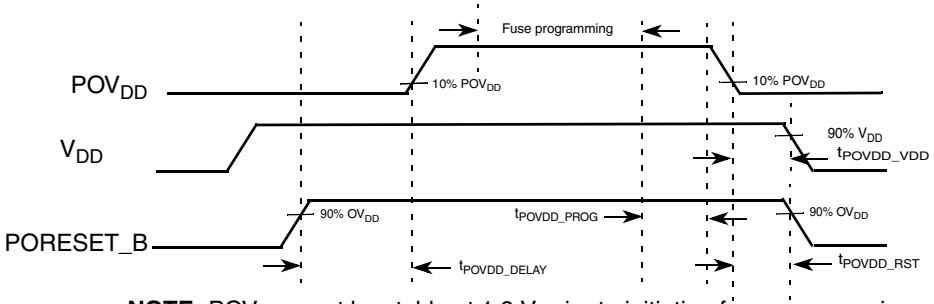
From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

WARNING

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

All supplies must be at their stable values within 75 ms.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.8 V prior to initiating fuse programming.

Figure 8. POV_{DD} timing diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 6. POV_{DD} timing[5]

Driver type	Min	Max	Unit	Notes
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the deassertion of PORESET_B to driving POV_{DD} ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to V_{DD} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD} is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to PORESET_B assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before PORESET_B assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

NOTE

While VDD is ramping, current may be supplied from VDD through the chip to G*n*V_{DD}. Nevertheless, G*n*V_{DD} from an external supply should follow the sequencing described above.

2.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power sequencing," it is required that POV_{DD} = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 6.

2.4 Power characteristics

Because it depends strongly on application type, the power characteristics for the average power and instantaneous peak current numbers are supplied by the device's detailed power calculator.

2.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 7. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/ G*n*V_{DD}/QV_{DD}/SV_{DD}/XV_{DD}, core V_{DD} supply, M*n*V_{REF} and all AV_{DD} supplies.)	—	25	V/ms	1, 2
Required ramp rate for POV_{DD}	—	25	V/ms	1, 2

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If nonlinear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. If needed to slow down the rate, usage of larger capacitors is recommended.
2. Over full recommended operating temperature range (see Table 4)

2.6 Input clocks

2.6.1 System clock (SYSCLK) timing specifications

This section provides the system clock DC and AC timing specifications.

2.6.1.1 System clock DC timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 8. SYSCLK DC electrical characteristics

At recommended operating conditions with QV_{DD} = 1.8 V, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = QV_{DD})	I_{IN}	—	—	± 50	µA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max QV_{IN} values found in Table 4.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.6.1.2 System clock AC timing specifications

This table provides the system clock (SYSCLK) AC timing specifications.

Table 9. SYSCLK AC timing specifications

At recommended operating conditions with OV_{DD} = 1.8 V, see Table 4.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66.667	—	133.333	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	50	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	±150	ps	—
SYSCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 1.8 V QV_{DD}	ΔV_{AC}	0.35 x QV_{DD}	—	0.65 x QV_{DD}	V	—

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $QV_{DD}/2$.
3. Slew rate is measured from 10% ~ 90% of V_{IL} to V_{IH}.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 10. Spread-spectrum clock source recommendations

At recommended operating conditions with OVDD = 1.8 V, see Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	—	60	kHz	—
Frequency spread	—	1.0	%	1, 2

Notes:
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 9.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

2.6.3 Real-time clock timing

The real-time clock timing (RTC) input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16× the period of the platform clock with a 50% duty cycle. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.6.4 DDR clock timing

2.6.4.1 DDR D1_DDRCLK/D2_DDRCLK clocks DC timing specifications

This table provides the system clock (MCLK) DC specifications.

Table 11. D1_DDRCLK[3]/D2_DDRCLK DC electrical characteristics

At recommended operating conditions with OV_{DD} = 1.8v, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance	C_{IN}	—	7	12	pF	—
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	± 50	μA	2

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 4.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”
3. D1_DDRCLK must toggle in order to get out of PORESET, even if the DDR1 interface is not required. AV_{DD}_DDR1 voltage must be supplied.

2.6.4.2 DDR D1_DDRCLK/D2_DDRCLK clocks AC timing specifications

This table provides the system clock (D1_DDRCLK/D2_DDRCLK) AC timing specifications.

Table 12. D*n*_DDRCLK AC timing specifications

At recommended operating conditions with OV_{DD} = 1.8V, see Table 4.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
D*n*_DDRCLK frequency	f_{MCLK}	66.667	—	133.333	MHz	1, 2
D*n*_DDRCLK cycle time	t_{MCLK}	7.5	—	15	ns	1, 2
D*n*_DDRCLK duty cycle	t_{KHK}/t_{MCLK}	40	50	60	%	2
D*n*_DDRCLK slew rate	—	1	—	4	V/ns	3

Table 12. D*n*_DDRCLK AC timing specifications (continued)

At recommended operating conditions with OV_{DD} = 1.8V, see Table 4.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
D*n*_DDRCLK peak period jitter	—	—	—	± 150	ps	—
D*n*_DDRCLK jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC Input Swing Limits at 1.8 V OV_{DD}	ΔV_{AC}	0.35 x OV_{DD}	—	0.65 x OV_{DD}	V	—

Notes:
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting D1_DDRCLK/D2_DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate is measured from 10% ~ 90% of V_{IL} to V_{IH}.
4. Phase noise is calculated as FFT of TIE jitter.

2.6.5 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, I2C, eSDHC, IFC, USB, and 1588, see the specific interface section.

2.7 RESET initialization

This table describes the AC electrical specifications for the RESET initialization timing.

Table 13. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	—	ms	3
Required input assertion time of HRESET_B	32	—	SYSCLKs	1, 2
Maximum rise/fall time of HRESET_B	—	1	SYSCLK	4
PLL input setup time with stable SYSCLK before HRESET_B negation	100	—	µs	—
Input setup time for POR configs with respect to negation of PORESET_B	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of PORESET_B	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the chip.
2. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in the “Power-On Reset Sequence” section of the chip reference manual.
3. PORESET_B must be driven asserted before the core and platform power supplies are powered up.
4. The system/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

This table provides the PLL lock times.

Table 14. PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

2.8 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required G*n*V_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the G*n*V_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at DDR data rates of 1866 MT/s, only one dual-ranked module per memory controller is supported.

2.8.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 15. DDR3 SDRAM interface DC electrical characteristics (G*n*V_{DD} = 1.5 V)[1]

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	M*n*V_{REF}	0.49 × G*n*V_{DD}	0.51 × G*n*V_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	M*n*V_{REF} + 0.100	G*n*V_{DD}	V	5
Input low voltage	V_{IL}	GND	M*n*V_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	µA	6

Notes:

1. G*n*V_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. M*n*$V_{REF}$is expected to be equal to 0.5 × G*n*V_{DD} and to track G*n*V_{DD} DC variations as measured at the receiver. Peak-to-peak noise on M*n*V_{REF}may not exceed the M*n*V_{REF}DC level by more than ±1% of the DC value (that is, ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to M*n*$V_{REF}$with a min value of M*n*V_{REF} – 0.04 and a max value of M*n*V_{REF} + 0.04. V_{TT} should track variations in the DC level of M*n*V_{REF}.
4. The voltage regulator for M*n*V_{REF}must meet the specifications stated in Table 18.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ G*n*V_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 16. DDR3L SDRAM interface DC electrical characteristics (G*n*V_{DD} = 1.35 V)[1]

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	M*n*V_{REF}	0.49 × G*n*V_{DD}	0.51 × G*n*V_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	M*n*V_{REF} + 0.090	G*n*V_{DD}	V	5
Input low voltage	V_{IL}	GND	M*n*V_{REF} – 0.090	V	5
I/O leakage current	I_{OZ}	–100	100	µA	6

Notes:

1. G*n*V_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. M*n*V_{REF} is expected to be equal to 0.5 × G*n*V_{DD} and to track G*n*V_{DD} DC variations as measured at the receiver. Peak-to-peak noise on M*n*V_{REF} may not exceed the M*n*V_{REF} DC level by more than ±1% of the DC value (that is, ±13.5mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to M*n*V_{REF} with a min value of M*n*V_{REF} – 0.04 and a max value of M*n*V_{REF} + 0.04. V_{TT} should track variations in the DC level of M*n*V_{REF}.
4. The voltage regulator for M*n*V_{REF} must meet the specifications stated in Table 18.
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ G*n*V_{DD}.
7. See the IBIS model for the complete output IV curve characteristics.

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 17. DDR3 and DDR3L SDRAM capacitance

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, DQS_B	C_{IO}	6	8	pF	—
Delta input/output capacitance: DQ, DQS, DQS_B	C_{DIO}	—	0.5	pF	—

This table provides the current draw characteristics for M*n*V_{REF}.

Table 18. Current draw characteristics for M*n*V_{REF}

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3 SDRAM for M*n*V_{REF}	I_{MnVREF}	—	500	µA	—
Current draw for DDR3L SDRAM for M*n*V_{REF}	I_{MnVREF}	—	500	µA	—

2.8.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required G*n*V_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the required G*n*V_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 19. DDR3 and DDR3L SDRAM interface input AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}			ps	1
1866 MT/s data rate		–93	93		
1600 MT/s data rate		–112	112		
1333 MT/s data rate		–125	125		
1200 MT/s data rate		–142	142		
1066 MT/s data rate		–170	170		
Tolerated Skew for MDQS—MDQ/MECC	t_{DISKEW}			ps	2
1866 MT/s data rate		–175	175		
1600 MT/s data rate		–200	200		
1333 MT/s data rate		–250	250		
1200 MT/s data rate		–275	275		
1066 MT/s data rate		–300	300		

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

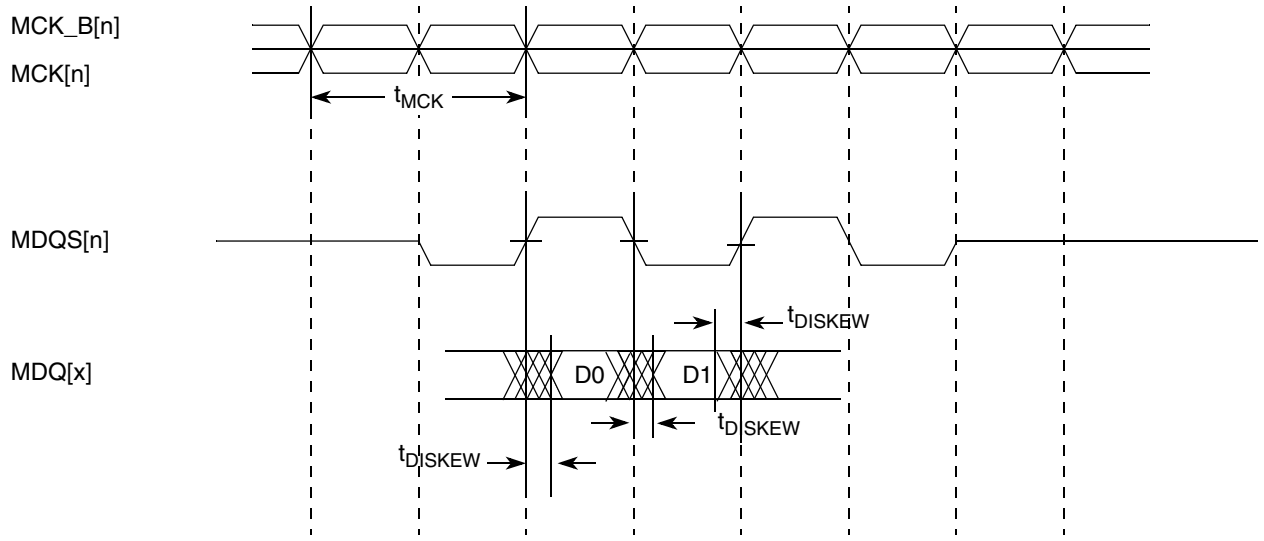


Figure 9. DDR3 and DDR3L SDRAM interface input timing diagram

2.8.2.2 DDR3 and DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 20. DDR3 and DDR3L SDRAM interface output AC timing specifications

For recommended operating conditions, see Table 4

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.072	1.876	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1866 MT/s data rate		0.410	—		
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1866 MT/s data rate		0.390	—		
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
MCK to MDQS skew	t_{DDKHMH}			ns	4
> 1600 MT/s data rate		-0.150	-0.150		4,6
data rate > 1066MT/s & =< 1600 MT/s		-0.245	0.245		4,6

Table 20. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)

For recommended operating conditions, see Table 4

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output Data eye	$t_{DDKXDEYE}$			ns	5
1866 MT/s data rate		0.350	—		
1600 MT/s data rate		0.400	—		
1333 MT/s data rate		0.500	—		
1200 MT/s data rate		0.550	—		
1066 MT/s data rate		0.600	—		
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	—	ns	—
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.
2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.
6. For data rates of 1200 MT/s and higher, it is required to program the start value of the DQS adjust for write leveling.

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

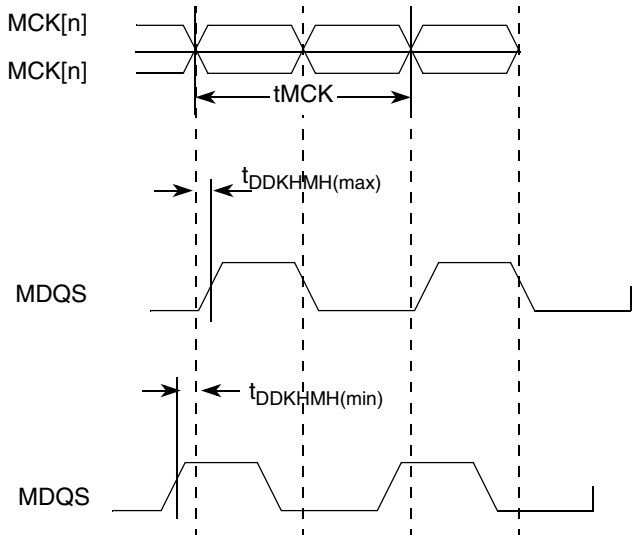


Figure 10. t_{DDKHMH} timing diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

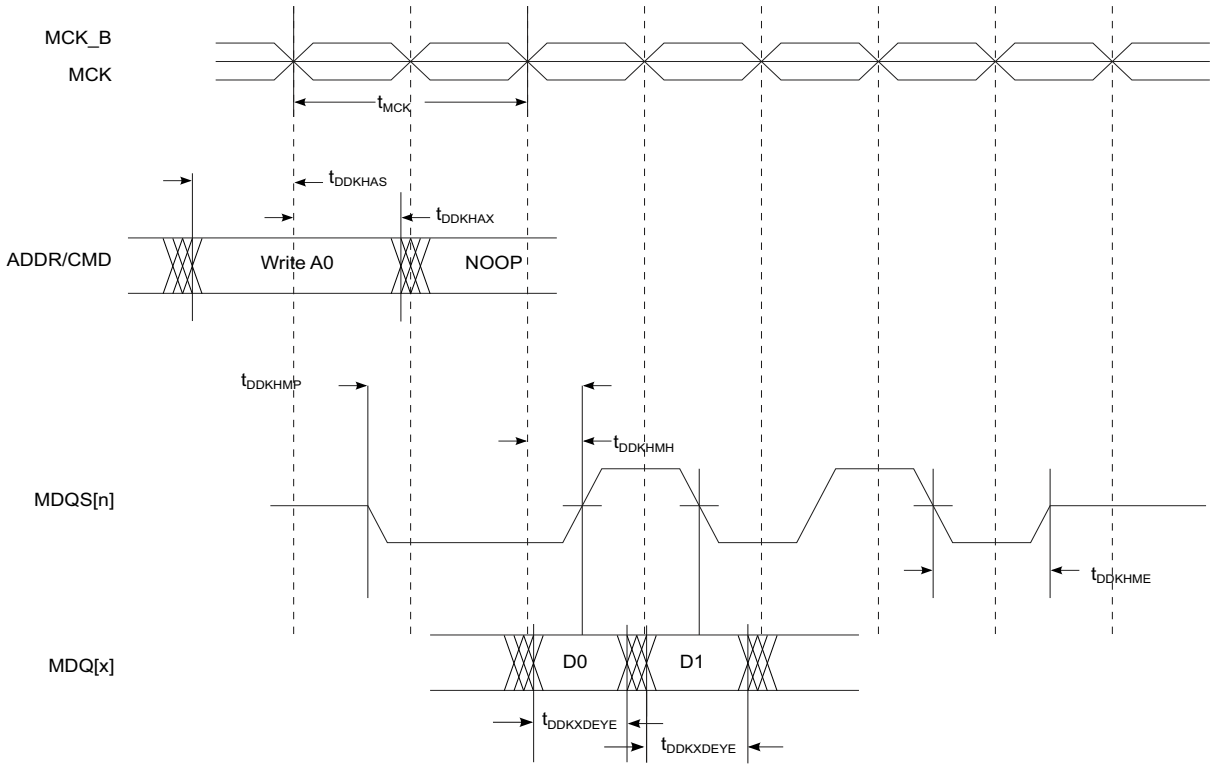


Figure 11. DDR3 and DDR3L output timing diagram

2.9 DC electrical characteristics

2.9.1 DC characteristics for 1.8 V IO cells

This table provides the DC electrical characteristics for the IFC, SPI, MPIC, Trust, power management, clocking, debug, JTAG, CPRI SYNC/RCLK, 1588, eSDHC, USB ULPI, DMA, Timers, UART and GPIO interface operating at VDDIO = $OV_{DD}/QV_{DD}/DV_{DD}$= 1.8 V.

Table 21. DC electrical characteristics (1.8 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
High-level output voltage	V_{OH}		—	—	V	—
I_{OH} = 1 mA		$VDDIO_{MIN}$ – 0.15				
I_{OH} = 2 mA		$VDDIO_{MIN}$ x 0.8				
I_{OH} = -100uA		$VDDIO_{MIN}$ – 0.2				3
Low-level output voltage	V_{OL}	—	—		V	—
I_{OL} = 1 mA				0.15		
I_{OL} = 2 mA				0.2 x $VDDIO_{MAX}$		
I_{OL} = 2 mA				0.3		3
Input current (V_{IN} = 0 V or V_{IN} = $OV_{DD}/QV_{DD}/DV_{DD}$)	I_{IN}	—	—	±50	µA	2
High-level DC input voltage	V_{IH}	0.7 x $VDDIO_{MAX}$	—	—	V	1
Low-level DC input voltage	V_{IL}	—	—	0.3 x $VDDIO_{MIN}$	V	1

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN}/QV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the OV_{IN}/QV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”
3. eSDHC protocol open-drain mode for MMC cards only.

2.9.2 DC characteristics for 2.5 V IO cells

This table provides the DC electrical characteristics for the UART, Ethernet MI1, and GPIO interface operating at DV_{DD} = 2.5 V.

Table 22. DC electrical characteristics (2.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
High-level output voltage	V_{OH}		—	—	V	—
I_{OH} = 1 mA		$VDDIO_{MIN}$ – 0.15				
I_{OH} = 2 mA		$VDDIO_{MIN}$ x 0.8				
Low-level output voltage	V_{OL}	—	—		V	—
I_{OL} = 1 mA				0.15		
I_{OL} = 2 mA				0.2 x $VDDIO_{MAX}$		

Table 22. DC electrical characteristics (2.5 V) (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD}/QV_{DD}/DV_{DD})	I_{IN}	—	—	±50	μA	2
High-level DC input voltage	V_{IH}	0.7 x $VDDIO_{MAX}$	—	—	V	1
Low-level DC input voltage	V_{IL}	—	—	0.3 x $VDDIO_{MIN}$	V	1

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max QV_{IN} values found in Table 4.
2. The symbol V_{IN}, in this case, represents the QV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.10 eSPI interface

This section describes the AC electrical specifications for the eSPI interface.

2.10.1 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 23. eSPI AC timing specifications[1]

Characteristic	Symbol [2]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	n1 + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	—	ns	2, 3, 4
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	n2 + ($t_{PLATFORM\_CLK/2}$ * SPMODE[HO_ADJ])	ns	2, 3, 4
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
SPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
SPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—
Clock-high/low time	t_{NIKCKH}/ t_{NIKCKL}	4	—	ns	—

Table 23. eSPI AC timing specifications[1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit	Note
CLKOUT period	SPI_CLK	12	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of SPI_CLK to the 50% level of the signal. Timings are measured at the pin.
3. See the chip reference manual for details about the SPMODE register.
4. The optimal n1 and n2 values are –1.0 and 1.0, respectively, based on the AC timing specifications for the majority of the SPI flash devices on the market.

This figure provides the AC test load for the eSPI.

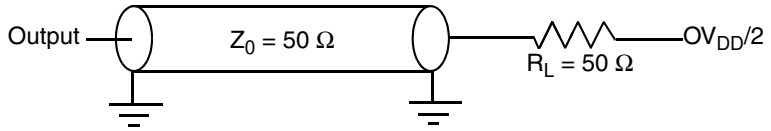


Figure 12. eSPI AC test load

This figure provides the eSPI clock output timing diagram.

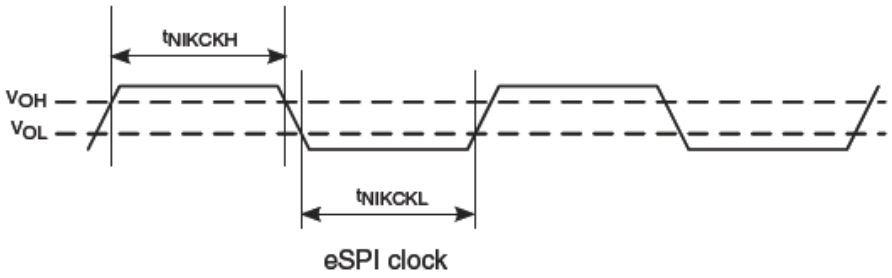


Figure 13. eSPI clock output timing diagram

This figure represents the AC timing from Table 23 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

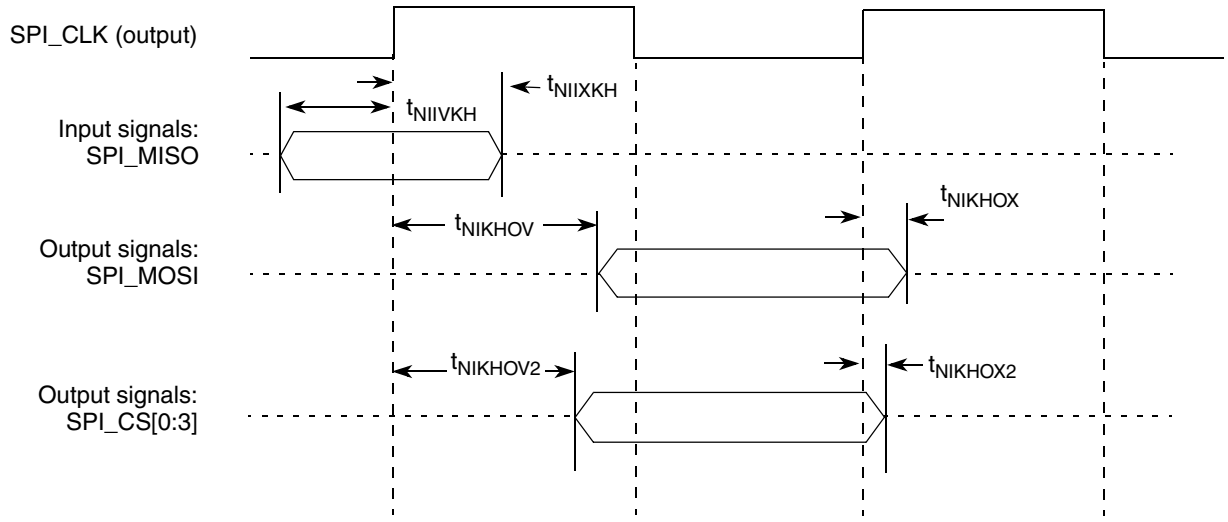


Figure 14. eSPI AC timing in master mode (internal clock) diagram

2.11 DUART interface

This section describes the AC electrical specifications for the DUART interface.

2.11.1 UART AC electrical specifications

This table provides the AC timing parameters for the UART interface.

Table 24. UART AC timing specifications

Parameter	Value	Unit	Notes
Minimum baud rate	$f_{PLAT}/(2 \times 1{,}048{,}576)$	baud	1, 3
Maximum baud rate	$f_{PLAT}/(2 \times 16)$	baud	1, 2

Notes:

1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.12 Ethernet interface, Ethernet management interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interfaces.

2.12.1 SGMII electrical specifications

See Section 2.23.8, "SGMII interface."

2.12.2 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces.

EMI1 is the PHY management interface controlled by the MDIO controller associated with Frame Manager GMAC1-6.

EMI2 is the XAUI, and XFI PHY management interface controlled by the MDIO controller associated with Frame Manager 10GMAC9-10.

Table 22, "DC electrical characteristics (2.5 V)," provides the Ethernet Management interface EMI1 DC electrical characteristics.

2.12.2.1 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC electrical characteristics.

Table 25. Ethernet management interface 1 AC timing specifications [6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(Y\times t_{enet\_clk}) - 4$	—	$(Y\times t_{enet\_clk}) + 4$	ns	3,4,5
MDIO to MDC setup time	t_{MDDVKH}	12.5	—	—	ns	—

Table 25. Ethernet management interface 1 AC timing specifications (continued)[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time.Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state(V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency. MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock MDIO_MDC.In Rev2 the default value of MDIO_CFG [MDIO_CLK_DIV] is 0 means no clock is available. Recommended to configure this field in PBL.
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to Y x Ethernet clock periods ±4 ns.

For example, with an Ethernet clock of 333 MHz, the min/max delay is (5 x 1/333M) = 15 ns ± 4 ns.

Default values for Rev 1: silicon:

MDIO_CFG[MDIO_HOLD] = 3'b010 which selects 5 tenet_clk cycles

Default values for Rev 2 silicon:

MDIO_CFG[MDIO_HOLD] = 3'b010 which selects 5 tenet_clk cycles

MDIO_CFG[NEG] = 1

MDIO_CFG[EHOLD] = 0

For Rev 1 silicon: Y = MDIO_CFG[MDIO_HOLD]

For Rev 2 silicon:

If MDIO_CFG[EHOLD] = 0 then Y = MDIO_CFG[MDIO_HOLD]

If MDIO_CFG[EHOLD] = 1 then Y = 8 x MDIO_CFG[MDIO_HOLD] +1

4. t_{MDKHDX} transition:

For Rev 1 silicon: t_{MDKHDX} is MDC positive edge to MDIO transition

For Rev 2 silicon:

If MDIO_CFG[NEG] = 0 then t_{MDKHDX} is MDC positive edge to MDIO transition

If MDIO_CFG[NEG] = 1 then t_{MDKHDX} is MDC negative edge to MDIO transition

5. t_{enet_clk} is the Ethernet clock period derived from Frame Manger clock, FM clock. t_{enet_clk}=1/2 × FM_clock.
6. For recommended operating conditions, see Table 4.

2.12.2.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. OV_{DD} must be powered to use this interface. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 26. Ethernet management interface 2 DC electrical characteristics (1.2 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.84	—	V	—
Input low voltage	V_{IL}	—	0.36	V	—
Output low voltage (I_{OL} = 5.5 mA)	V_{OL}	—	0.2	V	—
Input capacitance	C_{IN}	—	10	pF	—

2.12.2.3 Ethernet management interface 2 AC electrical specifications

This table provides the Ethernet management interface 2 AC electrical characteristics.

Table 27. Ethernet management interface 2 AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(Y\times t_{enet\_clk}) - 4$	—	$(Y\times t_{enet\_clk}) + 4$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	12.5	—	—	ns	6
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time.Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state(V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the Ethernet clock frequency. (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock MDIO_MDC).
3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to Y x Ethernet clock periods ±4 ns.

For example, in default rev1 silicon, with an Ethernet clock of 333 MHz, the min/max delay is (5 x 1/333M) = 15 ns ± 4 ns.

Default values for Rev 1: silicon:

MDIO_CFG[MDIO_HOLD] = 3'b010 which selects 5 tenet_clk cycles

Default values for Rev 2 silicon:

MDIO_CFG[MDIO_HOLD] = 3'b010 which selects 5 tenet_clk cycles

MDIO_CFG[NEG] = 1

MDIO_CFG[EHOLD] = 0

For Rev 1 silicon: Y = MDIO_CFG[MDIO_HOLD]

For Rev 2 silicon:

If MDIO_CFG[EHOLD] = 0 then Y = MDIO_CFG[MDIO_HOLD]

If MDIO_CFG[EHOLD] = 1 then Y = 8 x MDIO_CFG[MDIO_HOLD] +1

4. t_{MDKHDX} transition:

For Rev 1 silicon: t_{MDKHDX} is MDC positive edge to MDIO transition.

For Rev 2 silicon:

If MDIO_CFG[NEG] = 0 then t_{MDKHDX} is MDC positive edge to MDIO transition

If MDIO_CFG[NEG] = 1 then t_{MDKHDX} is MDC negative edge to MDIO transition

5. t_{enet_clk} is the Ethernet clock period derived from Frame Manger clock, FM clock. t_{enet_clk}=1/2 × FM_clock.
6. The actual setup time varies with the MDC slew rate. For a 180 Ω MDC pull-up and 470 pF load, the setup time is expected to be 68 ns measured at 50% points. To ensure setup time is met, the EMI2 clock frequency may need to be reduced from the default setting by selecting a larger clock divider via configuration of MDIO_CFG[MDIO_CLK_DIV] associated with EMI2.
7. For recommended operating conditions, see Table 4.

This figure shows the Ethernet management interface timing diagram.

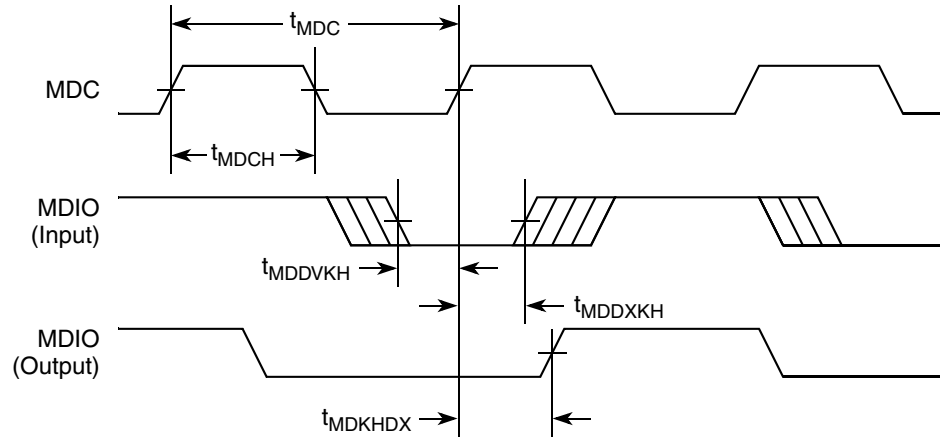


Figure 15. Ethernet management interface timing diagram

2.12.3 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 28. IEEE 1588 AC timing specifications

For recommended operating conditions, see Table 4.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	6.4	—	—	ns	1, 3
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	2
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time TSEC_1588_CLK_IN (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time TSEC_1588_CLK_IN (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT hold time	$t_{T1588OV}$	0.5	—	For rev 1, rev 2.0, rev 2.1: Max $t_{T1588OV}$ = 9.8ns For rev 2.2: Max $t_{T1588OV}$ = 5.3ns	ns	—

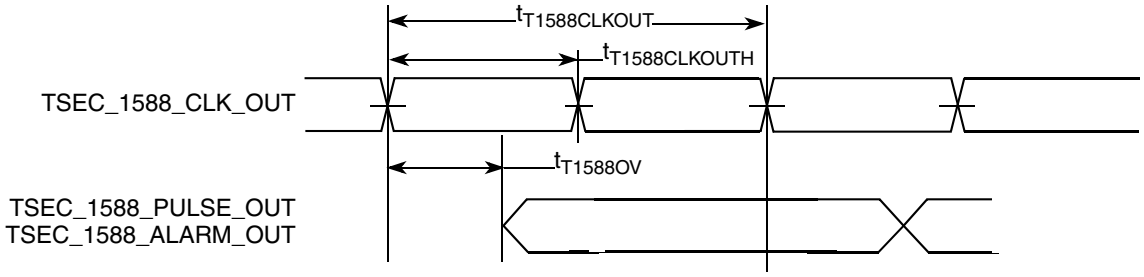
Table 28. IEEE 1588 AC timing specifications (continued)

For recommended operating conditions, see Table 4.

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	3

Notes:
1. T_{RX_CLK} is the maximum clock period of Ethernet receiving clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of the TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ are 2800, 280, and 56 ns, respectively.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 16. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

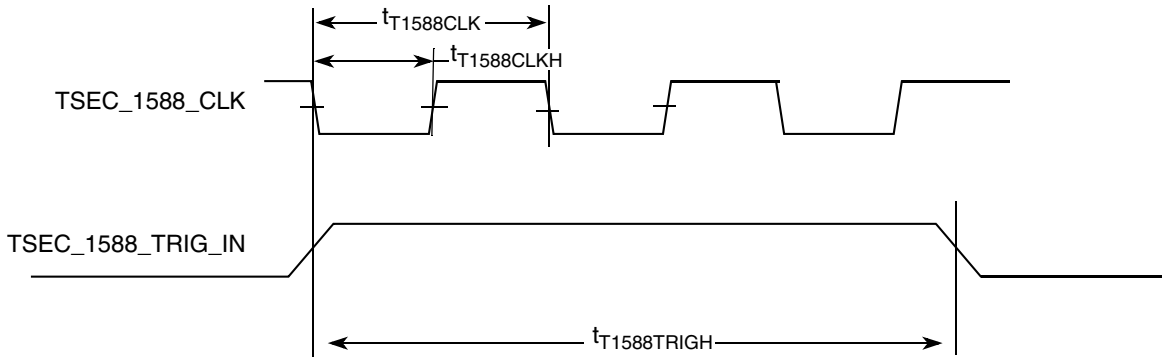


Figure 17. IEEE 1588 input AC timing

2.13 USB interface

This section provides the AC electrical specifications for the USB interface.

2.13.1 USB AC electrical specifications

This table describes the general timing parameters of the USB interface of the device.

Table 29. USB general timing parameters (ULPI mode only) [1,6]

For recommended operating conditions, see Table 4.

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $OV_{DD}/2$ of the signal.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the USB*n*_DIR pin, the output timings are violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per the ULPI specifications.

The following two figures provide the USB AC test load and signals, respectively.

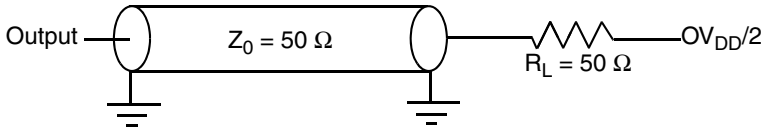


Figure 18. USB AC test load

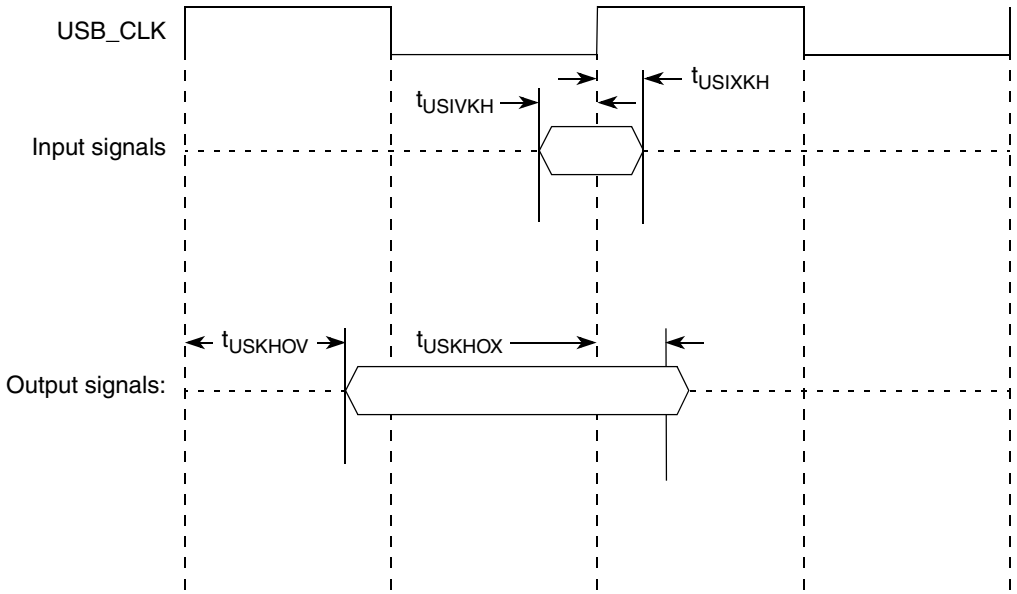


Figure 19. USB signals

2.14 Integrated flash controller

This section describes the AC electrical specifications for the integrated flash controller.

2.14.1 Integrated flash controller AC timing specifications

This section describes the AC timing specifications for the integrated flash controller.

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data.

All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 30. Integrated flash controller timing specifications (OV_{DD} = 1.8 V)

For recommended operating conditions, see Table 4

Parameter	Symbol[1]	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	12	—	ns	—
IFC_CLK duty cycle	t_{IBKH}/t_{IBK}	45	55	%	—
IFC_CLK[n] skew to IFC_CLK[m]	$t_{IBKSKEW}$	—	± 75	ps	2
Input setup	t_{IBIVKH}	4	—	ns	—
Input hold	t_{IBIXKH}	1	—	ns	—

Table 30. Integrated flash controller timing specifications (OV_{DD} = 1.8 V) (continued)

For recommended operating conditions, see Table 4

Parameter	Symbol[1]	Min	Max	Unit	Notes
Output delay	t_{IBKLOV}	—	1.5	ns	—
Output hold	t_{IBKLOX}	–2	—	ns	4
IFC_CLK to output high impedance for AD	t_{IBKLOZ}	—	2	ns	3

Note:

1. All signals are measured from $OV_{DD}/2$ of rising/falling edge of IFC_CLK to $OV_{DD}/2$ of the signal in question.
2. Skew is measured between different IFC_CLK signals at $OV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Here the negative sign means that the output transit happens earlier than the falling edge of IFC_CLK.

This figure shows the AC timing diagram.

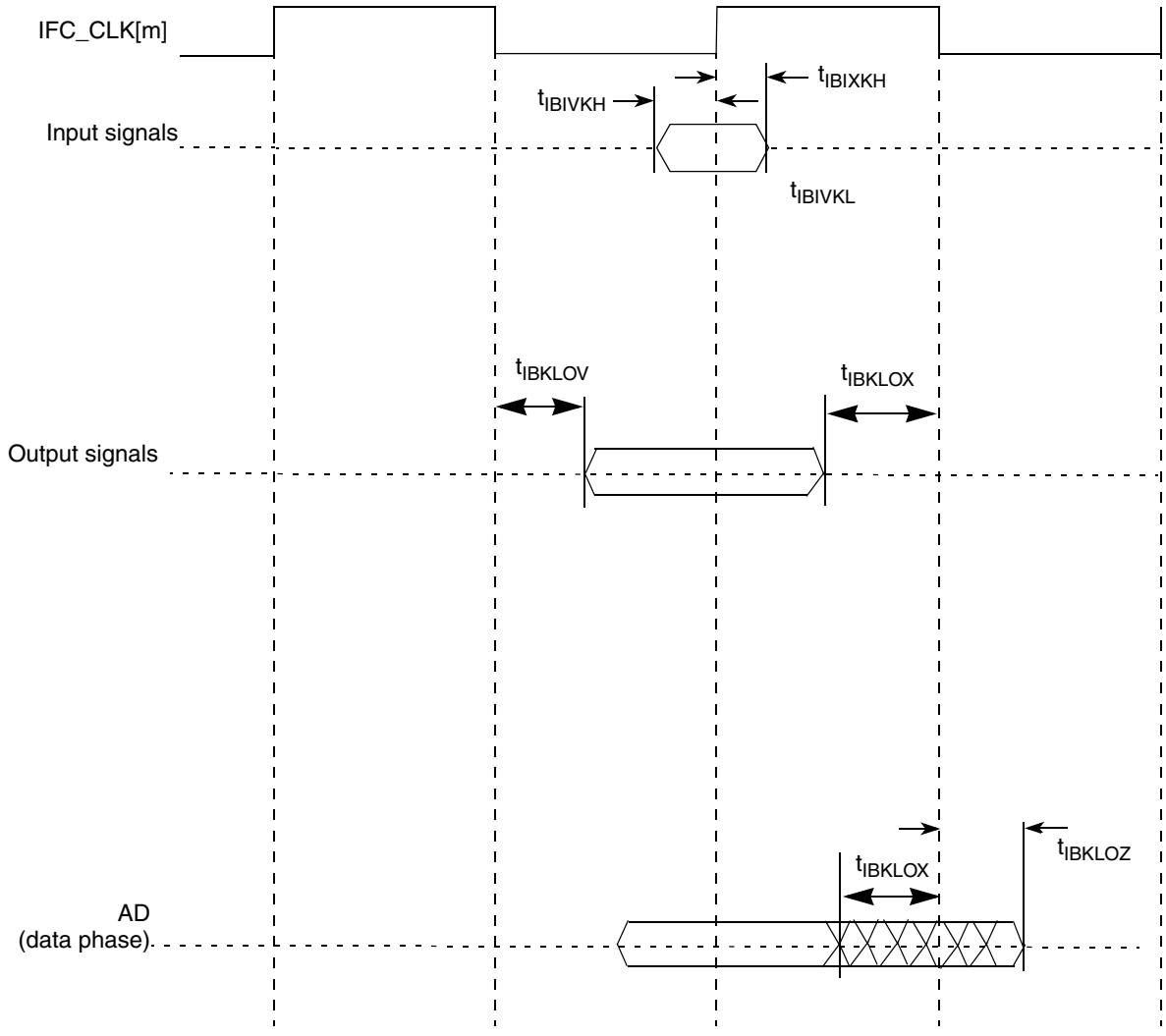
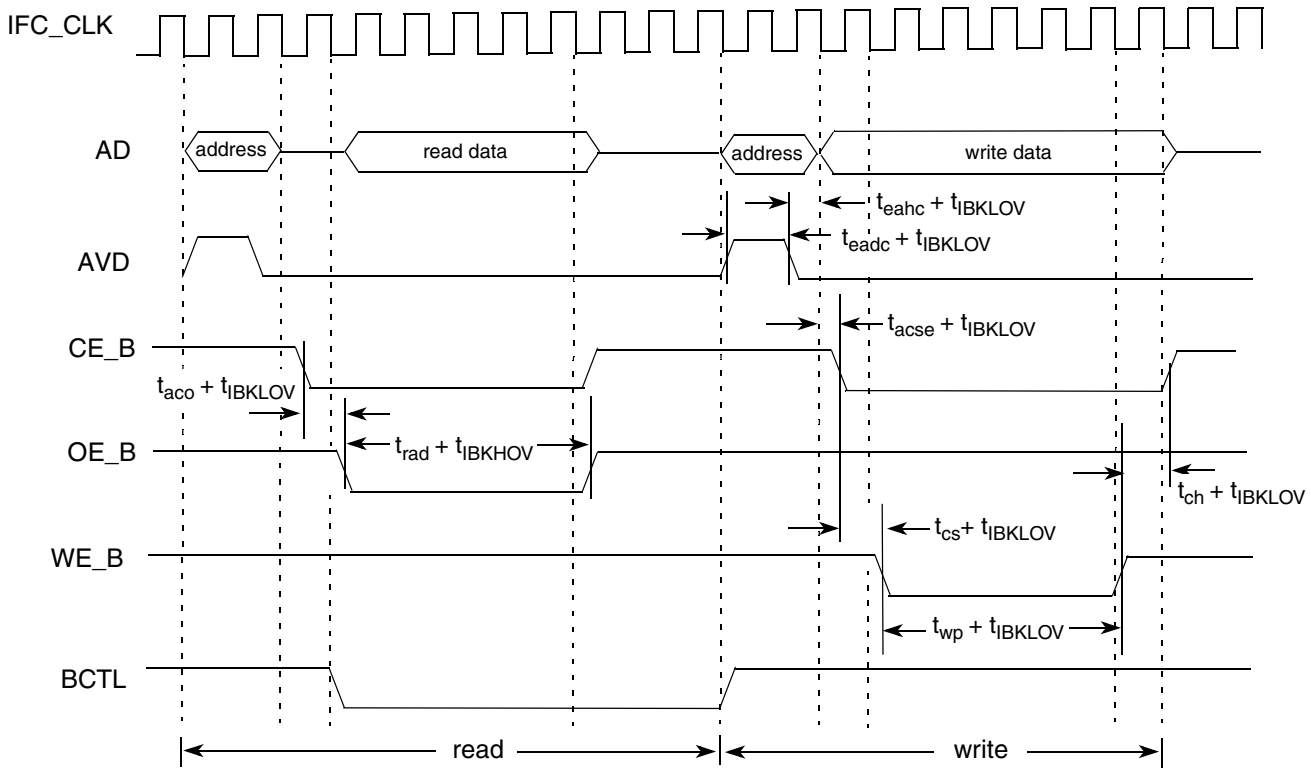


Figure 20. Integrated flash controller signals

Figure 20 applies to all the controllers that IFC supports.

- For input signals, the AC timing data is used directly for all controllers.
- For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.



1 t_{aco}, t_{rad}, t_{eahc}, t_{eadc}, t_{acse}, t_{cs}, t_{ch}, t_{wp} are programmable. See the chip reference manual.
2 For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

Figure 21. GPCM output timing diagram

2.14.2 Test condition

This figure provides the AC test load for the integrated flash controller.

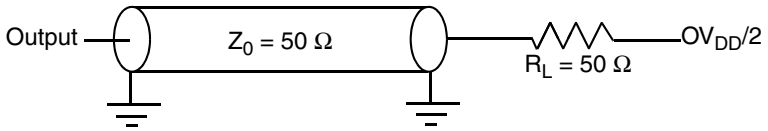


Figure 22. Integrated flash controller AC test load

2.15 Enhanced secure digital host controller (eSDHC)

This section describes the AC electrical specifications for the eSDHC interface. For the DC electrical specifications, see Table 21.

2.15.1 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 23.

Table 31. eSDHC AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SDHC_CLK clock frequency: eMMC Full-speed/high-speed mode	f_{SHSCK}	—	20/52	MHz	2, 4
SDHC_CLK clock low time—full-speed/high-speed mode	t_{SHSCKL}	10/7	—	ns	4
SDHC_CLK clock high time—full-speed/high-speed mode	t_{SHSCKH}	10/7	—	ns	4
SDHC_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIVKH}$	2.5	—	ns	3, 4, 5
Input hold times: SDHC_CMD, SDHC_DATx, SDHC_CD to SDHC_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 5
Output hold time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOX}$	–3	—	ns	4, 5
Output delay time: SDHC_CLK to SDHC_CMD, SDHC_DATx valid	$t_{SHSKHOV}$	—	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–52 MHz for an MMC card.
3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SDHC_CLK, SDHC_CMD, and SDHC_DATx should not exceed 1 ns.
4. $C_{CARD} \le 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \le 40$ pF.
5. The parameter values apply to both full-speed and high-speed modes.

This figure provides the eSDHC clock input timing diagram.

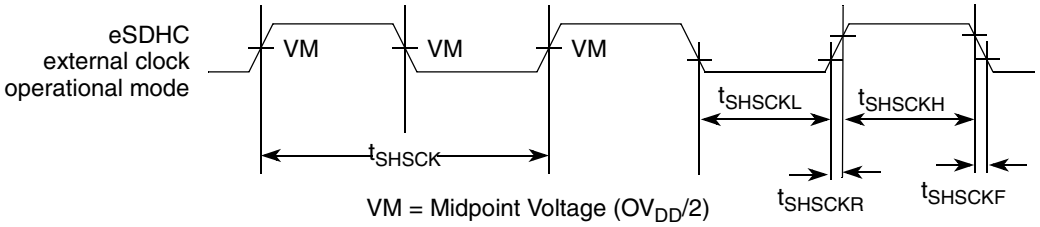


Figure 23. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.

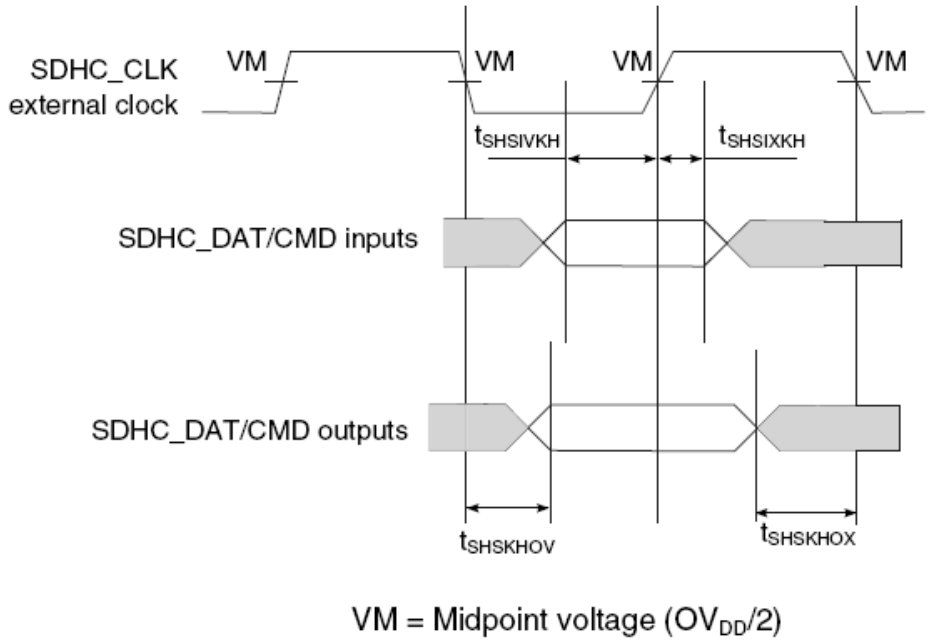


Figure 24. eSDHC data and command input/output timing diagram referenced to clock

2.16 Multicore programmable interrupt controller (MPIC) specifications

This section describes the AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 32. MPIC input AC timing specifications

For recommended operating conditions, see Table 4.

Characteristic	Symbol	Min	Max	Unit	Notes
MPIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLKs	1

Note:

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode

2.17 JTAG controller

This section describes the AC electrical specifications for the IEEE 1149.6 (JTAG) interface.

2.17.1 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 33. JTAG AC timing specifications

For recommended operating conditions, see Table 4

Parameter	Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}/t_{JTGF}	0	2	ns	—
TRST_B assert time	t_{TRST}	25	—	ns	2
Input setup times	t_{JTDVKH}	4	—	ns	—
Input hold times	t_{JTDXKH}	13	—	ns	—
Output valid times TCK to TDO output valid time TCK to boundary-scan data out times	 $t_{JTKLDV1}$ $t_{JTKLDV2}$	 — —	 13 34	ns	4
Output hold times	t_{JTKLDX}	0	—	ns	3

Note:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. Due to value of $t_{JTKLDV1}$, after Update-IR or Update-DR transitions for EXTEST* or CLAMP instructions, a transition through the optional Run-Test-Idle state is recommended to allow for board level propagation and setup times of observation points.

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

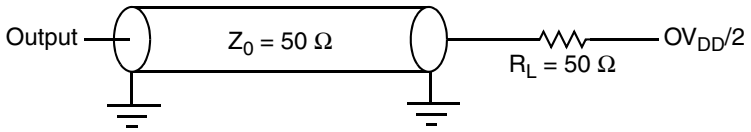


Figure 25. AC test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

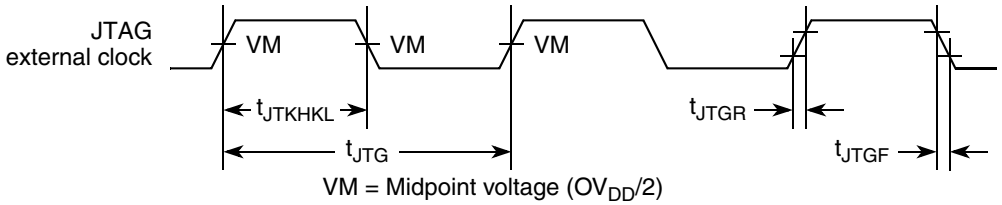


Figure 26. JTAG clock input timing diagram

This figure provides the TRST_B timing diagram.

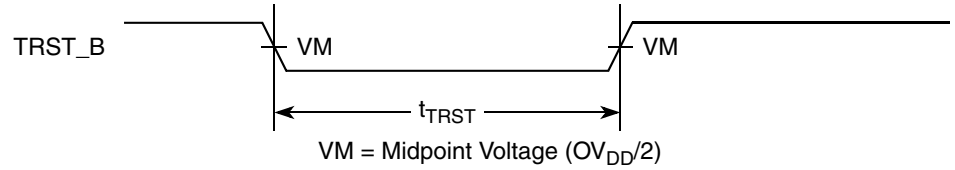


Figure 27. TRST_B timing diagram

This figure provides the TDI/TMS/TDO and boundary-scan data timing diagram.

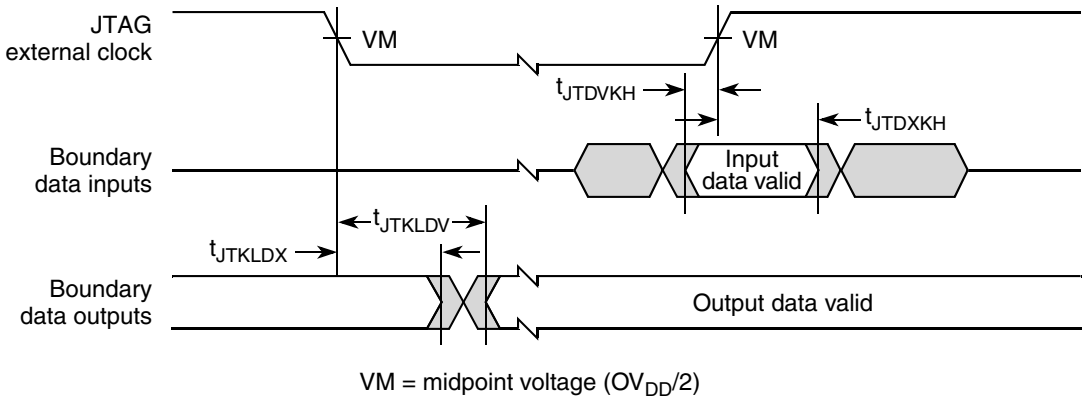


Figure 28. TDI/TMS/TDO and boundary-scan timing diagram

2.18 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

2.18.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at 2.5 V.

Table 34. I²C DC electrical characteristics (DV_{DD} = 2.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × DV_{DD} and 0.9 × DV_{DD}(max)	I_{IN}	—	±50	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max QV_{IN} values found in Table 4.
2. Output voltage (open drain or open collector) condition = 2 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

This table provides the DC electrical characteristics for the I²C interfaces operating at 1.8 V.

Table 35. I²C DC electrical characteristics (DV_{DD} = 1.8 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × DV_{DD} and 0.9 × DV_{DD}(max)	I_{IN}	—	±50	μA	4
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max QV_{IN} values found in Table 4.
2. Output voltage (open drain or open collector) condition = 2 mA sink current.
3. See the chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.

2.18.2 I²C AC timing specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 36. I²C AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	µs	—
High period of the SCL clock	t_{I2CH}	0.6	—	µs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	µs	3
Data output delay time	t_{I2OVKL}	—	0.9	µs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	µs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times DV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times DV_{DD}$	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).
4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I^2C.

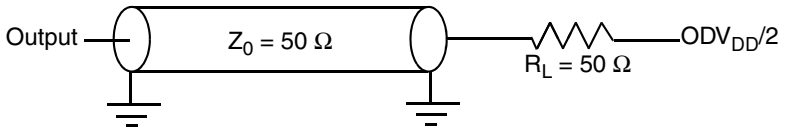


Figure 29. I^2C AC test load

This figure shows the AC timing diagram for the I^2C bus.

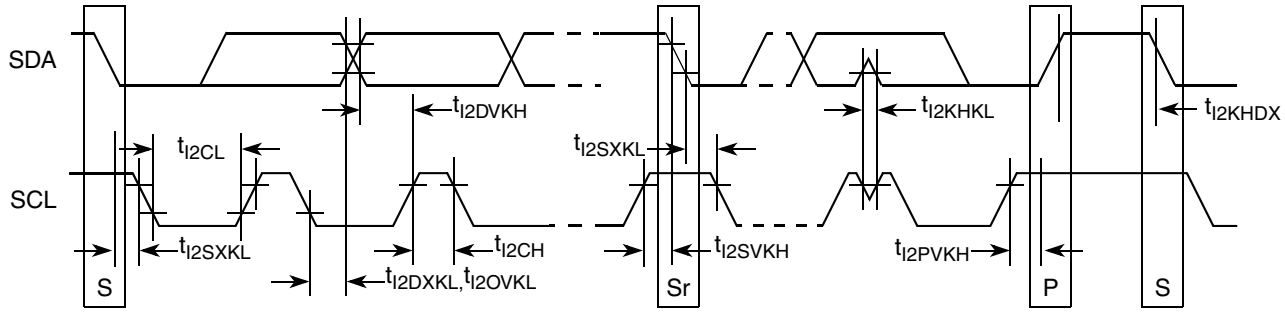


Figure 30. I^2C Bus AC timing diagram

2.19 GPIO interface

This section describes the AC electrical characteristics for the GPIO interface.

2.19.1 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 37. GPIO Input AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

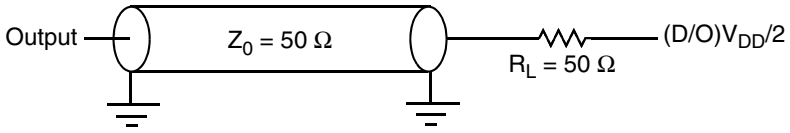


Figure 31. GPIO AC test load

2.20 Timers interface

This section describes the AC electrical characteristics for the Timers interface.

2.20.1 Timers AC timing specifications

This table provides the Timers input AC timing specifications.

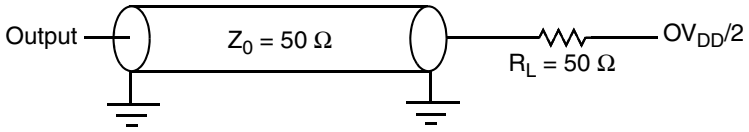
Table 38. GPIO input AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Unit	Notes
Timers inputs-minimum pulse width	t_{TIWID}	timers clock/2	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 1/(timers clock source/2). Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the timers.



2.21 Asynchronous signal timing

This table provides AS specifications for the asynchronous signal timing specifications.

Table 39. Signal timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One SYSCLK cycle
Output	t_{OUT}	Asynchronous	Application-dependent

Note: Input value relevant for DMA, EVT_B[9–0] only.

The following interfaces use the specified asynchronous signals:

- Debug port—Signals EVT_B[9–0]
- DMA signals
- Interrupt outputs—Signals IRQn, CKSTP_OUT_B

2.22 CPRI interface signals

This section describes the DC and AC electrical characteristics for the CPRI interface signals.

2.22.1 CPRI signals DC electrical characteristics

This table provides the DC electrical characteristics for the CPRI LOS interfaces operating at 2.5 V.

Table 40. CPRI signals DC electrical characteristics (DV_{DD} = 2.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Output high voltage (OV_{DD}/DV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.0	—	V	—
Output low voltage (OV_{DD}/DV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	—
Input current for each I/O pin (input voltage is between 0.1 × OV_{DD}/DV_{DD} and 0.9 × OV_{DD}/DV_{DD}(max)	I_I	–40	40	µA	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 4.

2.22.2 CPRI signals AC specifications

This table provides the CPRI signals timing specifications.

Table 41. CPRI signals timing specifications

For recommended operating conditions, see Table 4.

Parameter/condition	Symbol	Min	Typ	Max	Unit	Notes
CP_SYNC period	$t_{CP\text{-}SYNCCLK}$	—	10	—	ms	1, 3
CP_SYNC pulse width (output)	$t_{CP\text{-}SYNCCLKWDO}$	64	—	512	ns	—
CP_SYNC pulse width (input)	$t_{CP\text{-}SYNCCLKWDI}$	12	—	0.5 * $t_{CP\text{-}SYNCCLK}$	ns	—
CP_RCLK frequency	$t_{CP\text{-}RCLK}$	—	122.88	—	MHz	2

Notes:
1. $T_{CP\text{-}SYNCCLK}$ is the required sync period for both input or output sync.
2. The recovery output clock frequency. See Table 43 for details on using CP_RCLK as RefClk for RE to SLAVE configuration.
3. CP_SYNC and CPRI SerDes reference clock are generated from a common source with the following ratio: $t_{CP\_SYNCCLK}$ = 1228800 * t_{REFCLK}

2.23 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, Serial RapidIO, XAUI, XFI, SGMII, 10 GBase-KR, CPRI, Aurora, and 2.5x SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

2.23.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and SD_TX*n*_B) or a receiver input (SD_RX*n* and SD_RX*n*_B). Each signal swings between A volts and B volts where A > B.

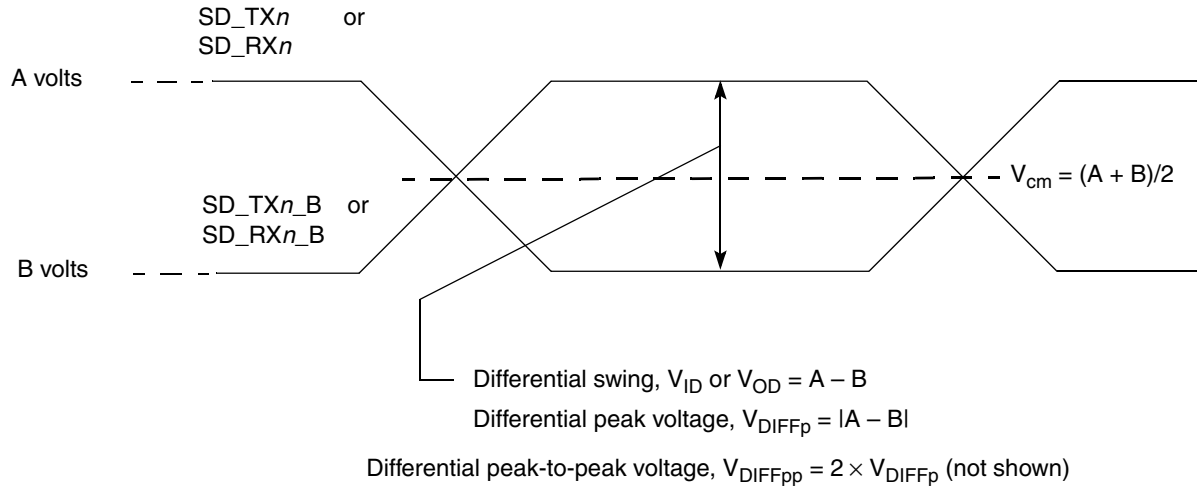


Figure 32. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing The transmitter output signals and the receiver input signals SD_TX*n*, SD_TX*n*_B, SD_RX*n,* and SD_RX*n*_B each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TXn} - V_{SD\_TXn\_B}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RXn} - V_{SD\_RXn\_B}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-to-peak voltage can also be calculated as $V_{TX\text{-}DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_B, for example) from the non-inverting signal (SD_TX*n*_B, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{SD\_TXn\_B}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.23.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF[1:2]_CLK and SD1_REF[1:2]_CLK_B for SerDes 1, SD2_REF[1:2]_CLK and SD2_REF[1:2]_CLK_B for SerDes 2.

SerDes 1–2 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: SGMII (1.25 and 3.125 Gbps), CPRI (1.2288, 2.4576, 3.072, 4.9152, 6.144, 9.8304 Gbps), Aurora (2.5, 3.125, 5 Gbps)
- SerDes 2: SGMII (1.25 and 3.125 Gbps), SRIO(2.5, 3.125, 5 Gbps), XAUI (3.125 Gbps), PCIe (2.5, 5 Gbps), XFI/10 GBase-KR (10.3125 Gbps), Aurora (2.5, 3.125, 5 Gbps).

The following sections describe the SerDes reference clock requirements and provide application information.

2.23.2.1 PCIe SerDes spread-spectrum clock source recommendations

SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B are designed to work with spread spectrum clock for PCI Express protocol only with the spreading specification defined in Table 42. When using spread spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

The spread spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread spectrum supported protocols. For example, if the spread spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SGMII or SRIO due to the SerDes lane usage mapping option, spread spectrum clocking cannot be used at all.

Table 42. SerDes spread-spectrum clock source recommendations

At recommended operating conditions. See Table 4.

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	—
Frequency spread	+0	–0.5	%	1

Note:
1. Only down-spreading is allowed.

2.23.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

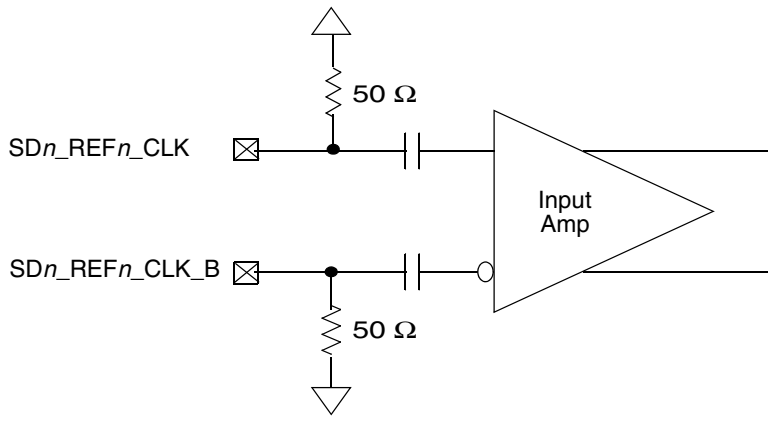


Figure 33. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes receivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended operating conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD*n*_REF*n*_CLK or SD*n*_REF*n*_CLK_B) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.

— If the device driving the SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.

- The input amplitude requirement is described in detail in the following sections.

2.23.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  — The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  — For an external DC-coupled connection, as described in Section 2.23.2.2, "SerDes reference clock receiver characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 34 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

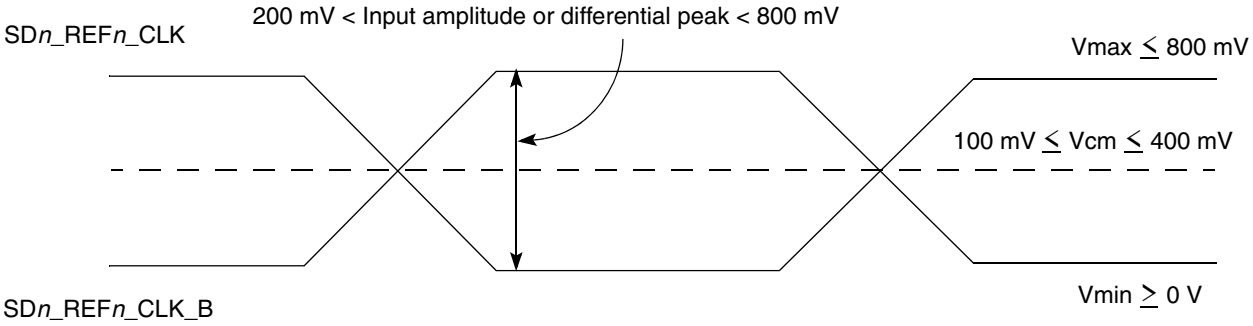


Figure 34. Differential reference clock input DC requirements (external DC-coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). Figure 35 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

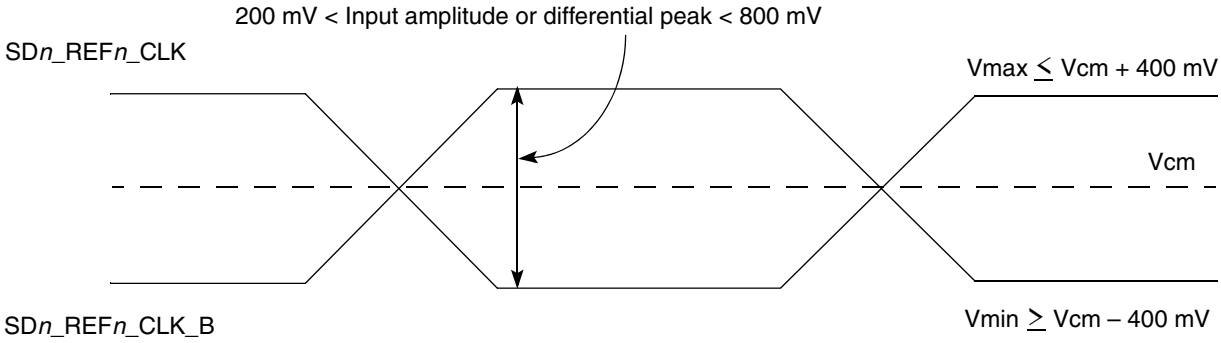


Figure 35. Differential reference clock input DC requirements (external AC-coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD*n*_REF*n*_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD*n*_REF*n*_CLK_B either left unconnected or tied to ground.
  - The SD*n*_REF*n*_CLK input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF*n*_CLK_B) through the same source impedance as the clock input (SD*n*_REF*n*_CLK) in use.

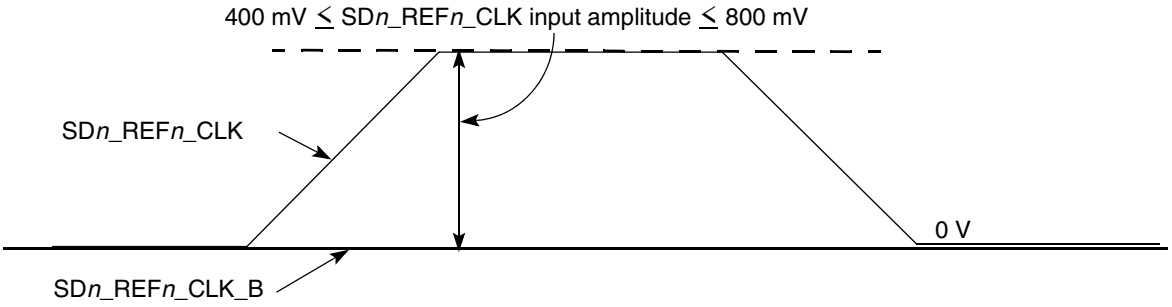


Figure 36. Single-ended reference clock input DC requirements

2.23.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 8 Gb/s.

This includes PCI Express (2.5, 5 GT/s), SGMII (1.25Gbps), 2.5x SGMII (3.125Gbps), Serial RapidIO (2.5, 3.125, 5 Gbps), Aurora (2.5, 3.125, 5 Gbps), CPRI (1.2288, 2.4576, 3.072, 4.9152, 6.144 Gbps), XAUI (3.125 Gbps). SerDes reference clocks to be guaranteed by the customer's application design.

Table 43. SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B input clock requirements (SV_{DD}= 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B frequency range	t_{CLK_REF}	—	100/122.88/ 125/156.25	—	MHz	1
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B clock frequency tolerance For PEX Gen 1, 2	t_{CLK_TOL}	–300	—	300	ppm	7, 10
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B clock frequency tolerance For SGMII, 2.5x SGMII, sRIO, XAUI, Aurora, CPRI	t_{CLK_TOL}	–100	—	100	ppm	8, 10
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2

Table 43. SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B input clock requirements (SV_{DD}= 1.0 V) (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B Allowed cut-off frequency of REC-slave synchronization mechanism	t_{CLK_TC}	—	—	300	Hz	9
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B df/f_0 contribution of jitter between REC master to REC slave to the frequency accuracy budget	t_{CLK_TF}	–0.002	—	0.002	ppm	9
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	V_{CM} + 200mV	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	V_{CM} – 200mV	mV	4
Rising edge rate (SD*n*_REF*n*_CLK) to falling edge rate (SD*n*_REF*n*_CLK_B) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:

1. **Caution:** Only 100, 122.88, 125 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF*n*_CLK minus SD*n*_REF*n*_CLK_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
4. Measurement taken from differential waveform.V_{CM} is the common mode voltage
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD*n*_REF*n*_CLK and falling edge rate for SD*n*_REF*n*_CLK_B. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF*n*_CLK rising meets SD*n*_REF*n*_CLK_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF*n*_CLK must be compared to the fall edge rate of SD*n*_REF*n*_CLK_B, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.
7. For PCI Express (2.5, 5 GT/s)
8. For SGMII, 2.5x SGMII, sRIO, XAUI, XFI, Aurora, CPRI.
9. This spec is applied to CPRI protocol clocks only. The T_{CLK_TC} is to comply with R-17 requirement in the protocol. T_{CLK_TF} to comply to R-18 requirement.
10. When two or more protocols share the same PLL on a SerDes module, the tightest SDn_REFn_CLK/ SDn_REFn_CLK_B clock frequency tolerance must be followed.

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 Gb/s. This includes XFI/10 GBase-KR (10.3125 Gbps) and CPRI (9.8304 Gbps). SerDes reference clocks to be guaranteed by the customer's application design.

Table 44. SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B frequency range	t_{CLK_REF}	—	122.88/ 156.25	—	MHz	1
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	7
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B single side band noise	@1 kHz	—	—	–85	dBC/Hz	2
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B single side band noise	@10 kHz	—	—	–108	dBC/Hz	2
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B single side band noise	@100 kHz	—	—	–128	dBC/Hz	2
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B single side band noise	@1 MHz	—	—	–138	dBC/Hz	2
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B single side band noise	@10MHz	—	—	–138	dBC/Hz	2
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	—	—	0.8	ps	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	—	—	11	ps	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B spurious noise (1.2 MHz to 15 MHz)	—	—	—	–75	dBC	—
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B Allowed cut-off frequency of REC-slave synchronization mechanism	t_{CLK_TC}	—	—	300	Hz	8
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B df/f_0 contribution of jitter between REC master to REC slave to the frequency accuracy budget	t_{CLK_TF}	–0.002	—	0.002	ppm	8
SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B rising/falling edge rate	t_{CLKRR}/ t_{CLKFR}	1	—	4	V/ns	3

Table 44. SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B input clock requirements (SV_{DD} = 1.0 V) (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input high voltage	V_{IH}	V_{CM} + 200mV	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	V_{CM} - 200mV	mV	4
Rising edge rate (SD*n*_REF*n*_CLK) to falling edge rate (SD*n*_REF*n*_CLK_B) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:

1. **Caution:** Only 122.88 and 156.25 have been tested. In-between values do not work correctly with the rest of the system.
2. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF*n*_CLK minus SDn_REFn_CLK_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD*n*_REF*n*_CLK and falling edge rate for SDn_REFn_CLK_B. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF*n*_CLK rising meets SDn_REFn_CLK_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF*n*_CLK must be compared to the fall edge rate of SDn_REFn_CLK_B, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.
7. When two or more protocols share the same PLL on a SerDes module, the tightest SDn_REFn_CLK/ SDn_REFn_CLK_B clock frequency tolerance must be followed.
8. This spec is applied to CPRI protocol clocks only. The T_{CLK_TC} is to comply with R-17 requirement in the protocol. T_{CLK_TF} to comply to R-18 requirement.

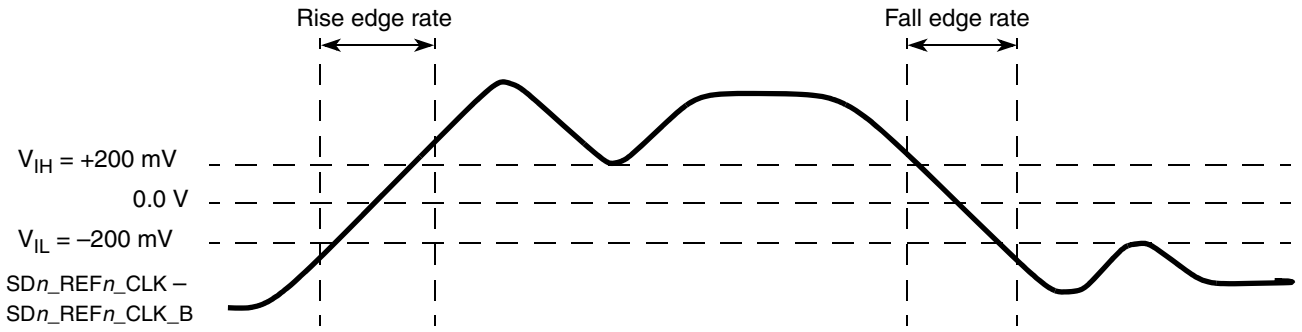


Figure 37. Differential measurement points for rise and fall time

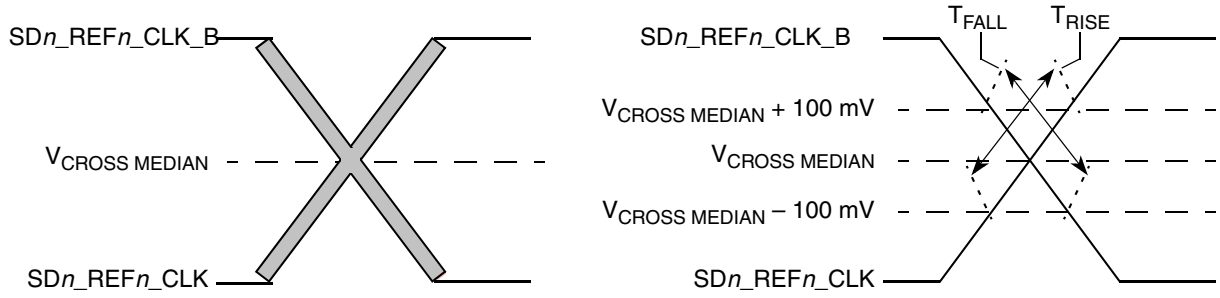


Figure 38. Single-ended measurement points for rise and fall time matching

2.23.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

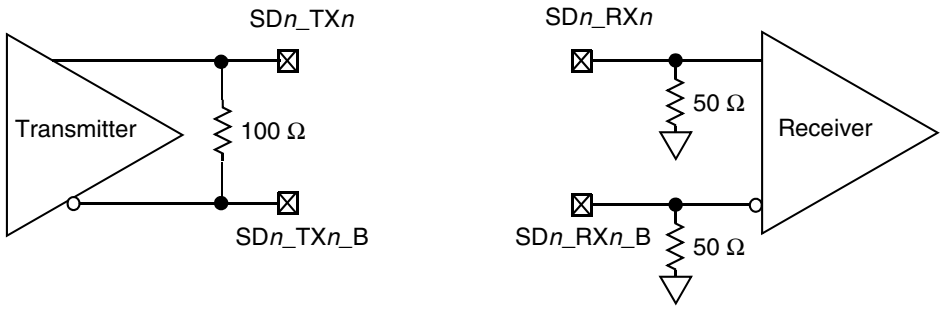


Figure 39. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage

- Section 2.23.4, "PCI Express interface"
- Section 2.23.5, "Serial RapidIO (sRIO) interface"
- Section 2.23.6, "XAUI interface"
- Section 2.23.7, "Aurora interface"
- Section 2.23.8, "SGMII interface"
- Section 2.23.9, "XFI interface"
- Section 2.23.10, "10GBase-KR interface"
- Section 2.23.11, "CPRI interface"

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

2.23.4 PCI Express interface

This section describes the clocking dependencies as well as the DC and AC electrical specifications for the PCI Express bus.

2.23.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ± 300 ppm tolerance.

2.23.4.2 PCI Express clocking requirements for SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B

SerDes 2 (SD2_REF[1:2]_CLK and SD2_REF[1:2]_CLK_B) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL_S2. PCI Express is supported on SerDes 2 only.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

2.23.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 45. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D– DC Impedance during all states

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 46. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p\_low}$	400	500	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

Table 46. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V) (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D– DC impedance during all states

2.23.4.3.2 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 47. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC single input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 48. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

2.23.4.4 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

2.23.4.4.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 49. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs.
2. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 50. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Note 1.

Table 50. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.

Notes:
1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs.
2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.23.4.4.2 PCI Express AC physical layer receiver specifications.

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s and 5 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 51. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 1 and 2.

Table 51. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1, 2 and 3.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 41 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter. If spread spectrum clocking is desired, the common clock must be used.

Table 52. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	Each UI is 200 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common and separate RefClk receiver architecture.
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common and separate RefClk receiver architecture

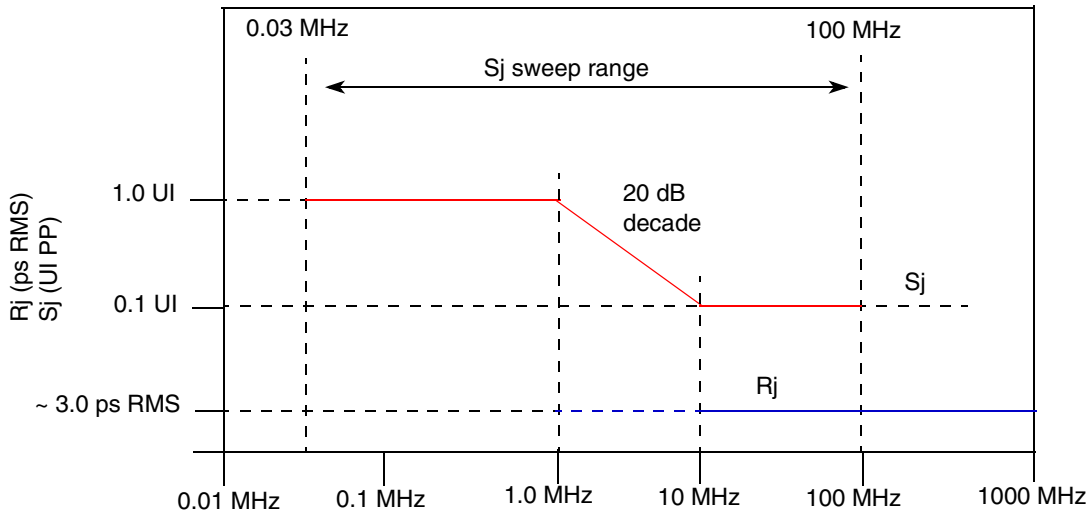


Figure 40. Swept sinusoidal jitter mask

2.23.4.5 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

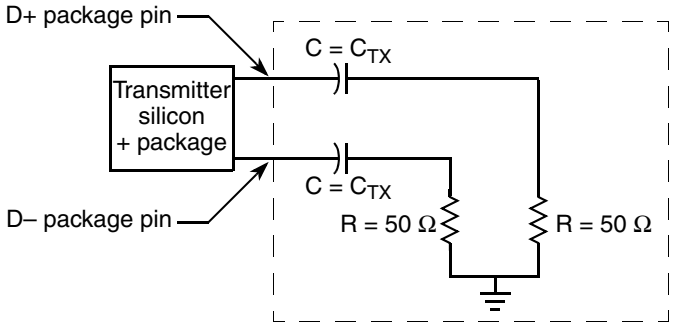


Figure 41. Test/Measurement load

2.23.5 Serial RapidIO (sRIO) interface

This section describes the DC and AC electrical specifications for the Serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125 and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane.

All unit intervals are specified with a tolerance of ±100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

2.23.5.1 Signal definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. The following figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and TD_B) or a receiver input (RD and $_{RD\_B}$). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals—TD, TD_B, RD, and RD_B—each have a peak-to-peak swing of A – B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{TD\_B}$
- The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{RD\_B}$
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A – B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ volts.

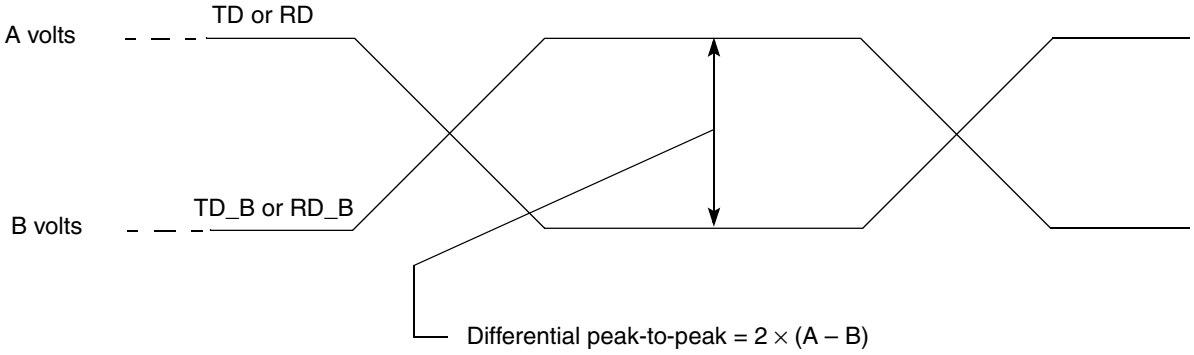


Figure 42. Differential peak-to-peak voltage of transmitter or receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs TD and TD_B, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD_B is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

2.23.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- De-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

2.23.5.3 Serial RapidIO clocking requirements for SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B

SerDes 2 (SD2_REF[1:2]_CLK and SD2_REF[1:2]_CLK_B) may be used for various SerDes Serial RapidIO configurations based on the RCW Configuration field SRDS_PRTCL_S2. Serial RapidIO is supported on SerDes 2 only.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.5.4 DC requirements for Serial RapidIO

This section explains the DC requirements for the Serial RapidIO interface.

2.23.5.4.1 DC Serial RapidIO transmitter specifications

This table defines the transmitter DC specifications for Serial RapidIO operating at 2.5 and 3.125 GBaud.

Table 53. Serial RapidIO transmitter DC specifications—2.5 GBaud, 3.125 GBaud (XV_{DD} = 1.35V or 1.5V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Long-run differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p	—
Short-run differential output voltage	V_{DIFFPP}	500	—	1000	mV p-p	—
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential impedance

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair

This table defines the transmitter DC specifications for Serial RapidIO operating at 5 GBaud.

Table 54. Serial RapidIO transmitter DC specifications—5 GBaud (XV_{DD} = 1.35V or 1.5V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Long-run differential output voltage	V_{DIFF}	800	—	1200	mV	—
Short-run differential output voltage	V_{DIFF}	400	—	750	mV	—
Long-run de-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	—
Long-run de-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
Differential resistance	RTD	80	100	120	Ω	—

Note:
1. Voltage relative to COMMON of either signal comprising a differential pair.

2.23.5.4.2 DC Serial RapidIO receiver specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) × (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

This table defines the receiver DC specifications for Serial RapidIO operating at 2.5 and 3.125 GBaud.

Table 55. Serial RapidIO receiver DC specifications—2.5 GBaud, 3.125 GBaud (SV_{DD} = 1.0V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1
DC Differential receiver input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential impedance

Note:
1. Measured at the receiver

This table defines the receiver DC specifications for Serial RapidIO operating at 5 GBaud.

Table 56. Serial RapidIO receiver DC specifications—5 GBaud (SV_{DD} = 1.0V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Long-run differential input voltage	V_{DIFF}	—	—	1200	mV	1
Short-run differential input voltage	V_{DIFF}	125	—	1200	mV	1
Differential resistance	R_{RTD}	80	—	120	Ω	—

Note:
1. Measured at the receiver

2.23.5.5 AC requirements for Serial RapidIO

This section explains the AC requirements for the Serial RapidIO interface.

2.23.5.5.1 AC requirements for Serial RapidIO transmitter

This table defines the transmitter AC specifications for the Serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

Table 57. Serial RapidIO transmitter AC timing specifications—2.5 GBaud, 3.125 GBaud

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100ppm	ps

This table defines the transmitter AC specifications for the Serial RapidIO operating at 5 GBaud. The AC timing specifications do not include RefClk jitter.

Table 58. Serial RapidIO transmitter AC timing specifications —5 GBaud

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Baud rate	T_{BAUD}	5.000 – 100ppm	5.000	5.000 + 100ppm	Gb/s
Uncorrelated high probability jitter	T_{UHPJ}	—	—	0.155	UI p-p
Total jitter	T_J	—	—	0.30	UI p-p

This table defines the receiver AC specifications for Serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

Table 59. Serial RapidIO receiver AC timing specifications —2.5 GBaud, 3.125 GBaud

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance[2]	J_T	—	—	0.65	UI p-p	1
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 2.5 GBaud	UI	400 – 100ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

This figure shows the single-frequency sinusoidal jitter limits for 2.5 GBaud and 3.125 GBaud rates.

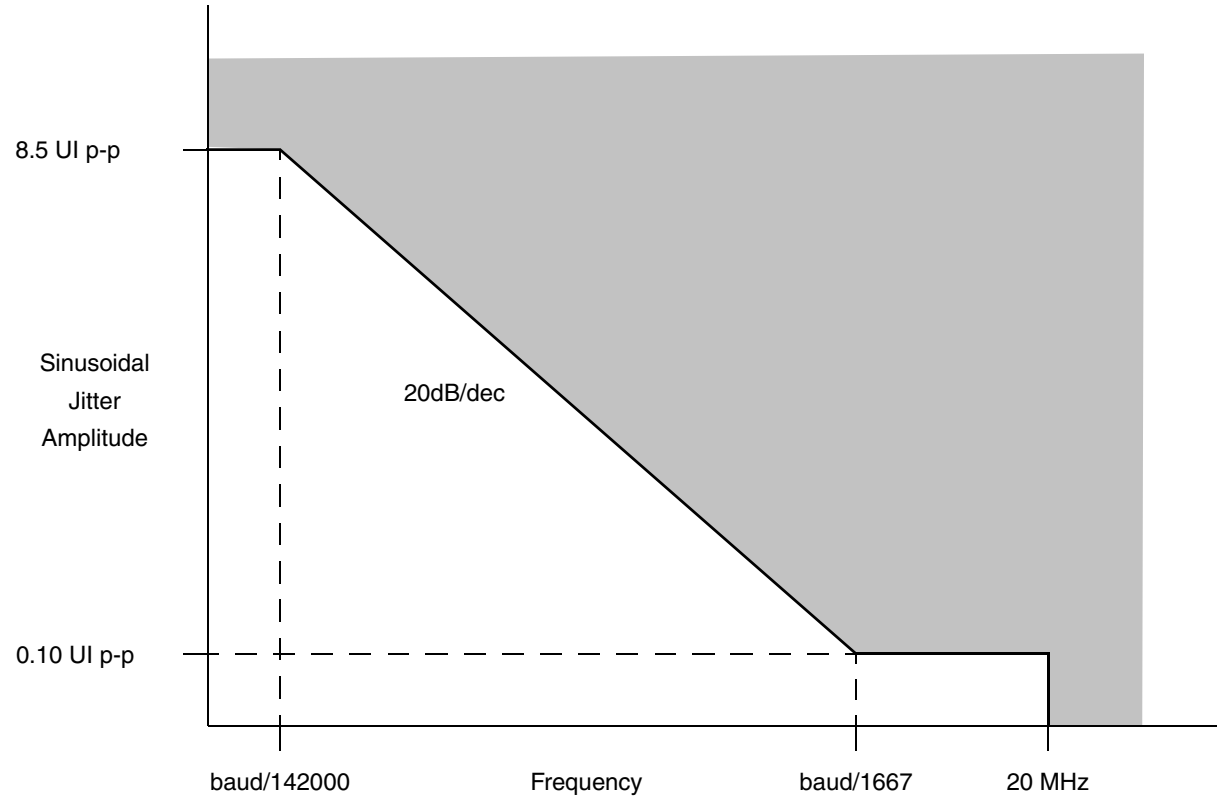


Figure 43. Single-frequency sinusoidal jitter limits

This table defines the receiver AC specifications for Serial RapidIO operating at 5 GBaud. The AC timing specifications do not include RefClk jitter.

Table 60. Serial RapidIO receiver AC timing specifications —5 GBaud

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 – 100 ppm	5.000	5.000 + 100 ppm	Gb/s	—
Long-run Gaussian jitter	R_{GJ}	—	—	0.2	UI p-p	—
Uncorrelated bounded high probability jitter	R_{DJ}	—	—	0.12	UI p-p	—
Long-run correlated bounded high probability jitter	R_{CBHPJ}	—	—	0.525	UI p-p	—
Short-run correlated bounded high probability jitter	R_{CBHPJ}	—	—	0.30	UI p-p	—
Long-run bounded high probability jitter	R_{BHPJ}	—	—	0.75	UI p-p	—
Short-run bounded high probability jitter	R_{BHPJ}	—	—	0.45	UI p-p	—

Table 60. Serial RapidIO receiver AC timing specifications (continued)—5 GBaud

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Sinusoidal jitter, maximum	R_{SJ-max}	—	—	5.00	UI p-p	—
Sinusoidal jitter, high frequency	R_{SJ-hf}	—	—	0.05	UI p-p	—
Long-run total jitter (does not include sinusoidal jitter)	R_{Tj}	—	—	0.95	UI p-p	—
Short-run total jitter (does not include sinusoidal jitter)	R_{Tj}	—	—	0.60	UI p-p	—

This figure shows the single-frequency sinusoidal jitter limits for 5 GBaud rate.

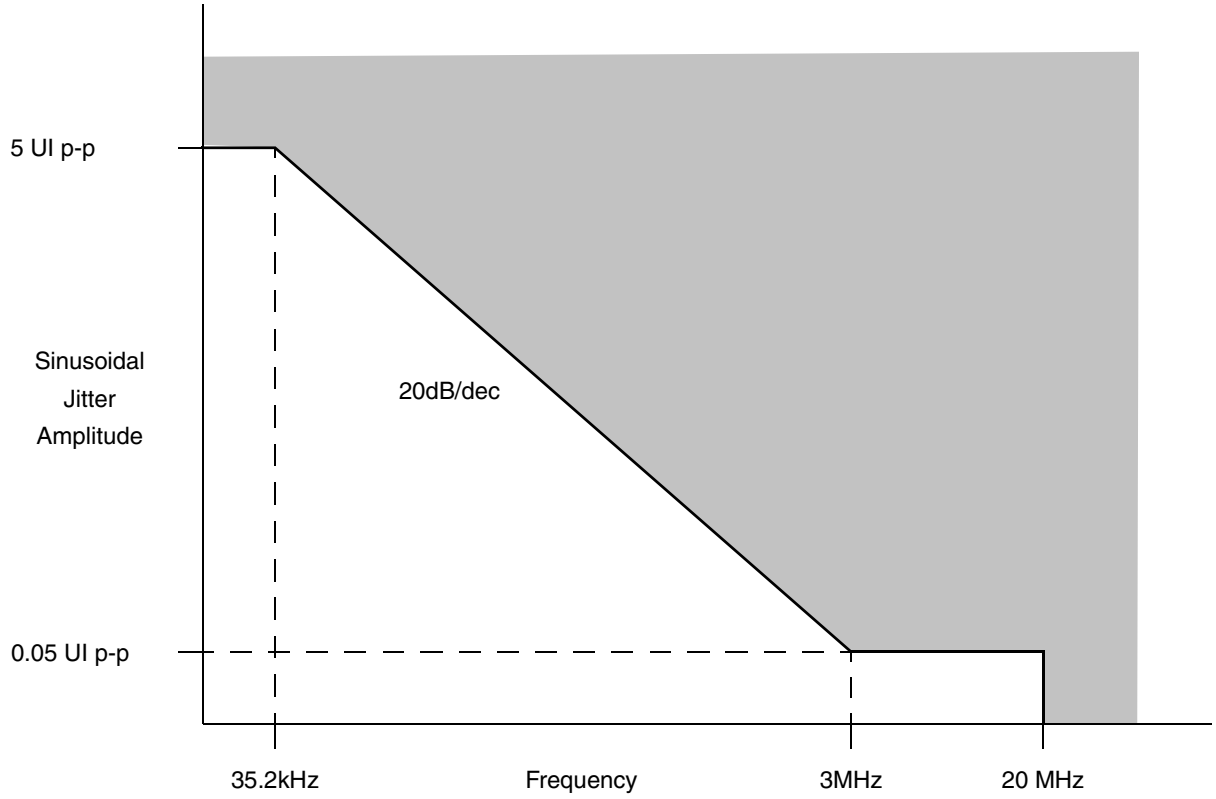


Figure 44. Single-frequency sinusoidal jitter limits

2.23.6 XAUI interface

This section describes the DC and AC electrical specifications for the XAUI bus.

2.23.6.1 XAUI clocking requirements for SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B

Only SerDes 2 (SD2_REF[1:2]_CLK and SD2_REF[1:2]_CLK_B) may be used for various SerDes2 XAUI configurations based on the RCW Configuration field SRDS_PRTCL_S2.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.6.2 XAUI DC electrical characteristics

This section discusses the XAUI DC electrical characteristics for the transmitter, and receiver.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.6.2.1 XAUI transmitter DC electrical characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 61. XAUI transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output voltage	V_O	–0.40	—	2.30	V	1
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	—
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	2

Note:

1. Absolute output voltage limit
2. Transmitter DC differential impedance.

2.23.6.2.2 XAUI receiver DC electrical characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 62. XAUI receiver DC timing specifications (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1
DC Differential receiver input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2

Note:

1. Measured at the receiver.
2. Receiver DC differential impedance

2.23.6.3 XAUI AC timing specifications

This section discusses the XAUI AC timing specifications for the transmitter, and receiver.

2.23.6.3.1 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 63. XAUI transmitter AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

2.23.6.3.2 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 64. XAUI receiver AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver.
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

2.23.7 Aurora interface

This section describes the Aurora clocking requirements and its DC and AC electrical characteristics.

2.23.7.1 Aurora clocking requirements for SD*n* _REF*n* _CLK and SD*n* _REFn _CLK_B

SerDes 1 and SerDes 2 (SD[1:2]_REF[1:2]_CLK and SD[1:2]_REF[1:2]_CLK_B) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL_Sn.

For more information on these specifications, see Section 2.23.2, “SerDes reference clocks.”

2.23.7.2 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for the Aurora interface.

2.23.7.2.1 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 65. Aurora transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω

2.23.7.2.2 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for the Aurora interface.

Table 66. Aurora receiver DC electrical characteristics (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	—	1600	mV p-p	1
DC Differential receiver impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	2

Note:

1. Measured at receiver.
2. DC Differential receiver impedance

2.23.7.3 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

2.23.7.3.1 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 67. Aurora transmitter AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	—	—	0.17	UI p-p
Total jitter	J_T	—	—	0.35	UI p-p
Unit interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps
Unit interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps
Unit interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps

2.23.7.3.2 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 68. Aurora receiver AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance	J_T	—	—	0.65	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 2.5 GBaud	UI	400 – 100 ppm	400	400 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
Unit Interval: 5.0 GBaud	UI	200 – 100 ppm	200	200 + 100 ppm	ps	—

Note:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 41. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

2.23.8 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 45, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

2.23.8.1 SGMII clocking requirements for SD*n*_REF*n*_CLK and SD*n*_REF*n*_CLK_B

When operating in SGMII mode, a SerDes reference clock is required on SD[1:2]_REF[1:2]_CLK and SD[1:2]_REF[1:2]_CLK_B pins. SerDes 1–2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL_Sn.

For more information on these specifications, see Section 2.23.2, “SerDes reference clocks.”

2.23.8.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.23.8.2.1 SGMII and SGMII 2.5x transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B) as shown in Figure 46.

Table 69. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

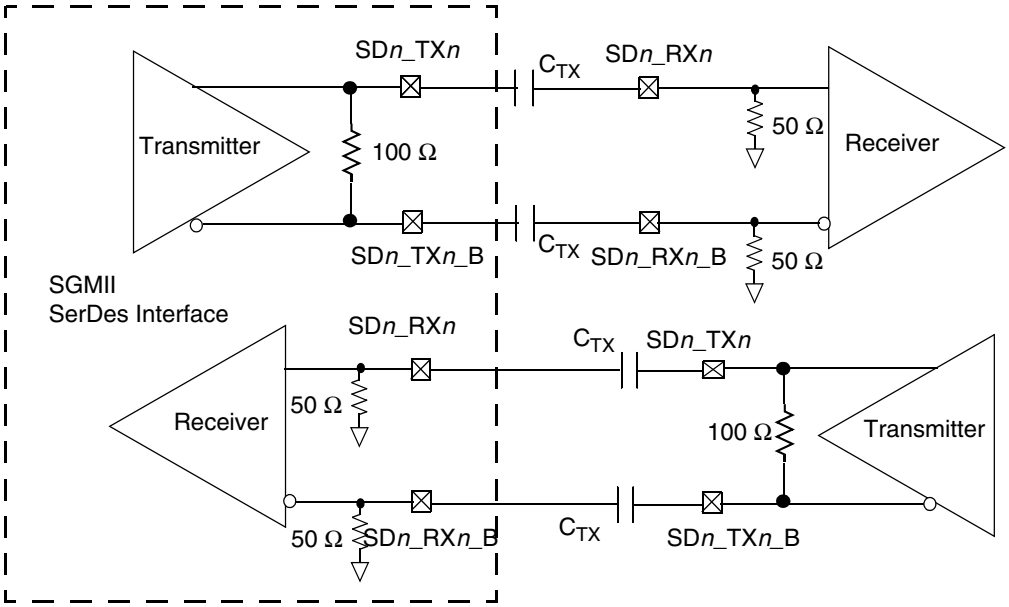
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\|V_{OD}\|_{-max}$	mV	1
Output low voltage	V_{OL}	$\|V_{OD}\|_{-min}/2$	—	—	mV	1
Output differential voltage[2, 3] (XV_{DD-Typ} at 1.35 V and 1.5 V)	$\|V_{OD}\|$	320	500.0	725.0	mV	Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b0
		293.8	459.0	665.6		Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b1
		266.9	417.0	604.7		Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b11
		240.6	376.0	545.2		Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b10
		213.1	333.0	482.9		Amp **Default** Setting: SRDSxLNmTECR0 [AMP_RED] = 6b110
		186.9	292.0	423.4		Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b111
		160.0	250.0	362.5		Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b10000
Output impedance differential	R_O	80	100	120	Ω	—

Notes:

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn} - V_{SD\_TXn\_B}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XVDD-Typ = 1.35 V or 1.5 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD*n* _TX*n* and SD*n*_TX*n*_B.

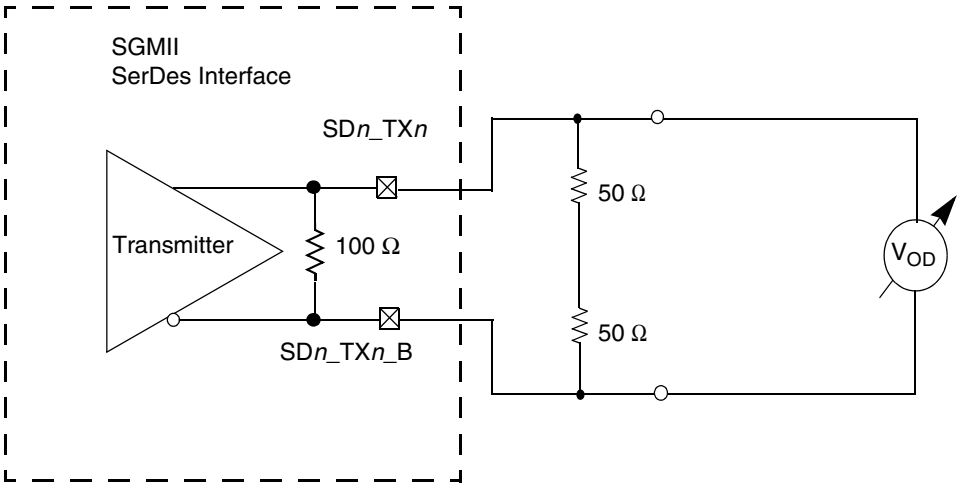
This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

Figure 45. 4-wire AC-coupled SGMII serial link connection example



This figure shows the SGMII transmitter DC measurement circuit.

Figure 46. SGMII transmitter DC measurement circuit



This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 70. SGMII 2.5x transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	—	600	mV	Amp Setting: SRDSxLNmTECR0 [AMP_RED] = 6b0
Output impedance (differential)	R_O	80	100	120	Ω	—

2.23.8.2.2 SGMII and SGMII 2.5x DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 71. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		—	N/A			—	1
Input differential voltage	—	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	—		175	—			
Loss of signal threshold	—	V_{LOS}	30	—	100	mV	3, 4
	—		65	—	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—

Notes:
1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See Section 2.23.4.3.2, “PCI Express DC physical layer receiver specifications,” and Section 2.23.4.4.2, “PCI Express AC physical layer receiver specifications.,” for further explanation.
4. Default lost threshold sel = ‘001.’

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 72. SGMII 2.5x receiver DC timing specifications (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp-p}$	200	—	1200	mV	—
Loss of signal threshold	V_{LOS}	75	—	200	mV	—
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

2.23.8.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

2.23.8.3.1 SGMII and SGMII 2.5x transmit AC timing specifications

This table provides the SGMII and SGMII 2.5x transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 73. SGMII transmit AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	2
Unit Interval: 1.25 GBaud (SGMII)	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII)	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1
AC coupling capacitor	C_{TX}	10	—	200	nF	3

Notes:
1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 43 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.23.8.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B) or at the receiver inputs (SD*n*_RX*n* and SD*n*_RX*n*_B) respectively.

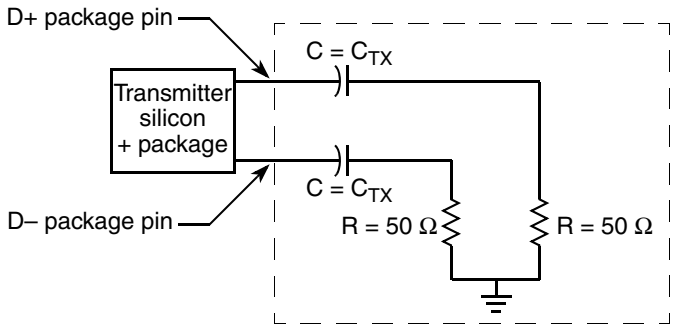


Figure 47. SGMII AC test/measurement load

2.23.8.3.3 SGMII and SGMII 2.5x receiver AC timing specifications

This table provides the SGMII and SGMII 2.5x receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 74. SGMII receive AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	—	—	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	—	—	0.55	UI p-p	1
Total jitter tolerance	J_T	—	—	0.65	UI p-p	1, 2

Table 74. SGMII receive AC timing specifications (continued)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud (SGMII)	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 43.

2.23.9 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

2.23.9.1 XFI clocking requirements for SD2_REF2_CLK and SD2_REF2_CLK_B

Only SerDes 2 RefClk2 (SD2_REF2_CLK and SD2_REF2_CLK_B) may be used for SerDes XFI configurations based on the RCW configuration field SRDS_PRTCL_S2.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.9.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

2.23.9.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 75. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	—	770	mV	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	—

Table 75. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35 (continued)V or 1.5 (continued)V) (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}4.66dB}$	4.1	4.6	5.1	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}6.0dB}$	5.5	6.0	6.5	dB	—
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO\text{-}9.5dB}$	9	9.5	10	dB	—
Differential resistance	T_{RD}	80	100	120	Ω	—

2.23.9.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 76. XFI receiver DC electrical characteristics (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\text{-}DIFF}$	110	—	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	—

Note:

1. Measured at receiver

2.23.9.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

2.23.9.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 77. XFI transmitter AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s
Unit Interval	UI	—	96.96	—	ps
Deterministic jitter	D_J	—	—	0.15	UI p-p
Total jitter	T_J	—	—	0.30	UI p-p

2.23.9.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 78. XFI receiver AC timing specifications

For recommended operating conditions, see Table 4.

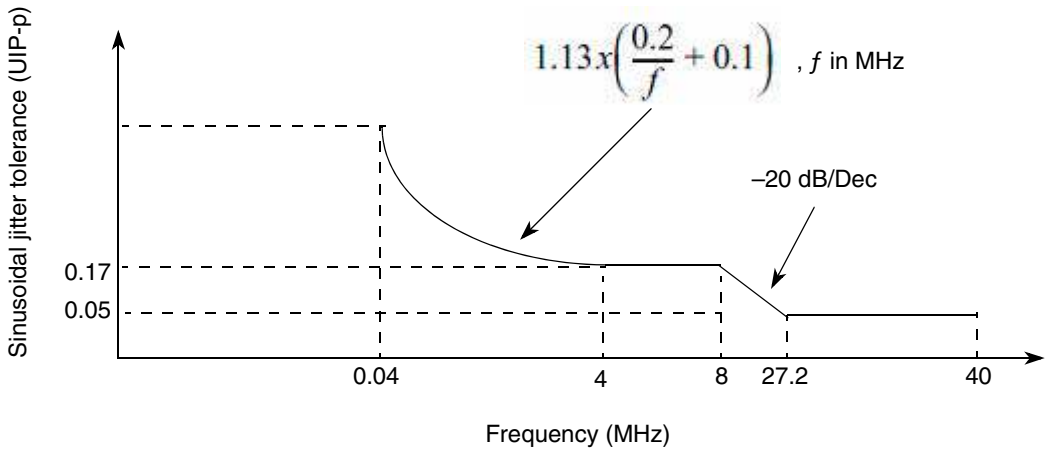
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 – 100 ppm	10.3125	10.3125 + 100 ppm	Gb/s	—
Unit Interval	UI	—	96.96	—	ps	—
Total non-EQJ jitter	$T_{NON-EQJ}$	—	—	0.45	UI p-p	1
Total jitter tolerance	T_J	—	—	0.65	UI p-p	1, 2

Note:

1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non – EQJ = T_J – ISI = R_J + DCD + P_J
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude are required for performance optimization.

This figure shows the sinusoidal jitter tolerance of XFI receiver.

Figure 48. XFI host receiver input sinusoidal jitter tolerance



2.23.10 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

2.23.10.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 2 RefClk2 (SD2_REF2_CLK and SD2_REF2_CLK_B) may be used for SerDes 10GBase-KR configurations based on the RCW configuration field SRDS_PRTCL_S2.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.10.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

2.23.10.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 79. 10GBase-KR transmitter DC electrical characteristics (XV_{DD}=1.35V or 1.5V)

Table 80. For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	—
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	—
	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	—
	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	—
	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	—
	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	—
Differential resistance	T_{RD}	80	100	120	Ω	—

2.23.10.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 81. 10GBase-KR receiver DC electrical characteristics (XV_{DD}=1.35V or 1.5V)

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	—
Differential resistance	R_{RD}	80	-	120	Ω	—

2.23.10.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

2.23.10.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications RefClk jitter is not included.

Table 82. 10GBase-KR transmitter AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Deterministic jitter	D_J	-	-	0.155	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

2.23.10.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 83. 10GBase-KR receiver AC timing specifications

For recommended operating conditions, see Table 4.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	Gbd	—
Random jitter	R_J	-	-	0.130	UI p-p	1
Sinusoidal jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1
Total jitter	T_J	-	-	1.0	UI p-p	1,2

1. The AC specifications do not include Refclk jitter.
2. The total applied Jitter Tj = ISI + Rj + DCD + Sj-max where ISI is jitter due to frequency dependent loss.
3. TX Equalization and amplitude tuning is through software for performance optimization, as in NXP provided SDKs.

2.23.11 CPRI interface

This section describes the CPRI clocking requirements and its DC and AC electrical characteristics.

2.23.11.1 CPRI clocking requirements for SD1_REF*n*_CLK and SD1_REF*n*_CLK_B

Only SerDes 1 (SD1_REF[1:2]_CLK and SD1_REF[1:2]_CLK_B) may be used for SerDes CPRI configurations based on the RCW Configuration field SRDS_PRTCL_S1.

For more information on these specifications, see Section 2.23.2, "SerDes reference clocks."

2.23.11.2 CPRI LV

This section describes the CPRI LV XAUI based interface, designed to work at 1.2288, 2.4576 and 3.072 GB/s.

2.23.11.2.1 Transmitter specifications

This table defines the DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 84. Transmitter DC specifications (XV_{DD} = 1.35 V or 1.5 V)

Characteristic	Symbol	Min	Nom	Max	Unit
Output voltage	VO	–0.40	—	2.30	Volts

Table 84. Transmitter DC specifications (XV_{DD} = 1.35 V or 1.5 V)

Differential output voltage	VDIFFPP	800	—	1600	mV p-p
Differential resistance	T_Rd	80	100	120	Ω

The following table defines the AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 85. Transmitter AC specifications

Characteristic	Symbol	Min	Nom	Max	Unit
Deterministic jitter	JD	—	—	0.17	UI p-p
Total jitter	JT	—	—	0.35	UI p-p
Unit interval: **1.2288 GBaud**	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	us
Unit interval: **2.4576 GBaud**	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	us
Unit interval: **3.072 GBaud**	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	us

Note:
The AC specifications do not include Refclk jitter.

2.23.11.2.2 Receiver specifications

This table defines the DC specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 86. Receiver DC specifications (SV_{DD} = 1.0 V)

Characteristic	Symbol	Min	Nom	Max	Unit
Differential input voltage	VIN	200	—	1600	mV p-p
Differential resistance	R_Rdin	80	—	120	Ω

This table defines the AC specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 87. Receiver AC specifications

Characteristic	Symbol	Min	Nom	Max	Unit	Condition
Deterministic jitter tolerance	JD	—	—	0.37	UI p-p	Measured at receiver
Combined deterministic and random jitter tolerance	JDR	—	—	0.55	UI p-p	Measured at receiver
Total jitter tolerance	JT	—	—	0.65	UI p-p	Measured at receiver
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit interval: **1.2288 GBaud**	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	ps	—

Table 87. Receiver AC specifications (continued)

Characteristic	Symbol	Min	Nom	Max	Unit	Condition
Unit interval: **2.4576 GBaud**	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	ps	—
Unit interval: **3.072 GBaud**	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	ps	—

Note:

1. Total random jitter is composed of deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter's amplitude and frequency is defined in agreement with XAUI specification IEEE 802.3-2005 [1], clause 47.
2. The AC specifications do not include Refclk jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 41.

2.23.11.3 CPRI LV-II/LV-III

This section describes the CPRI LV-II CEI-6G-LR based (1.2288, 2.4576, 3.072, 4.9152 and 6.144 Gb/s) and CPRI LV-III IEEE 802.3 [22], clause 72.7 based (9.8304 Gb/s)

2.23.11.3.1 CPRI LV-II and LV-III transmitter specifications

This table provides the CPRI-LV-II and LV-III transmitter DC specifications.

Table 88. CPRI LV-II and LV-III transmitter DC specifications (XV_{DD} = 1.35 V or 1.5 V)

Parameter	Symbols	Min	Nom	Max	Units	Condition
Output differential voltage (into floating load Rload=100 Ω)	T_Vdiff	800	—	1200	mV	Amp Setting: SRDS1LNmTECR0 [AMP_RED] = 6b0
De-emphasized differential output voltage (ratio)	T_VTX-DE-RATIO-1.14dB	-0.6	-1.1	-1.6	dB	Ratio of full swing: SRDS1LNmTECR0 [RATIO_PST1Q] = 5b00011
De-emphasized differential output voltage (ratio)	T_VTX-DE-RATIO-3.5dB	-3	-3.5	-4	dB	Ratio of full swing: SRDS1LNmTECR0 [RATIO_PST1Q] = 5b01000
De-emphasized differential output voltage (ratio)	T_VTX-DE-RATIO-4.66dB	-4.1	-4.6	-5.1	dB	Ratio of full swing: SRDS1LNmTECR0 [RATIO_PST1Q] = 5b01010
De-emphasized differential output voltage (ratio)	T_VTX-DE-RATIO-6.0dB	-5.5	-6.0	-6.5	dB	Ratio of full swing: SRDS1LNmTECR0 [RATIO_PST1Q] = 5b01100
De-emphasized differential output voltage (ratio)	T_VTX-DE-RATIO-9.5dB	-9	-9.5	-10	dB	Ratio of full swing: SRDS1LNmTECR0 [RATIO_PST1Q] = 5b10000
Differential resistance	T_Rd	80	100	120	Ω	

This table provides the CPRI-LV-II/LV-III transmitter AC specifications.

Table 89. CPRI LV-II/LV-III transmitter AC specifications

Parameter	Symbols	Min	Nom	Max	Units
Uncorrelated high-probability jitter/random jitter	T_UHPJ/T_RJ	—	—	0.15	UI p-p
Deterministic jitter	T_DJ	—	—	0.15	UI p-p
Total jitter	T_TJ	—	—	0.30	UI p-p
Unit interval: **1.2288 GBaud**	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	us
Unit interval: **2.4576 GBaud**	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	us
Unit interval: **3.072 GBaud**	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	us
Unit interval: **4.9152 GBaud**	UI	1/4915.2-100ppm	1/4915.2.0	1/4915.2+100ppm	us
Unit interval: **9.8304 GBaud**	UI	1/9830.4-100ppm	1/9.8304	1/9830.4+100ppm	us

Note:

1. The Refclk jitter measured using Golden PLL is to be less than 0.05UI. The Golden PLL should have at maximum a bandwidth of baud rate over 1667, with a maximum of 20dB/dec rolloff, until at least baud rate over 16.67, with no peaking around the corner frequency.

This table provides the CPRI-LV-II/LV-III transmitter AC specifications for 6.144 GBaud.

Table 90. CPRI LV-II/LV-III transmitter AC specifications (6.144 GBaud)

Parameter	Symbols	Min	Nom	Max	Units
Uncorrelated high-probability jitter/random jitter	T_UHPJ/T_RJ	—	—	0.2	UI p-p
Deterministic jitter	T_DJ	—	—	0.17	UI p-p
Total jitter	T_TJ	—	—	0.37	UI p-p
Unit interval: **6.144 GBaud**	UI	1/6144.0-100ppm	1/61440	1/6144.0+100ppm	us

Note:

1. The Refclk jitter measured using Golden PLL is to be less than 0.05UI. The Golden PLL should have at maximum a bandwidth of baud rate over 1667, with a maximum of 20dB/dec rolloff, until at least baud rate over 16.67, with no peaking around the corner frequency.

2.23.11.3.2 CPRI LV-II and LV-III receiver specifications

This table provides the CPRI LV-II and the CPRI LV-III receiver DC timing specifications.

Table 91. CPRI-LV-II receiver DC specifications (SV_{DD} = 1.0 V)

Parameter	Symbols	Min	Nom	Max	Units
Input differential voltage	R_Vdiff	N/A	—	1200	mV
Differential Resistance	R_Rdin	80	—	120	Ω

Note:

1. It is assumed that for the R_diff Min spec, the eye can be closed at the receiver after passing the signal through a CEI/CPRI Level II LR-compliant channel.

Table 92. CPRI LV-II receiver AC specifications

Parameter	Symbols	Min	Nom	Max	Units
Gaussian jitter	R_GJ	—	—	0.275	UI p-p
Uncorrelated bounded high-probability jitter	R_UBHPJ	—	—	0.150	UI p-p
Correlated bounded high-probability jitter	R_CBHPJ	—	—	0.525	UI p-p
Bounded high-probability jitter	R_BHPJ	—	—	0.675	UI p-p
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p-p
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.050	UI p-p
Total jitter does not include sinusoidal jitter	R_Tj	—	—	0.950	UI p-p
Unit Interval: **1.2288 GBaud**	UI	1/1228.8-100ppm	1/1228.8	1/1228.8+100ppm	us
Unit Interval: **2.4576 GBaud**	UI	1/2457.6-100ppm	1/2457.6	1/2457.6+100ppm	us
Unit Interval: **3.072 GBaud**	UI	1/3072.0-100ppm	1/3072.0	1/3072.0+100ppm	us
Unit Interval: **4.9152 GBaud**	UI	1/4915.2-100ppm	1/4915.2.0	1/4915.2+100ppm	us

Note:

1. The AC specifications do not include Refclk jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 41.
2. The ISI jitter (R_CBHPJ) and amplitude have to be correlated for example by a PCB trace.
3. The intended application is as a point-to-point interface of approximately 100cm and up to two connectors. The maximum allowed total loss (channel + interconnect+ other loss) is 20.6dB @ 6.144 Gb/s.

This table provides the CPRI LV-II receiver AC specifications for 6.144 GBaud.

Table 93. CPRI LV-II receiver AC specifications (6.144 GBaud)

Parameter	Symbols	Min	Nom	Max	Units
Gaussian jitter	R_GJ	—	—	0.2	UI p-p
Uncorrelated bounded high-probability jitter	R_UBHPJ	—	—	0.05	UI p-p
Correlated bounded high-probability jitter	R_CBHPJ	—	—	0.35	UI p-p
Bounded high-probability jitter	R_BHPJ	—	—	0.40	UI p-p
Sinusoidal jitter, maximum	R_SJ-max	—	—	5.000	UI p-p
Sinusoidal jitter, high frequency	R_SJ-hf	—	—	0.125	UI p-p
Total jitter does not include sinusoidal jitter	R_Tj	—	—	0.6	UI p-p
Unit Interval: **6.144 GBaud**	UI	1/6144.0-100ppm	1/61440	1/6144.0+100ppm	us

Note:

1. The AC specifications do not include Refclk jitter. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 41.
2. The ISI jitter (R_CBHPJ) and amplitude have to be correlated for example by a PCB trace.
3. The intended application is as a point-to-point interface of approximately 60cm and up to two connectors. The maximum allowed total loss (channel + interconnect+ other loss) is 12.2dB @ 6.144 Gb/s.
4. R_Tj total jitter is measured at receiver inputs without post-equalizer.

This table provides the LV-III RX parameters guided by 10GBase-KR electrical interface (IEEE 802.3 [22], clause 72.7.2).

Table 94. CPRI LV-III receiver AC specifications

Symbols	Parameter	Min	Nom	Max	Units
Gaussian Jitter	R_GJ	—	—	0.130	UI p-p
Sinusoidal Jitter, maximum	R_SJ-max	—	—	0.115	UI p-p
DCD - Duty Cycle Distortion	R_dcd	—	—	0.035	UI p-p
Total jitter	R_Tj	—	—	See Note 1.	UI p-p
Unit Interval: **9.8304 GBaud**	UI	1/9.8304-100ppm	1/9.8304	1/9.8304+100ppm	us

Note:

1. The R_Tj is per Interference Tolerance Test IEEE Std 802.3ap-2007 specified in Annex 69A.
2. The AC specifications do not include Refclk jitter.
3. The maximum channel insertion loss is achieved by manual tuning TX equalization.

3 Hardware design considerations

3.1 System clocking

This section describes the PLL configuration of the chip.

3.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are a total of 11 PLLs on the chip.
- There are two selectable e6500 core cluster PLLs which generate a core clock from the externally supplied SYSCLK input. The e6500 core complex can select from CGA1 PLL or CGA2 PLL. The frequency ratio between e6500 core cluster PLLs and SYSCLK is selected using the configuration bits as described in the applicable chip reference manual.
- There are two selectable SC3900 core clusters PLLs which generate a core clock from the externally supplied SYSCLK input. The SC3900 core clusters can select from CGB1 PLL or CGB2 PLL. The frequency ratio between SC3900 core clusters PLLs and SYSCLK is selected using the configuration bits as described in the applicable chip reference manual.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in the applicable chip reference manual.
- There are two DDR PLLs which generate the two DDR clocks (one per each), from the externally supplied DDR(1, 2)_CLK input per PLL (asynchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in the applicable chip reference manual.
- Each of the two SerDes blocks has 2 PLLs which generate a core clock from their respective externally supplied SD*n*_REF*n*_CLK/SD*n*_REF*n*_CLK_B inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.5, "SerDes PLL ratio."

3.1.2 Clock ranges

This table provides the clocking specifications for the e6500 core, SC3900 core, Maple ETVPE, Maple/CPRI, Maple ULB, platform, and DDR memory.

Table 95. Clocking specifications

Characteristic	Frequency		Unit	Notes
	Min	Max		—
e6500 core frequency	250	1600	MHz	1,2,3
SC3900 core frequency	250	1200	MHz	1,2,3
Maple ETVPE frequency	250	1000	MHz	—
Maple/CPRI frequency	250	600	MHz	—
Maple ULB frequency	250	800	MHz	—
Platform clock frequency	400	667	MHz	1, 5
DDR memory bus clock frequency	1067	1866	MHz	6
FM frequency	450	667	MHz	4

Notes:

1. **Caution:** The platform clock to SYSCLK ratio and any core to SYSCLK ratio settings must be chosen such that the resulting cores frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The core can run at core complex PLL/1, PLL/2 or PLL/4 with a minimum PLL frequency of 1000.0 MHz. This results in a minimum allowable core frequency of 250 MHz for PLL/4.
3. The e6500 and SC3900 clusters frequency must be at least the (Platform frequency)/2 and higher.
4. FM minimum frequency is 450 MHz when only SGMII at 1 Gbps ports are required (for example, no usage of SGMII2.5). Otherwise, FM minimum frequency is 625 MHz.
5. 5G SRIO port operation is not supported for platform frequencies below 528 MHz.
6. DDR1 PLL and DDR2 PLL must have a reference clock of 133.333 MHz to achieve a frequency of 1866.667 MHz.

NOTE

Hardware accelerators cannot run at core/3 and core/4 speeds if the core speed is configured to less than 1 GHz. When the core speed is configured to less than 1 GHz, core/4 speed is not feasible for DFS. Cluster PLL maximum output frequency is 1800 MHz if SYSCLK is lower than 100 MHz.

3.1.3 Platform to SYSCLK PLL ratio

The allowed platform clock to SYSCLK ratio is from 3:1 to 12:1.

3.1.4 PPC core cluster to SYSCLK PLL ratio

The allowed e6500 core cluster or SC3900 cluster PLL clock to SYSCLK ratio are from 6:1 to 27:1.

3.1.5 SerDes PLL ratio

The allowed platform clock to SYSCLK ratio are from 3:1 to 12:1.

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD*n*_REF*n*_CLK/SDn_REFn_CLK_B inputs is determined by a set of RCW Configuration fields—SRDS_PRTCL_S*n*, SRDS_PLL_REF_CLK_SEL_S*n* — as shown in this table.

Table 96. Valid SerDes RCW encoding and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S*n*	Legal setting for SRDS_PLL_REF_CLK_SEL_S*n*	Notes
High-speed serial and debug interfaces				
PCI Express 2.5 Gbps (doesn't negotiate upwards)	100 MHz	Any PCIe	0b0: 100 MHz	1
	125 MHz		0b1: 125 MHz	1
PCI Express 5 Gbps (can negotiate up to 5 Gbps)	100 MHz	Any PCIe	0b0: 100 MHz	1
	125 MHz		0b1: 125 MHz	1
Serial RapidIO 2.5 Gbps	100 MHz	sRIO @ 2.5/5 Gbps	0b0: 100 MHz	—
	125 MHz		0b1: 125 MHz	—
Serial RapidIO 3.125 Gbps	125 MHz	sRIO @ 3.125 Gbps	0b0: 125 MHz	—
	156.25 MHz		0b1: 156.25 MHz	—
Serial RapidIO 5 Gbps	100 MHz	sRIO @ 2.5/5 Gbps	0b0: 100 MHz	—
	125 MHz		0b1: 125 MHz	—
CPRI 1.2288 Gbps	122.88 MHz	CPRI @ 1.2288 Gbps	0b0: 122.88 MHz	—
CPRI 2.4576 Gbps	122.88 MHz	CPRI @ 2.4576 Gbps	0b0: 122.88 MHz	—
CPRI 3.072 Gbps	122.88 MHz	CPRI @ 3.072 Gbps	0b0: 122.88 MHz	—
CPRI 4.9152 Gbps	122.88 MHz	CPRI @ 4.9152 Gbps	0b0: 122.88 MHz	—
CPRI 6.144 Gbps	122.88 MHz	CPRI @ 6.144 Gbps	0b0: 122.88 MHz	—
CPRI 9.8304 Gbps	122.88 MHz	CPRI @ 9.8304 Gbps	0b0: 122.88 MHz	—
Debug (2.5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	—
	125 MHz		0b1: 125 MHz	—
Debug (3.125 Gbps)	125 MHz	Aurora @ 3.125 Gbps	0b0: 125 MHz	—
	156.25 MHz		0b1: 156.25 MHz	—

Table 96. Valid SerDes RCW encoding and reference clocks (continued)

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S*n*	Legal setting for SRDS_PLL_REF_CLK_SEL_S*n*	Notes
Debug (5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	—
	125 MHz		0b1: 125 MHz	—
Networking interfaces				
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0b0: 100 MHz	—
	125 MHz		0b1: 125 MHz	—
2.5x SGMII (3.125 Gbps)	125 MHz	SGMII @ 3.125 Gbps	0b0: 125 MHz	—
	156.25 MHz		0b1: 156.25 MHz	—
XAUI (3.125 Gbps)	125 MHz	XAUI @ 3.125 Gbps	0b0: 125 MHz	—
	156.25 MHz		0b1: 156.25 MHz	—
XFI (10.3125 Gbps)	156.25 Mhz	XFI @ 10.3125 Gbps	0b0: 156.25 MHz	—

Note:

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interfaces such as sRIO, or debug is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

3.1.5.1 D*n*_DDRCLK and DDR*n* memory frequency options

This table shows the expected frequency options for D*n*_DDRCLK and DDR*n* memory frequencies.

Table 97. D*n*_DDRCLK and DDR*n* data rate options

DDR*n* data rate: D*n*_DDRCLK	D*n*_DDRCLK (MHz)			
	66.667	100.000	125.000	133.333
	DDR*n* data rate (MT/s)[1]			
8:1				1066.667
9:1				
10:1				1333.333
11:1				
12:1				1600.000
13:1		1300.000		
14:1				1866.667
15:1				
16:1	1066.667	1600.000		
17:1				

Table 97. D*n*_DDRCLK and DDR*n* data rate options (continued)

18:1	1200.000	1800.000	
19:1			
20:1	1333.333		

Notes:

1. DDR data rate values are shown rounded to the nearest whole number (decimal place accuracy removed)

3.2 Power supply design

3.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (DCFG_CCSR_FUSESR) and then configure the external voltage regulator based on this information. This method requires an adjustable point of load voltage regulator (POL).

NOTE

During the power-on reset process, the fuse values are read and stored in the DCFG_CCSR_FUSESR. It is expected that the chip's boot code reads the DCFG_CCSR_FUSESR register very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating VDD at initial start-up of 1.05 V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution.

For additional information on VID, see the chip reference manual.

3.2.1.1 Options for system design

There are several widely-accepted options available to the system designer for obtaining the benefits of a VID solution. The most common option is to use the VID solution to drive a system's controllable voltage-regulators through a sideband interface such as a simple parallel bus or PMBus interface. PMBus is similar to I2C but with extensions to improve robustness and address shortcomings of I2C; the PMBus specification can be found at www.pmbus.org. The simple parallel bus is supported by the chip through GPIO pins and the PMBus interface is supported by an I2C interface. Other VID solutions may be to access an FPGA/ASIC or separate power management chip through the IFC, SPI, or other chip-specific interface, where the other device then manages the voltage regulator. The method chosen for implementing the chip-specific voltage in the system is decided by the user.

3.2.1.1.1 Example 1: Regulators supporting parallel bus configuration

In this example, a user builds a VID solution using controllable regulators with a parallel bus. In this implementation, the user chooses to utilize any subset of the available GPIO pins on the chip except those noted below.

NOTE

GPIO pins that are muxed on an interface used by the application for loading RCW information are not available for VID use.

It is recommended that all GPIO pins used for VID are located in the same 32-bit GPIO IP block so that all bits can be accessed with a single read or write.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The GPIO pins are released to high-impedance at POR. Because GPIO pins default to being inputs, they do not begin automatically driving after POR, and only work as outputs under software control.
2. The board is responsible for a default voltage regulator setting that is "safe" for the system to boot. To achieve this, the user puts pull-up and/or pull-down resistors on the GPIO pins as needed for that specific system. For the case where the regulator's interface operates at a different voltage than OVDD, the chip's GPIO module can be operated in an open drain configuration.
3. There is no direct connection between the Fuse Status Register (FUSESR) and the chip's pins. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software determines the proper value for the parallel interface and writes it to the GPIO block data (GPDAT) register. It then changes the GPIO direction (GPDIR) register from input to output to drive the new value on the device pins, thus overriding the board configuration default value. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
4. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task if desired.

3.2.1.1.2 Example 2: Regulators supporting PMBus configuration

In this example, a user builds a VID solution using controllable regulators with a PMBus interface. For the case where the regulator's interface operates at a different voltage than DVDD, the chip's I2C module can be operated in an open-drain configuration.

In this implementation, the user chooses to utilize any I2C interface available on the chip. These regulators have a means for setting a safe, default, operating value either through strapping pins or through a default, non-volatile store.

NOTE

If I2C1 controller is selected, it is important that its calling address is different than the 7-bit value of 0x50h used by the pre-boot loader (PBL) for RCW and pre-boot initialization.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR register and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the I2C interface connected to the regulator's PMBus interface. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

3.2.1.1.3 Example 3: Regulators supporting FPGA/ASIC or separate power management device configuration

In this example, a user builds a VID solution using controllable regulators that are managed by a FPGA/ASIC or a separate power-management device. In this implementation, the user chooses to utilize the IFC, eSPI or any other available chip interface to connect to the power-management device.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.

2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the IFC, eSPI, or any other interface that is used to connect to the FPGA/ASIC or separate power-management device that manages the regulator. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

3.2.2 Core supply voltage filtering

The V_{DD} supply is normally derived from a high current capacity or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the power supply voltage within ± 30 mV.

These bulk decoupling capacitors ideally supply a stable voltage for current transients into the megahertz range. Above that, see Section 3.3, "Decoupling recommendations for further decoupling recommendations.

3.2.3 PLL power supply filtering

Each of the PLLs described in Section 3.1, "System clocking," is provided with power through independent power supply pins (AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_DDRn and AV_{DD}_SRDSn_PLLn). AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_DDRn voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme. AV_{DD}_SRDSn_PLLn voltages must be derived directly from the XVDD voltage source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 49, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%

C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH

C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

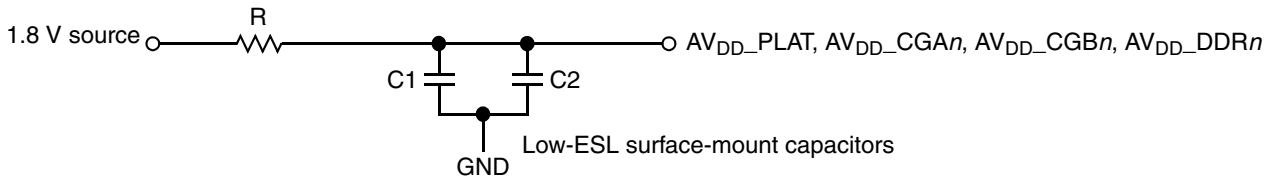


Figure 49. PLL power supply filter circuit

The AV_{DD}_SRDSn_PLLn signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 50. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SRDSn_PLLn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SRDSn_PLLn balls. The 0.003-µF capacitors closest to the balls, followed by a 4.7-µF and 47-µF capacitor, and finally the 0.33 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SRDS*n*_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

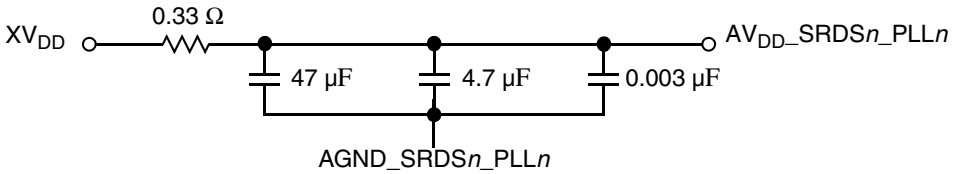


Figure 50. SerDes PLL power supply filter circuit

Note the following:

- AV_{DD}_SRDS*n*_PLL*n* should be a filtered version of XV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD}_SRDSn_PLLn is defined at the PLL supply filter and not the pin of AV_{DD}_SRDS*n*_PLL*n*.
- A 47-µF 0805 XR5 or XR7, 4.7-µF, and 0.003-µF or smaller capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, AGND_SRDS*n*_PLL*n* for each AV_{DD}_SRDS*n*_PLL*n* pin up to the physical local of the filters themselves.

3.2.4 SV_{DD} power supply filtering

SV_{DD} should be supplied by a dedicated linear regulator. Systems may design to allow flexibility to address system noise dependencies.

NOTE

For initial system bring-up, the linear regulator option is highly recommended.

An example solution for SV_{DD} filtering, where SV_{DD} is sourced from linear regulator, is illustrated in Figure 51. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH

C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

F1 to F4 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05, or 0.0125 for the parallel resultant, and each has about a 120+-25% of AC impedance at 100 MHz, which will be

quarter valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps. Bulk and decoupling capacitors are added, as needed, per power supply design.

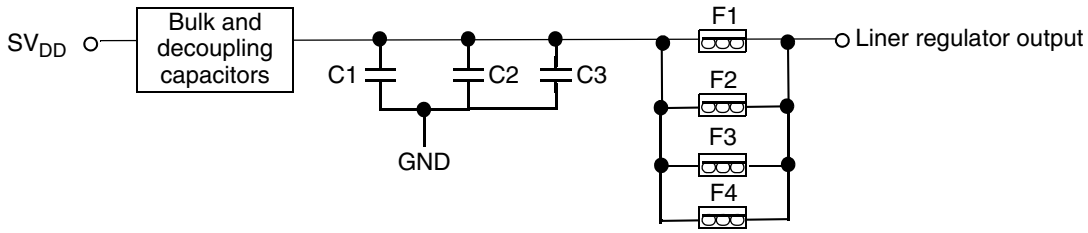


Figure 51. SV_{DD} power supply filter circuit

3.2.5 XV_{DD} power supply filtering

XV_{DD} must be supplied by a linear regulator or sourced by a filtered GnV_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies.

NOTE

For initial system bring-up, the linear regulator option is highly recommended.

An example solution for XV_{DD} filtering, where XV_{DD} is sourced from a linear regulator, is illustrated in Figure 52. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH

C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH

F1 to F4 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05, or 0.0125 for the parallel resultant, and each has about a 120+-25% of AC impedance at 100 MHz, which will be quarter valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps.Bulk and decoupling capacitors are added, as needed, per power supply design.

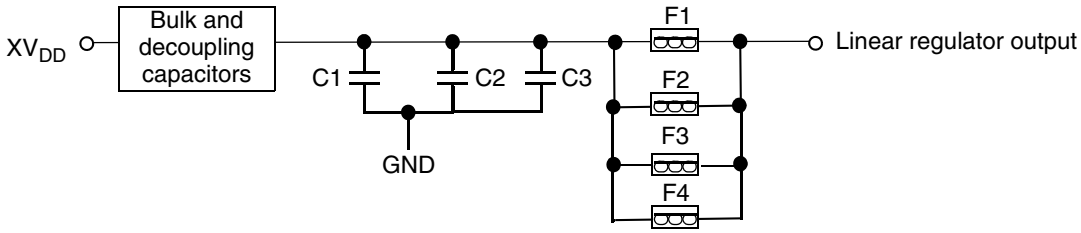


Figure 52. XV_{DD} power supply filter circuit

3.2.6 Remote power-supply sense recommendations

There is a practice of connecting the remote sense signal of an on-board power supply to one of power supply pins of an IC device. The advantage of this connection is the ability to compensate for the slow components of the IR droop caused by the resistive supply current path from the on-board power supply to the C5 pins layer on-package (for flip-chip packages).

However, not every C5 pin is selected to be the remote sense pin. It may be a reserved pin that requires a connection to be a supply or ground pin, and therefore must remain connected to the corresponding supply. Alternatively, the C5 pin may be

supplying the critical power-consuming area of the IC die whose usage as non-supply pin may cause shortage in the supply current during high-current peaks.

It is recommended that these pins be used as the board supply remote sense output, because they do not degrade the power and ground supply quality:

- VDD/VSS sense pair: K9/J9 or AE12/AD11

Connect to either sense pair and leave the other pair unconnected.

3.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place decoupling capacitors at each V_{DD}, OV_{DD}, QV_{DD}, DV_{DD} and GnV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, QV_{DD}, DV_{DD} and GnV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in Section 3.2.2, "Core supply voltage filtering," it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (For example, OV_{DD}, QV_{DD}, DV_{DD} and GnV_{DD}), to enable quick recharging of the smaller chip capacitors.

3.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1×0.1-µF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor, for example, a 10-µF, low ESR SMT tantalum or ceramic chip capacitor and a higher bulk capacitor, for example, a 100-µF–300-µF low ESR SMT tantalum or ceramic chip capacitor.

3.5 Connection recommendations for unused pins

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs and open-drain I/O should be tied to V_{DD}, QV_{DD}, DV_{DD}, OV_{DD} and GnV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, QV_{DD}, DV_{DD}, OV_{DD}, $GnV_{DD}$and GND pins of the chip.

Unused LVCMOS pins recommendations:

- For unused input only and bidirectional pins, connect with a pull-down resistor of 10 kΩ.

- Unused output only pins can be left floating.

Unused DDR pins recommendations:

- When the following conditions are met, clocks, address, control, mask, cmd, data, strobes, MAPAR_OUT pin, and MAPAR_ERR_B pins can be left floating:
  - the output buffer is tristated,
  - the receiver is in sleep mode,
  - and termination is off.
- When the conditions above are not met, connect the clocks, address, control, mask, cmd, data, positive strobes, MAPAR_OUT pin, and MAPAR_ERR_B pins to GND via a 1 kΩ resistor. Negative strobes should be pulled-up to GnV_{DD} via a 1 kΩ resistor.
- If the whole DDR module is not used, connect GV_{DD} and MVREF to GND and connect DDR_AVDD to OV_{DD}.
- If the DDR2 interface is not used, D2_DDRCLK can be connected to GND via a 10 kΩ resistor.
- If the DDR1 interface is not used, D1_DDRCLK still needs to toggle.

3.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 54. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 54 allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 53, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 53 is common to all known emulators.

3.5.1.1 Termination of unused signals

If the JTAG interface and COP header are not used, NXP recommends the following connections:

- TRST_B should be tied to PORESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. NXP

recommends that the COP header be designed into the system as shown in Figure 54. If this is not possible, the isolation resistor will allow future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS or TDO.

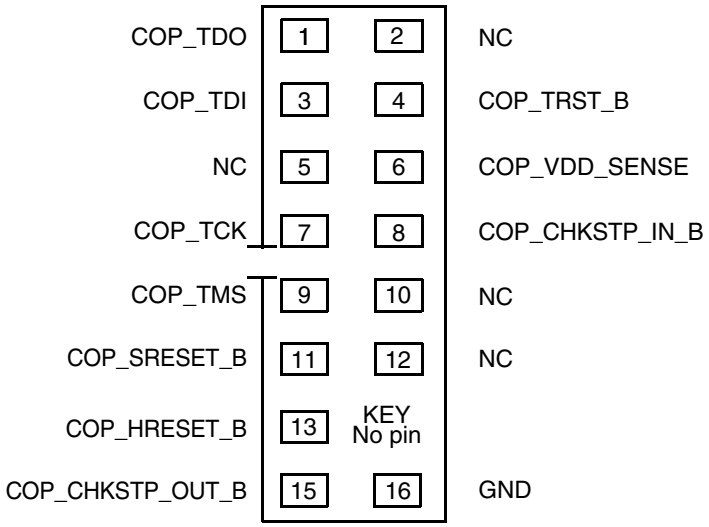
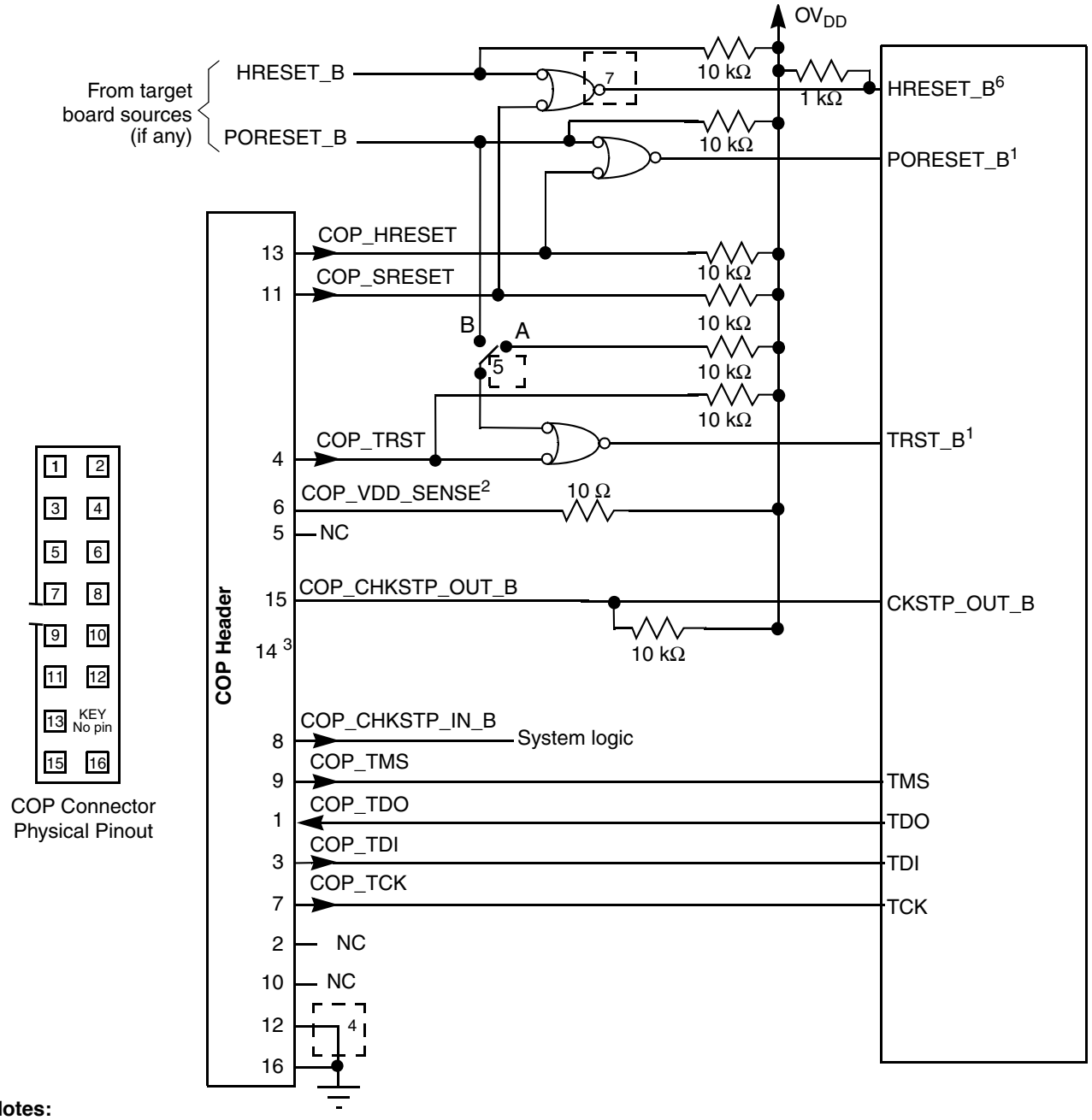


Figure 53. Legacy COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert POREST_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting HRESET_B causes a hard reset on the chip.
7. This gate is an open-drain gate.

Figure 54. Legacy JTAG interface connection

3.5.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 56. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

NXP recommends the Aurora 34 or 70 pin duplex connectors be designed into the system as shown in the following figures.

If the Aurora interface is not used, NXP recommends the legacy COP header be designed into the system as described in Section 3.5.1.1, "Termination of unused signals."

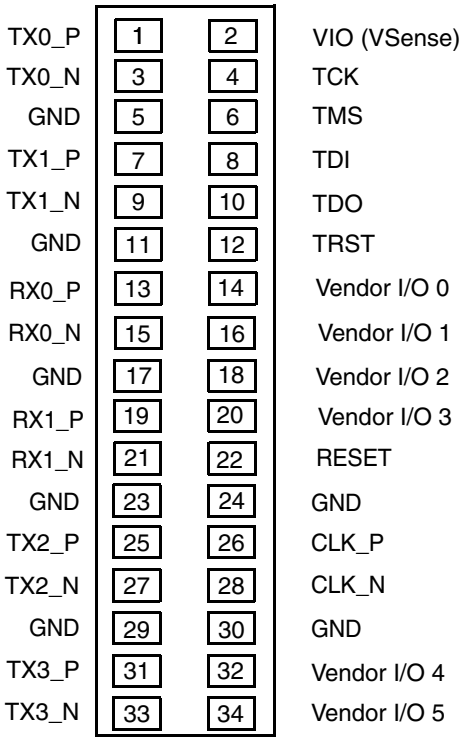


Figure 55. Aurora 34 pin connector duplex pinout

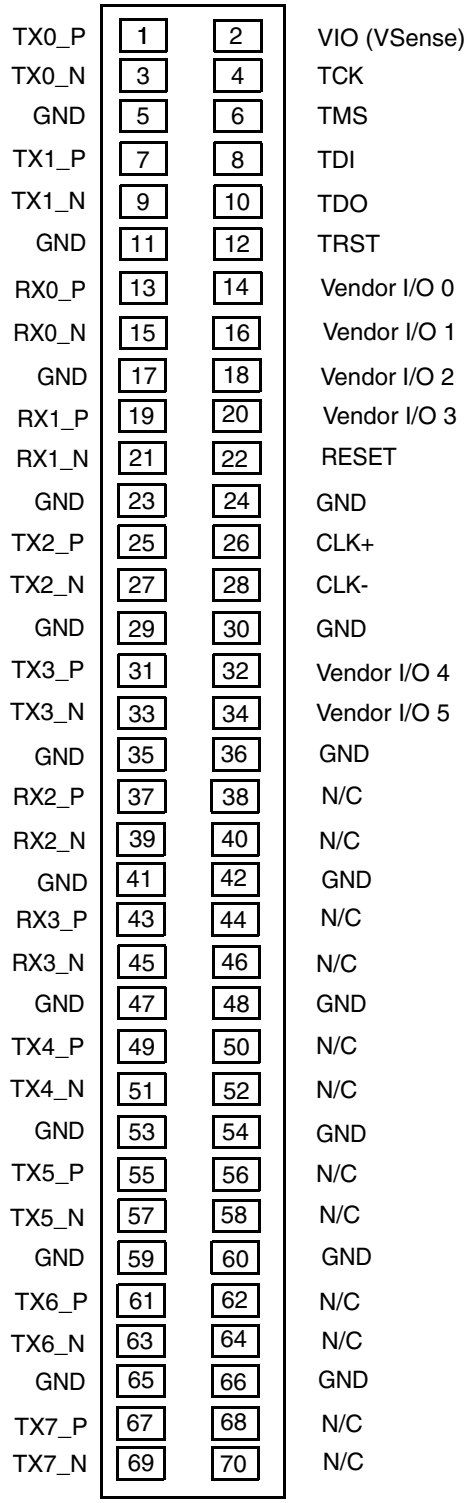
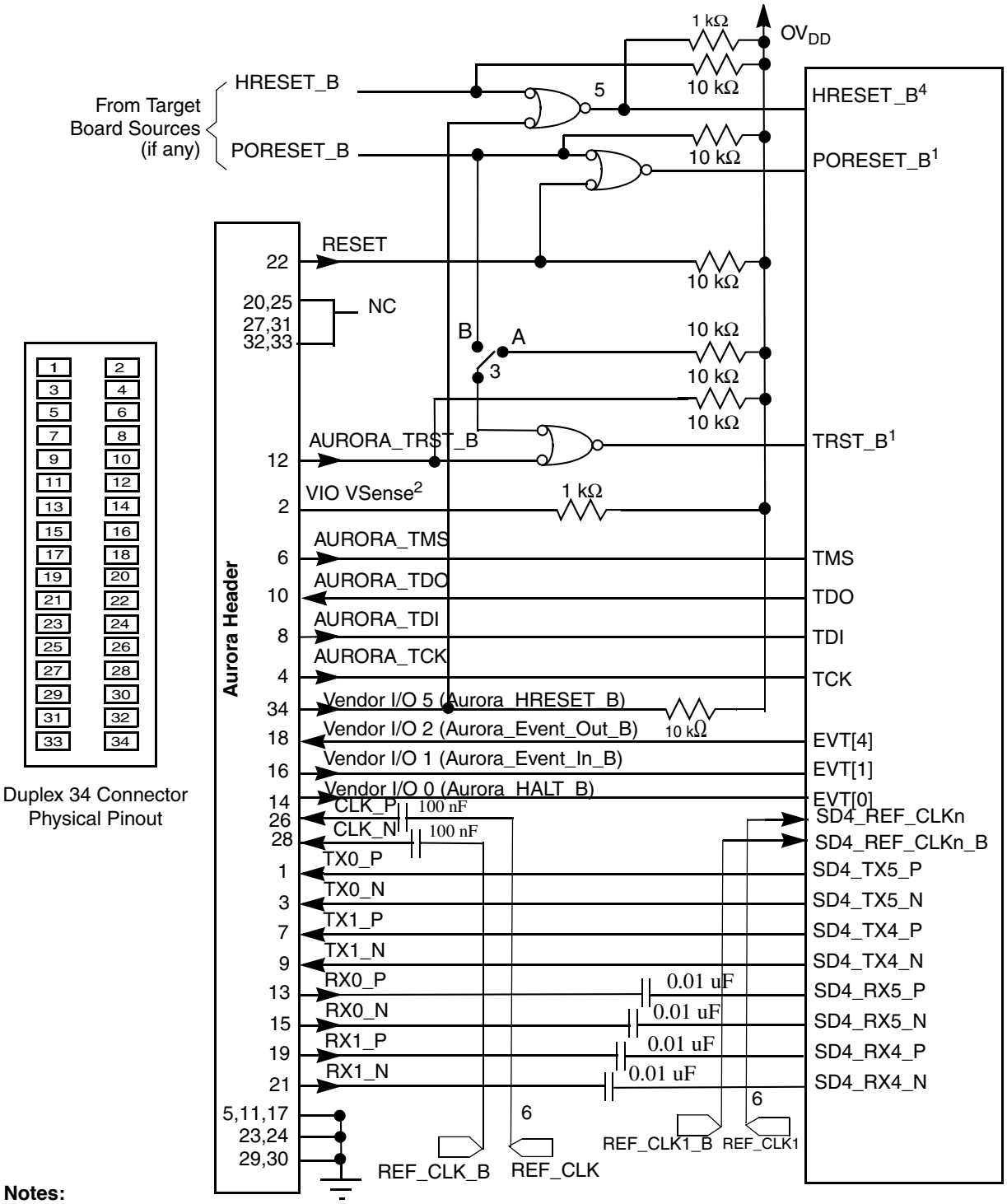


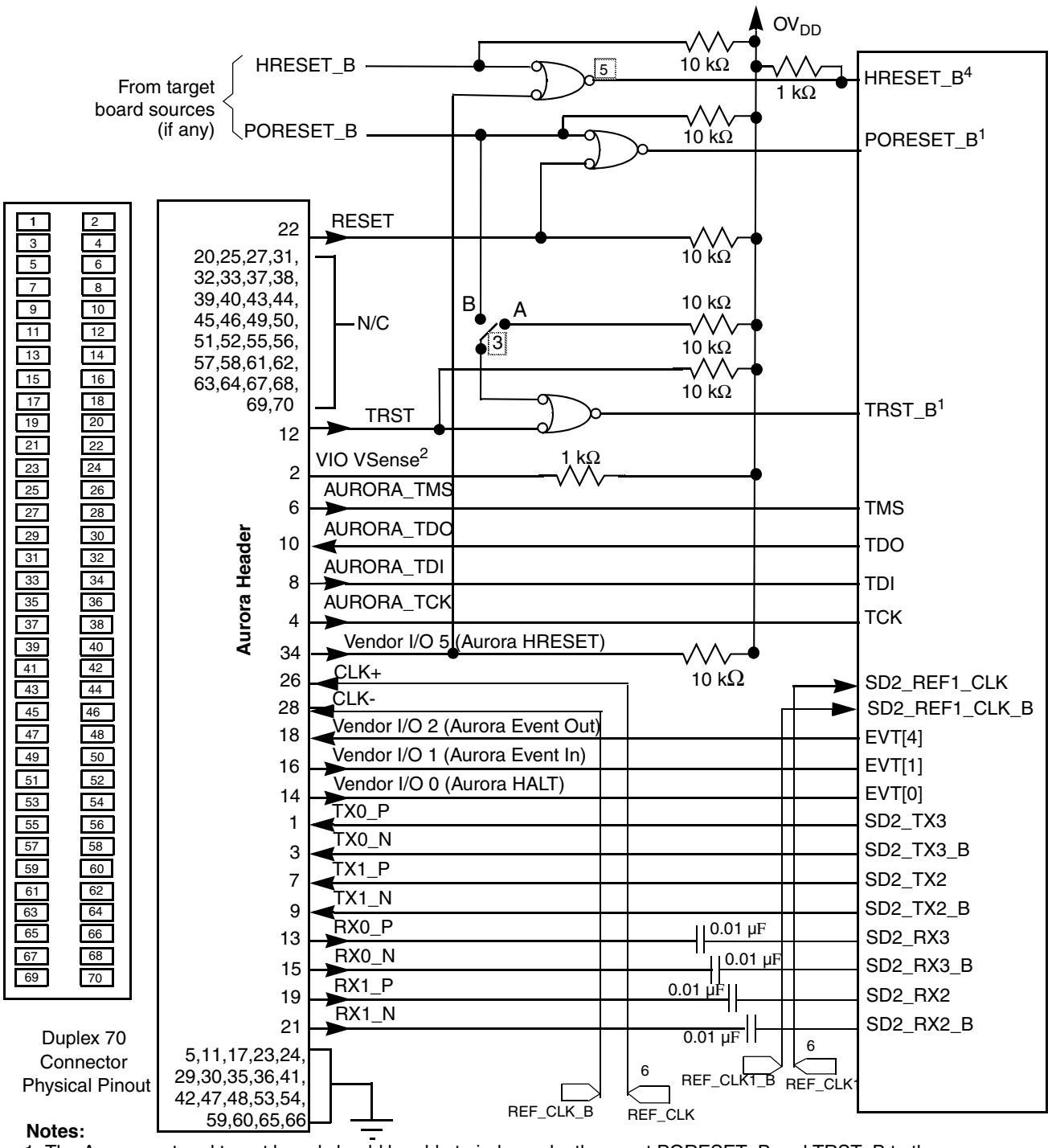
Figure 56. Aurora 70 pin connector duplex pinout



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. Close the switch to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, close this switch to position B.
4. Asserting HRESET_B causes a hard reset on the device.
5. This is an open-drain output gate.
6. REF_CLK/REF_CLK_B and REF_CLK1/REF_CLK1_B are buffered clocks from the same common source.

Figure 57. Aurora 34 pin connector duplex interface connection



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting HRESET_B causes a hard reset on the chip.
5. This gate is an open-drain gate.
6. REF_CLK/REF_CLK_B and REF_CLK1/REF_CLK1_B are buffered clocks from the same common source.

Figure 58. Aurora 70 pin connector duplex interface connection

3.5.3 Guidelines for high-speed interface termination

3.5.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that both SV_{DD} and XV_{DD} must remain powered.

The following pins must be left unconnected:

- SD*n*_TX[7:0]
- SD*n*_TX[7:0]_B

The following pins must be connected to SGND:

- SD*n*_RX[7:0]
- SD$\overline{n}$_RX[7:0]_B
- SD*n*_REF1_CLK, SDn_REF2_CLK
- SD*n*_REF1_CLK_B, SDn_REF2_CLK_B

The following pins must be left unconnected:

- SD*n*_IMP_CAL_RX
- SD*n*_IMP_CAL_TX

In the RCW configuration fields SRDS_PLL_PD_S1, and SRDS_PLL_PD_S2, all bits must be set to power down both PLLs of the corresponding SerDes module. A module is disabled when both its PLLs are turned off.

3.5.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following unused pins must be left unconnected:

- SDn_TX[*n*]
- SDn_TX[*n*]_B

The following unused pins must be connected to SGND:

- SDn_RX[*n*]
- SDn_RX[*n*]_B
- SDn_REF[1:2]_CLK, SDn_REF[1:2]_CLK_B (Clock pair that is not used)

In the RCW configuration field SRDS_PLL_PD_S*n*, the respective bits for each unused module must be set to power down the PLLs of the corresponding SerDes module.

After POR, if an entire SerDes module is unused, it can be powered down by clearing the SDEN fields of its corresponding PLL1 and PLL2 reset control registers (SRDS*n*_PLL*m*RSQCTL).

Unused lanes can be powered down by clearing the RRST and TRST fields and setting the RX_PD and TX_PD fields in the corresponding lane's general control register (SRDSn_LxGCR0).

3.6 Thermal

This table shows the thermal characteristics for the chip.

Table 98. Package thermal characteristics [6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	16	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	11	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	10	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2
Junction to board	—	$R_{\Theta JB}$	3.3	°C/W	3
Junction-to-case top	—	$R_{\Theta JCtop}$	0.37	°C/W	4
Junction-to-lid top	—	$R_{\Theta JClid}$	0.18	°C/W	5

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51–3 and JESD51–6 with the board (JESD51–9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51–8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Junction-to-lid-top thermal resistance is determined using the MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid-top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and the cold plate.
6. See Section 3.7, “Thermal management information,” for additional details.

3.7 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 59. The heat sink

should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 31 lbs (137 Newton).

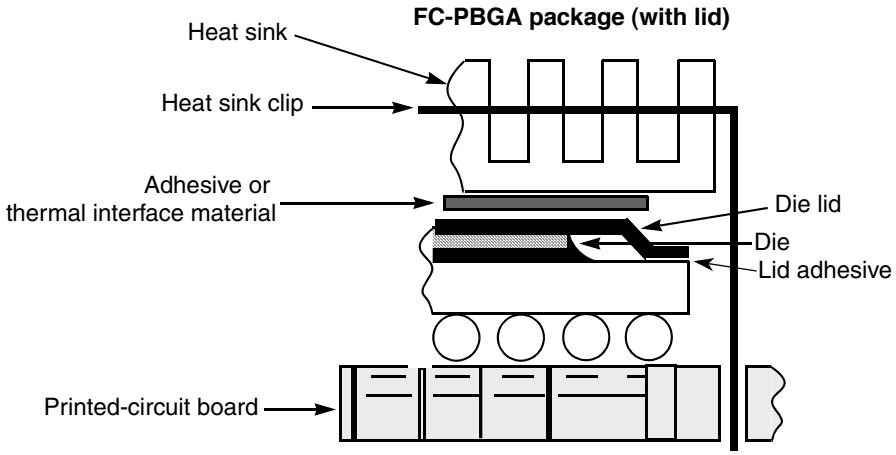


Figure 59. Package exploded, cross-sectional view—FC-PBGA (with lid)

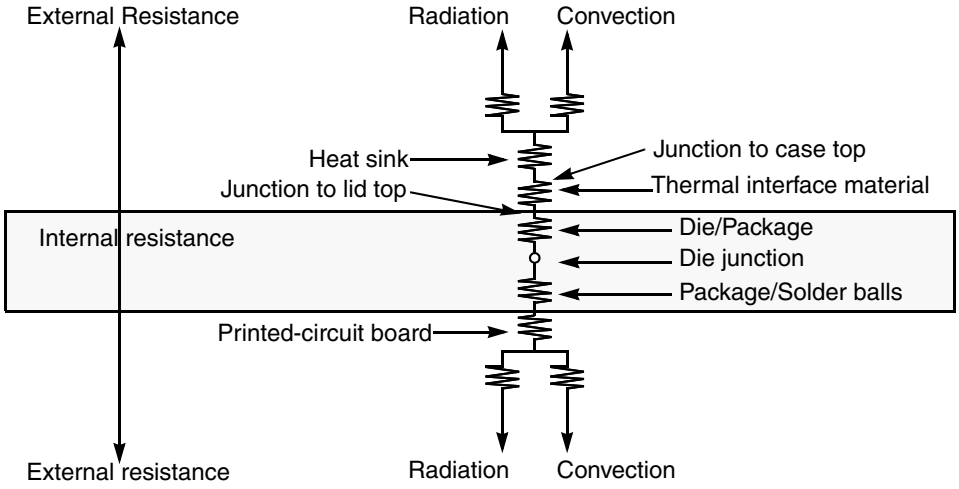
The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.7.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 60. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

3.7.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 59).

The system board designer can choose among several types of commercially-available thermal interface materials.

3.8 Temperature diode

The chip has temperature diodes that can be used to monitor its temperature using external temperature monitoring devices (such as Analog Devices, ADT7461A™). These on-chip temperature diodes have pins that may be connected to test points, or left as a no connect when they are not used.

The following are specifications of the chip temperature diodes:

- Operating range: 10–230μA
- Non-ideality factor over entire temperature range: n = 1.006 ± 0.003

4 Package information

4.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 33 mm × 33 mm, 1020 flip-chip, plastic-ball, grid array (FC-PBGA). The device part is designed to be RoHS and Pb-free compliant.

Package outline	33 mm × 33 mm
Interconnects	1020
Ball Pitch	1.0 mm
Ball Diameter (typical)	0.60 mm
Solder Balls	96.5% Sn, 3% Ag, 0.5% Cu
Module height (typical)	2.63 mm to 2.93 mm (maximum)

4.2 Mechanical dimensions of the B4860 FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.

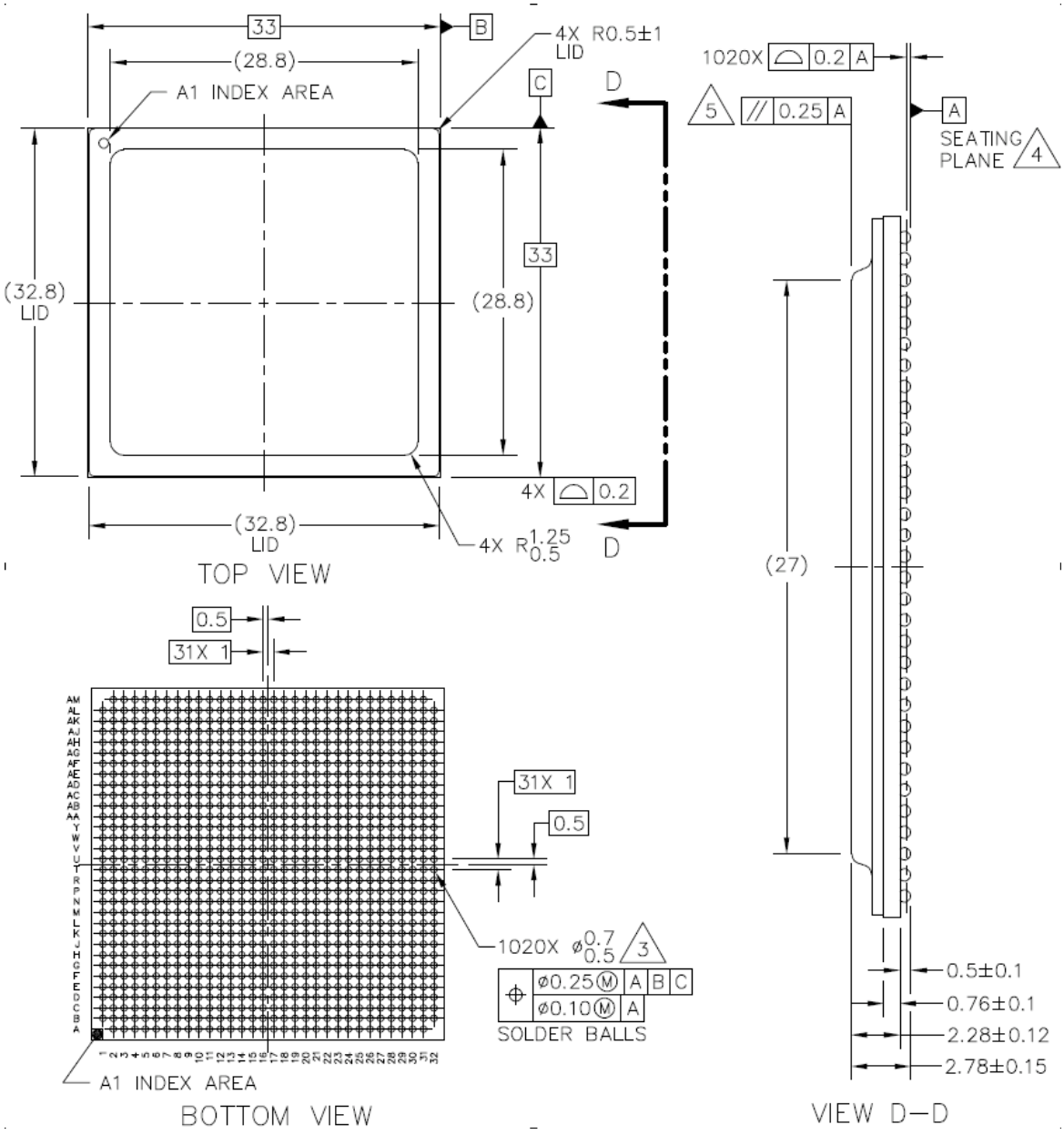


Figure 61. Mechanical dimensions of the FC-PBGA with full lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines unless dimensioned otherwise.
4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
6. Parallelism measurement excludes any effect of mark on top surface of package.

5 Security fuse processor

This chip implements the trust architecture, supporting capabilities such as secure boot. Use of the trust architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the trust architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the POV_{DD} pin per Section 2.2, "Power sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times POV_{DD} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 4.

NOTE

Users not implementing the QorIQ platform's trust architecture features should connect POV_{DD} to GND.

6 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

6.1 Part numbering nomenclature

This table provides the NXP QorIQ Qonverge platform part numbering nomenclature.

Table 99. Part numbering nomenclature

B	4	8	6	X	N	S[1]	E	7	Q	U	M	A
Platform		**Number of Power core threads**	**Number of DSP cores**	**Deriv-ative**	**Qual status**	**Temperature range and power levels**	**Encryp-tion**	**Package type**	**CPU speed**	**DDR speed**	**DSP speed**	**Die revision**
B = Base-band PB = Proto Base-band	4 = Macro	8 = 8 core threads	6 = 6 DSP cores	X = Generic	P = Prototype N = Indust tier	S = Standard temperature (0 to 105) and standard power X = Extended temperature (–40 to 105) and standard power	E = SEC present N = No SEC	7 = FC-PBGA C4/C5 Pb-free	Q = 1600 MHz	U = 1866 MHz	M = 1200 MHz	A = Rev 1.0 B = Rev 2.0 C = Rev 2.1 D = Rev 2.2

Note:

1. One XVDD = 1.35 V option is available for part 'X' extended temperature range.

6.1.1 Part marking

Parts are marked as in the example shown in this figure.

FC-PBGA

Notes:
B486XXXX7XXMX represents the orderable part number.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.
CCCCC is the assembly country code.
ATWLYYWW is the test traceability code.

Figure 62. Part marking for FC-PBGA chip

7 Revision history

This table summarizes changes to this document.

Table 100. Revision history

Revision Number	Date	Description
3	09/2016	• Updated Figure 11 • In Table 15, updated I/O leakage current min value as -50 and max value as 50 • In Table 16, removed rows and note for output high and low current • Updated the document template for NXP standards • Replaced all Freescale instances with NXP • Updated the data Sheet status to “Technical Data” • Removed footer security for Preliminary and NDA release
2	11/’2015	• Updated Section 6, “Ordering information”
1	09/2015	• Updated Section 2.23.10, “10GBase-KR interface”
0	08/2015	• First release after qualification of silicon

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