CY7C1061DV18

16-Mbit (1 M × 16) Static RAM

Features

- High Speed
  - t_{AA} = 15 ns
- Low Active Power
  - I_{CC} = 150 mA at 67 MHz
- Low complementary metal oxide semiconductor (CMOS) Standby Power
  - I_{SB2} = 25 mA
- Operating voltages of 1.7 V to 2.2 V
- 1.5 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free 54-Pin thin small outline package (TSOP) II package

Functional Description

The CY7C1061DV18 is a high performance CMOS Static RAM (SRAM) organized as 1,048,576 words by 16 bits.

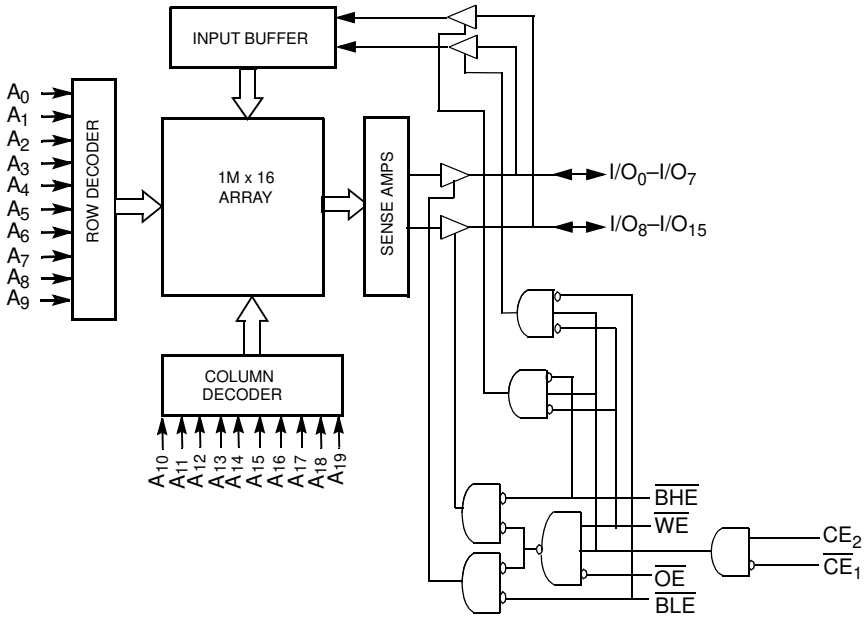
To write to the device, enable the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) while forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, enable the chip by taking $\overline{CE}_1$ LOW and CE_2 HIGH while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 9 for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1061DV18 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



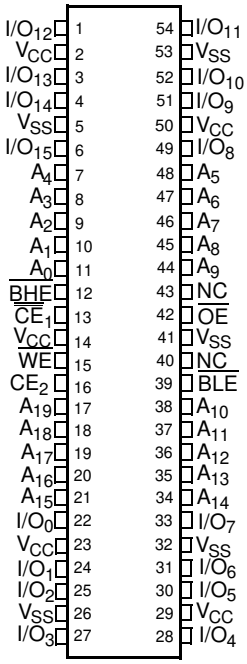
Contents

Selection Guide

Description	–15	Unit
Maximum access time	15	ns
Maximum operating current	150	mA
Maximum CMOS standby current	25	mA

Pin Configurations

Figure 1. 54-Pin TSOP II (Top View)



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +15 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[1]...–0.2 V to +2.45 V

DC voltage applied to outputs in High Z state[1] .....–0.2 V to +2.45 V

DC input voltage[1].....–0.2 V to +2.45 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... .....>2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	1.7 V to 2.2 V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	–15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –0.1 mA	1.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 0.1 mA	–	0.2	V
V_{IH}	Input HIGH voltage		1.4	V_{CC} + 0.2	V
V_{IL}	Input LOW voltage[1]		–0.2	0.4	V
I_{IX}	Input leakage current	GND ≤ V_{IN} ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	Max V_{CC}, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA CMOS levels	–	150	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	$\overline{CE_1}$ ≥ V_{IH}, CE_2 <= V_{IL}, Max V_{CC}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	30	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V, CE_2 <= 0.2 V, Max V_{CC}, V_{IN} ≥ V_{CC} – 0.2 V, or V_{IN} ≤ 0.2 V, f = 0	–	25	mA

Capacitance[2]

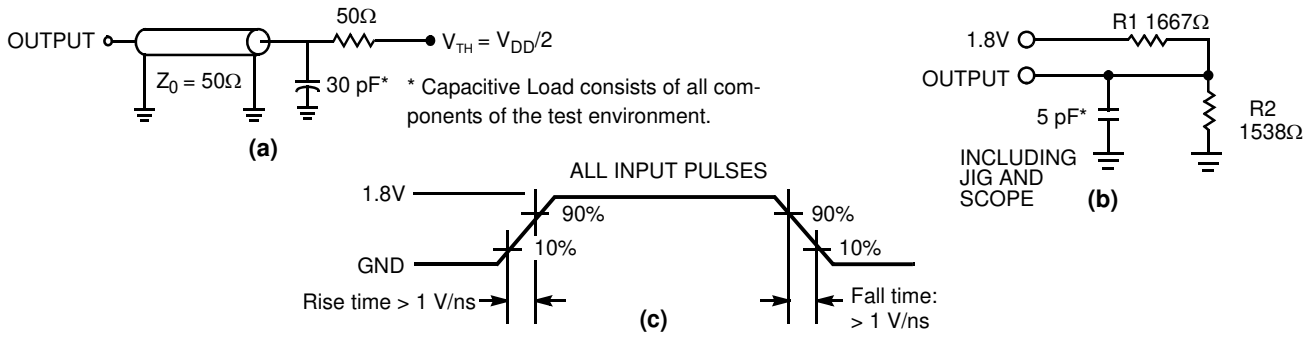
Parameter	Description	Test Conditions	TSOP II	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 1.8 V.	6	pF
C_{OUT}	I/O capacitance		8	pF

Thermal Resistance

Parameter[2]	Description	Test Conditions	TSOP II	Unit
Θ_{JA}	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	24.18	°C/W
Θ_{JC}	Thermal resistance (Junction to case)		5.40	°C/W

Notes
1. V_{IL} (min) = –2.0 V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms[3]



AC Switching Characteristics Over the Operating Range[4]

Parameter	Description	–15		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(typical) to the first access[5]	150	–	µs
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Data hold from address change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to data valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]	–	7	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low-Z[6]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High-Z[6]	–	7	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power-up[7]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power-down[7]	–	15	ns
t_{DBE}	Byte Enable to data valid	–	7	ns
t_{LZBE}	Byte Enable to Low Z	1	–	ns
t_{HZBE}	Byte Disable to High Z	–	7	ns
Write Cycle[8, 9]				
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to write end	10	–	ns
t_{AW}	Address setup to write end	10	–	ns
t_{HA}	Address hold from write end	0	–	ns

Notes

3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (1.5 V). 150 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 1.5 V) voltage.
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 0.9 V, input pulse levels of 0 to 1.8 V. Test conditions for the Read cycle use output loading shown in part a) of the Figure 2, unless specified otherwise.
5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, $t_{\backslash LZWE}$, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 2. Transition is measured ±200 mV from steady-state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal Write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW (CE_2 HIGH) and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
9. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

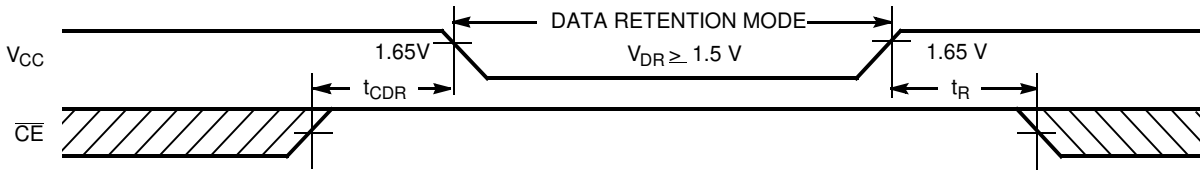
AC Switching Characteristics Over the Operating Range[4](continued)

Parameter	Description	–15		Unit
		Min	Max	
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	10	–	ns
t_{SD}	Data setup to write end	7	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[10]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]	–	7	ns
t_{BW}	Byte enable to end of write	10	–	ns

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ[11]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, or $V_{IN} \leq 0.2$ V	–	–	25	mA
t_{CDR}[12]	Chip deselect to data retention time		0	–	–	ns
t_R[13]	Operation recovery time		t_{RC}	–	–	ns

Figure 3. Data Retention Waveform



Notes

10. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of Figure 2. Transition is measured ±200 mV from steady-state voltage
11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (typ), TA = 25 °C.
12. Tested initially and after any design or process changes that may affect these parameters
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Waveforms

Figure 4. Read Cycle No. 1[14,15]

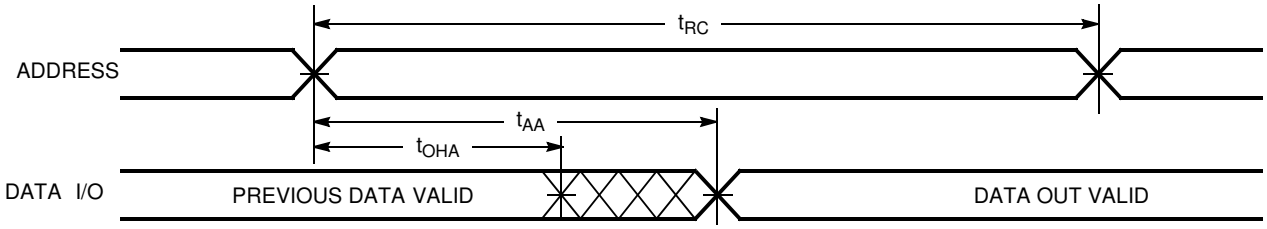
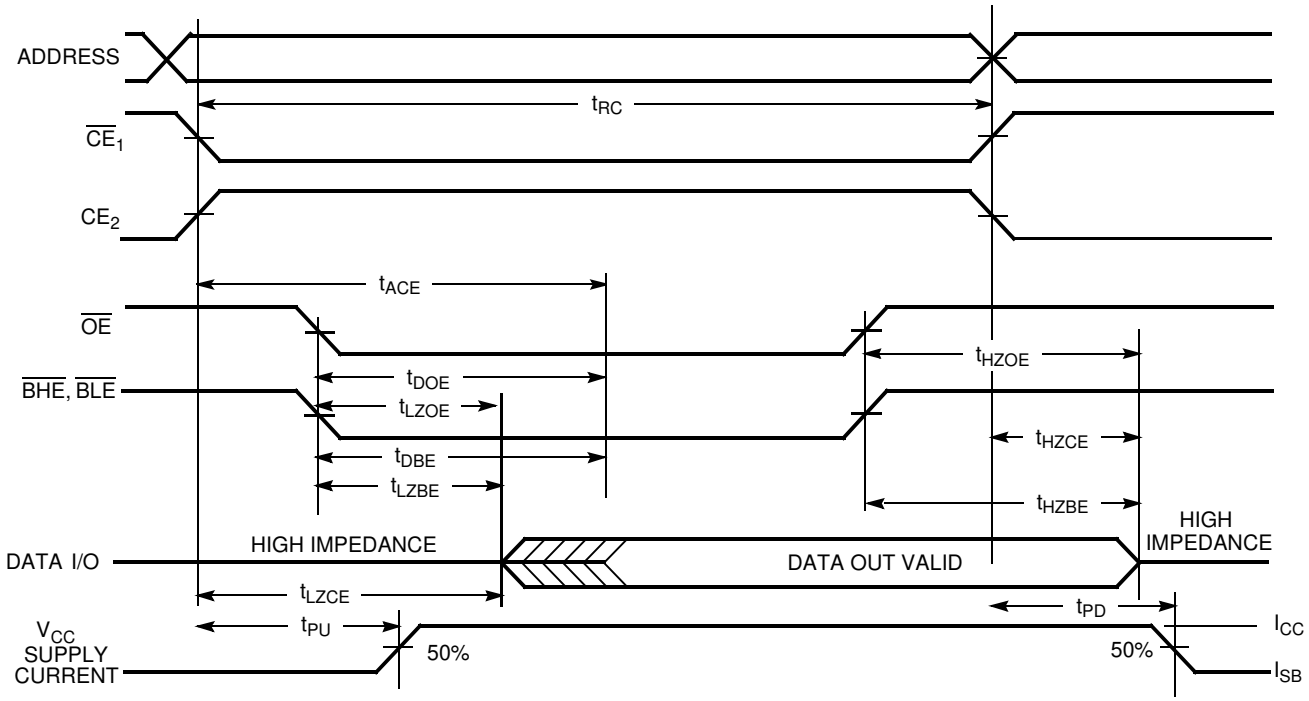


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)[16,17]



Notes
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\ \mu s$ or stable at $V_{CC(min)} \geq 100\ \mu s$.
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}. CE_2 = V_{IH}.
16. $\overline{WE}$ is HIGH for Read cycle.
17. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled)[18,19,20]

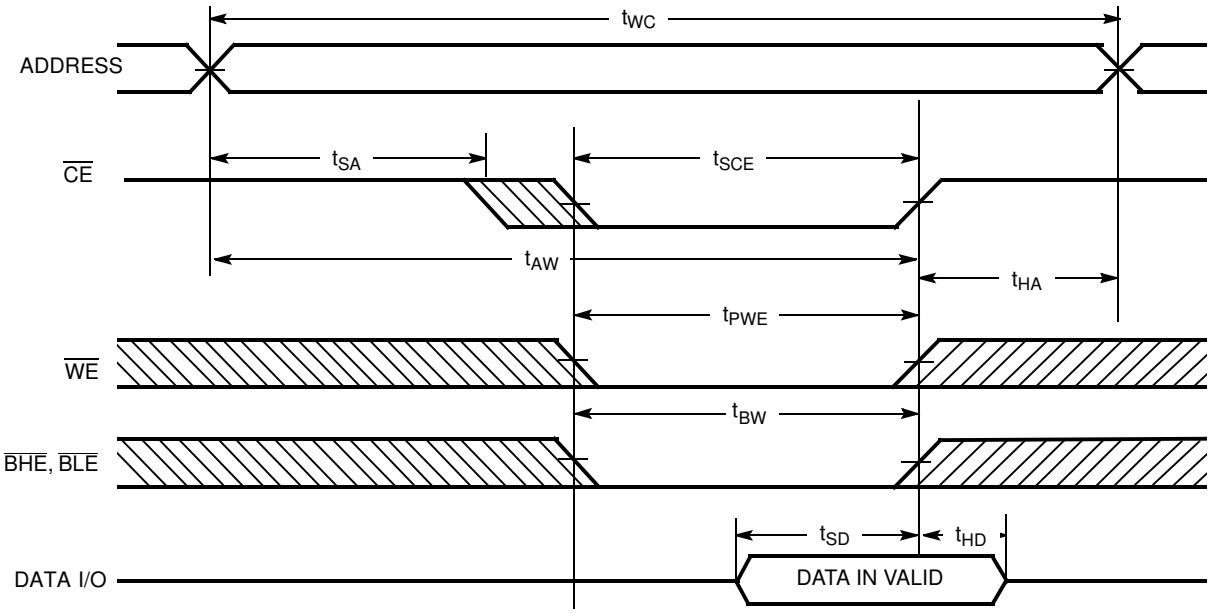
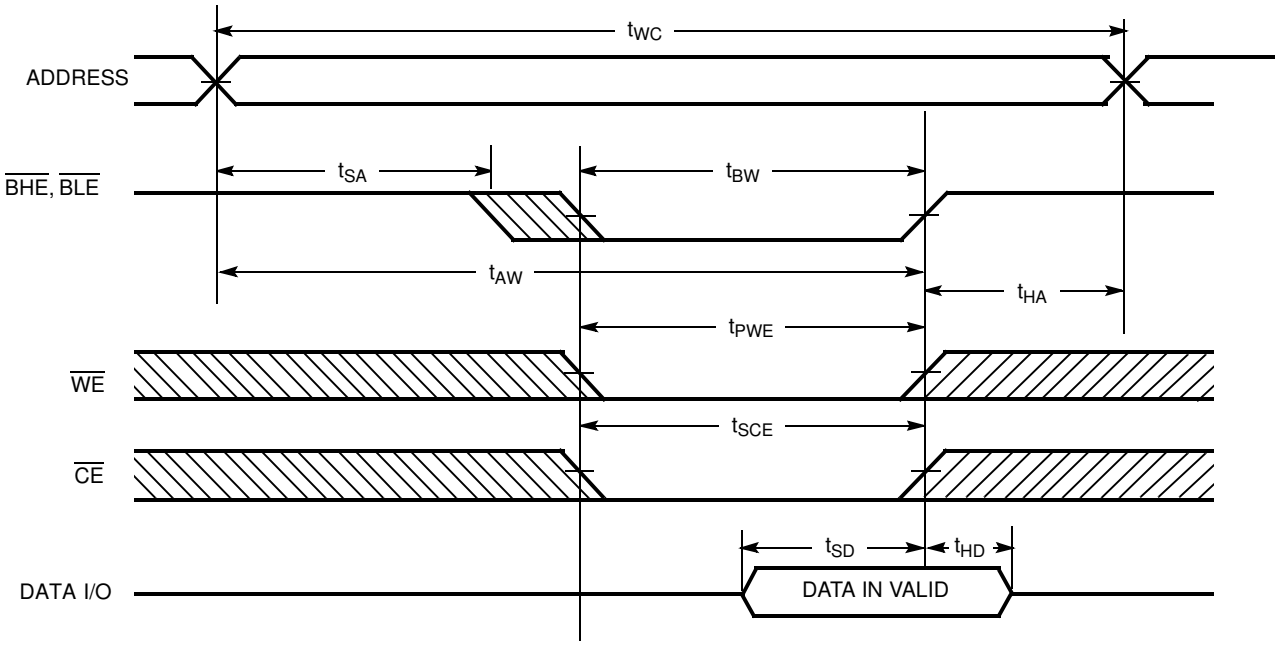
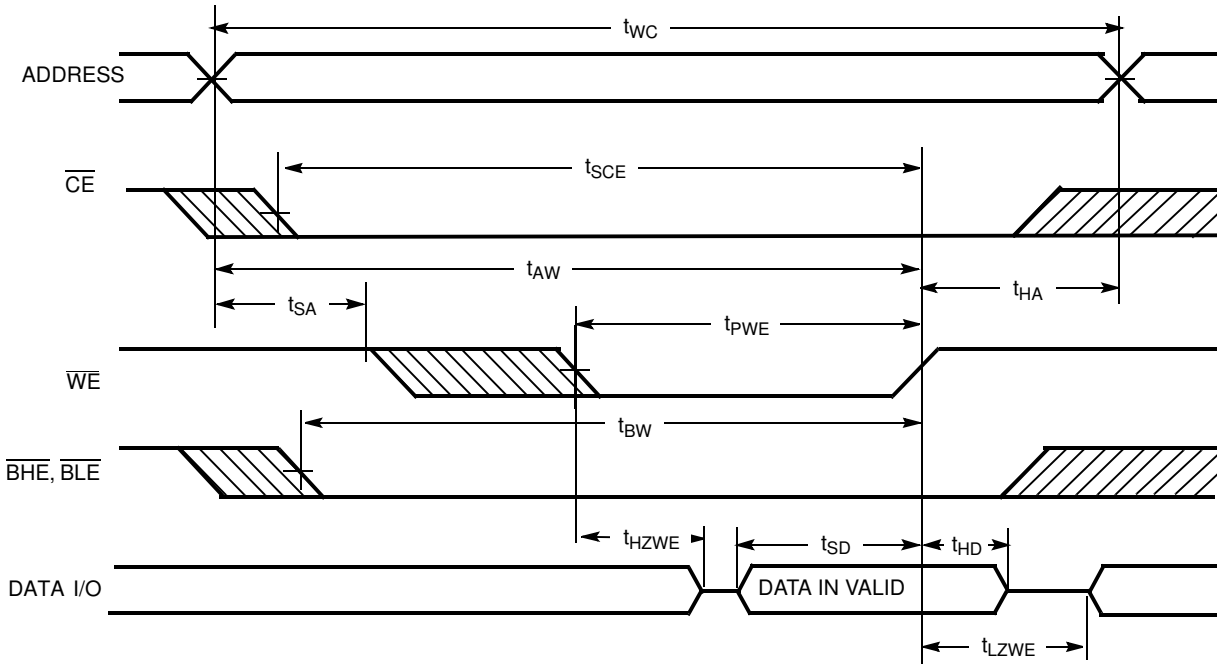


Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
18. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
19. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
20. CE is the logical combination of CE1 and CE2. When CE1 is LOW and CE2 is HIGH, CE is LOW; when CE1 is HIGH or CE2 is LOW, CE is HIGH

Figure 8. Write Cycle No. 3 (WE Controlled, OE Low)[21,22,23]



Truth Table

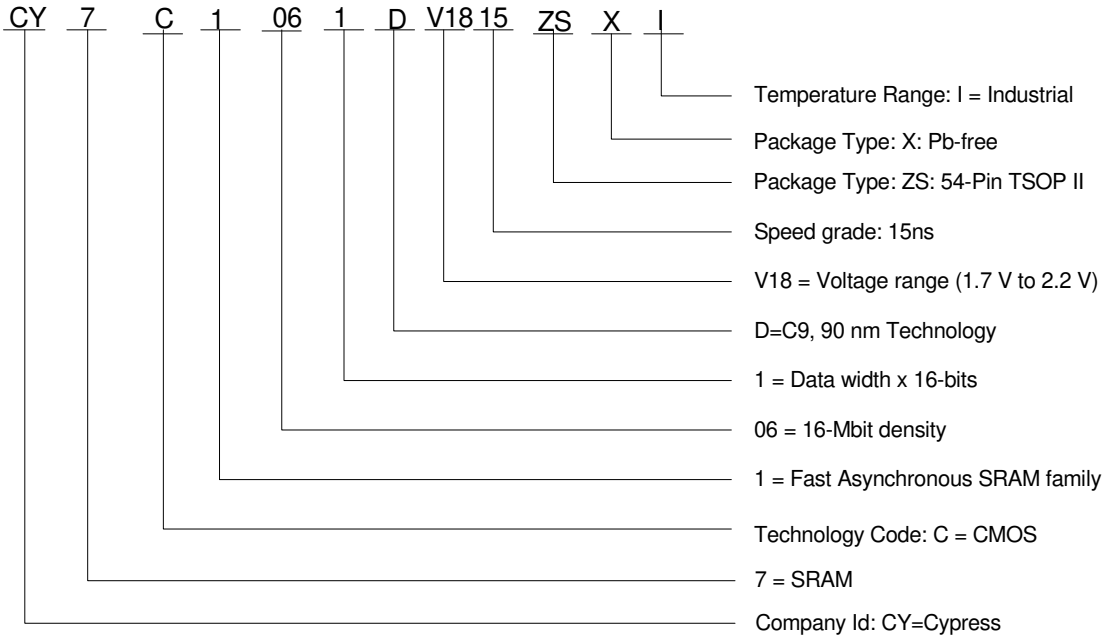
$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	H	L	H	H	L	High -Z	Data out	Read upper bits only	Active (I_{CC})
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Notes
21. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
22. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.
23. $\overline{CE}$ is a shorthand combination of both $\overline{CE}_1$ and CE_2 combined. It is active LOW.

Ordering Information

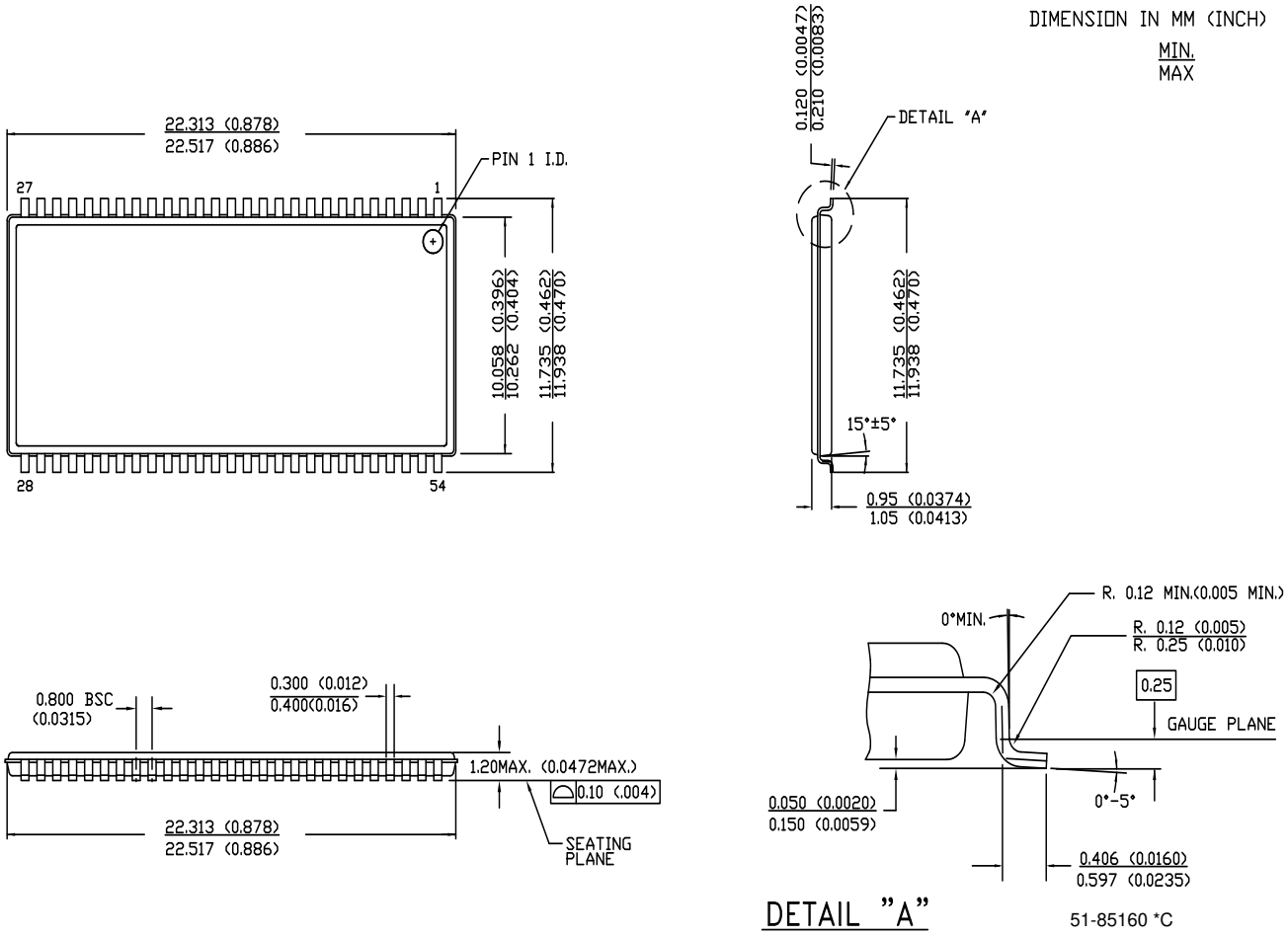
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1061DV18-15ZSXI	51-85160	54 pin TSOP II (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 9. 54-pin TSOP Type II



Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
TSOP	thin small outline package
TTL	Transistor-transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C1061DV18 16-Mbit (1 M × 16) Static RAM Document Number: 001-08350				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	469420	See ECN	NXR	New data sheet
*A	2761557	09/09/2009	VKN	Updated package code
*B	2800121	11/06/2009	VKN	Increased I_{CC} limit from 100mA to 150mA Changed V_{DR} from 1.2V to 1.5V Included Thermal specs Changed t_{LZOE} and t_{LZBE} from 0ns to 1ns Changed t_{LZCE} from 0ns to 3ns Replaced 6 x 8 x 1mm FBGA package with 8 x 9.5 x 1mm FBGA package Changed status from Final to Preliminary
*C	2915361	04/16/2010	VKN	Converted from Preliminary to Final Removed 48-Ball FBGA package from the data sheet Updated links in Sales, Solutions, and Legal Information
*D	2923463	04/27/2010	RAME	Post to external web
*E	3109102	12/13/2010	PRAS	Added Ordering Code Definitions.
*F	3147322	01/19/2011	PRAS	Updated all tables notes as per template Added Acronyms and Units of Measure table.
*G	3387026	09/29/2011	TAVA	Minor technical edits. Updated Package Diagram.

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