

## Features

- High Speed
  - $t_{AA} = 15 \text{ ns}$
- Low Active Power
  - $I_{CC} = 150 \text{ mA}$  at 67 MHz
- Low complementary metal oxide semiconductor (CMOS) Standby Power
  - $I_{SB2} = 25 \text{ mA}$
- Operating voltages of 1.7 V to 2.2 V
- 1.5 V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-Pin thin small outline package (TSOP II) package

## Functional Description

The CY7C1061DV18 is a high performance CMOS Static RAM (SRAM) organized as 1,048,576 words by 16 bits.

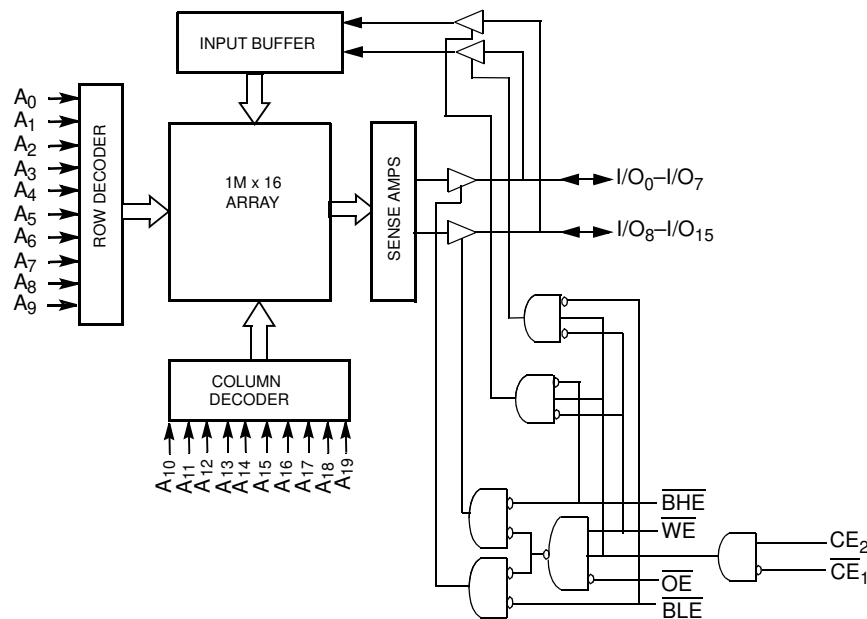
To write to the device, enable the chip ( $\overline{CE}_1$  LOW and  $CE_2$  HIGH) while forcing the Write Enable (WE) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable (BHE) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, enable the chip by taking  $\overline{CE}_1$  LOW and  $CE_2$  HIGH while forcing the Output Enable ( $\overline{OE}$ ) LOW and the Write Enable (WE) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on  $I/O_0$  to  $I/O_7$ . If Byte High Enable (BHE) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . See the [Truth Table on page 9](#) for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high impedance state when the device is deselected ( $\overline{CE}_1$  HIGH/ $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), the BHE and  $\overline{BLE}$  are disabled (BHE,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and WE LOW).

The CY7C1061DV18 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Contents

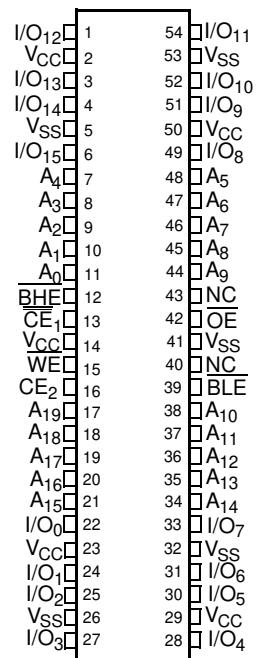
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### Selection Guide

Description	-15	Unit
Maximum access time	15	ns
Maximum operating current	150	mA
Maximum CMOS standby current	25	mA

### Pin Configurations

Figure 1. 54-Pin TSOP II (Top View)



### Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +15 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on V<sub>CC</sub> to relative GND<sup>[1]</sup>... -0.2 V to +2.45 V  
 DC voltage applied to outputs in High Z state<sup>[1]</sup> ..... -0.2 V to +2.45 V  
 DC input voltage<sup>[1]</sup> ..... -0.2 V to +2.45 V

Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage..... >2001 V (per MIL-STD-883, method 3015)  
 Latch-up current ..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40 °C to +85 °C	1.7 V to 2.2 V

### DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-15		Unit
			Min	Max	
V <sub>OH</sub>	Output HIGH voltage	Min V <sub>CC</sub> , I <sub>OH</sub> = -0.1 mA	1.4	-	V
V <sub>OL</sub>	Output LOW voltage	Min V <sub>CC</sub> , I <sub>OL</sub> = 0.1 mA	-	0.2	V
V <sub>IH</sub>	Input HIGH voltage		1.4	V <sub>CC</sub> + 0.2	V
V <sub>IL</sub>	Input LOW voltage <sup>[1]</sup>		-0.2	0.4	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , output disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	Max V <sub>CC</sub> , f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , I <sub>OUT</sub> = 0 mA CMOS levels	-	150	mA
I <sub>SB1</sub>	Automatic CE power-down current – TTL inputs	CE <sub>1</sub> ≥ V <sub>IH</sub> , CE <sub>2</sub> ≤ V <sub>IL</sub> , Max V <sub>CC</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	-	30	mA
I <sub>SB2</sub>	Automatic CE power-down current – CMOS inputs	CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2 V, CE <sub>2</sub> ≤ 0.2 V, Max V <sub>CC</sub> , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	25	mA

### Capacitance<sup>[2]</sup>

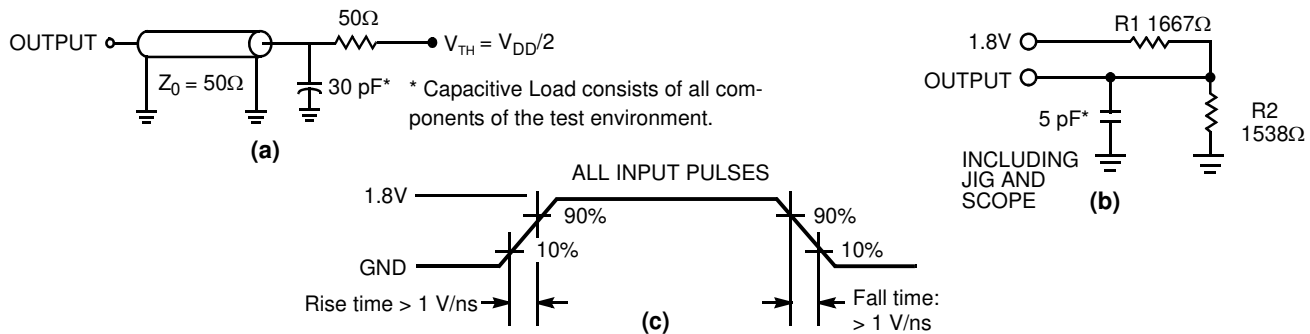
Parameter	Description	Test Conditions	TSOP II	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 1.8 V.	6	pF
C <sub>OUT</sub>	I/O capacitance		8	pF

### Thermal Resistance

Parameter <sup>[2]</sup>	Description	Test Conditions	TSOP II	Unit
θ <sub>JA</sub>	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	24.18	°C/W
θ <sub>JC</sub>	Thermal resistance (Junction to case)		5.40	°C/W

#### Notes

- V<sub>IL</sub> (min) = -2.0 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**Figure 2. AC Test Loads and Waveforms<sup>[3]</sup>**

**AC Switching Characteristics Over the Operating Range<sup>[4]</sup>**

Parameter	Description	-15		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{\text{power}}$	$V_{CC}(\text{typical})$ to the first access <sup>[5]</sup>	150	–	$\mu\text{s}$
$t_{\text{RC}}$	Read cycle time	15	–	ns
$t_{\text{AA}}$	Address to data valid	–	15	ns
$t_{\text{OHA}}$	Data hold from address change	3	–	ns
$t_{\text{ACE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to data valid	–	15	ns
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to data valid	–	7	ns
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to Low Z	1	–	ns
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to High Z <sup>[6]</sup>	–	7	ns
$t_{\text{LZCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Low-Z <sup>[6]</sup>	3	–	ns
$t_{\text{HZCE}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to High-Z <sup>[6]</sup>	–	7	ns
$t_{\text{PU}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to Power-up <sup>[7]</sup>	0	–	ns
$t_{\text{PD}}$	$\overline{\text{CE}}_1$ HIGH/ $\text{CE}_2$ LOW to Power-down <sup>[7]</sup>	–	15	ns
$t_{\text{DBE}}$	Byte Enable to data valid	–	7	ns
$t_{\text{LZBE}}$	Byte Enable to Low Z	1	–	ns
$t_{\text{HZBE}}$	Byte Disable to High Z	–	7	ns
<b>Write Cycle<sup>[8, 9]</sup></b>				
$t_{\text{WC}}$	Write cycle time	15	–	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}_1$ LOW/ $\text{CE}_2$ HIGH to write end	10	–	ns
$t_{\text{AW}}$	Address setup to write end	10	–	ns
$t_{\text{HA}}$	Address hold from write end	0	–	ns

**Notes**

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (1.5 V). 150  $\mu\text{s}$  ( $t_{\text{power}}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{\text{CCDR}}$ , 1.5 V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 0.9 V, input pulse levels of 0 to 1.8 V. Test conditions for the Read cycle use output loading shown in part a) of the Figure 2, unless specified otherwise.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{HZBE}}$ , and  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ ,  $t_{\text{LZWE}}$ ,  $t_{\text{LZBE}}$  are specified with a load capacitance of 5 pF as in (b) of Figure 2. Transition is measured  $\pm 200\text{ mV}$  from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  LOW ( $\text{CE}_2$  HIGH) and  $\overline{\text{WE}}$  LOW. Chip enables must be active and  $\overline{\text{WE}}$  and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

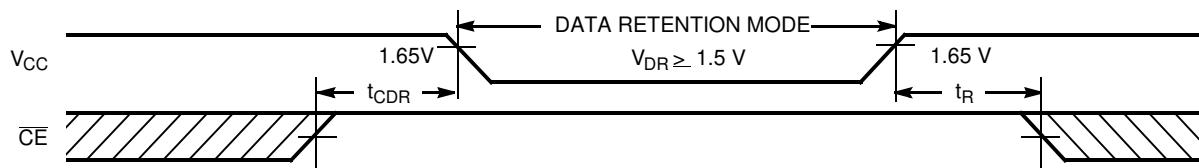
**AC Switching Characteristics** Over the Operating Range<sup>[4]</sup>(continued)

Parameter	Description	-15		Unit
		Min	Max	
t <sub>SA</sub>	Address setup to write start	0	–	ns
t <sub>PWE</sub>	$\overline{WE}$ pulse width	10	–	ns
t <sub>SD</sub>	Data setup to write end	7	–	ns
t <sub>HD</sub>	Data hold from write end	0	–	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[10]</sup>	3	–	ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[10]</sup>	–	7	ns
t <sub>BW</sub>	Byte enable to end of write	10	–	ns

**Data Retention Characteristics** (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ <sup>[11]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.5	–	–	V
I <sub>CCDR</sub>	Data retention current	V <sub>CC</sub> = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $\overline{CE}_2 \leq 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V, or V <sub>IN</sub> ≤ 0.2 V	–	–	25	mA
t <sub>CDR</sub> <sup>[12]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[13]</sup>	Operation recovery time		t <sub>RC</sub>	–	–	ns

Figure 3. Data Retention Waveform



**Notes**

- 10. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub>, t<sub>HZBE</sub>, and t<sub>LZOE</sub>, t<sub>LZCE</sub>, t<sub>LZWE</sub>, t<sub>LZBE</sub> are specified with a load capacitance of 5 pF as in (b) of Figure 2. Transition is measured ±200 mV from steady-state voltage
- 11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub> (typ), TA = 25 °C.
- 12. Tested initially and after any design or process changes that may affect these parameters
- 13. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs.

### Switching Waveforms

Figure 4. Read Cycle No. 1<sup>[14,15]</sup>

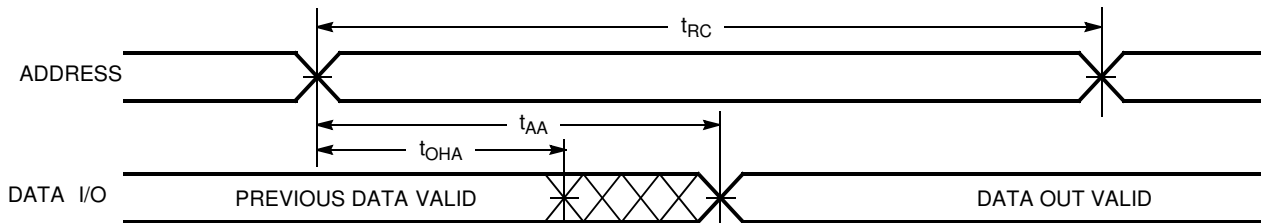
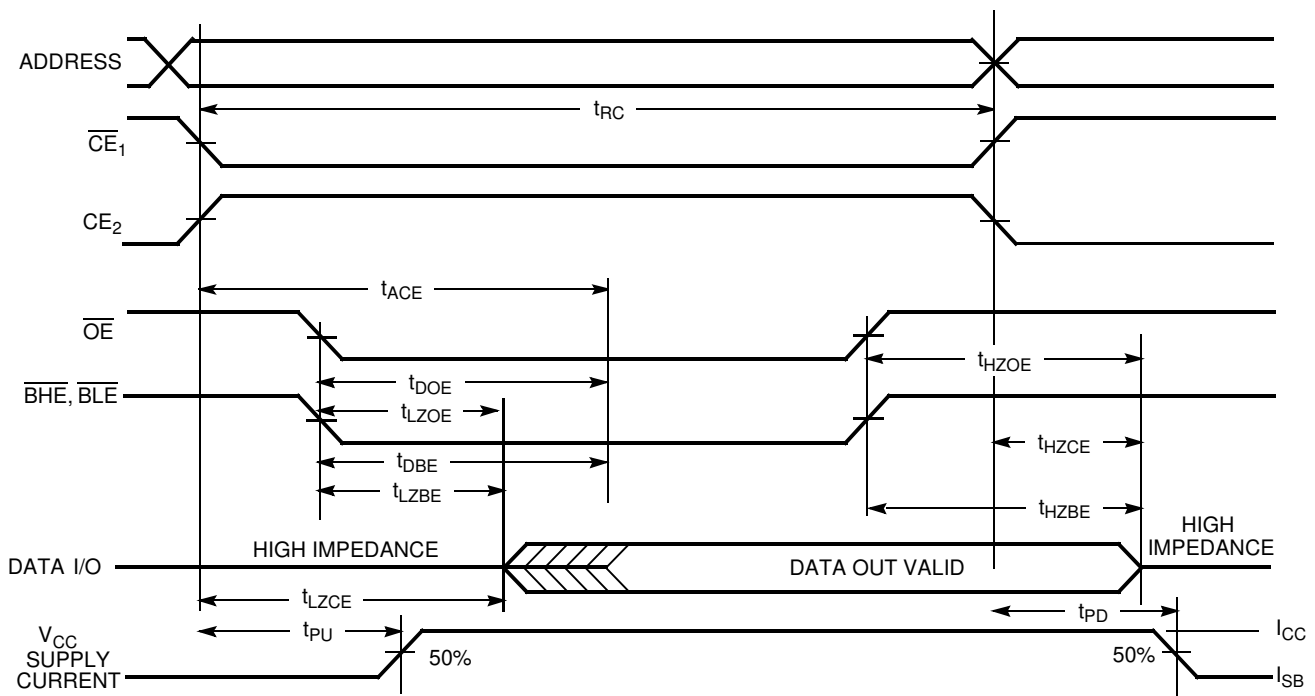


Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[16,17]</sup>



#### Notes

14. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DB}$  to  $V_{CC(min)}$   $\geq 100 \mu s$  or stable at  $V_{CC(min)}$   $\geq 100 \mu s$ .
15. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ , BHE and/or BHE =  $V_{IL}$ .  $CE_2 = V_{IH}$ .
16. WE is HIGH for Read cycle.
17. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

Figure 6. Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[18,19,20]</sup>

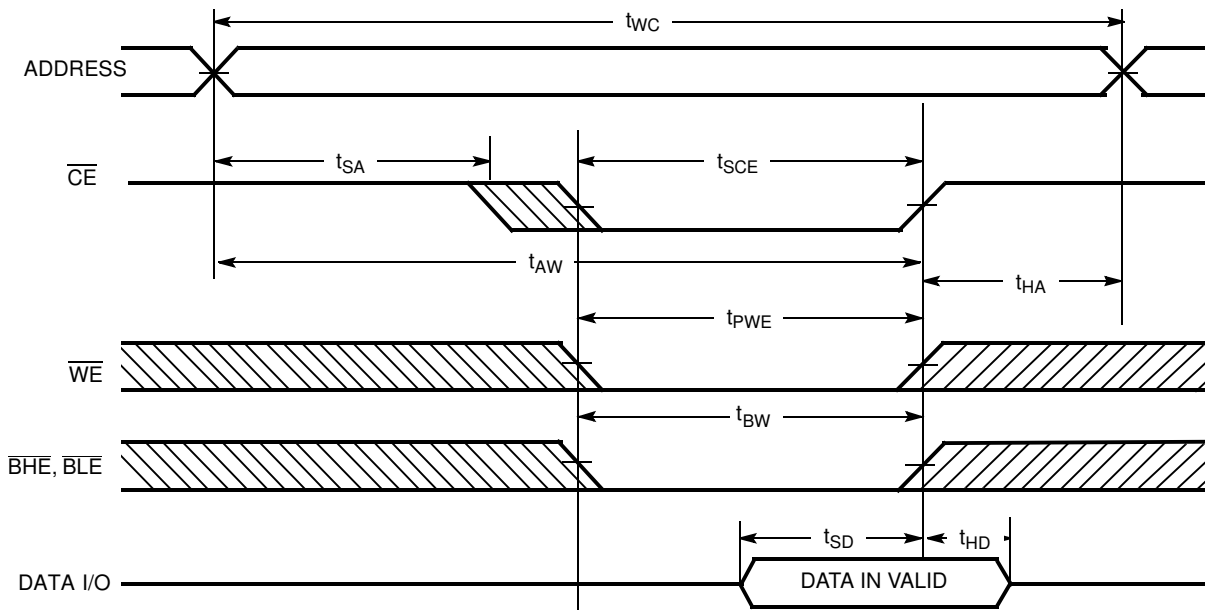
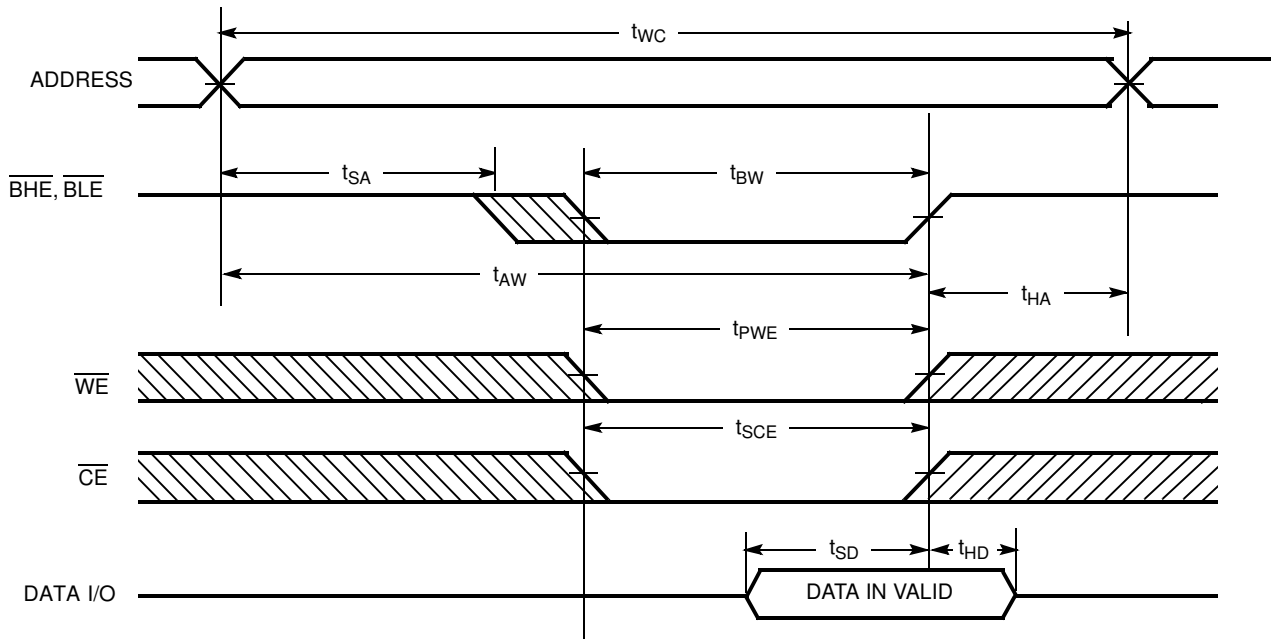


Figure 7. Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)

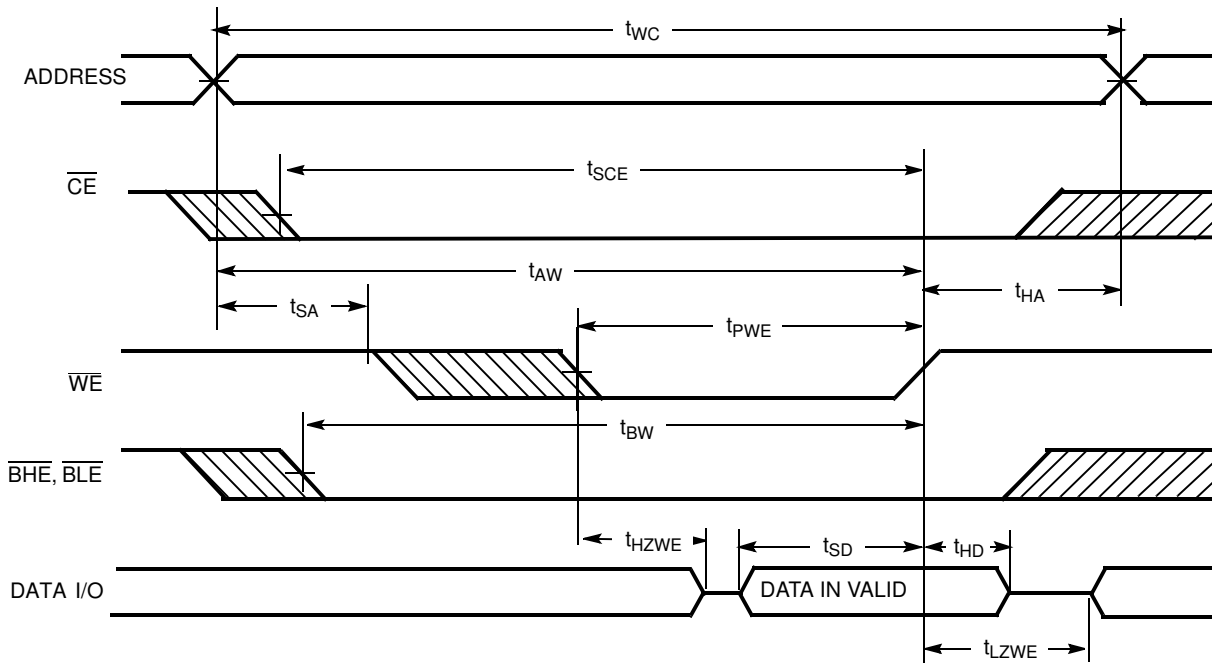


**Notes**

- 18. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 19. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high impedance state.
- 20.  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . When  $\overline{CE}_1$  is LOW and  $\overline{CE}_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW,  $\overline{CE}$  is HIGH



Figure 8. Write Cycle No. 3 (WE Controlled, OE Low)<sup>[21,22,23]</sup>



Truth Table

$\overline{CE}_1$	$CE_2$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power-down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	High Z	Power-down	Standby ( $I_{SB}$ )
L	H	L	H	L	L	Data out	Data out	Read all bits	Active ( $I_{CC}$ )
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active ( $I_{CC}$ )
L	H	L	H	H	L	High -Z	Data out	Read upper bits only	Active ( $I_{CC}$ )
L	H	X	L	L	L	Data in	Data in	Write all bits	Active ( $I_{CC}$ )
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active ( $I_{CC}$ )
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active ( $I_{CC}$ )
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active ( $I_{CC}$ )

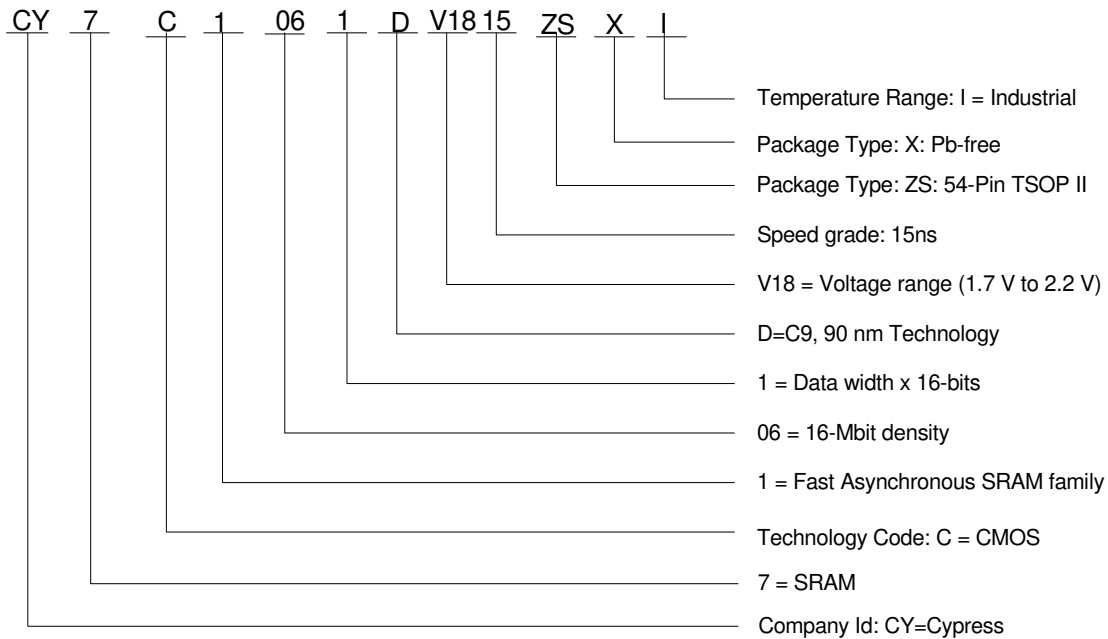
Notes

- 21. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 22. If  $\overline{CE}_1$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high impedance state.
- 23.  $\overline{CE}$  is a shorthand combination of both  $\overline{CE}_1$  and  $\overline{CE}_2$  combined. It is active LOW.

**Ordering Information**

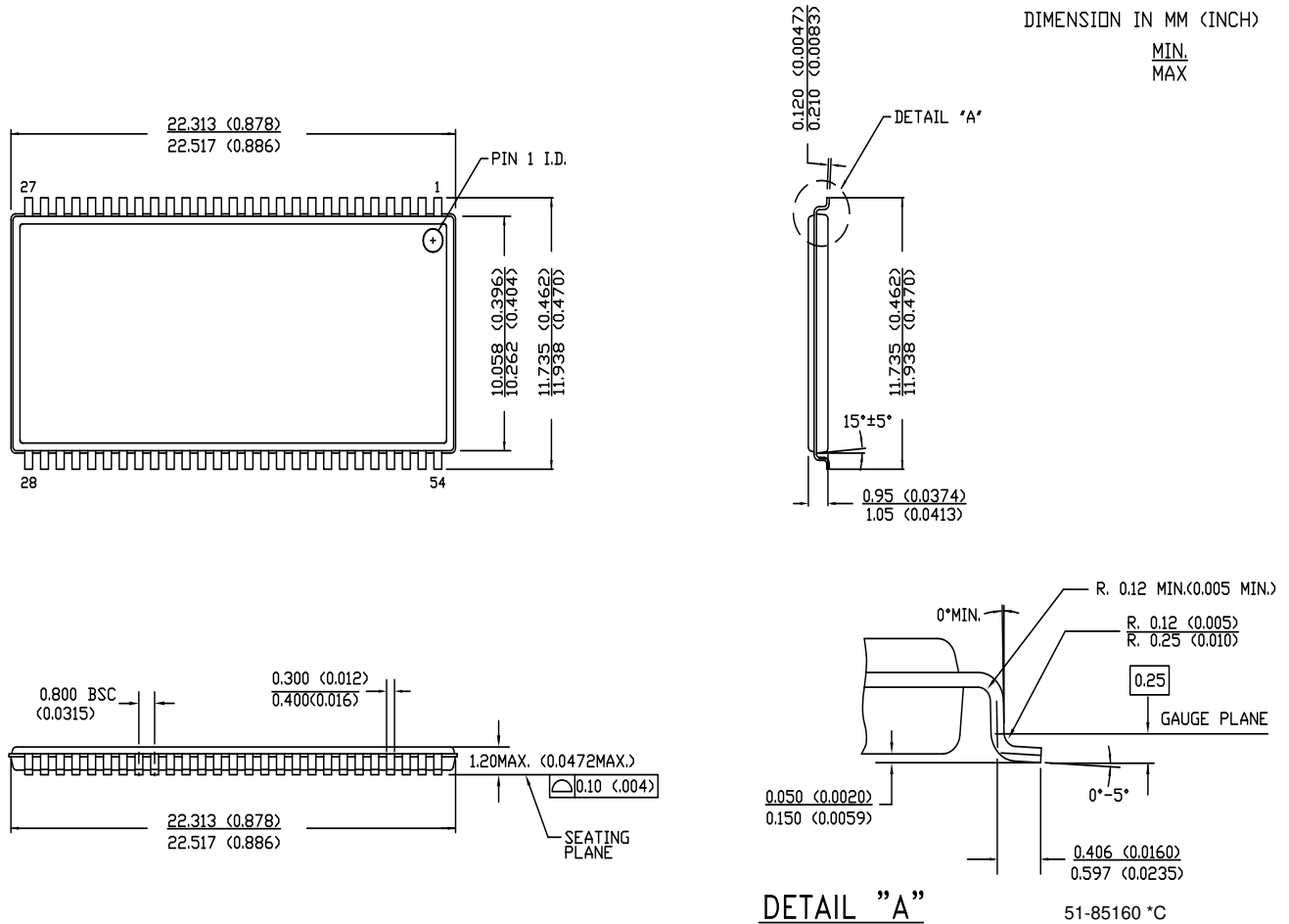
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1061DV18-15ZSXI	51-85160	54 pin TSOP II (Pb-free)	Industrial

**Ordering Code Definitions**



Package Diagram

Figure 9. 54-pin TSOP Type II



## Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
TSOP	thin small outline package
TTL	Transistor-transistor logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C1061DV18 16-Mbit (1 M × 16) Static RAM				
Document Number: 001-08350				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	469420	See ECN	NXR	New data sheet
*A	2761557	09/09/2009	VKN	Updated package code
*B	2800121	11/06/2009	VKN	Increased I <sub>CC</sub> limit from 100mA to 150mA Changed V <sub>DR</sub> from 1.2V to 1.5V Included Thermal specs Changed t <sub>LZOE</sub> and t <sub>LZBE</sub> from 0ns to 1ns Changed t <sub>LZCE</sub> from 0ns to 3ns Replaced 6 x 8 x 1mm FBGA package with 8 x 9.5 x 1mm FBGA package Changed status from Final to Preliminary
*C	2915361	04/16/2010	VKN	Converted from Preliminary to Final Removed 48-Ball FBGA package from the data sheet Updated links in Sales, Solutions, and Legal Information
*D	2923463	04/27/2010	RAME	Post to external web
*E	3109102	12/13/2010	PRAS	Added <a href="#">Ordering Code Definitions</a> .
*F	3147322	01/19/2011	PRAS	Updated all tables notes as per template Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> table.
*G	3387026	09/29/2011	TAVA	Minor technical edits. Updated <a href="#">Package Diagram</a> .

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