

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

To learn more about onsemi™, please visit our website at  
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ON Semiconductor®

QFET®

# FQP3N50C/FQPF3N50C 500V N-Channel MOSFET

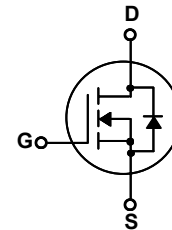
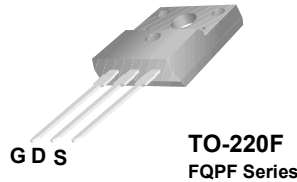
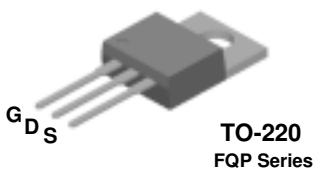
## Features

- 3 A, 500 V,  $R_{DS(on)} = 2.5 \Omega @ V_{GS} = 10 \text{ V}$
- Low gate charge ( typical 10 nC )
- Low  $C_{rss}$  ( typical 8.5 pF)
- Fast switching
- 100 % avalanche tested
- Improved dv/dt capability

## Description

These N-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.



## Absolute Maximum Ratings

Symbol	Parameter	FQP3N50C	FQPF3N50C	Units
$V_{DSS}$	Drain-Source Voltage	500		V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	3	3 *
		- Continuous ( $T_C = 100^\circ\text{C}$ )	1.8	1.8 *
$I_{DM}$	Drain Current - Pulsed (Note 1)	12	12 *	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	200		mJ
$I_{AR}$	Avalanche Current (Note 1)	3		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	6.2		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )		62	25
		- Derate above $25^\circ\text{C}$	0.5	0.2
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

\* Drain current limited by maximum junction temperature

## Thermal Characteristics

Symbol	Parameter	FQP3N50C	FQPF3N50C	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.0	4.9	$^\circ\text{C}/\text{W}$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ\text{C}/\text{W}$

FQP3N50C/FQPF3N50C 500V N-Channel MOSFET

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQP3N50C	FQP3N50C	TO-220	--	--	50
FQPF3N50C	FQPF3N50C	TO-220F	--	--	50

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

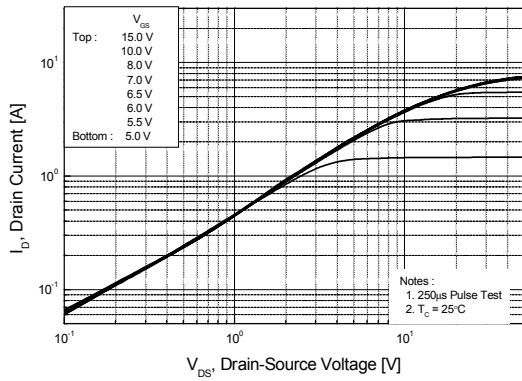
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	--	--	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.7	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	--	--	1	μA
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	--	--	10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	--	4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.5 A	--	2.1	2.5	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 1.5 A (Note 4)	--	1.5	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	280	365	pF
C <sub>oss</sub>	Output Capacitance		--	50	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	8.5	11	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 3 A, R <sub>G</sub> = 25 Ω (Note 4, 5)	--	10	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	35	80	ns
t <sub>f</sub>	Turn-Off Fall Time		--	25	60	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 400 V, I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V (Note 4, 5)	--	10	13	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.5	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	5.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	3	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	170	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.7	--	μC

### Notes:

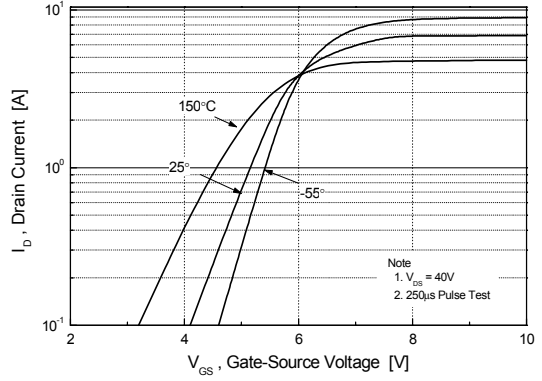
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 40mH, I<sub>AS</sub> = 3A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 3A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Performance Characteristics

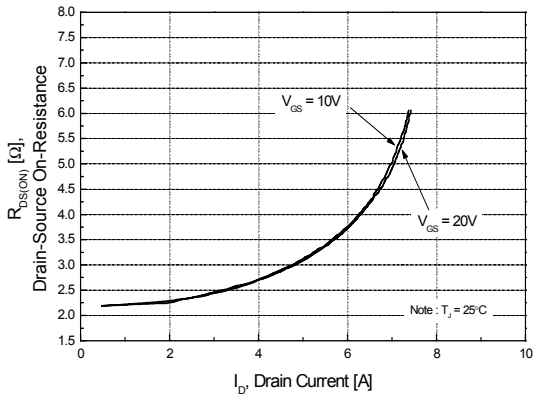
**Figure 1. On-Region Characteristics**



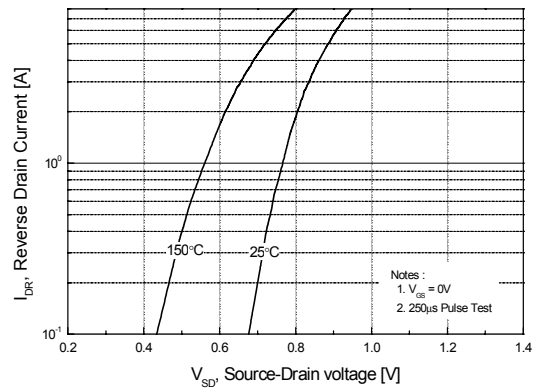
**Figure 2. Transfer Characteristics**



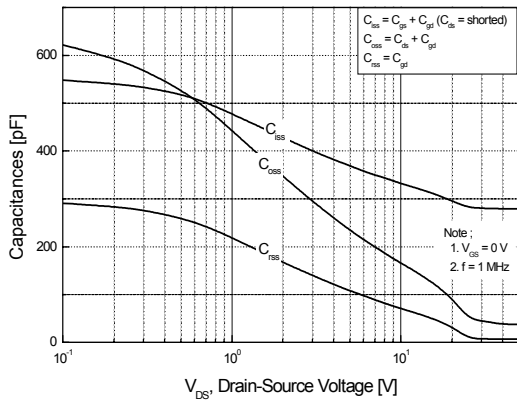
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



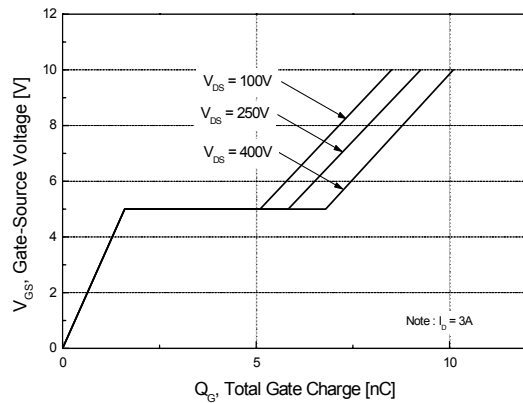
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

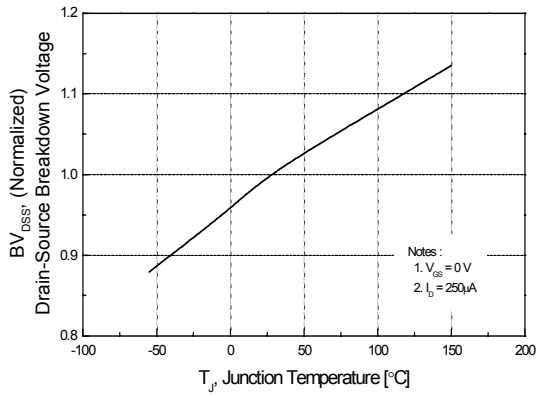


**Figure 6. Gate Charge Characteristics**

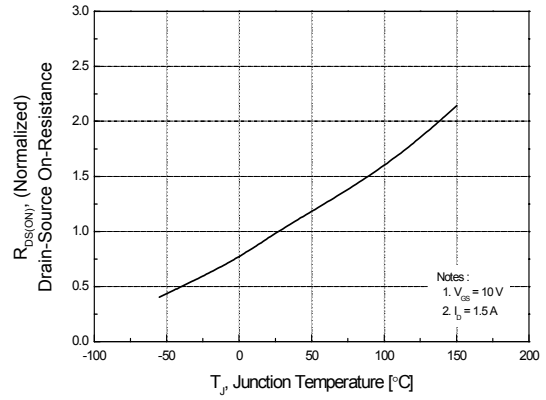


**Typical Performance Characteristics** (Continued)

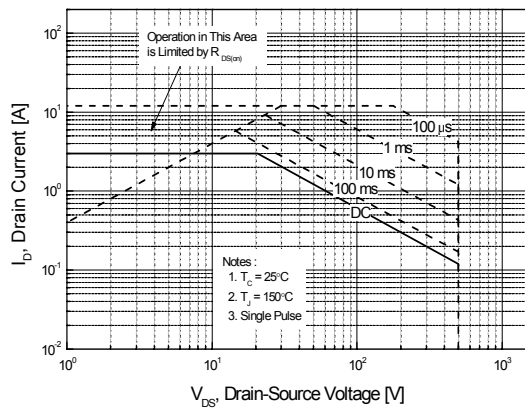
**Figure 7. Breakdown Voltage Variation vs. Temperature**



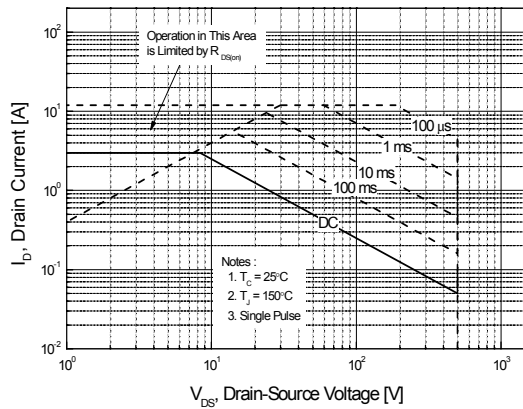
**Figure 8. On-Resistance Variation vs. Temperature**



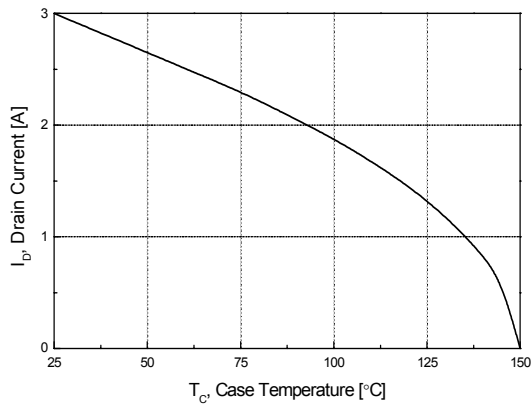
**Figure 9-1. Maximum Safe Operating Area of FQP3N50C**



**Figure 9-2. Maximum Safe Operating Area of FQPF3N50C**



**Figure 10. Maximum Drain Current**



Typical Performance Characteristics (Continued)

Figure 11-1. ransient Thermal Response Curve of FQP3N50C

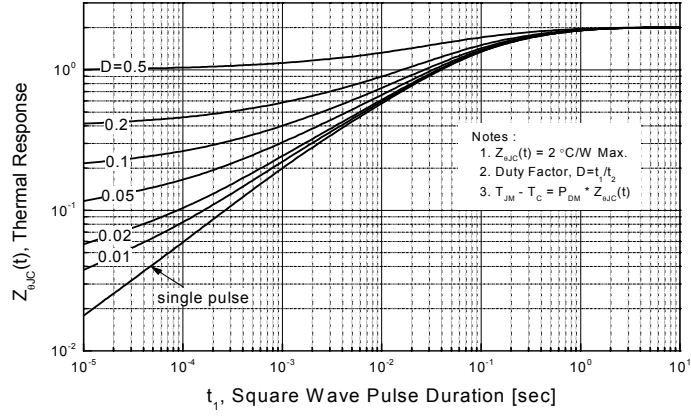
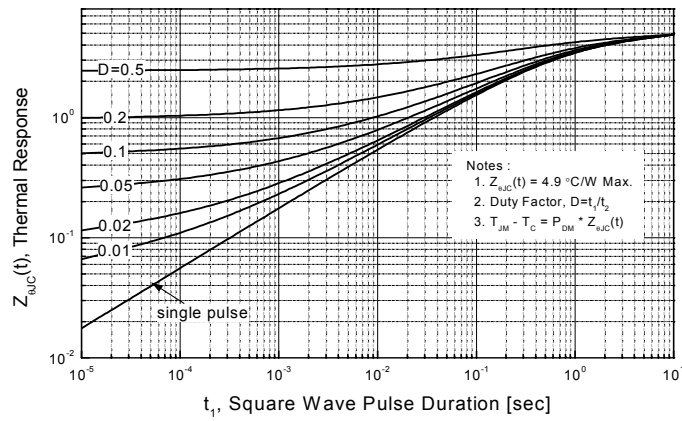
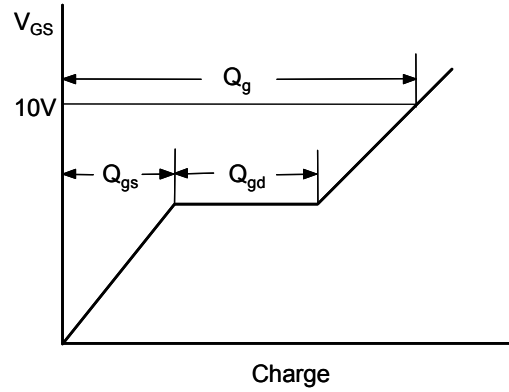
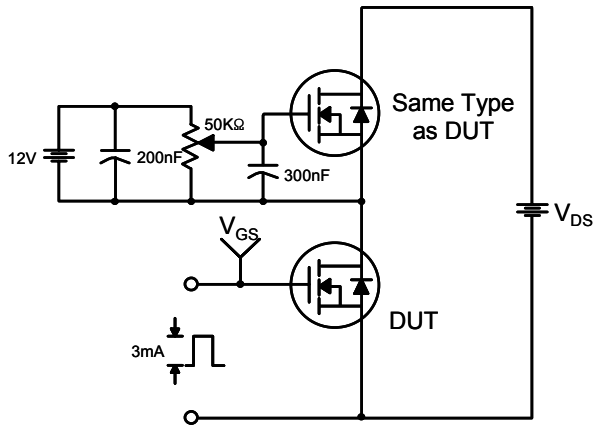


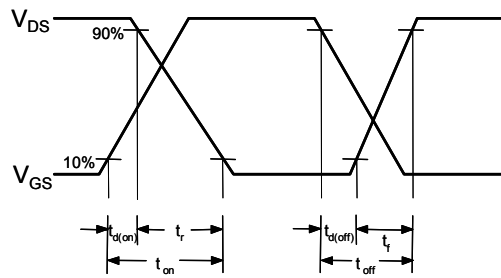
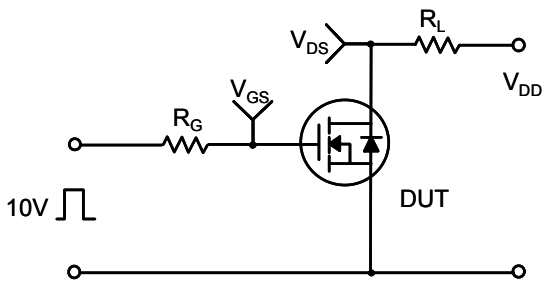
Figure 11-2. ransient Thermal Response Curve of FQPF3N50C



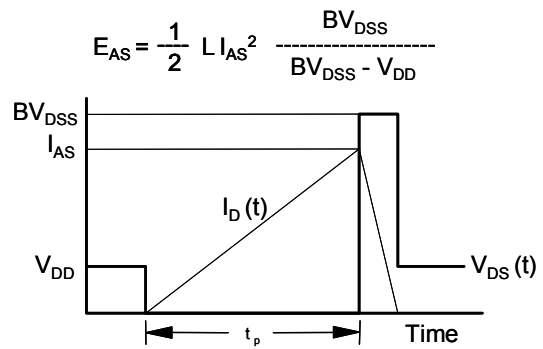
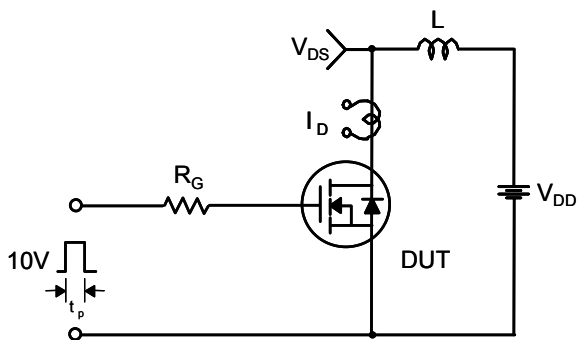
**Gate Charge Test Circuit & Waveform**



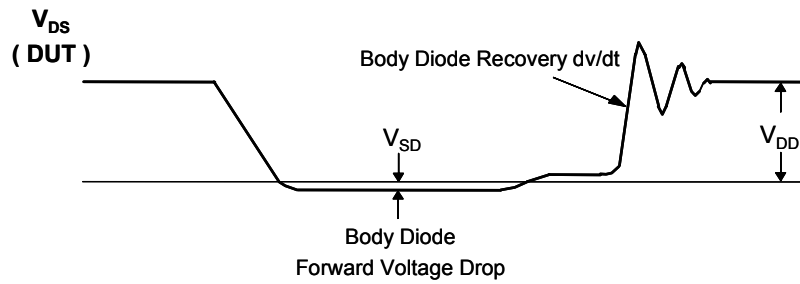
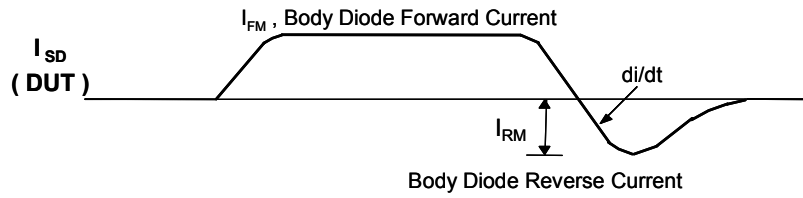
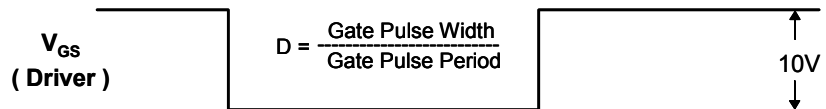
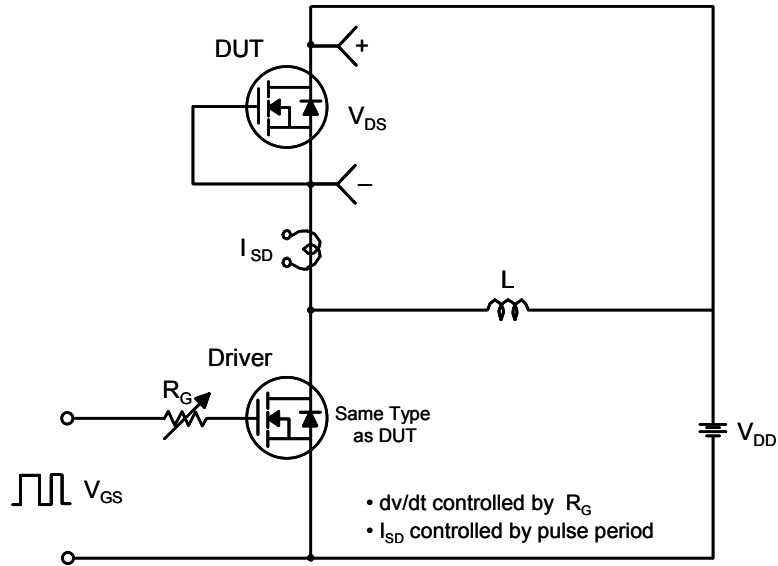
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



Peak Diode Recovery dv/dt Test Circuit & Waveforms

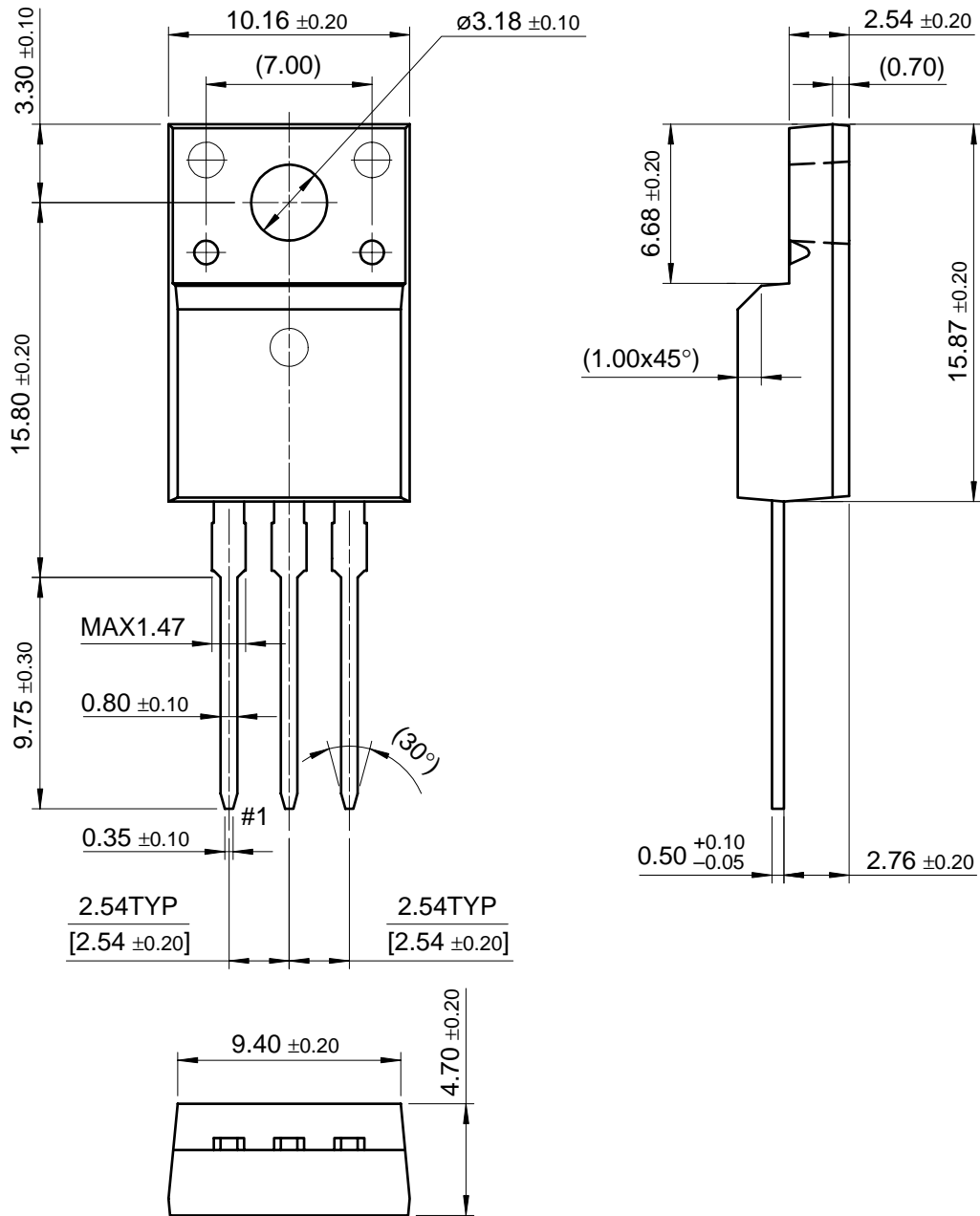







Mechanical Dimensions (Continued)

TO-220F



Dimensions in Millimeters

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