4539B
DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The 4539B is a Dual 4-Input Digital Multiplexer with common select logic. Each multiplexer has four Multiplexer Inputs (I_0-I_3), an active LOW Enable Input ($\overline{E}$) and a Multiplexer Output (Z). When HIGH, the Enable Input ($\overline{E}$) forces the Multiplexer Output (Z) of the respective multiplexer LOW, independent of the Select (S_0, S_1) and Multiplexer (I_0-I_3) Inputs. With the Enable Input ($\overline{E}$) LOW, the common Select Inputs (S_0, S_1) determine which Multiplexer Input (I_0-I_3) on each of the multiplexers is routed to the respective Multiplexer Output (Z).

- **COMMON SELECT LOGIC**
- **ACTIVE LOW ENABLES**

PIN NAMES

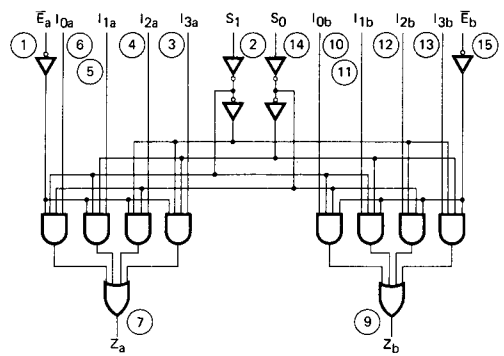
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs
I_{0b}, I_{1b}, I_{2b}, I_{3b}	
S_0, S_1	Select Inputs
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)
Z_a, Z_b	Multiplexer Outputs

TRUTH TABLE

INPUTS			OUTPUT
S_0	S_1	$\overline{E}$	Z
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

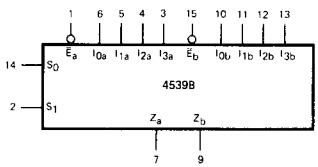
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



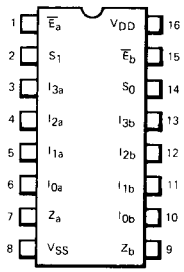
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_X to Z		166	375		71	160		51	125	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			140	350		58	140		40	110		
t_{PLH}	Propagation Delay, Select to Z		210	470		88	190		62	150	ns	
t_{PHL}			210	470		88	190		62	150		
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		120	275		53	110		37	85	ns	
t_{PHL}			118	275		51	110		38	85		
t_{TLH}	Output Transition Time		76	135		39	75		29	45	ns	
t_{THL}			66	135		30	75		22	45		

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.