

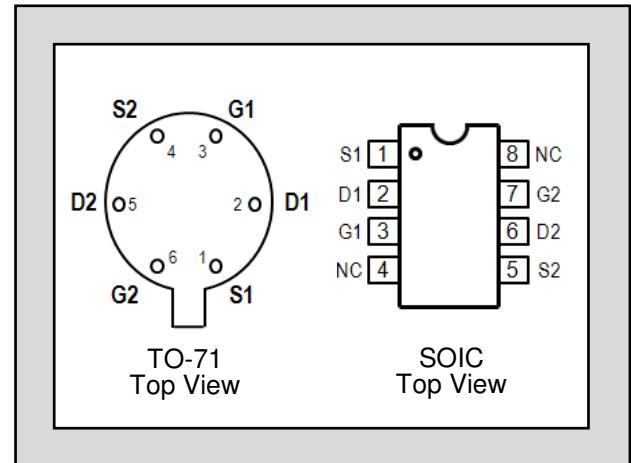
# LINEAR SYSTEMS

Improved Standard Products®

## SST/U401 – SST/U406

LOW NOISE LOW DRIFT  
MONOLITHIC DUAL N-CHANNEL  
JFET AMPLIFIER

FEATURES		
LOW DRIFT	$ V_{GS1-2}/T  = 10\mu V/^{\circ}C$ TYP.	
LOW NOISE	$e_n = 6nV/Hz@10Hz$ TYP.	
LOW PINCHOFF	$V_P = 2.5V$ MAX.	
ABSOLUTE MAXIMUM RATINGS NOTE 1		
@ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature	-55 to +150°C	
Operating Junction Temperature	-55 to +150°C	
Maximum Voltage and Current for Each Transistor NOTE 1		
-V <sub>GSS</sub>	Gate Voltage to Drain or Source	50V
-V <sub>DSO</sub>	Drain to Source Voltage	50V
-I <sub>G(f)</sub>	Gate Forward Current	10mA
Maximum Power Dissipation per side NOTE 2		
Device Dissipation	T <sub>A</sub> = 25°C	300mW



### MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

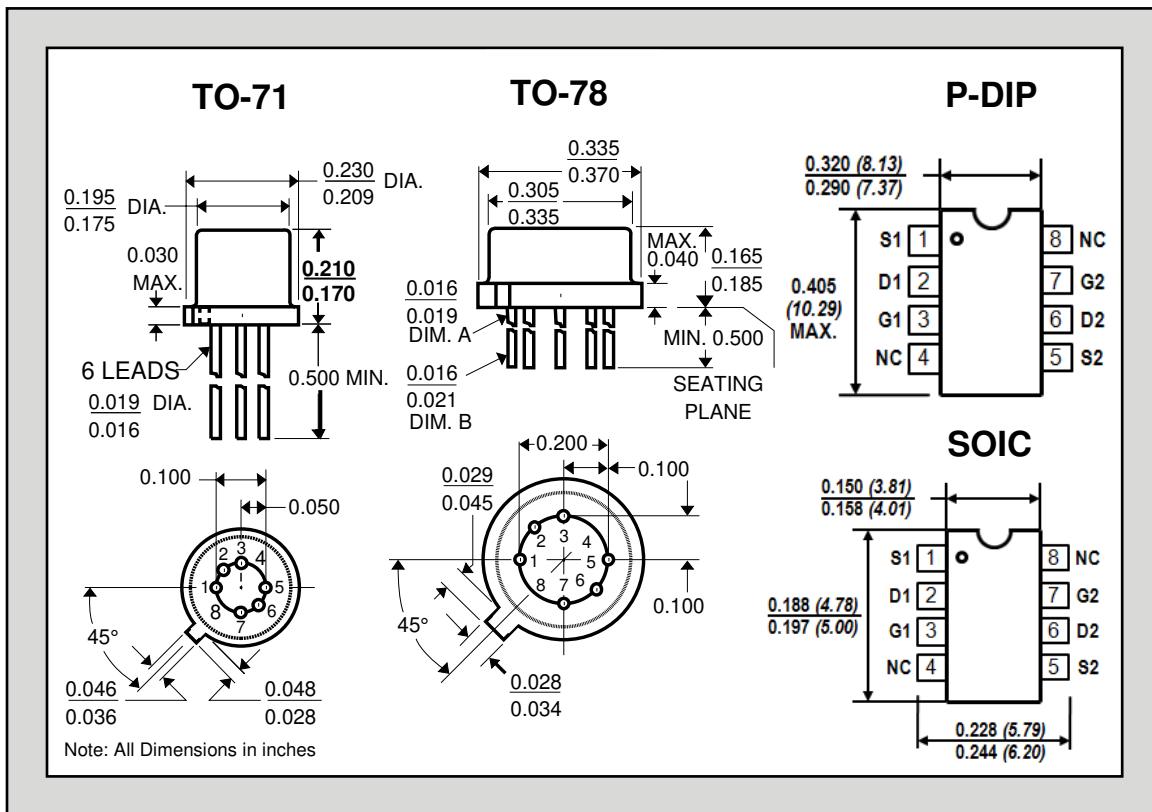
SYMBOL	CHARACTERISTIC	U401	U402	U403	U404	U405	U406	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	Drift vs. Temperature	10	10	25	25	40	80	$\mu V/^{\circ}C$	$V_{DG} = 10V, I_D = 200\mu A$ $T_A = -55^{\circ}C$ to $+125^{\circ}C$
$ V_{GS1-2} $ max.	Offset Voltage	5	10	10	15	20	40	mV	$V_{DG} = 10V, I_D = 200\mu A$

### ELECTRICAL CHARACTERISTICS T<sub>A</sub> = 25°C (unless otherwise noted) NOTE 3

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV <sub>GSS</sub>	Breakdown Voltage	-50	-60	--	V	$V_{DS} = 0, I_D = 1nA$
BV <sub>G1G2</sub>	Gate-to-Gate Breakdown	$\pm 50$	--	--	V	$I_G = \pm 1\mu A, I_D = 0, I_S = 0$
G <sub>fss</sub>	<b>TRANSCONDUCTANCE</b>					
	Full Conduction	2000	--	7000	$\mu S$	$V_{DG} = 10V, V_{GS} = 0, f = 1kHz$
G <sub>fs</sub>	Typical Operation	1000	--	2000	$\mu S$	$V_{DG} = 15V, I_D = 200\mu A, f = 1kHz$
$ G_{fs1}/G_{fs2} $	Mismatch	0.97	--	1.0		
I <sub>DSS</sub>	Saturation Drain Current	0.5	--	10	mA	$V_{DG} = 10V, V_{GS} = 0$
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Current Ratio	0.9	0.98	1.0		
V <sub>GS(off)</sub> or V <sub>P</sub>	<b>GATE VOLTAGE</b>					
	Pinchoff Voltage	-0.5	--	-2.5	V	$V_{DS} = 15V, I_D = 1nA$
V <sub>GS</sub>	Operating Range	--	--	-2.3	V	$V_{DS} = 15V, I_D = 200\mu A$
I <sub>G</sub>	<b>GATE CURRENT</b>					
	Operating	--	-4	-15	pA	$V_{DG} = 15V, I_D = 200\mu A$
I <sub>G</sub>	High Temperature	--	--	-10	nA	$T_A = +125^{\circ}C$
I <sub>GSS</sub>	Gate Reverse Current	--	--	-100	pA	$V_{GS} = -30V, V_{DS} = 0V$
I <sub>G1G2</sub>	Gate to Gate Isolation Current	--	--	$\pm 1.0$	$\mu A$	$V_{G1} - V_{G2} = \pm 50V, I_D = I_S = 0$

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SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
<b>OUTPUT CONDUCTANCE</b>						
G <sub>oss</sub>	Full Conduction	--	--	40	μS	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1kHz
G <sub>os</sub>	Operating	--	2	2.7	μS	V <sub>DS</sub> = 15V, I <sub>D</sub> = 200μA, f = 1kHz
<b>COMMON MODE REJECTION</b>						
CMRR	$-20 \log [(V_{GS1}-V_{GS2})/\Delta V_{DG1-2}]$	95	--	--	dB	V <sub>DG1</sub> = 10V V <sub>DG2</sub> = 20V I <sub>D1</sub> = I <sub>D2</sub> =200μA
<b>NOISE</b>						
NF	Figure	--	--	0.5	dB	V <sub>DS</sub> = 15V V <sub>GS</sub> = 0 R <sub>G</sub> =10M f= 100Hz NBW= 6Hz
e <sub>n</sub>	Voltage	--	6	20	nV/Hz	V <sub>DS</sub> = 15V I <sub>D</sub> = 200μA f= 10Hz NBW= 1Hz
<b>CAPACITANCE</b>						
C <sub>ISS</sub>	Input	--	4	8	pF	V <sub>DS</sub> = 15V I <sub>D</sub> = 200μA f= 1MHz
C <sub>RSS</sub>	Reverse Transfer	--	1.5	3	pF	



### NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 2.4mW/°C when TA is greater than 25°C
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

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