



# AP4410AEC

## Ultra Low Power Dual Voltage Detector

### 1. General Description

The AP4410AEC is a voltage detector IC for monitoring battery, power supply and system voltage. The circuit includes dual voltage detection with built-in gate logic and MOSFETs. The AP4410AEC offers ultra-low power consumption that is 0.026 $\mu$ A per channel.

The built-in CMOS logic circuit can be controlled independently from the voltage detector. The polarity of the voltage detection results is controlled by pins. This function enables the AP4410AEC as a load switch by using the results of the voltage detection. The AP4410AEC achieves better performance and PCB area than conventional CMOS voltage detector ICs, with discrete logics and external MOSFETs.

The AP4410AEC is ideal for voltage conversion or load switch of thin and small wearable devices, over charge/discharge protection of Lithium-ion batteries, power management part of energy harvesting applications.

### 2. Features

- Power management function
  - Dual voltage detection circuits
  - Control logic with independent power supply
  - Built in P-channel MOSFETs and N-Channel MOSFETs for each channel
- Wide range for detection voltage
 

|                          |                        |
|--------------------------|------------------------|
| Detection voltage "High" | 1.8 to 2.7V (Options)  |
| Detection voltage "Low"  | 1.7 to 2.65V (Options) |
- Voltage detection accuracy  $\pm 35$ mV
- Ultra-low power consumption 0.026 $\mu$ A typical/ch. 0.050 $\mu$ A maximum/ ch
- Response Speed 500 $\mu$ s maximum
- On resistance
 

|                           |                    |
|---------------------------|--------------------|
| On-chip P-channel MOSFETs | 1 $\Omega$ typical |
| On-chip N-channel MOSFETs | 2 $\Omega$ typical |
- Operation temperature -40 - +85 °C
- Package 20-pin WLCSP (1.955 $\times$ 1.555mm, 0.4mm pitch)

|                             |
|-----------------------------|
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4. Block Diagram

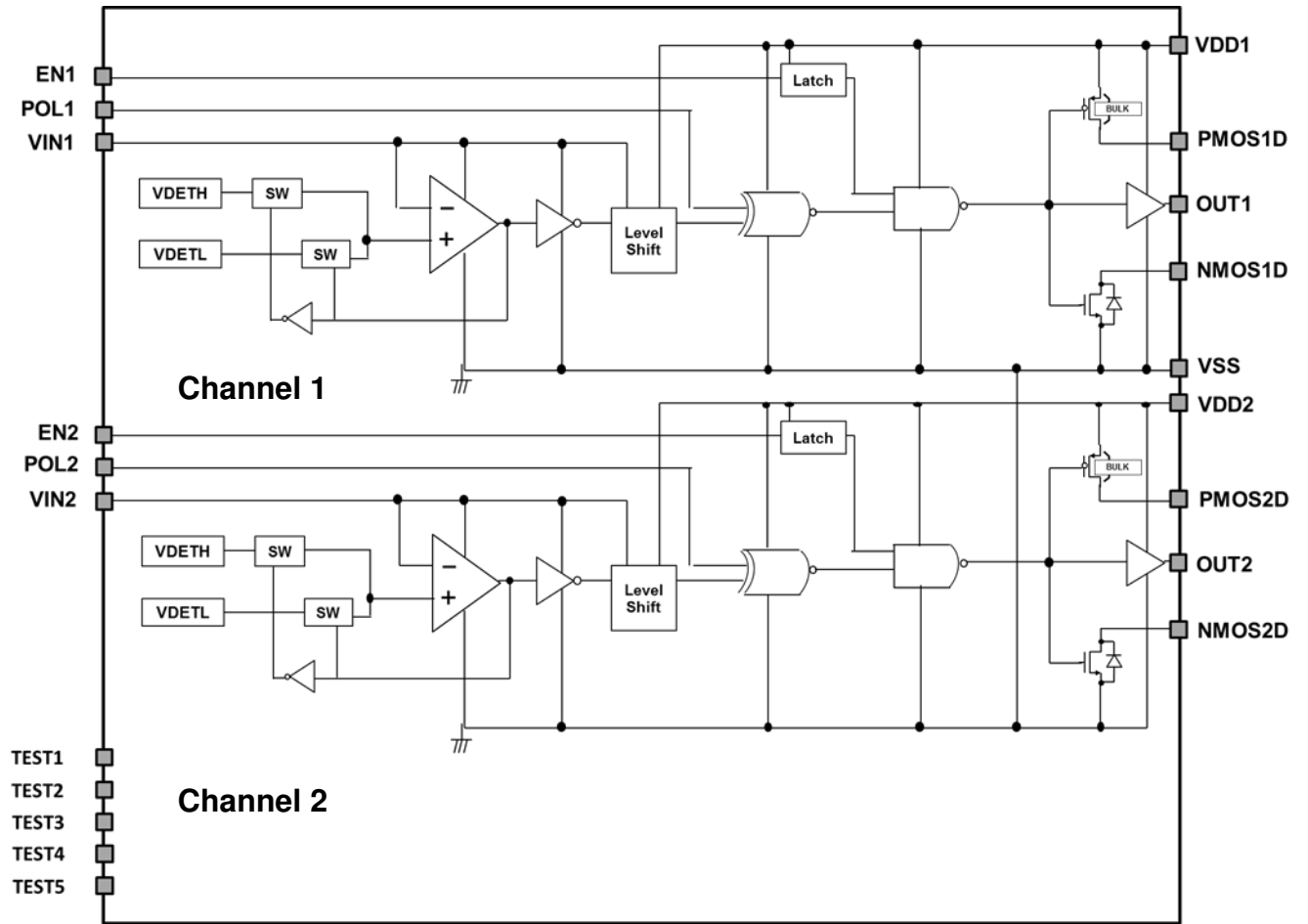
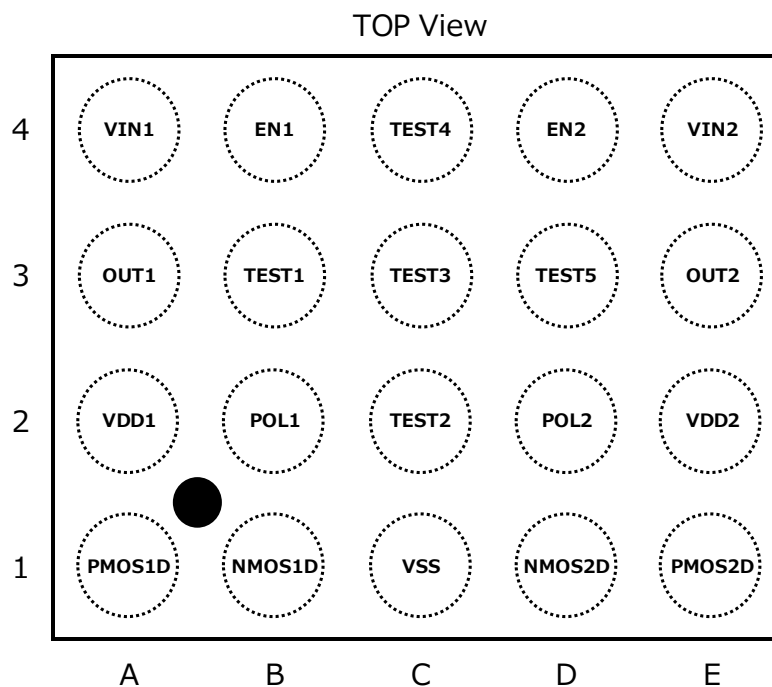


Figure 1. Block Diagram

**5. Pin Configuration and Function**

■ **Pin Configuration**

• 20-pin WLCSP



■ **Function**

| WLCSP Pin | Pin Name | I/O            | Function  |
|-----------|----------|----------------|---|
| A1        | PMOS1D   | Input/Output   | PMOS drain pin (Channel 1)                              |
| A2        | VDD1     | Power          | Power supply(Channel 1)                                 |
| A3        | OUT1     | Output         | Logic output (Channel 1)                                |
| A4        | VIN1     | Power          | Detection input pin (Channel 1)                         |
| B1        | NMOS1D   | Output         | NMOS1 drain pin(Channel 1)                              |
| B2        | POL1     | Input          | Polarity cotrol pin (Channel 1)                         |
| B3        | TEST1    | -              | For test purposes. This pin should be connected to VSS. |
| B4        | EN1      | Input          | Enable pin (Channel 1)                                  |
| C1        | VSS      | Ground         | Ground  |
| C2        | TEST2    | -              | For test purposes. This pin should be connected to VSS. |
| C3        | TEST3    | -              | For test purposes. This pin should be connected to VSS. |
| C4        | TEST4    | -              | For test purposes. This pin should be connected to VSS. |
| D1        | NMOS2D   | Output         | NMOS drain pin(Channel 2)                               |
| D2        | POL2     | Input          | Polarity cotrol pin (Channel 2)                         |
| D3        | TEST5    | -              | For test purposes. This pin should be connected to VSS. |
| D4        | EN2      | Input          | Enable pin (Channel 2)                                  |
| E1        | PMOS2D   | Input / Output | PMOS drain pin (Channel 2)                              |
| E2        | VDD2     | Power          | Power supply(Channel 2)                                 |
| E3        | OUT2     | Output         | Logic output (Channel 2)                                |
| E4        | VIN2     | Power          | Detection input pin (Channel 2)                         |

## 6. Absolute Maximum Ratings

| Parameter               | Symbol                  | min     | max        | Unit |
|-------------------------|-------------------------|---------|------------|------|
| Pin Voltage<br>(Note 1) | VIN1,VIN2,<br>VDD1,VDD2 | -0.3    | 6.5        | V    |
|                         | OUT1,EN1,POL1           | VSS-0.3 | VDD1 + 0.3 | V    |
|                         | OUT2,EN2,POL2           | VSS-0.3 | VDD2 + 0.3 | V    |
|                         | PMOS1D<br>PMOS2D        | -0.3    | 6.5        | V    |
|                         | NMOS1D<br>NMOS2D        | -0.3    | 6.5        | V    |
| Power dissipation       | Pd                      | -       | 0.8        | W    |
| Storage Temperature     | Tstg                    | -55     | 150        | °C   |

Note 1. All voltages are with reference to VSS = 0 V.

WARNING: Stresses exceeding Maximum Ratings may damage the device. Normal operation is not guarantee if the condition exceeds the maximum rating.

## 7. Recommended Operating Conditions

| Parameter             | Symbol                       | min | max | Unit |
|-----------------------|------------------------------|-----|-----|------|
| Operation Temperature | Ta                           | -40 | 85  | °C   |
| Power Supply Voltage  | VIN1<br>VIN2<br>VDD1<br>VDD2 | 1.3 | 5.5 | V    |

## 8. Electrical Characteristics

(Ta= -40 – +85°C, VIN1, VIN2, VDD1 and VDD2 =1.3V to 5.5V, OUT=open, PMOSD=open, NMOSD=open, unless otherwise specified.)

| Parameter                              | Symbol                       | min                         | typ               | max                         | Unit | Condition   |
|--|------------------------------|-----------------------------|-------------------|-----------------------------|------|---|
| Detection Voltage "High"               | V <sub>DETH</sub>            | V <sub>DETH</sub><br>-0.035 | V <sub>DETH</sub> | V <sub>DETH</sub><br>+0.035 | V    | Ta=25°C<br>VIN= "L" → "H"<br>Please refer 10. Reference data (Detection Voltage vs Ta)  |
|  |                              | V <sub>DETH</sub><br>-0.045 |                   | V <sub>DETH</sub><br>+0.045 | V    | Ta=85°C<br>VIN= "L" → "H"<br>Please refer 10. Reference data (Detection Voltage vs Ta)  |
| Detection Voltage "Low"                | V <sub>DETL</sub>            | V <sub>DETL</sub><br>-0.035 | V <sub>DETL</sub> | V <sub>DETL</sub><br>+0.035 | V    | Ta=25°C<br>VIN= "H" → "L"<br>Please refer 10. Reference data (Detection Voltage vs Ta)  |
|  |                              | V <sub>DETL</sub><br>-0.045 |                   | V <sub>DETL</sub><br>+0.045 | V    | Ta=85°C<br>VIN= "H" → "L"<br>Please refer 10. Reference data (Detection Voltage vs Ta)  |
| Power Consumption                      | IVIN                         | -                           | 0.026             | 0.050                       | μA   | Consumption for VIN per channel while the voltage detection circuit is active. Please refer 10. Reference data (Current consumption vs VIN & VDD) |
|  | IVDD<br>(Note 2)<br>(Note 3) | -                           | 0.0001            | 0.100                       | μA   | Consumption for VDD1 and VDD2. Please refer 10. Reference data (Current consumption vs VIN & VDD)   |
| "High" Level Input Voltage             | V <sub>IH</sub>              | VDD<br>×0.8                 | -                 | -                           | V    |   |
| "Low" Level Input Voltage              | V <sub>IL</sub>              | -                           | -                 | VDD<br>×0.2                 | V    |   |
| EN pin reverse current<br>(Push, Pull) | I <sub>EN</sub>              | 0.15                        | -                 | -                           | μA   |   |
| IOH (Note 4)                           | I <sub>OH</sub>              | 0.15                        | -                 | -                           | mA   | VIN=V <sub>DETH</sub> +0.1V,<br>OUT=VDD-0.5V  |
| IOL(Note 4)                            | I <sub>OL</sub>              | 0.2                         | -                 | -                           | mA   | VIN=V <sub>DETL</sub> -0.1V,<br>OUT=0.5V  |
| Response Time<br>(Note 5)              | t <sub>PLH</sub>             | -                           | 0.2               | 0.5                         | ms   | VIN=V <sub>DETH</sub> -0.1V→V <sub>DETH</sub> +0.1V   |
|  | t <sub>PHL</sub>             | -                           | 0.2               | 0.5                         | ms   | VIN= V <sub>DETL</sub> +0.1V→V <sub>DETL</sub> -0.1V<br>Please refer 10. Reference data (Response time)   |
| P-ch MOSFET<br>On-resistance           | R <sub>onP</sub>             | -                           | 1                 | 2.3                         | Ω    | VDD ≥ 1.7V  |
| N-ch MOSFET<br>On-resistance           | R <sub>onN</sub>             | -                           | 2                 | 5                           | Ω    | VDD ≥ 1.7V  |

Note 2. Output drive is not included.

Note 3. Total power consumption VDD1 and VDD2 (VDD1+VDD2).

Note 4. Output current depends on VDD1 and VDD2.

IOL shows N-Channel pull current when AP4410AEC OUT1/OUT2 output low.

IOH shows P-Channel push current when AP4410AEC OUT1/OUT2 output high.

Note 5. Response time for OUT1 pin and OUT2 pin

## 9. Description

### ■ Voltage Detection Function

VIN1 pin and VIN2 pin = (Abbreviation ;VIN)  
 VDD1 pin and VDD2 pin = (Abbreviation ;VDD)  
 POL1 pin and POL2 pin = (Abbreviation ;POL)  
 EN1 pin and EN2 pin = (Abbreviation ;EN)

- 1) When the input voltage is increasing,  
 The OUT1 pin and OUT2 pin(Abbreviation ;OUT) will be in undefined status when VIN voltage is from VSS to AP4410AEC minimum operating voltage(1.3V). The AP4410AEC internal signal A(Please refer Figure 2) outputs VSS when VIN voltage exceeds minimum operating voltage. When VIN voltage reaches to the detection voltage (VDETH), the internal signal A outputs VIN voltage.
- 2) When the input voltage is decreasing,  
 When VIN voltage is higher than VDETH, internal signal A outputs VIN. When VIN goes under the detection voltage (VDETL), OUT outputs VSS. The internal signal A will be undefined status when VIN voltage becomes lower than AP4410AEC minimum operating voltage(1.3V).

The logic inputs POL and EN become valid when VDD voltage exceeds 1.3V which is the minimum operation voltage. In case of POL = "L", EN="H", OUT behaves as Figure. 3. The AP4410AEC is able to output the inverted results of the voltage detection using POL. EN can control P-channel MOSFET and N-channel MOSFET ON and OFF. EN has latch function so that it keeps its present state if the input becomes Hi-Z. The BULK of the P-channel MOSFET is connected to the higher voltage pin between VDD and PMOSD.

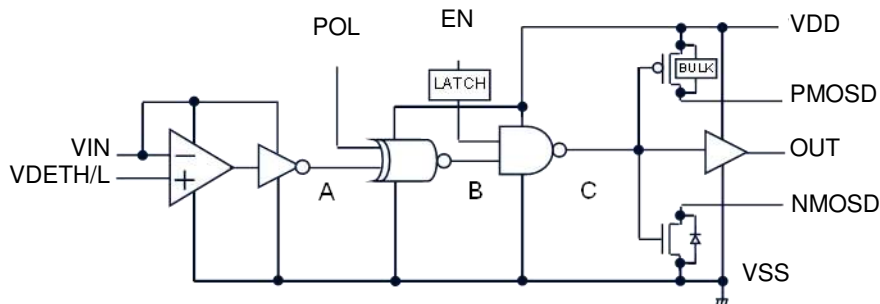


Figure 2. Block Diagram of Control Logic Part (Each channel)

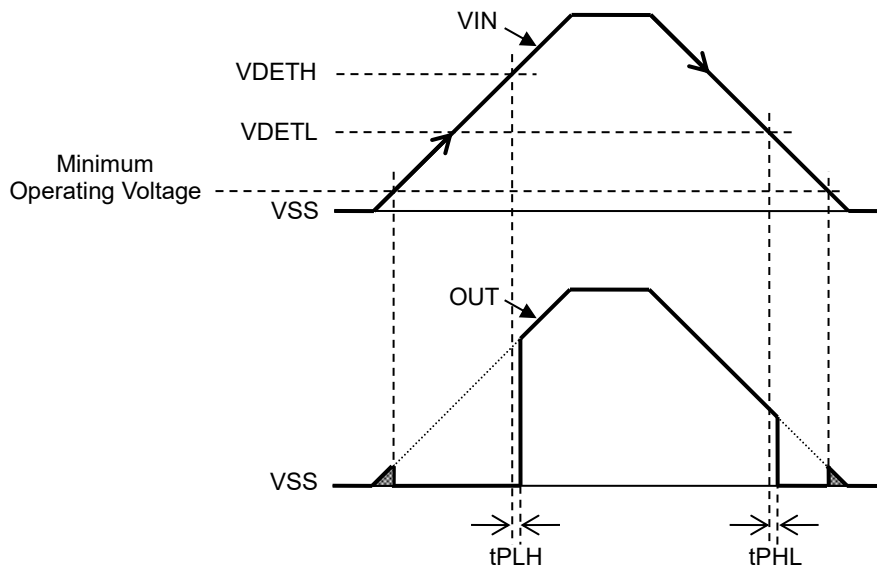


Figure 3. Function of AP4410AEC voltage detection

Table 1. Control logic truth table (Note 6)

| POL input | VIN                    | EN input | Internal signal A | Internal signal B | Internal signal C | PMOSD | NMOSD | OUT | Note                   |
|-----------|------------------------|----------|-------------------|-------------------|-------------------|-------|-------|-----|------------------------|
| L         | $V_{IN} < V_{DETH}$    | L        | L                 | H                 | H                 | OPEN  | L     | H   | -                      |
| L         | $V_{IN} < V_{DETH}$    | H        | L                 | H                 | L                 | H     | OPEN  | L   | OUT= positive polarity |
| L         | $V_{IN} \geq V_{DETH}$ | H        | H                 | L                 | H                 | OPEN  | L     | H   |                        |
| L         | $V_{IN} \geq V_{DETH}$ | L        | H                 | L                 | H                 | OPEN  | L     | H   | -                      |
| H         | $V_{IN} < V_{DETH}$    | L        | L                 | L                 | H                 | OPEN  | L     | H   | -                      |
| H         | $V_{IN} < V_{DETH}$    | H        | L                 | L                 | H                 | OPEN  | L     | H   | OUT= negative polarity |
| H         | $V_{IN} \geq V_{DETH}$ | H        | H                 | H                 | L                 | H     | OPEN  | L   |                        |
| H         | $V_{IN} \geq V_{DETH}$ | L        | H                 | H                 | H                 | OPEN  | L     | H   | -                      |

Note 6. When the VIN voltage is increasing from VDETL or lower.

Table 2 Control logic truth table (Note 7)

| POL input | VIN                    | EN input | Internal signal A | Internal signal B | Internal signal C | PMOSD | NMOSD | OUT | Note                   |
|-----------|------------------------|----------|-------------------|-------------------|-------------------|-------|-------|-----|------------------------|
| L         | $V_{IN} > V_{DETL}$    | L        | H                 | L                 | H                 | OPEN  | L     | H   | -                      |
| L         | $V_{IN} > V_{DETL}$    | H        | H                 | L                 | H                 | OPEN  | L     | H   | OUT= positive polarity |
| L         | $V_{IN} \leq V_{DETL}$ | H        | L                 | H                 | L                 | H     | OPEN  | L   |                        |
| L         | $V_{IN} \leq V_{DETL}$ | L        | L                 | H                 | H                 | OPEN  | L     | H   | -                      |
| H         | $V_{IN} > V_{DETL}$    | L        | H                 | H                 | H                 | OPEN  | L     | H   | -                      |
| H         | $V_{IN} > V_{DETL}$    | H        | H                 | H                 | L                 | H     | OPEN  | L   | OUT= negative polarity |
| H         | $V_{IN} \leq V_{DETL}$ | H        | L                 | L                 | H                 | OPEN  | L     | H   |                        |
| H         | $V_{IN} \leq V_{DETL}$ | L        | L                 | L                 | H                 | OPEN  | L     | H   | -                      |

Note 7. When the VIN voltage is decreasing from VDETH or higher.



**10. Reference Data**

■ **Detection Voltage “High” (VDETH) and “Low” (VDETL) vs VIN**

1) VDETH=2.5V, VDETL=2.1V (POL=“L”)

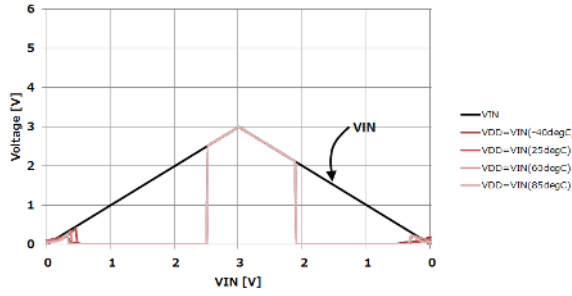


Figure 4. VDD=VIN

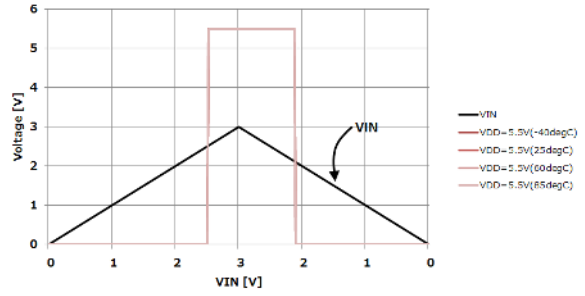


Figure 5. VDD=5.5V

2) VDETH=1.8V, VDETL=1.7V (POL=“L”)

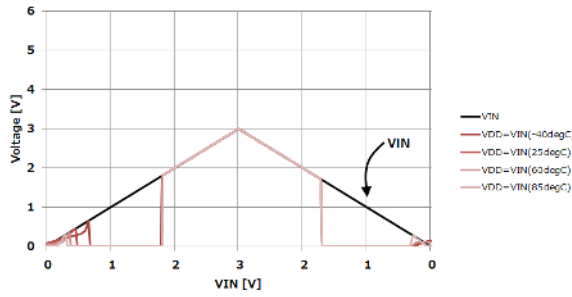


Figure 6. VDD=VIN

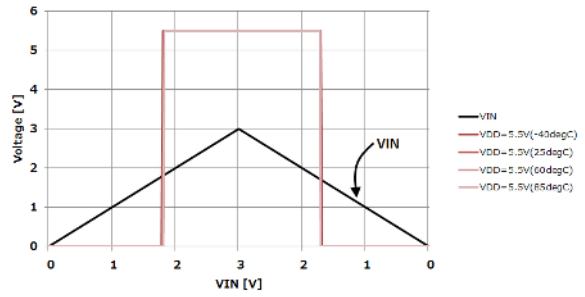


Figure 7. VDD=5.5V

■ Detection Voltage “High” (VDETH) and “Low” (VDETL) vs Ta

$\Delta$ VDET(mV) vs Ta

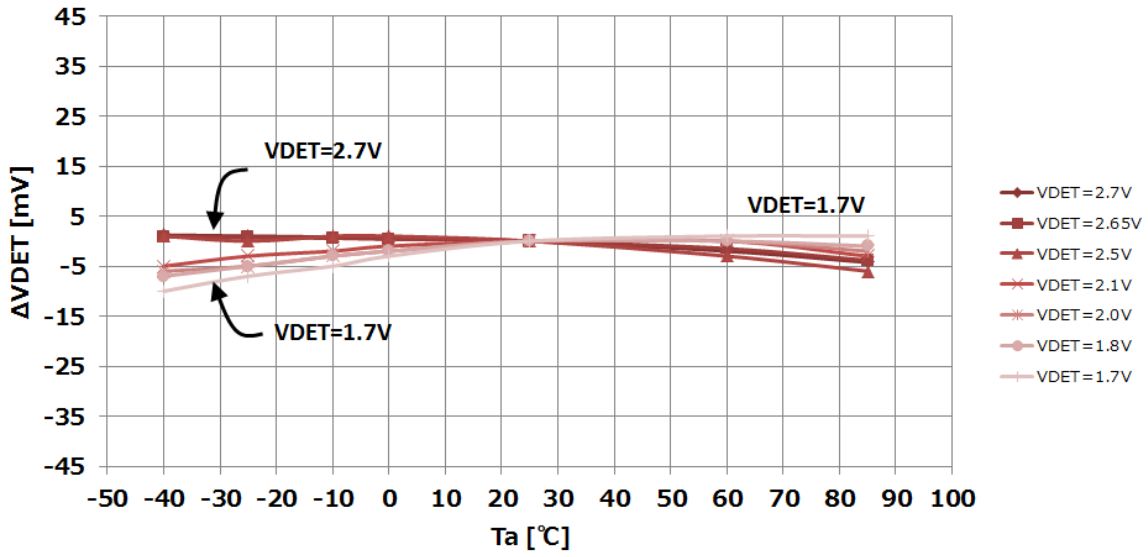


Figure 8.  $\Delta$ VDET(mV) vs Ta

1)  $\Delta$ VDET(%) vs Ta

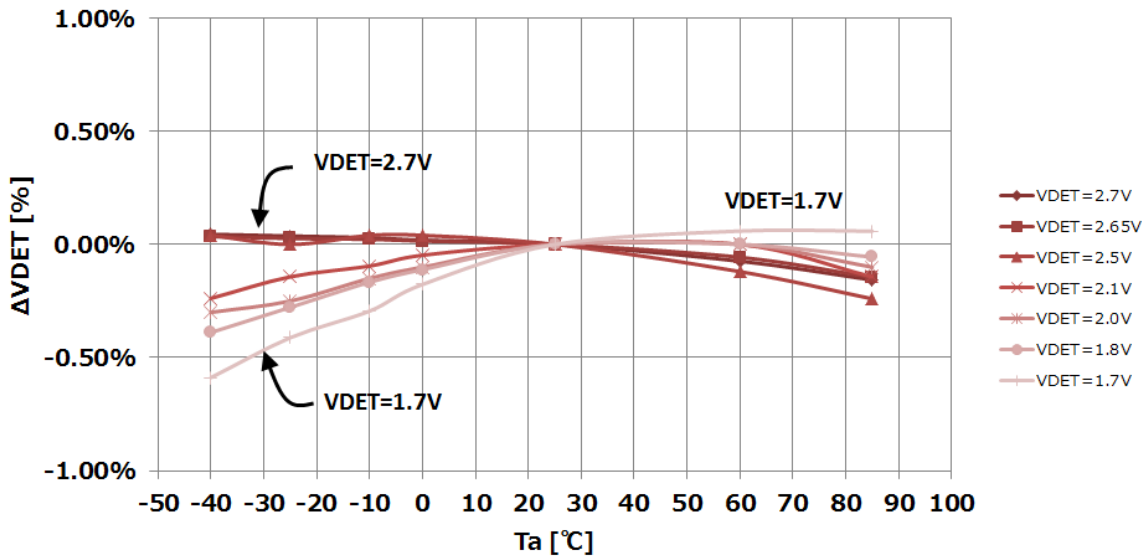


Figure 9.  $\Delta$ VDET(%) vs Ta

Note 8.  $\Delta$ VDET(%)= $\Delta$ VDET/ VDET (V)

■ Current consumption vs VIN & VDD

1) VDETH=2.5V, VDETL=2.1V (POL="L")

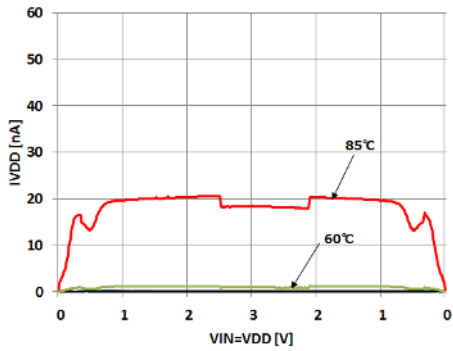


Figure 10. VDD=VIN

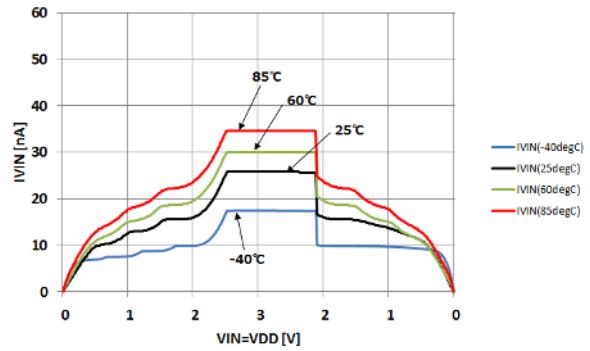


Figure 11. VDD=5.5V

2) VDETH=1.8V, VDETL=1.7V (POL="L")

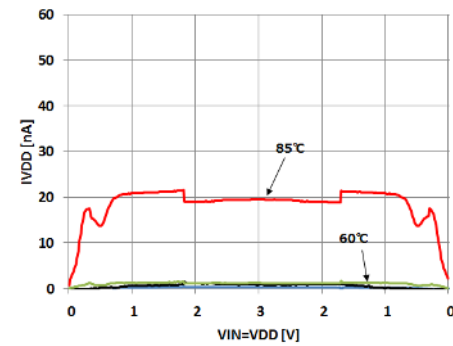


Figure 12. IVDD

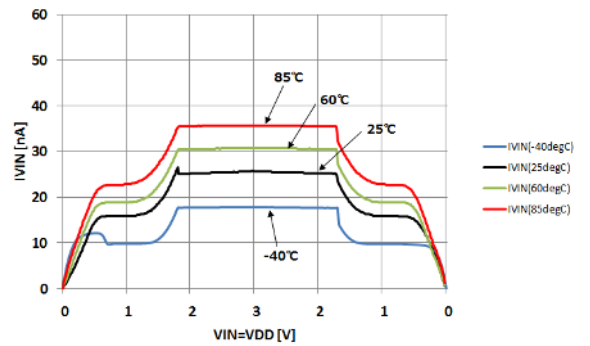


Figure 13. IVIN

■ Power Consumption vs Ta (VIN=VDD=5.5V)

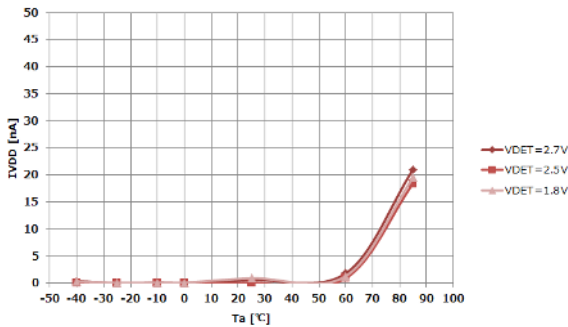


Figure 14. IVDD

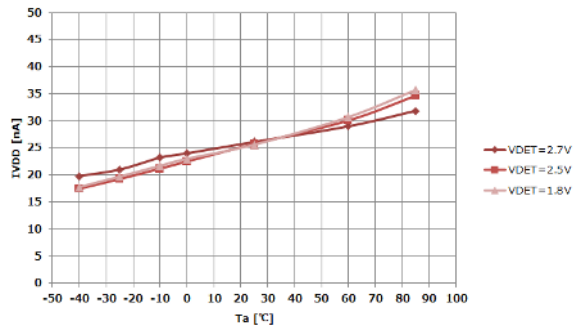


Figure 15. IVIN

■ Response time (tPLH, tPHL)

1) VDETH=2.5V, VDETL=2.1V (POL="L")

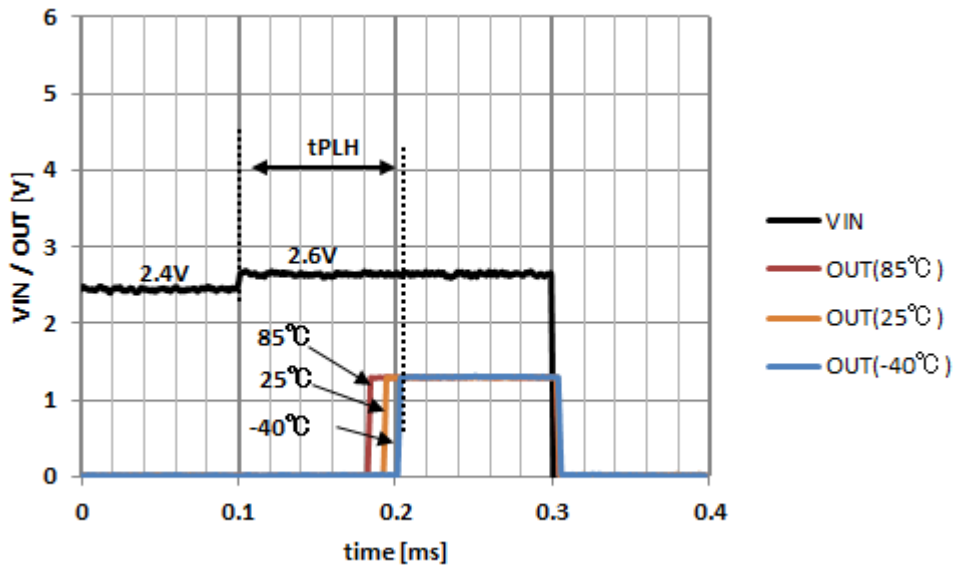


Figure 16. tPLH for VDETH=2.5V, VDETL=2.1V (POL="L"), VDD=1.3V

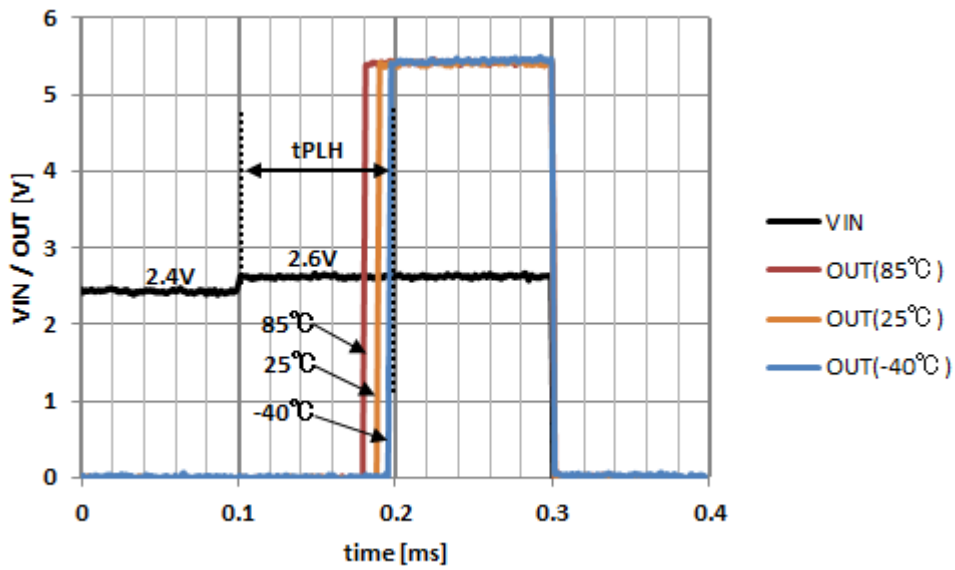


Figure 17. tPLH for VDETH=2.5V, VDETL=2.1V (POL="L"), VDD=5.5V

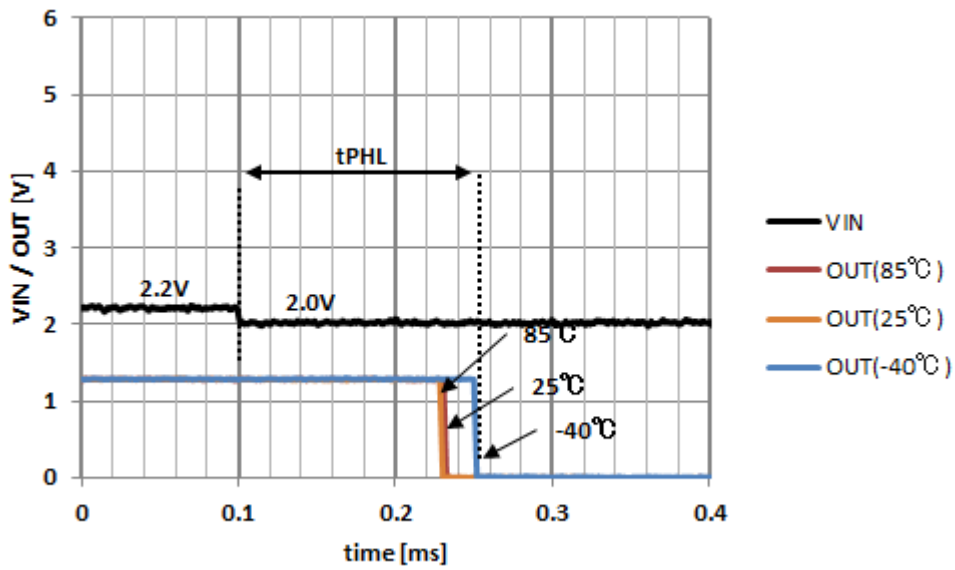


Figure 18. tPHL for VDETH=2.5V, VDETL=2.1V (POL="L"), VDD=1.3V

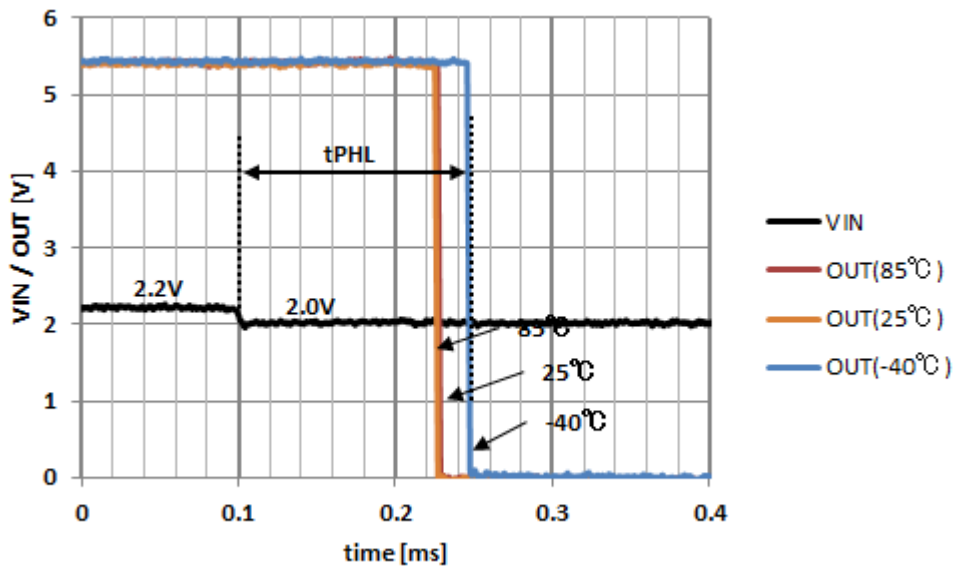


Figure 19. tPHL for VDETH=2.5V, VDETL=2.1V (POL="L"), VDD=5.5V

2)  $V_{DETH}=1.8V$ ,  $V_{DETL}=1.7V$  (POL="L")

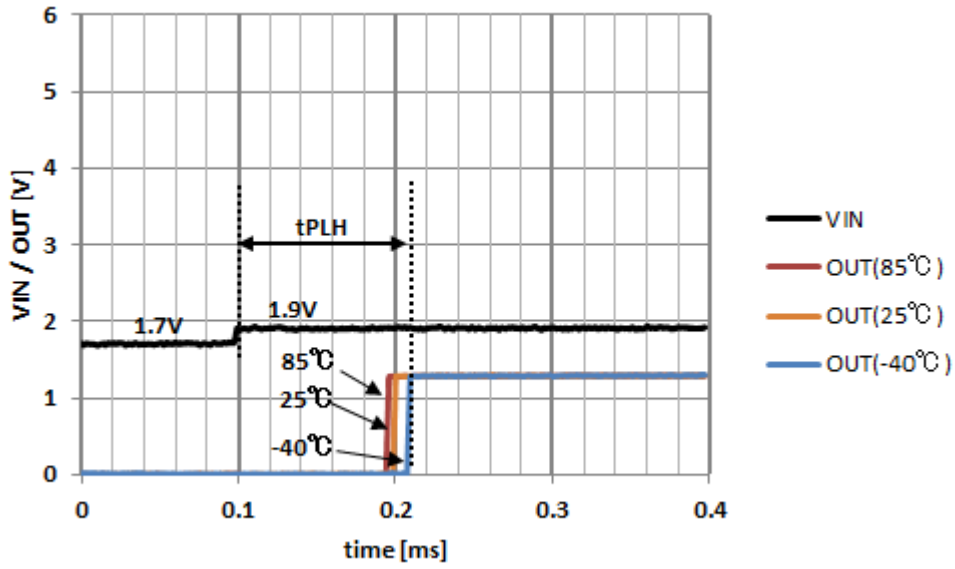


Figure 20.  $t_{PLH}$  for  $V_{DETH}=1.8V$ ,  $V_{DETL}=1.7V$  (POL="L"),  $V_{DD}=1.3V$

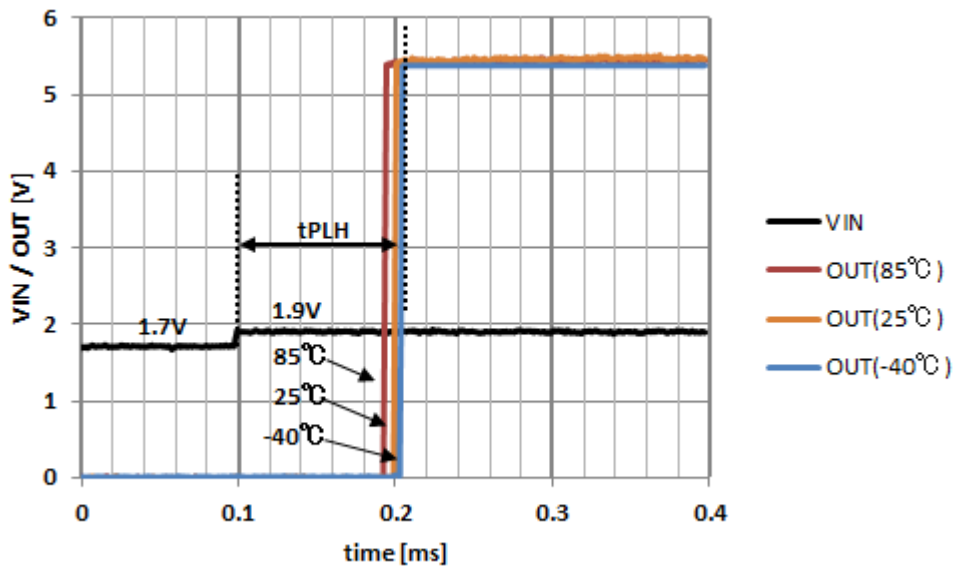


Figure 21.  $t_{PLH}$  for  $V_{DETH}=1.8V$ ,  $V_{DETL}=1.7V$  (POL="L"),  $V_{DD}=5.5V$

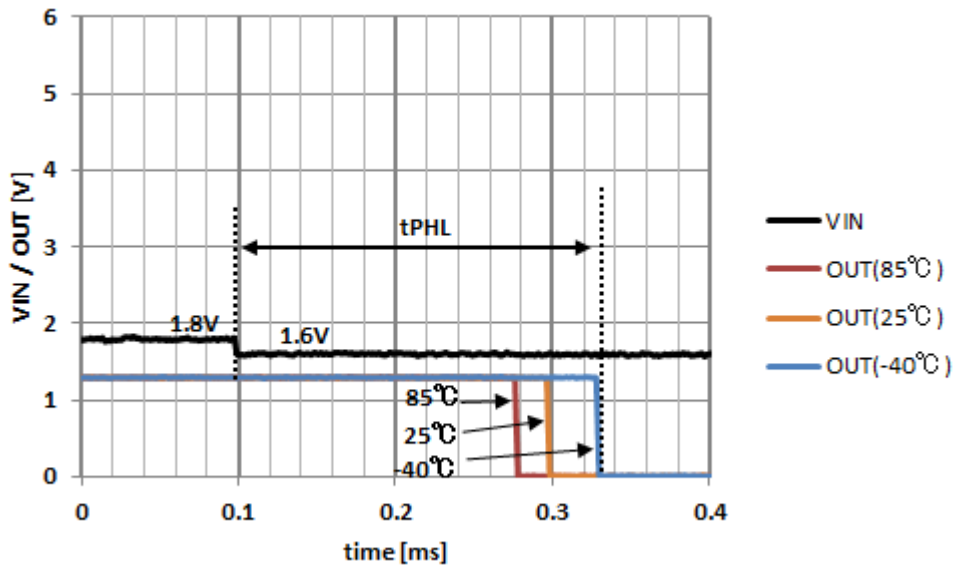


Figure 22. tPHL for VDETH=1.8V, VDETL=1.7V (POL="L"), VDD=1.3V

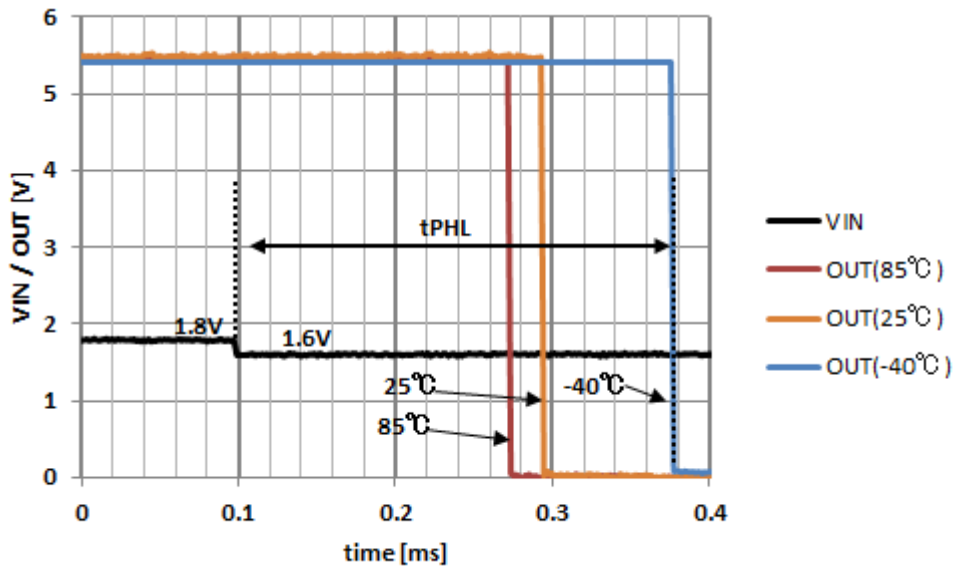


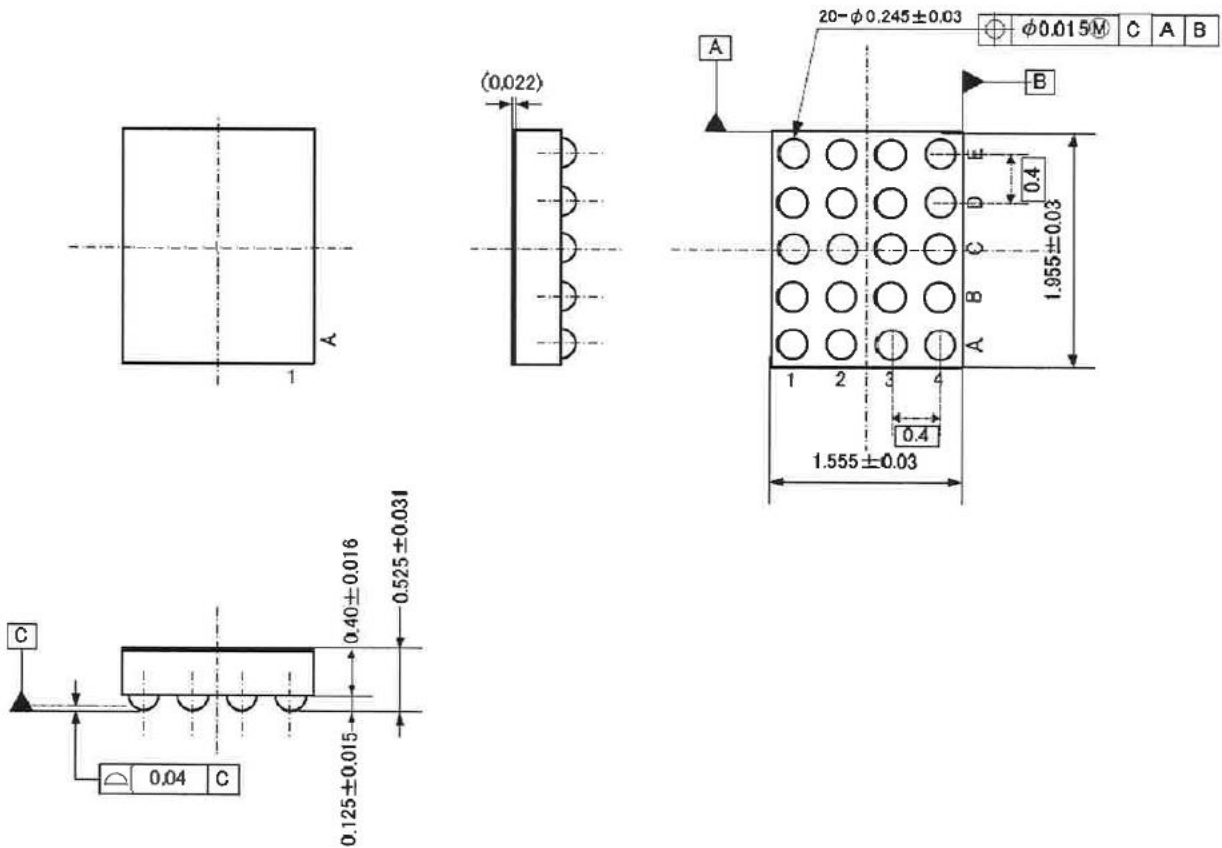
Figure 23. tPHL for VDETH=1.8V, VDETL=1.7V (POL="L"), VDD=5.5V

**11. Package**

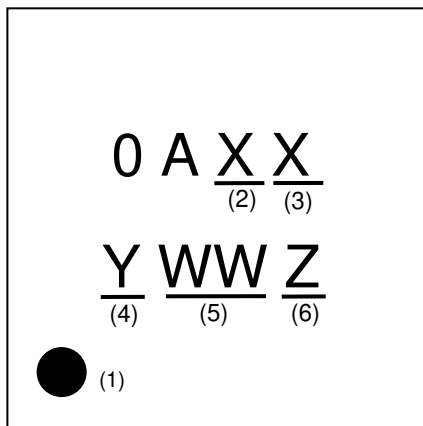
■ **Outline Dimensions**

20-pin WLCSP (Unit: mm)

When the IC is exposed to light, it might affect the electrical characteristics of the IC due to the light sensitivity of WLCSP package structures.



■ **Marking**



- (1) 1 Pin Indication
- (2) Symbol of the detection voltage of system 1
- (3) Symbol of the detection voltage of system 2
- (4) Year code (last 1 digit)
- (5) Week code
- (6) Management code



**12. Revision History**

| Date (YY/MM/DD) | Revision                                  | Page | Contents   |
|-----------------|---|------|--|
| 2017/09/07      | 00  | -    | First Edition  |
| 2018/06/04      | 01  | 1    | 1. General Description<br>detection → detector               |
|                 |   |      | 2. Features<br>-40 - 85 °C → -40 - +85 °C                    |
|                 |   | 6    | 8. Electrical Characteristics<br>-40 to 85 °C → -40 - +85 °C |
|                 |   |      | 8. Electrical Characteristics<br>5,5V → 5.5V                 |
|                 |   | 7    | 9. Description<br>AP4410A → AP4410AEC                        |
|                 |   |      | 9. Description<br>increasing → increasing                    |
|                 |   |      | 9. Description<br>Vref → VDET                                |
| 8               | 9. Description<br>increasing → increasing |      |  |
| 16              | 11. Package<br>updated                    |      |  |

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