NCV8881

Buck Regulator - Automotive, Watchdog

1.5 A

ON Semiconductor®

http://onsemi.com

The NCV8881 consists of a Buck switching regulator (SMPS) with a combination SMPS output undervoltage monitor and CPU watchdog circuit. In addition, two fixed−voltage low dropout regulator outputs are provided, and share an LDO output voltage status output. Once enabled, regulator operation continues until the Watchdog signal is no longer present. The NCV8881 is intended for Automotive, battery−connected applications that must withstand a 40 V load dump. The switching regulator is capable of converting the typical 9 V to 19 V automotive input voltage range to outputs from 3.3 V to 8 V at a constant switching frequency, which can be resistor programmed or synchronized to an external clock signal. Enable input threshold and hysteresis are programmable, with the enable input state replicated at an open drain Ignition Buffer output. The regulators are protected by current limiting, input overvoltage and overtemperature shutdown, as well as SMPS short circuit shutdown.

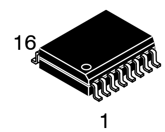
Features

- 1.5 A Switching Regulator (internal power switch)
- 100 mA, 5 V LDO Output
- 40 mA, 8.5 V LDO Output
- Operating Range 5 V to 19 V
- Programmable SMPS Frequency
- SMPS can be Synchronized to an External Clock
- Programmable SMPS Output Voltage Down to 0.8 V
- ±2% Reference Voltage Tolerance
- Internal SMPS Soft−Start
- Voltage−mode SMPS Control
- SMPS Cycle−by−Cycle Current Limit and Short−Circuit Protection
- Internal Bootstrap Diode
- Logic level Enable Input
- Enable Input Hysteresis Programmable by External Resistor Divider
- Enable Input State is Replicated at an Open Drain Output
- CPU Watchdog with Resistor Programmable Delays
- Watchdog Reset Output also Indicates SMPS Output Out of Regulation
- Battery Input Withstands Load Dump to 40 V
- Low Standby Current
- Thermal Shutdown (TSD)
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb−Free Devices

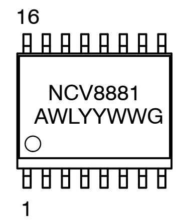
Applications

- Audio
- Infotainment
- Safety – Vision Systems
- Instrumentation

MARKING DIAGRAMS



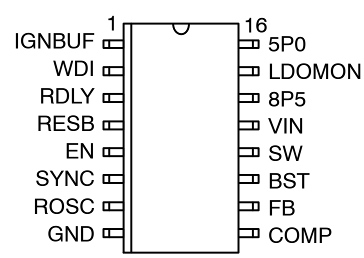
SO−16W EP PW SUFFIX CASE 751AG



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 32 of this data sheet.

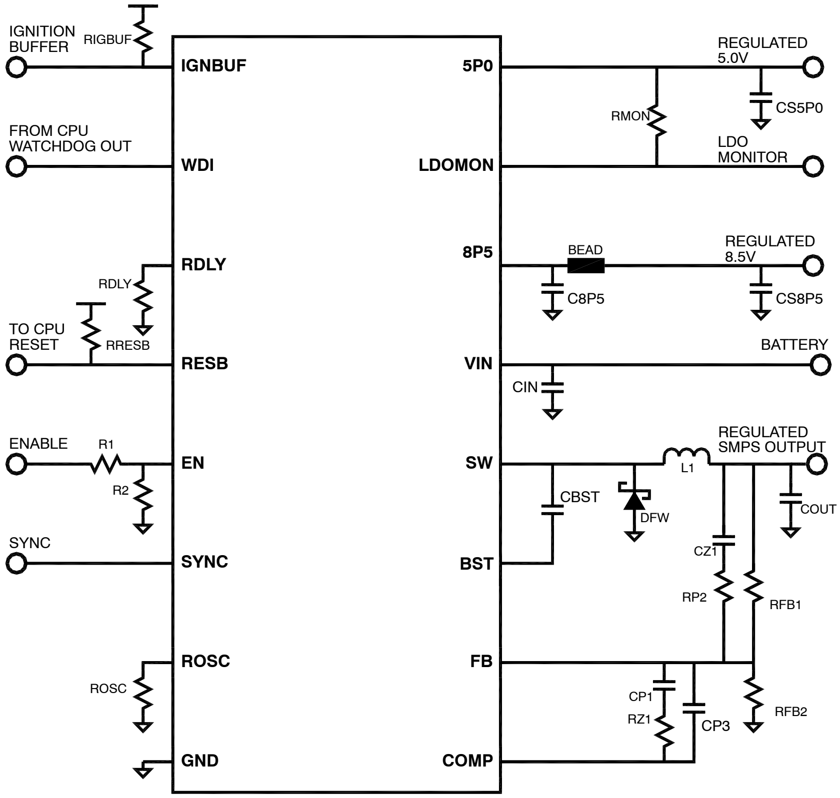


Figure 1. Typical Application

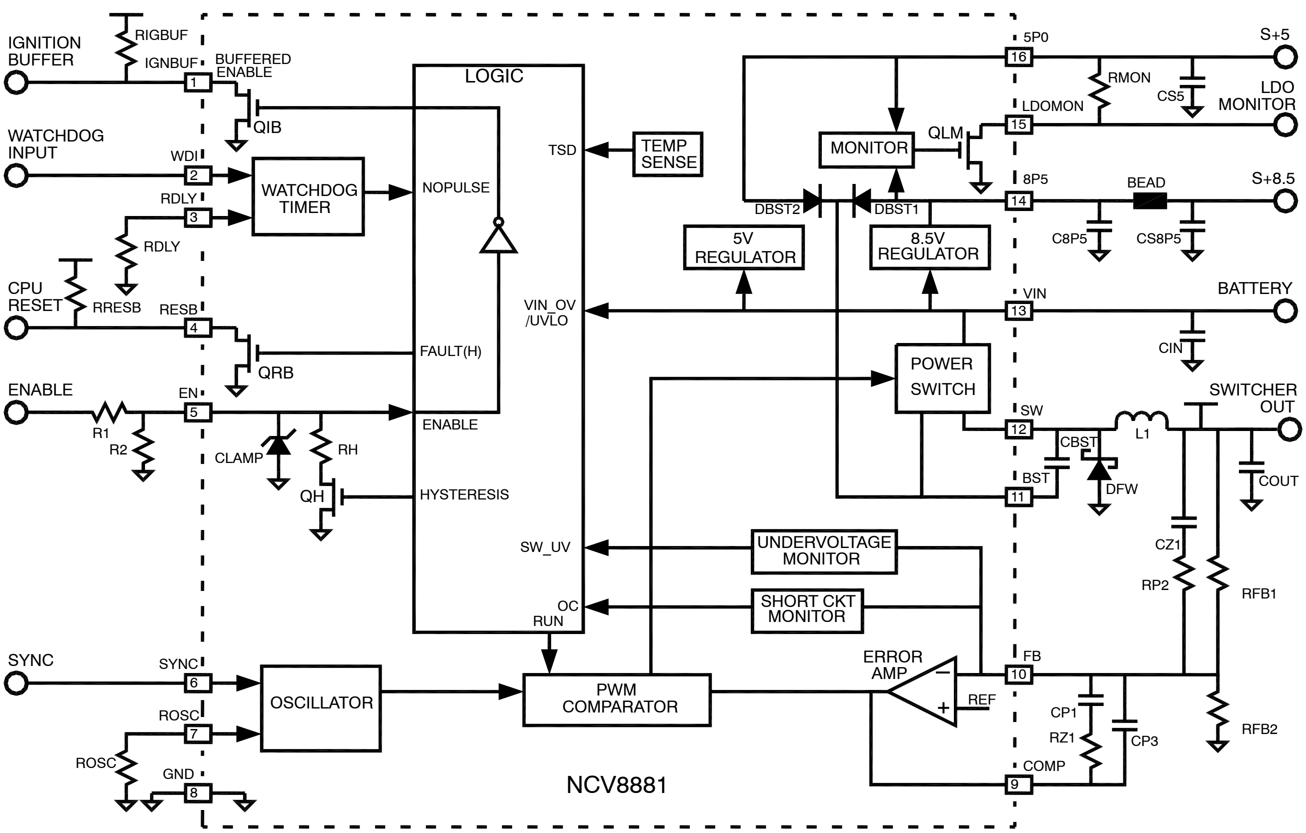


Figure 2. NCV8881 Detailed Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage on WDI		−0.3 to 7	V
Min/Max Voltage on RDLY		−0.3 to 7	V
Min/Max Voltage on RESB		−0.3 to 7	V
Min/Max Voltage on EN		−0.3 to 10	V
Max EN Current		10	mA
Min EN Current (with zero VIN voltage)		−10	mA
Min/Max Voltage on SYNC		−0.3 to 7	V
Min/Max Voltage on ROSC		−0.3 to 7	V
Min/Max Voltage COMP		−0.3 to 7	V
Min/Max Voltage FB		−0.3 to 7	V
Min Voltage SW – DC – 20 ns		−0.7 −3	V
Max Voltage VIN to SW		40	V
Max Voltage VIN		40	V
Min/Max Voltage BST		−0.3 to 30	V
Min/Max Voltage BST to SW		−0.3 to 15	V
Min/Max Voltage on 8P5		−0.3 to 9.5	V
Max 8P5 Current		70	mA
Min/Max Voltage on LDOMON		−0.3 to 7	V
Min/Max Voltage on 5P0		−0.3 to 7	V
Min/Max Voltage IGNBUF		−0.3 to 7	V
Storage Temperature range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to + 150	°C
ESD withstand Voltage Human Body Model Machine Model Charged Device Model	V_{ESD}	2.0 200 >1.0	kV V kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Parameter	Board/Mounting Conditions Typical Value		Unit
	Minimum Pad (Note 1)	1 sq. inch (Note 2)	
Junction−to−case top (Ψ_{JT}, θ_{JT})	30	16	°C/W
Junction−to−pin 1(Ψ_{JL1}, θ_{JL1})	70	65	°C/W
Junction−to−board (Ψ_{JB}, θ_{JB}) (Note 3)	15	17	°C/W
Junction−to−ambient ($R_{\theta JA}$, θ_{JA})	150	55	°C/W

Specific Notes on Thermal Characterization Conditions:

NOTE: All boards are 0.062” thick FR4, 3” square, with varying amounts of copper heat spreader, in still air (free convection) conditions. Numerical values are derived from an axisymmetric finite−element model where active die area, total die area, flag area, pad area, and board area are equated to the actual corresponding areas.

1. 1 oz. copper, 17.2 mm^2 spreader area (minimum exposed pad, not including traces which are assumed).
2. 1 oz. copper, 645 mm^2 (1 in^2) spreader area (includes exposed pad).
3. “Board” is defined as center of exposed pad soldered to board; this is the recommended number to be used for thermal calculations, as it best represents the primary heat flow path and is least sensitive to board and ambient properties.

PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	IGNBUF	This open drain output is pulled low whenever the EN signal is latched and a low level is recognized at the EN input.
2	WDI	CMOS compatible Watchdog pulse input from a CPU. To be valid, the time between falling edges of this signal must be less than the programmed Watchdog Delay.
3	RDLY	Delay programming pin for POR, BOOT and Watchdog delays. Connect a resistor between this pin and ground.
4	RESB	This is an open drain output for resetting a CPU. RESB goes low if the WDI signal period is longer than the programmed Watchdog delay, if VIN is above or below operating voltage, if the SMPS output is out of regulation, or if the part is in thermal shutdown.
5	EN	Logic compatible Enable input. Once a high is received at the EN pin, the part enters a startup sequence. Until expiration of the Soft−Start Timer, a low at the EN pin will shut off the part. Upon expiration of the Soft−Start Timer, a low at the EN pin will shut the part off only if the SMPS output is out of regulation, or the signal at the WDI input is not valid.
6	SYNC	Logic compatible Synchronization input. Grounding this input allows a resistor between the ROSC pin and ground to control the switching frequency. Connecting this pin to an external clock synchronizes switching to the rising edge of the clock.
7	ROSC	Oscillator frequency programming pin. Connect an external resistor from this pin to GND to set the switching frequency. Leave this pin floating to operate at the default frequency of the internal oscillator. Switching frequency is not controlled by this resistance if a clock is present at the SYNC pin, but the resistance remains in control of the modulator ramp amplitude.
8	GND	Battery return, and ground reference for output voltages.
9	COMP	Switching Regulator Error Amplifier output for tailoring SMPS transient response with external compensation components.
10	FB	Feedback input pin to program Switching Regulator output voltage, and detect a low or shorted SMPS output condition.
11	BST	Bootstrap input provides drive voltage higher than VIN to the SMPS N−channel Power Switch for minimum switch $R_{DS(on)}$ and highest efficiency. For a typical application connect a 0.1 μF ceramic capacitor from this pin to the SW pin, in close proximity to both pins.
12	SW	Switching node of the Switching Regulator. Connect the SMPS output inductor and cathode of the SMPS freewheeling diode to this pin.
13	VIN	Input voltage from battery. Place an input filter capacitor in close proximity to this pin.
14	8P5	Output of the internal 8.5 V linear regulator. This provides regulated gate drive voltage to the SMPS Power Switch. For a typical application connect a 4.7 μF ceramic capacitor in series with 0.5 Ω from this pin to ground.
15	LDOMON	This open drain output is pulled low if either the 5P0 or 8P5 output is out of regulation.
16	5P0	Output of the internal 5 V linear regulator. For a typical application connect a 4.7 μF ceramic capacitor in series with 0.5 Ω from this pin to ground.
	EXPOSED PAD	Solder this to a low thermal impedance path for cooling.

GENERAL SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{VIN} = 13.2 V, V_{EN} = 2.0 V, C_{IN} = 4.7 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN UVLO						
START Voltage Threshold	V_{STRT}		5.0	5.6	6.0	V
STOP Voltage Threshold	V_{STP}		4.2	4.6	5.0	V
VIN UVLO Hysteresis	V_{INHYST}		0.7	1.1		V
VIN OVERVOLTAGE						
STOP Voltage Threshold	V_{OVSTP}		19	20	21	V
RESTART Voltage Threshold	V_{OVSTT}		18	19.2		V
QUIESCENT CURRENT						
VIN Quiescent Current	I_{qMAX}	V_{FB} = 1 V, T_J = 25°C, V_{SW} = 0 V		2	5	mA
VIN Shutdown Current	I_{qSBMAX}	V_{EN} = 0 V, T_J = 25°C, V_{SW} = 0 V		10	15	μA
ENABLE (EN PIN)						
EN Logic High Threshold	V_{ENSTHH}				1.6	V
EN Logic Low Threshold	V_{ENSTHL}		1.2			V
EN Input Current	I_{ENSWL}	V_{EN} = 1.2 V	35	42	55	μA
EN Input Current	I_{ENSWH}	V_{EN} = 1.6 V	0.8	1.4	3.0	μA
Response to Open Input			NCV8881 is disabled			
Enable Delay		EN high to LDO turn−on		38	50	μs
Clamp Current		V_{EN} = 5 V		5	20	μA
Clamp Voltage		I_{EN} = 10 mA	9	10.5	12	V
IGNITION BUFFER (IGNBUF PIN)						
IGNBUF Output leakage		V_{EN} > 1.6 V		0	5	μA
IGNBUF Output Voltage Low	V_{IGBLO}	V_{EN} < 1.2 V, sinking 0.5 mA		0.02	0.1	V
THERMAL SHUTDOWN (TSD)						
Thermal Shutdown	T_{TSD}	(Note 4)	160	170	180	°C
Thermal Shutdown Hysteresis		(Note 4)		35		°C

4. Guaranteed by design.

LDO REGULATORS

ELECTRICAL CHARACTERISTICS (V_{VIN} = 13.2 V, V_{EN} = 2.0 V, C_{IN} = 4.7 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
5P0 OUTPUT						
Output UV START Threshold	V_{5UVSTT}	Percent of $\mathbf{V_{O5P0}}$	91	95	99	%
Output UV STOP Threshold	V_{5UVSTP}	Percent of $\mathbf{V_{O5P0}}$	89	93	97	%
Output UV Hysteresis	V_{5VUVH}	Percent of $\mathbf{V_{O5P0}}$		2		%
Output Voltage Range	V_{O5P0}	No load	4.8	5.0	5.2	V
Line Regulation		I_{OUT} = 1 mA, 6 V < V_{IN} < 19 V			4	mV/V
Current Limit			105	160	205	mA
Dropout Voltage		I_{5P0} = 70 mA, ΔV_{5P0} = 2%		315 (Note 6)	400	mV
Output Load Capacitance Range	C_O	Output capacitance for stability (Note 5)	3.9		100	μF
Output Load Capacitance ESR Range	ESR_{Co}	ESR for stability (Note 5)	0.2		5	Ω
Power Supply Ripple Rejection	PSRR	V_{VIN} = 13.2 V + 0.5 V_{pp} 100 Hz sine−wave, C_{5P0} = 10 μF (Note 5)		60		dB
Startup Overshoot		$R_{5P0LOAD}$ = 5 kΩ; C_{5P0} = 10 μF (Note 5)			3	%
8P5 OUTPUT						
Output UV START Threshold	V_{8UVSTT}	Percent of $\mathbf{V_{O8P5}}$	91	95	99	%
Output UV STOP Threshold	V_{8UVSTP}	Percent of $\mathbf{V_{O8P5}}$	89	93	97	%
Output UV Hysteresis	V_{8VUVH}	Percent of $\mathbf{V_{O8P5}}$		2		%
Output Voltage Range	V_{O8P5}	No load; 9 V < V_{IN} < 19 V	8.26	8.5	8.74	V
Line Regulation		I_{OUT} = 1 mA, 9.5 V < V_{IN} < 19 V			7	mV/V
Current Limit			44	68	85	mA
Dropout Voltage		I_{8P5} = 20 mA, ΔV_{8P5} = 2%		165 (Note 6)	300	mV
Output Load Capacitance Range	C_O	Output capacitance for stability (Note 5)	3.9		100	μF
Output Load Capacitance ESR Range	ESR_{Co}	ESR for stability (Note 5)	0.2		5	Ω
Power Supply Ripple Rejection	PSRR	V_{VIN} = 13.2 V + 0.5 V_{pp} 100 Hz sine wave, C_{8P5} = 10 μF (Note 5)		60		dB
Startup Overshoot		$R_{8P5LOAD}$ = 10 kΩ; C_{8P5} = 10 μF (Note 5)			3	%
Output Clamp Voltage	V_{CLP8P5}	I_{8P5} = 67 mA into the NCV8881	9	11	13	V
LDOMON OUTPUT						
Output leakage		$V_{5P0} > V_{5UVSTT}$ and $V_{8P5} > V_{8UVSTT}$		0.2	5	μA
Output Voltage Low	V_{RBLO}	$V_{5P0} < V_{5UVSTP}$ or $V_{8P5} < V_{8UVSTP}$, sinking 0.5 mA		0.03	0.1	V

5. Guaranteed by design.
6. T_J = 125°C

SMPS REGULATOR

ELECTRICAL CHARACTERISTICS (V_{VIN} = 13.2 V, V_{EN} = 2.0 V, V_{BST} = V_{SW} + 8.2 V, C_{BST} = 0.1 μF, C_{IN} = 4.7 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SOFT−START						
Soft−Start Completion Time	t_{SS}		3	5	7	ms
VOLTAGE REFERENCE (FB Pin)						
FB Voltage (COMP connected to FB)	V_{FBR}	T_J = 25°C −40°C ≤ T_J ≤ 150°C	0.792 0.784	0.8 0.8	0.808 0.816	V
FB PIN MONITOR (SMPS Output Monitor)						
FB Monitor High Threshold	V_{FBMONH}	V_{FB} increasing; Percent of V_{FBR}	91	95	99	%
FB Monitor Low Threshold	V_{FBMONL}	V_{FB} decreasing; Percent of V_{FBR}	89	93	97	%
FB Monitor Hysteresis	V_{FBMONY}		10	20		mV
FB Low to RESB Output Delay	t_{FBLDLY}			2.5	10	μs
ERROR AMPLIFIER						
FB Bias Current	I_{FBBIAS}	V_{FB} = V_{FBR}	−0.1		0.1	μA
DC Gain	A_V	(Note 7)	70			dB
Gain−Bandwidth Product	GBW	(Note 7)	8			MHz
Slew Rate COMP Rising		V_{FB} = V_{FBR} − 25 mV, C_{COMP} = 50 pF, **I_{COMP}** = −1 mA, **V_{COMP}** within ramp voltage levels. (Note 7)	6			V/μs
Slew Rate COMP Falling		V_{FB} = V_{FBR} +25 mV, C_{COMP} = 50 pF, **I_{COMP}** = 1 mA, **V_{COMP}** within ramp voltage levels. (Note 7)	6			V/μs
COMP Source Current	I_{SOURCE}	V_{COMP} = 2.2 V V_{COMP} = 3.2 V	1.5 1.8	4 4	10 10	mA mA
COMP Sink Current	I_{SINK}	V_{COMP} = 2.2 V V_{COMP} = 1.1 V	1.3 0.6	3 1.6	10 10	mA mA
Ramp Peak Voltage			2.8	3.1	3.2	V
Ramp Valley Voltage			1.1	1.2	1.3	V
Ramp Amplitude			1.6	1.9	2.0	V
OSCILLATOR						
Frequency	F_{OSC}	R_{ROSC} = open ROSC = 36 kΩ	154 337	170	186 429	kHz
Maximum ROSC Controlled Frequency	F_{OSCMAX}	Resistor from ROSC to GND	500	700	850	kHz
ROSC Pin Voltage	V_{ROSC}	R_{ROSC} = open	0.970	1.02	1.080	V
SYNCHRONIZATION						
Frequency Range	f_{SYNCMX}	(Note 7)	160		600	kHz
Synchronization Delay	t_{SNCDLY}	From rising SYNC edge	200	370	500	ns
De−Synchronization Delay	$t_{USNCDLY}$	From last rising SYNC edge; ROSC = open	6.6	7.8	10	μs
Input Current		V_{SYNC} = 5.0 V		5	10	μA
SYNC Logic High Threshold	V_{SNCTHH}				2	V
SYNC Logic Low Threshold	V_{SNCTHL}		0.8			V
Response to Input Held High		Reverts to internal oscillator (Note 7)				

7. Guaranteed by design.

SMPS REGULATOR

ELECTRICAL CHARACTERISTICS (V_{VIN} = 13.2 V, V_{EN} = 2.0 V, V_{BST} = V_{SW} + 8.2 V, C_{BST} = 0.1 μF, C_{IN} = 4.7 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150 °C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYNCHRONIZATION						
Minimum High Pulse Width	$t_{PWHIMIN}$	time $\mathbf{V_{SYNC}}$ is above 2 V (Note 7)	50			ns
Minimum Low Pulse Width	$t_{PWLIMIN}$	time $\mathbf{V_{SYNC}}$ is below 0.8 V (Note 7)	50			ns
DUTY CYCLE LIMITATIONS						
Minimum Off Time	t_{MINOFF}	SW falling to SW rising	50	120	200	ns
Minimum On Time	t_{MINON}	SW rising to SW falling	100	330	550	ns
CURRENT LIMIT						
Current Limit			1.75	2.2	3	A
Current Limit Response Time (Note 7)		From time of power switch turn−on			200	ns
SHORT CIRCUIT DETECTOR						
FB Pin Threshold	V_{FBSC}	% of $\mathbf{V_{FBR}}$	70	76	85	%
Soft−Start Timer	t_{SSTIMR}	From start of Soft−start, % of $\mathbf{t_{SS}}$ (Note 7)	100		250	%
POWER SWITCH						
ON Resistance	R_{DSON}	V_{BST}= V_{SW} + 6.0 V, T_J = 25°C (Note 7)			360	mΩ
SW Risetime		Inductor current = 1 A, T_J = 25°C (Note 7)		30		ns
SW Falltime		Inductor current = 1 A, T_J = 25°C (Note 7)		30		ns

7. Guaranteed by design.

WATCHDOG

ELECTRICAL CHARACTERISTICS (V_{VIN} = 13.2 V, V_{EN} = 2 V, C_{IN} = 4.7 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
WATCHDOG INPUT (WDI pin)						
Input High Voltage			2.0			V
Input Low Voltage					0.8	V
Input Current		V_{WDI} = 5.0 V		5	10	μA
Threshold Frequency	f_{WDTH}	to prevent RESB low R_{DLY} = 10 kΩ R_{DLY} = 20 kΩ R_{DLY} = 30 kΩ	 20.85 10.42 6.95			Hz
RDLY INPUT						
Output Voltage		R_{DLY} = 10 kΩ	0.917	0.99	1.067	V
Output Voltage		R_{DLY} = 30 kΩ	0.940	1.02	1.092	V
RESB OUTPUT						
Output Voltage Low	V_{RBLO}	$V_{FB} < V_{FBMONL}$, sinking 0.5 mA		0.03	0.1	V
Output leakage		$V_{FB} > V_{FBMONH}$		0.4	5	μA
POR Delay Time	t_{POR}	$V_{FB} > V_{FBMONH}$ to RESB high; R_{DLY} = 10 kΩ R_{DLY} = 20 kΩ (Note 8) R_{DLY} = 30 kΩ (Note 8) R_{DLY} = open; R_{OSC} = 36 kΩ (Note 8) R_{DLY} = open; R_{OSC} = open	 4.0 8 12	 5 10 15	 6.0 12 18 50 110	ms
Boot Delay Time	t_{BD}	RESB high to low; R_{DLY} = 10 kΩ R_{DLY} = 20 kΩ (Note 8) R_{DLY} = 30 kΩ (Note 8) R_{DLY} = open; R_{OSC} = 36 kΩ (Note 8) R_{DLY} = open; R_{OSC} = open	 40 80 120	 50 100 150	 60 120 180 500 1100	ms
Watchdog Delay Time	t_{WD}	WDI low to RESB low; R_{DLY} = 10 kΩ R_{DLY} = 20 kΩ (Note 8) R_{DLY} = 30 kΩ (Note 8) R_{DLY} = open; R_{OSC} = 36 kΩ (Note 8) R_{DLY} = open; R_{OSC} = open	 48 96 144	 60 120 180	 72 144 216 550 1300	ms

8. Guaranteed by design.

FAULT RESPONSES

INPUTS		RESPONSE TO A SINGLE FAULT EVENT					FULL OPERATION RESTORED BY:
FAULT EVENT	EN	EN Latch	5P0	8P5	SMPS	RESB	
VIN Undervoltage	L	UNLATCH	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	VIN > UVLO, EN High
VIN Undervoltage	H	UNLATCH	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	VIN > UVLO
VIN Overvoltage	L	Stays Latched	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	VIN < OV Threshold
VIN Overvoltage	H	Stays Latched	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	VIN < OV Threshold
Thermal Shutdown	L	Stays Latched	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	Decrease Temp
Thermal Shutdown	H	Stays Latched	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	Decrease Temp
5P0 Out of Regulation	L	Stays Latched	Current limited	Stays ON	Stays ON	No Effect	Remove Overload
5P0 Out of Regulation	H	Stays Latched	Current limited	Stays ON	Stays ON	No Effect	Remove Overload
8P5 Out of Regulation	L	Stays Latched	Stays ON	Current limited	Stays ON	No Effect	Remove Overload
8P5 Out of Regulation	H	Stays Latched	Stays ON	Current limited	Stays ON	No Effect	Remove Overload
SMPS Out of Regulation	L	UNLATCH	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	EN High
SMPS Out of Regulation	H	Stays Latched	Stays ON	Stays ON	Stays ON	LOW	Remove Overload
SMPS shorted to ground	L	UNLATCH	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	EN High
SMPS shorted to ground	H	UNLATCH	Stays ON	Stays ON	Latched OFF	LOW	EN Low, then High
Watchdog Signal Invalid	L	UNLATCH	SHUTDOWN	SHUTDOWN	SHUTDOWN	LOW	EN High
Watchdog Signal Invalid	H	Stays Latched	Stays ON	Stays ON	Stays ON	Pulses Low	Apply Valid WDI

TYPICAL PERFORMANCE CHARACTERISTICS

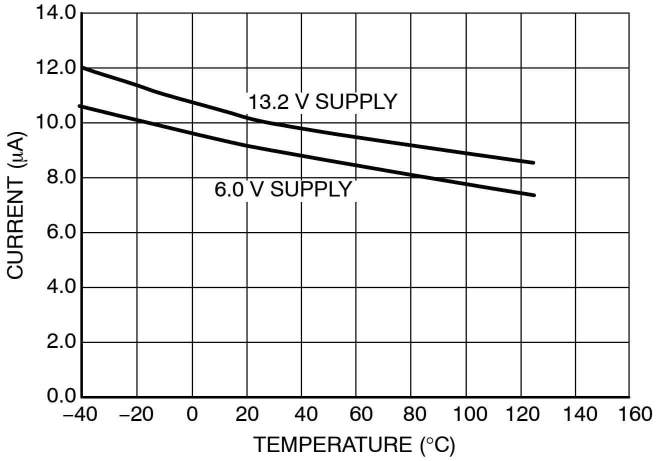


Figure 3. Supply Current (EN Low) vs. Temperature

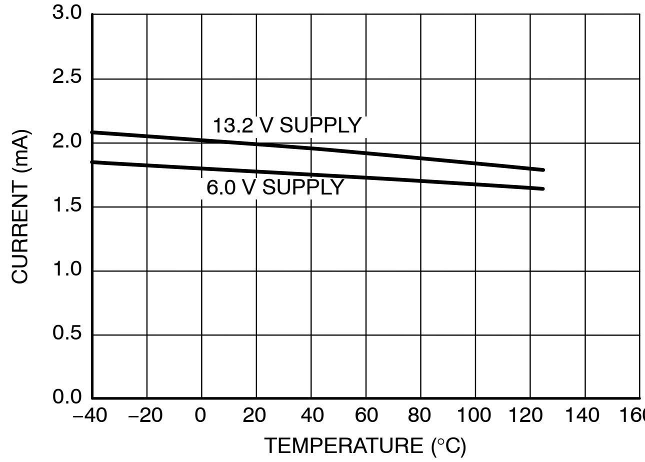


Figure 4. Supply Current (EN High) vs. Temperature

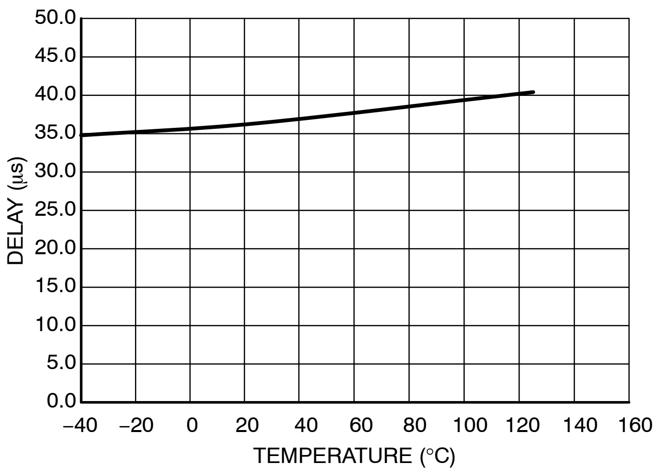


Figure 5. En Delay vs. Temperature

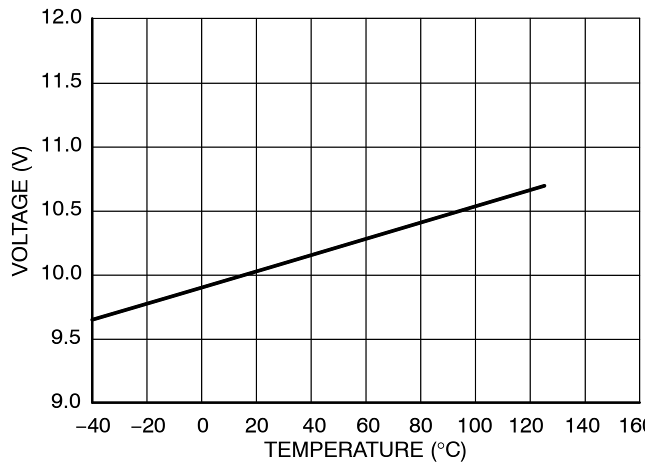


Figure 6. EN Clamp Voltage vs. Temperature

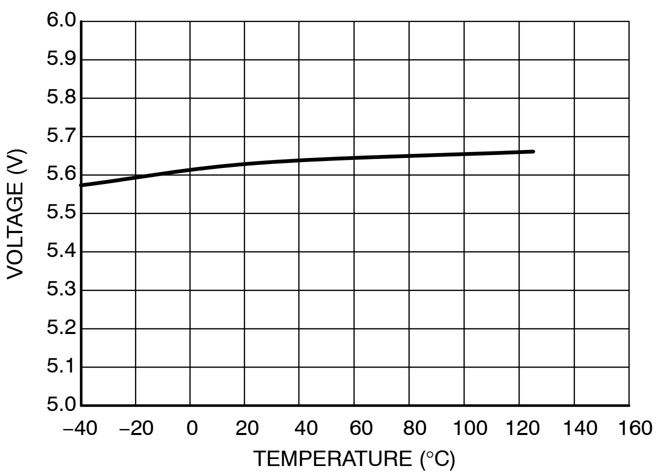


Figure 7. V_{IN} UVLO START Voltage vs. Temperature

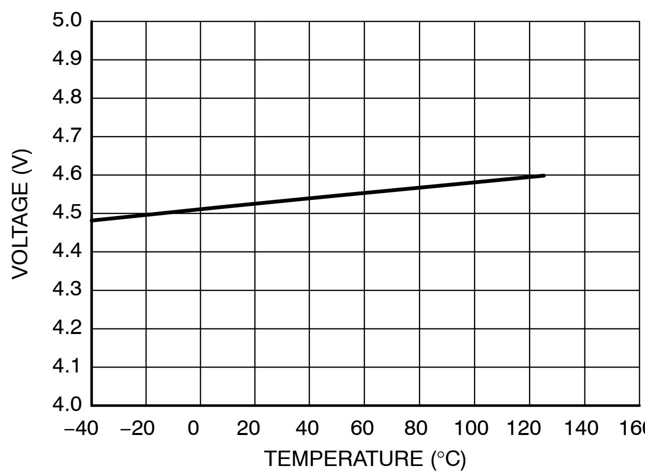


Figure 8. V_{IN} UVLO STOP Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

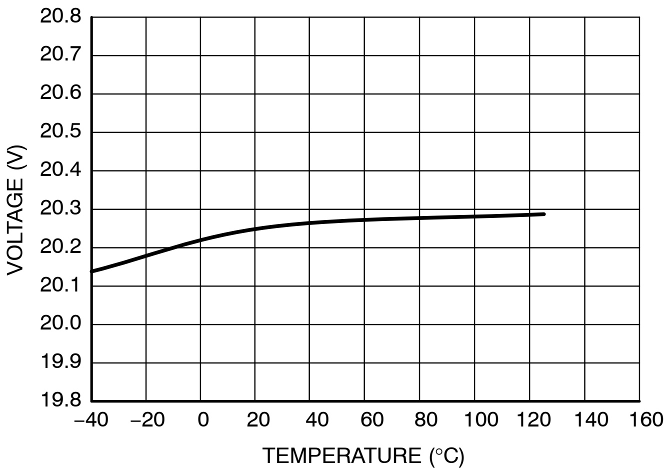


Figure 9. V_{IN} OV STOP Voltage vs. Temperature

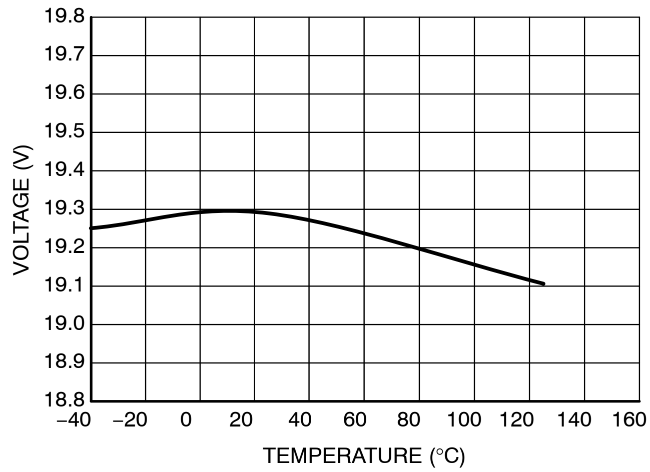


Figure 10. V_{IN} OV RESTART Voltage vs. Temperature

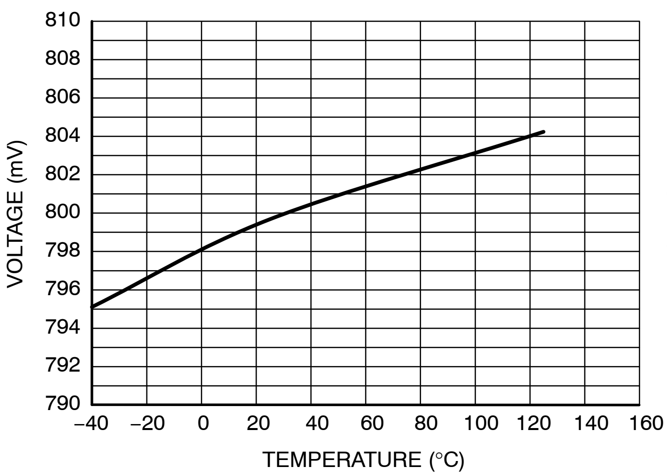


Figure 11. Reference Voltage vs. Temperature

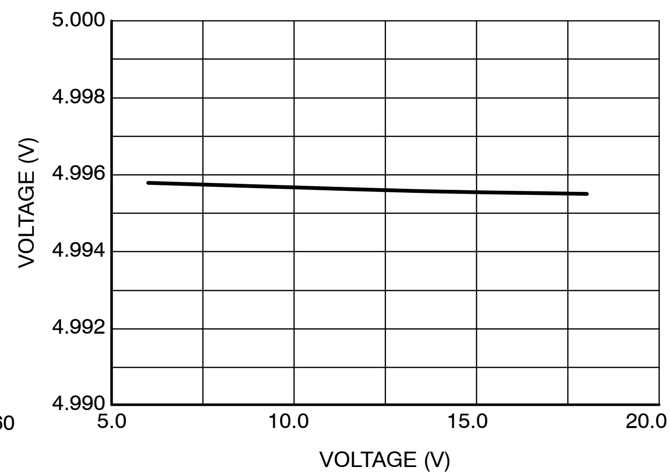


Figure 12. 5P0 Output Voltage vs. Input Voltage

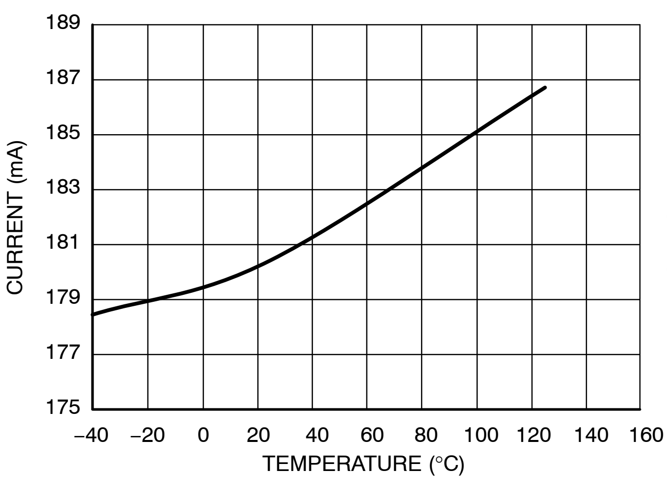


Figure 13. 5P0 Output Current Limit vs. Temperature

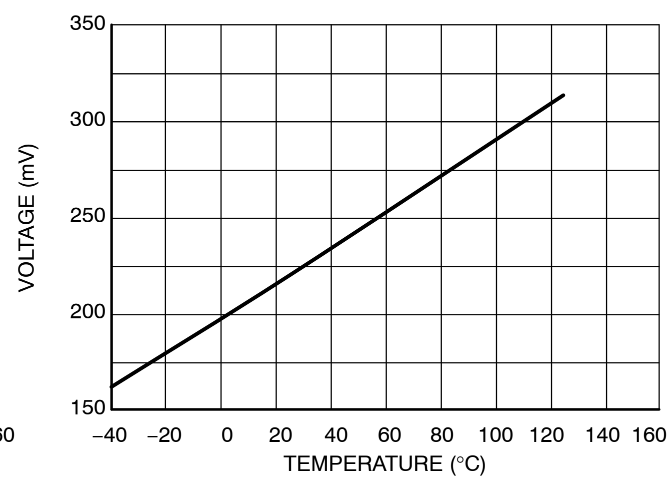


Figure 14. 5P0 Dropout Voltage Limit vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

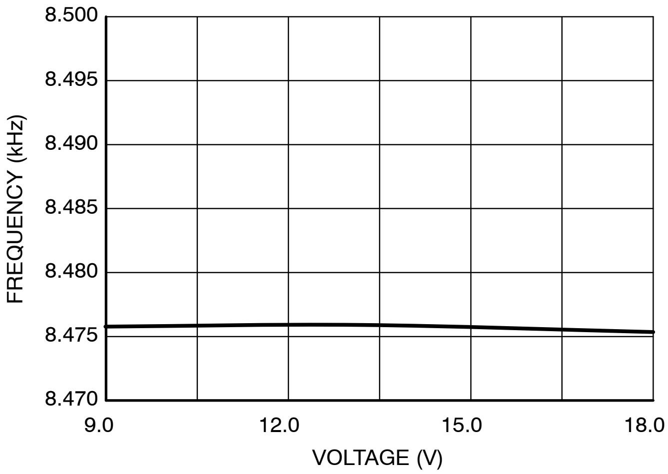


Figure 15. 8P5 Output Voltage vs. Input Voltage

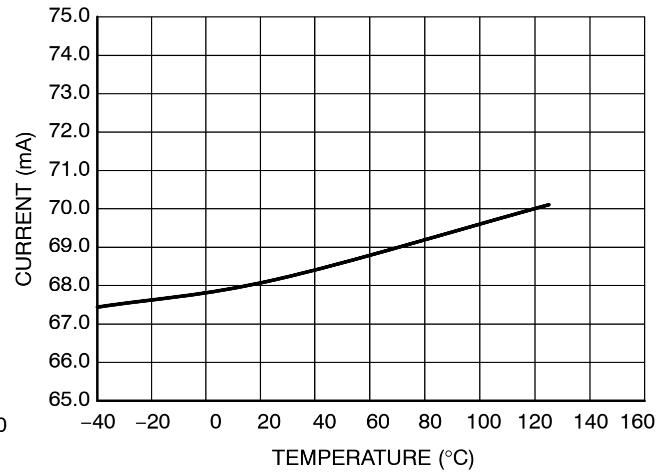


Figure 16. 8P5 Output Current Limit vs. Temperature

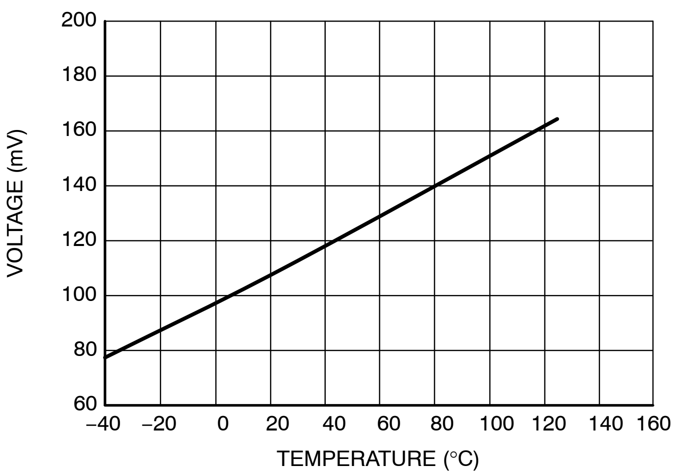


Figure 17. 8P5 Dropout Voltage vs. Temperature

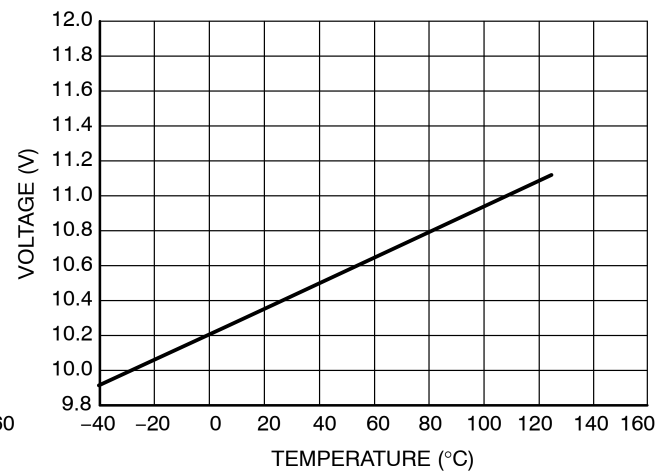


Figure 18. 8P5 Output Clamp vs. Temperature

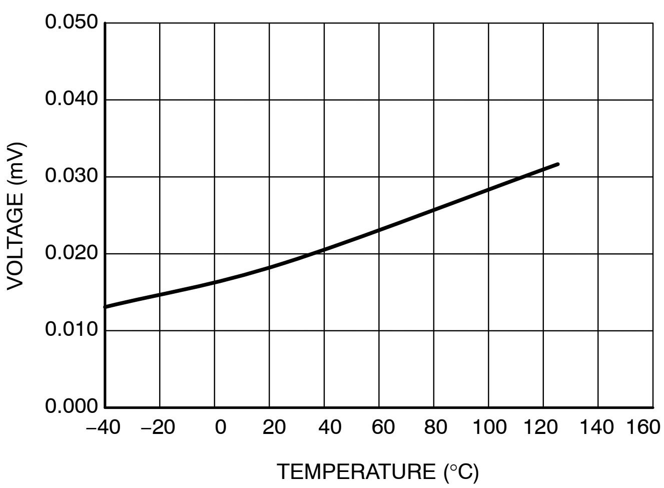


Figure 19. LDOMON Low Voltage vs. Temperature

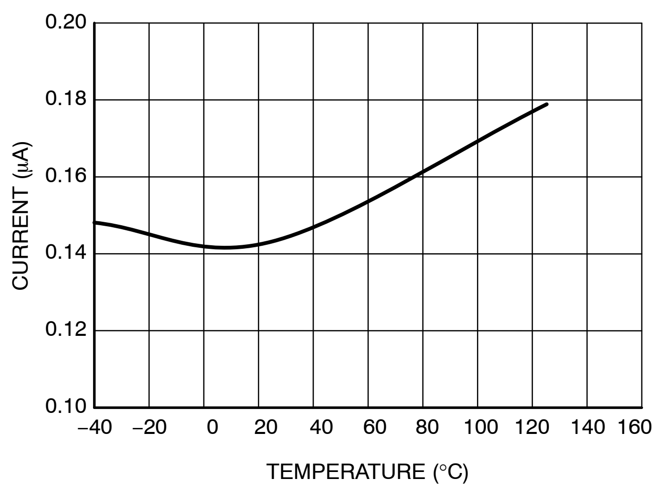


Figure 20. LDOMON Leakage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

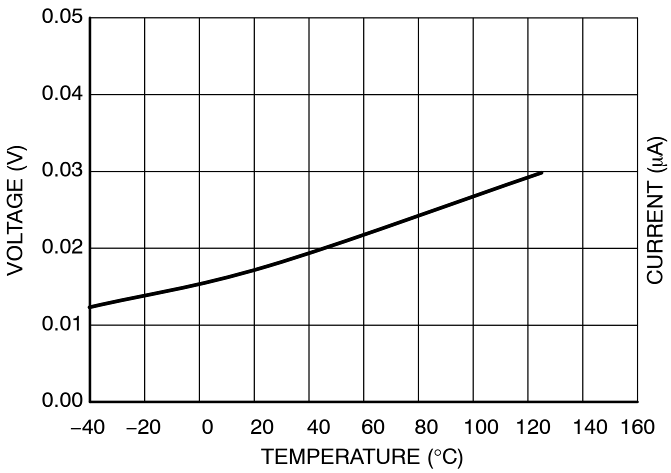


Figure 21. RESB Low Voltage vs. Temperature

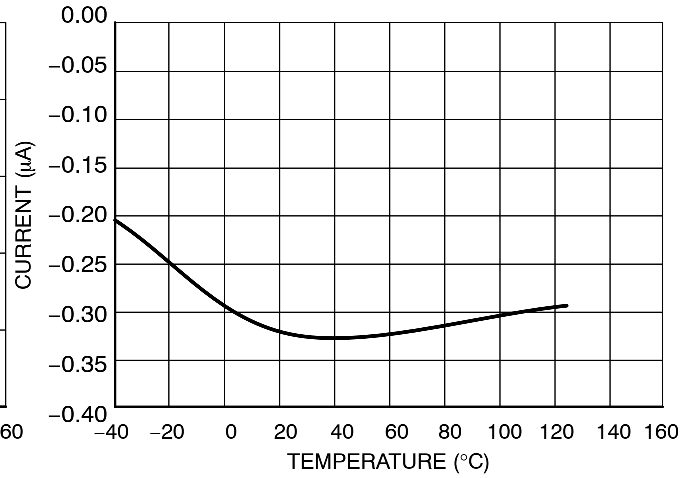


Figure 22. RESB Leakage vs. Temperature

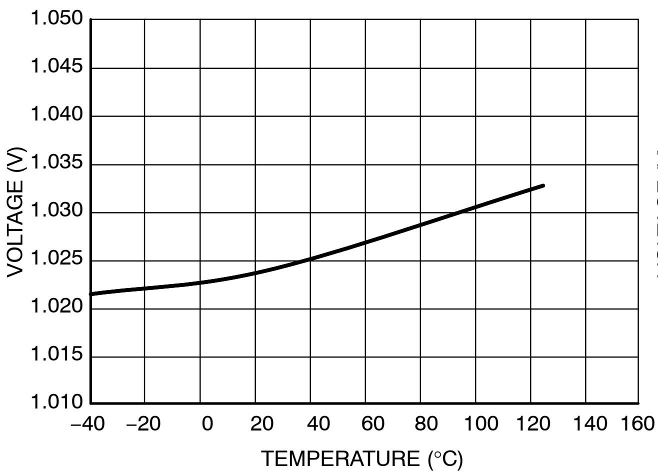


Figure 23. ROSC Voltage vs. Temperature

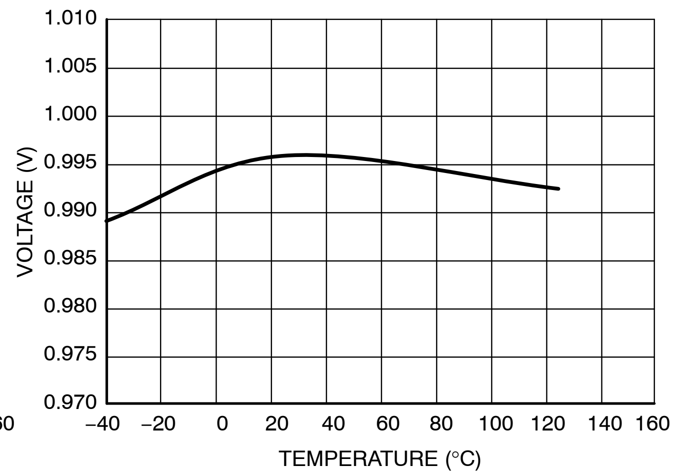


Figure 24. RDLY Voltage vs. Temperature

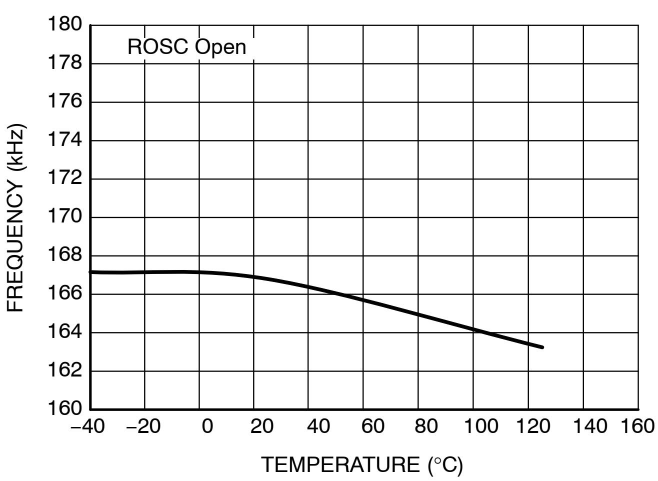


Figure 25. Switching Frequency vs. Temperature

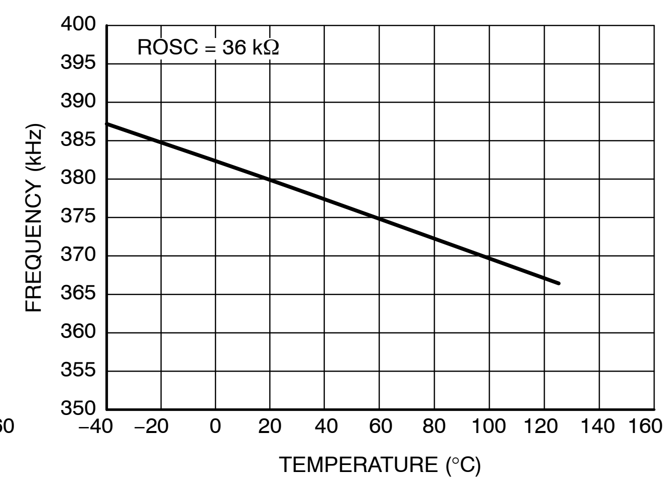


Figure 26. Switching Frequency vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

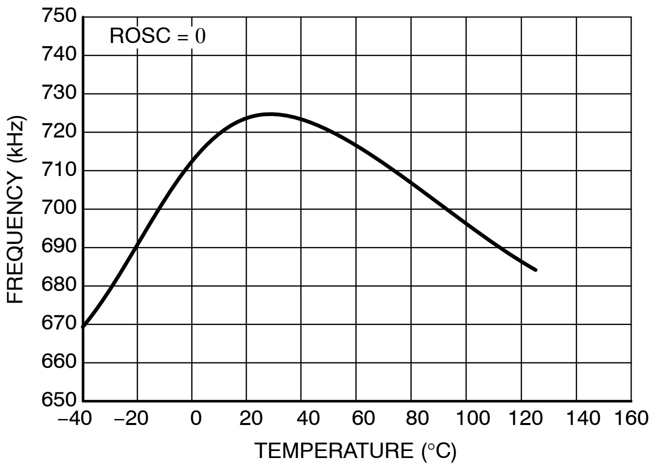


Figure 27. Maximum Switching Frequency vs. Temperature

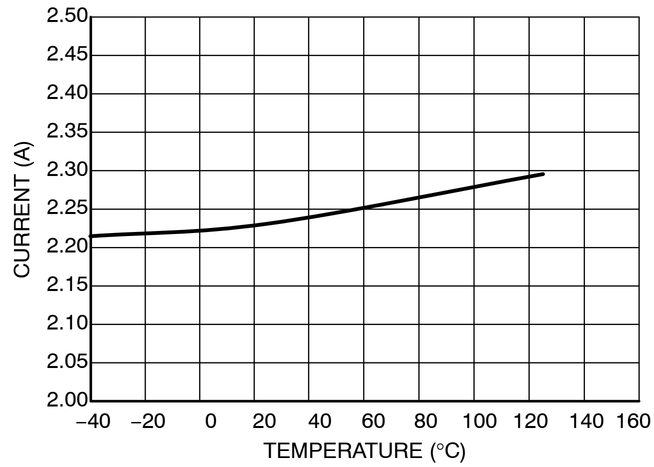


Figure 28. SMPS Current Limit vs. Temperature

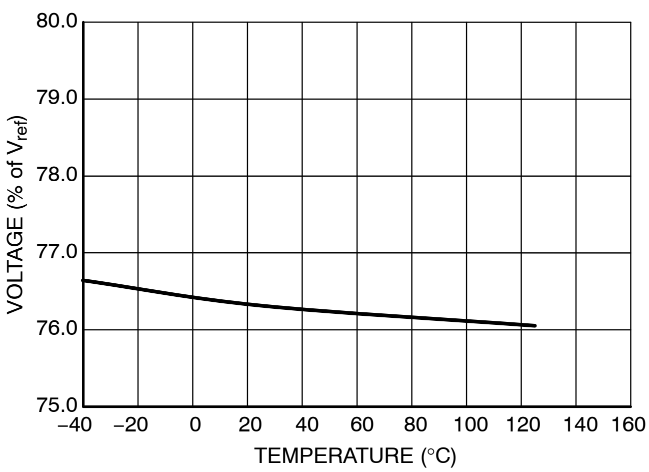


Figure 29. SMPS Short−Circuit Threshold vs. Temperature

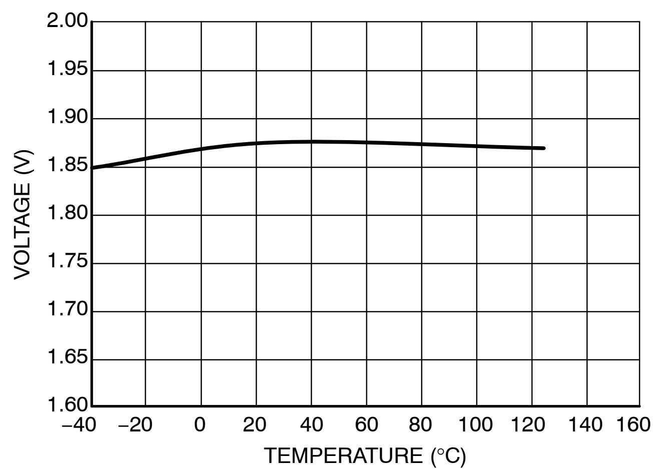


Figure 30. SMPS Ramp Amplitude vs. Temperature

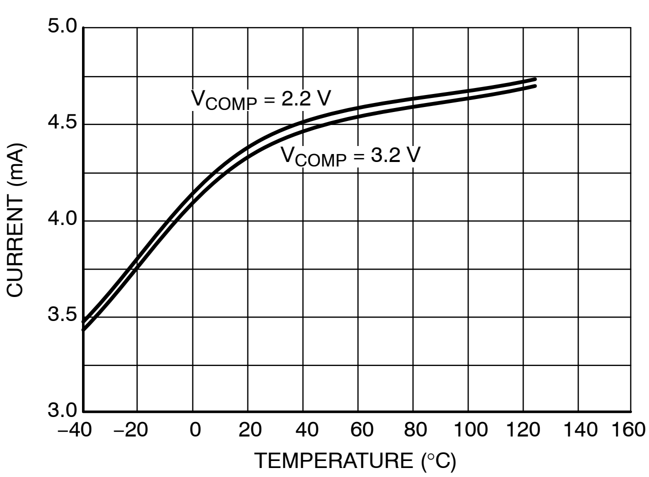


Figure 31. Error Amp Source Current vs. Temperature

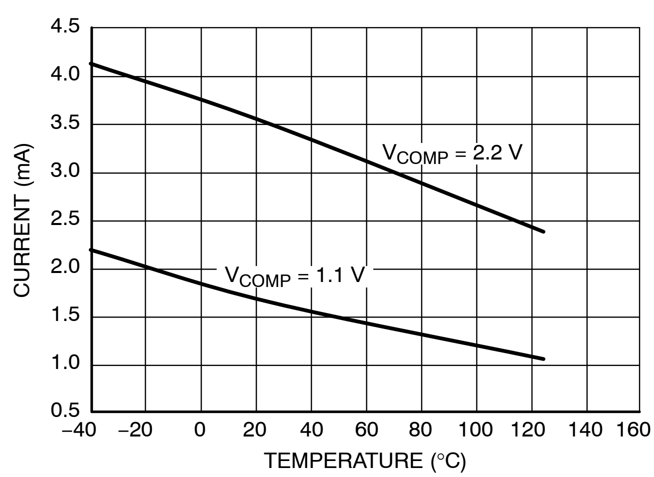


Figure 32. Error Amp Sink Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

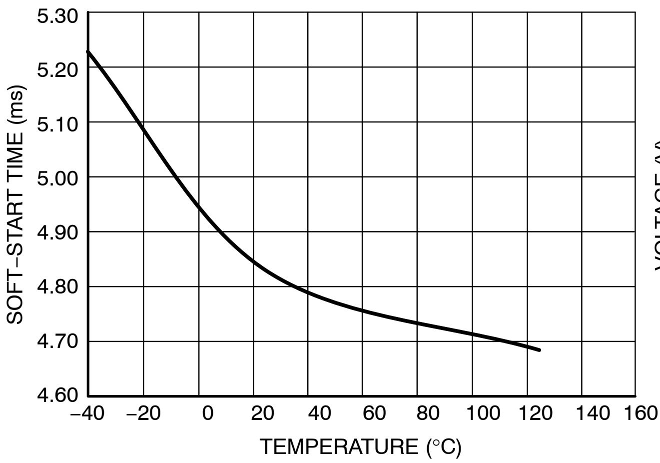


Figure 33. Soft−Start Time vs. Temperature

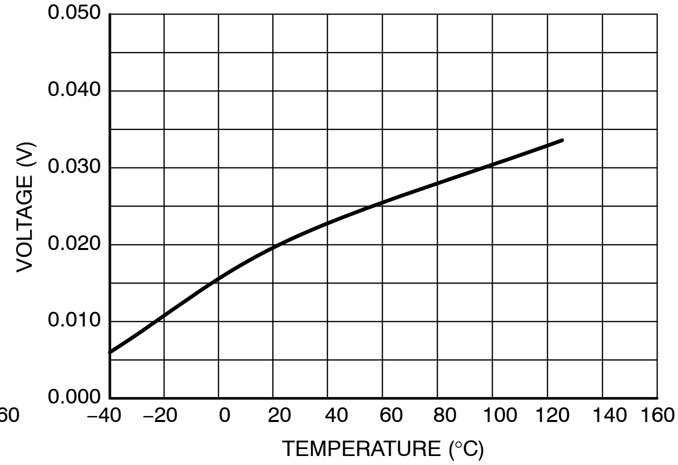


Figure 34. IGNBUF Low Voltage vs. Temperature

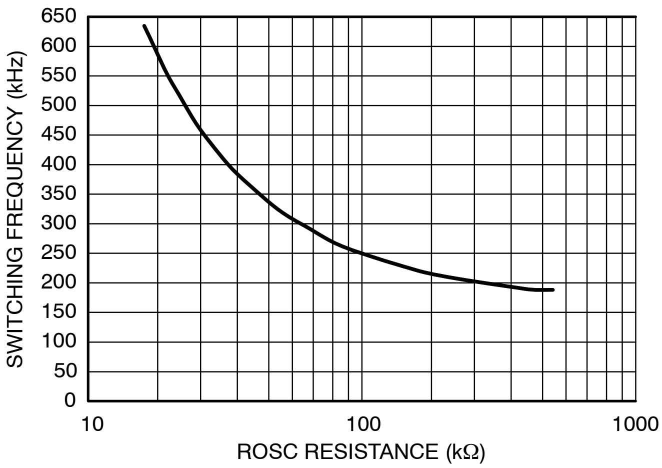


Figure 35. Switching Frequency vs. ROSC Resistance

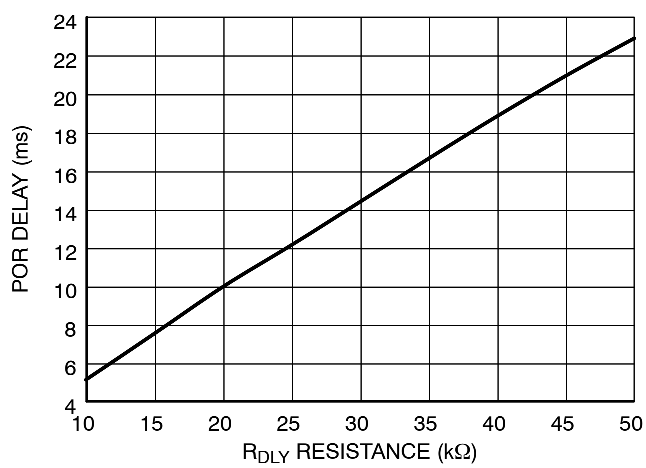


Figure 36. POR Delay vs. R_{DLY} Resistance

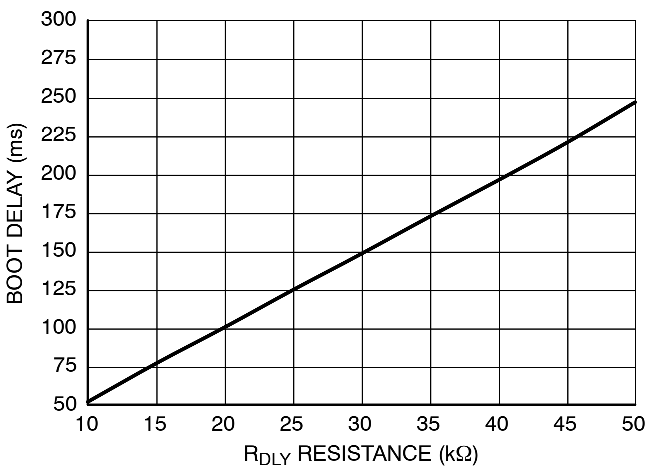


Figure 37. Boot Delay vs. R_{DLY} Resistance

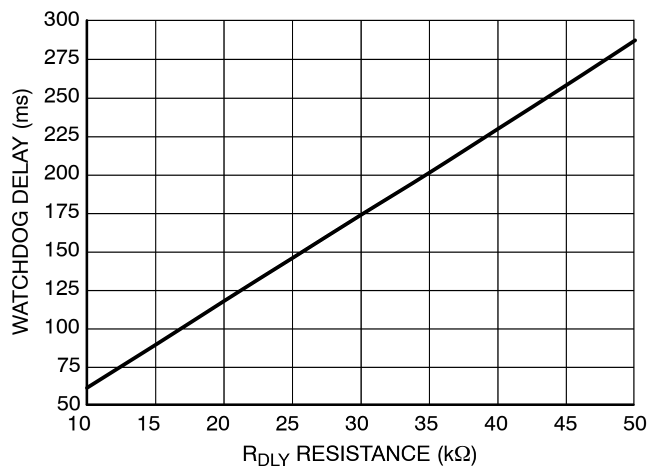


Figure 38. Watchdog Delay vs. R_{DLY} Resistance

TYPICAL PERFORMANCE CHARACTERISTICS

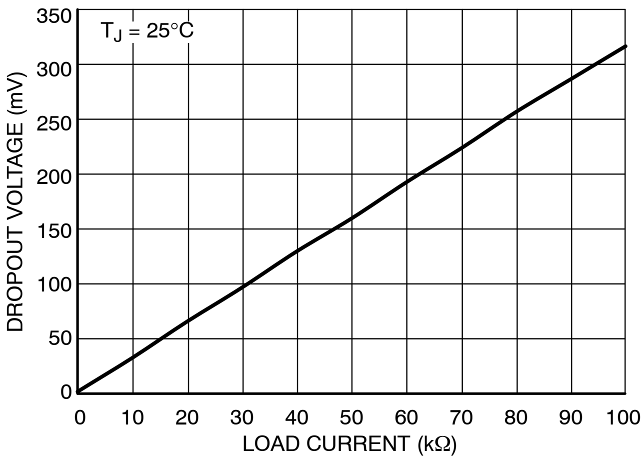


Figure 39. 5P0 Dropout Voltage vs. Load Current

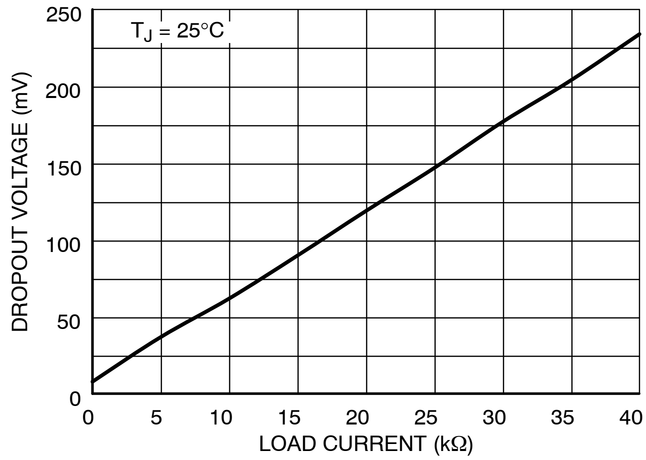


Figure 40. 8P5 Dropout Voltage vs. Load Current

OPERATING DESCRIPTION

INPUT VOLTAGE

VIN is the power supply input for all NCV8881 functions. Prior to the appearance of a valid high at the Enable input (EN pin), VIN voltage above the V_{STRT} threshold produces a low level at the Reset output (RESB).

INPUT UNDERVOLTAGE SHUTDOWN

An Undervoltage Lockout (UVLO) circuit monitors the voltage at the VIN pin. If the voltage is below the V_{STP} threshold it pulls RESB low, inhibits switching, and shuts down the LDOs.

INPUT OVERVOLTAGE SHUTDOWN

If input voltage is above the V_{OVSTP} threshold, RESB is pulled low, switching is inhibited, the Soft−start circuit is reset, and the LDOs are shut off. Upon dropping below the V_{OVSTT} threshold, the LDOs will powerup and the SMPS will begin a soft−start sequence regardless of the state of the EN signal.

STATE DIAGRAM

Figure 41 shows the State Diagram for the NCV8881. States within numbered ellipses have common responses (such as to input overvoltage and high temperature shutdown) which force an exit from all states within.

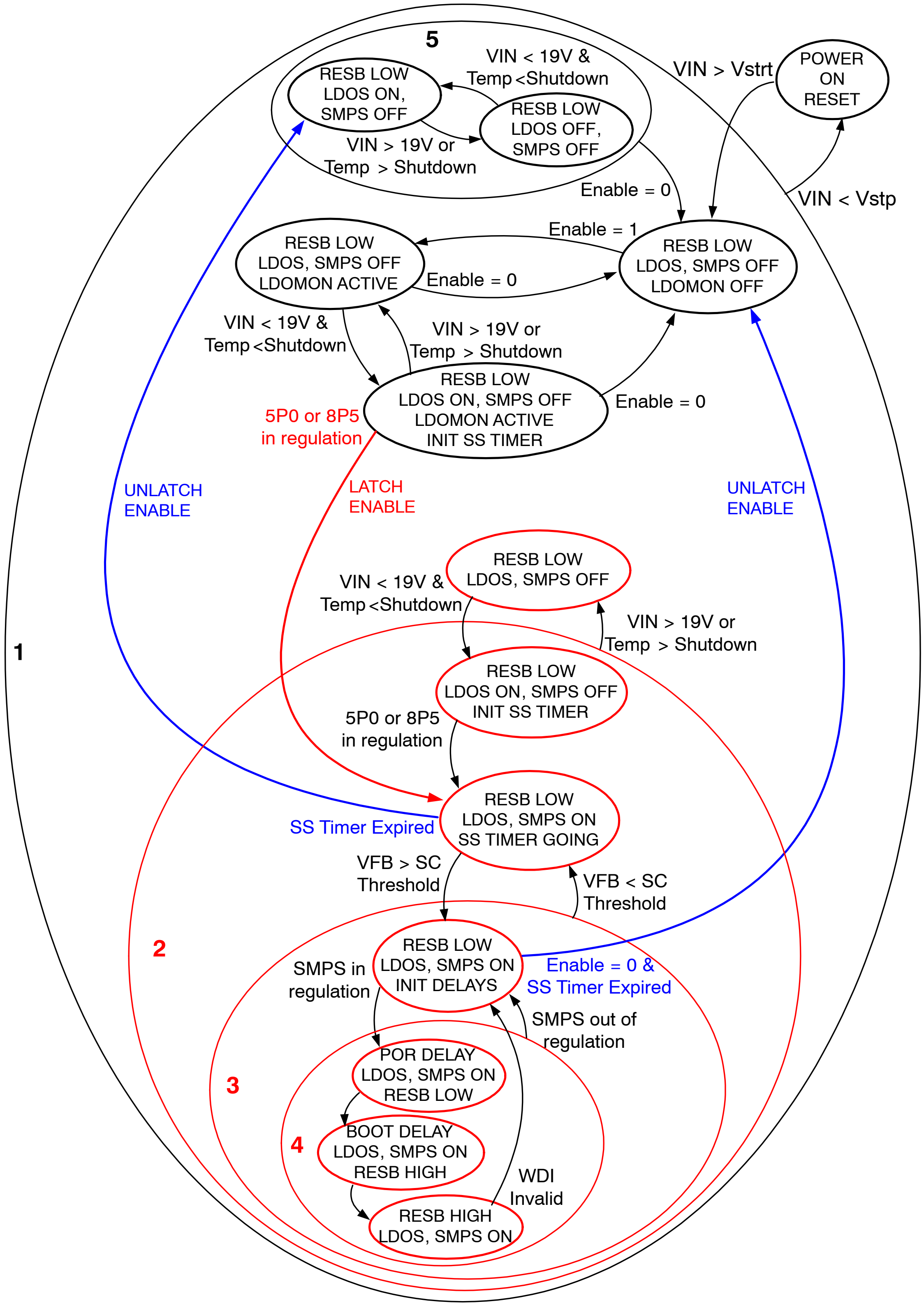


Figure 41. State Diagram

ENABLE (EN PIN)

After VIN rises above V_{STRT}, EN below V_{ENSTHL} will maintain a standby mode which keeps the switching regulator, Watchdog Circuit, and LDO outputs off, and minimizes supply current. In this state the RESB output is low. A high logic level at the EN input activates all functions. Upon EN exceeding V_{ENSTHH}, 5P0 and 8P5 voltages are established, followed by soft−start of the switching regulator. Once either the 5P0 or 8P5 LDO reaches regulation, EN dropping below V_{ENSTHL} has no effect until the SS Timer expires. Thereafter, if the SMPS output voltage is out of regulation, or WDI pulse period exceeds the Watchdog Delay time t_{WD}, EN below V_{ENSTHL} puts the part in standby mode.

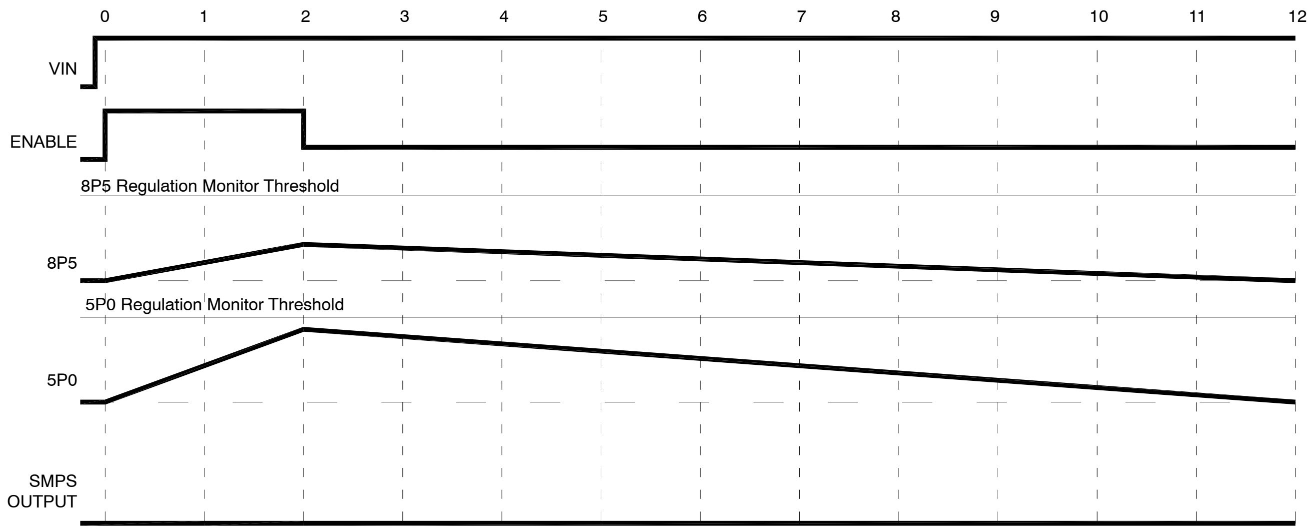


Figure 42. Enable High Time Insufficient to be Latched

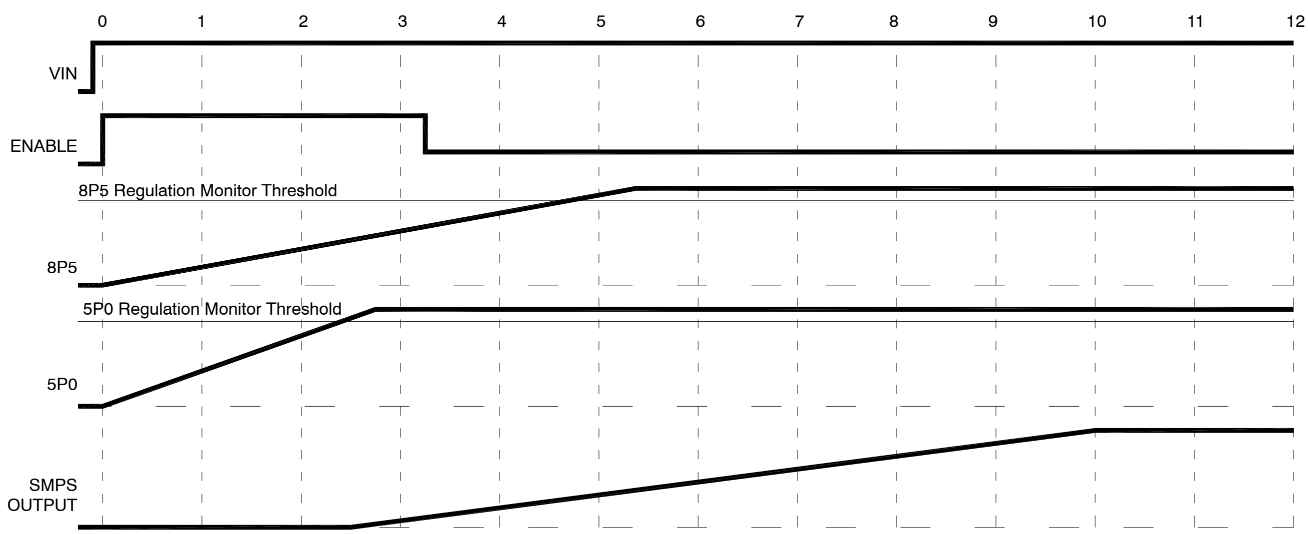


Figure 43. Enable High Time Long Enough to be Latched

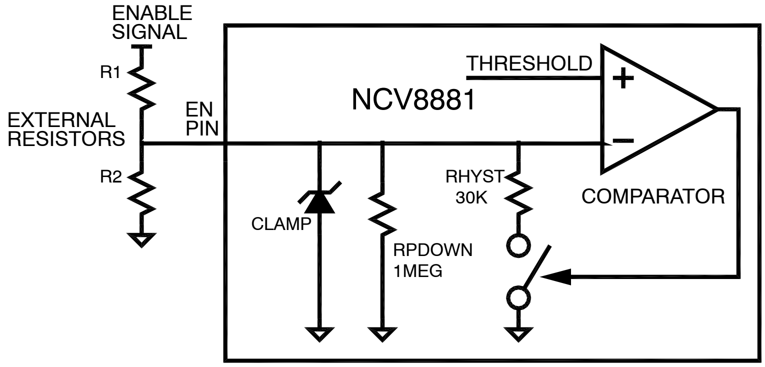


Figure 44. Enable Input Hysteresis Mechanism

When the EN pin is below $\mathbf{V_{ENSTHL}}$, RHYST is in parallel with RPDOWN making the internal resistance from the EN pin to ground lower than when the EN pin is above $\mathbf{V_{ENSTHH}}$. This produces hysteresis in the Enable function when there is resistance between the source of the Enable signal and the EN pin. A resistive divider from the Enable signal source to the EN pin (**Figure 44**) allows a wide range of activation/deactivation voltages. Note that this divider is also used in conjunction with an internal zener clamp to keep the EN pin voltage below the maximum voltage rating when battery is the enable signal. Given the lowest voltage that must enable the part $\mathbf{VIH_{MIN}}$, and the highest voltage that must disable the part $\mathbf{VIL_{MAX}}$ the divider resistor values are:

$R1 = 0.7874 * (\mathbf{VIL_{MAX}} - 1.27)/(0.0005556 * 1/R2)$ [kΩ] [R2 in kΩ]

$R2 = 1800*(1.2283 * \mathbf{VIL_{MAX}} - \mathbf{VIH_{MIN}})/(\mathbf{VIH_{MIN}} - 86.823 * \mathbf{VIL_{MAX}} + 108.7)$ [kΩ]

Minimum hysteresis is: 0.0415 * R1 [V] [R1 in kΩ]

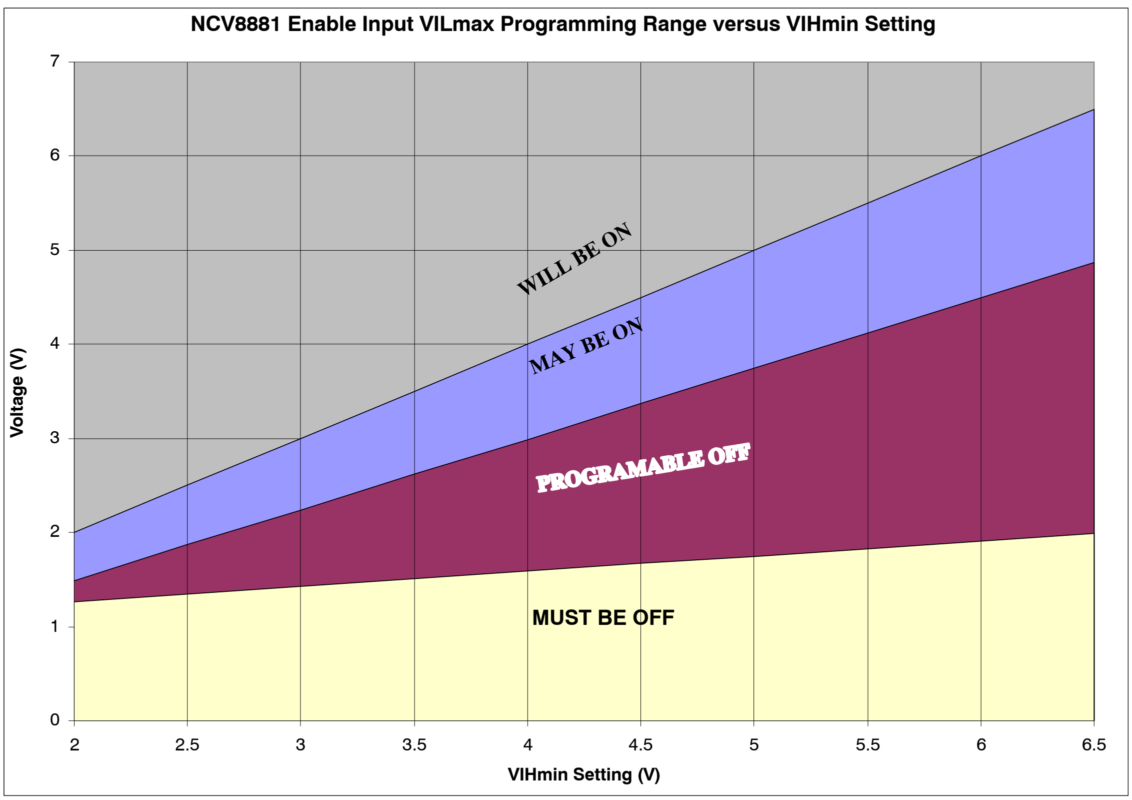


Figure 45. Enable Input VILmax Programming Range versus VIH_{min} Setting

IGNITION BUFFER

The Ignition Buffer output IGNBUF reports the EN pin voltage level (high or low) detected by the EN input circuitry when the EN signal is latched. The NCV8881 will pull the IGNBUF output low if the Enable signal is low, and release the IGNBUF output if the Enable signal is high. The IGNBUF output is an open drain device which requires an external pullup resistor to a logic supply. IGNBUF is no longer controlled by EN when EN transitions low if the EN signal is not latched.

THERMAL SHUTDOWN

A thermal shutdown circuit will inhibit switching, reset the Soft−start circuit, and power down the 5P0 and 8P5 outputs if internal die temperature exceeds a safe level. Operation is automatically restored when die temperature has dropped below the thermal restart threshold regardless of the state of the EN signal.

5P0 OUTPUT

CURRENT LIMIT

5P0 output current is limited above the specified output current capability in order to limit inrush current at turn−on and also minimize power dissipation in the event of an output short circuit.

OUTPUT UNDERVOLTAGE MONITOR

Either the 5P0 output voltage must exceed V_{5UVSTT} or the 8P5 output voltage must exceed V_{8UVSTT} before the SMPS will begin soft−start. If the output is below V_{5UVSTP}, the LDOMON output will be pulled low.

STABILITY CONSIDERATIONS

The output capacitor helps determine three main performance characteristics of a linear regulator: starting delay, load transient response, and loop stability. The optimum capacitor type and value will depend on these three characteristics, as well as cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, and ceramic are all acceptable capacitor types for most applications. Values of 1 μF or more work in many cases, however attention must be paid to the Equivalent Series Resistance (ESR). Aluminum electrolytic capacitors are the least expensive solution but both the value and ESR of this type of capacitor change considerably at low temperatures (−25°C or −40°C). The capacitor manufacturer’s data sheet must be consulted for this information. Stability under all load and temperature conditions is guaranteed by a capacitor value greater than or equal to 4.7 μF and ESR between 0.2 and 5 Ω.

Besides powering external loads, the 5P0 output can be used to provide a regulated voltage to an ROSC pullup resistor as a convenient way to decrease the factory−set switching frequency.

8P5 OUTPUT

The regulated voltage provided by the 8P5 output is used to power the internal gate drive circuitry, but can also provide current to modest external circuit loads that can tolerate significant spike noise at the SMPS switching frequency.

CURRENT LIMIT

8P5 output current is limited above the specified output current capability in order to limit inrush current at turn−on and also minimize power dissipation in the event of an output short circuit.

OUTPUT UNDERVOLTAGE MONITOR

Either the 8P5 output voltage must exceed V_{8UVSTT} or the 5P0 output voltage must exceed V_{5UVSTT} before the SMPS will begin soft−start. The LDOMON output will be pulled low if the 8P5 output voltage is below V_{8UVSTP}.

OUTPUT OVERVOLTAGE CLAMP

If current is forced into the 8P5 output, a clamp will limit the voltage in order to protect the gate driver circuit from excessive voltage.

STABILITY CONSIDERATIONS

The output capacitor helps determine three main performance characteristics of a linear regulator: starting delay, load transient response, and loop stability. The optimum capacitor type and value will depend on these three characteristics, as well as cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, and ceramic are all acceptable capacitor types for most applications. Values of 1 μF or more work in many cases, however attention must be paid to the Equivalent Series Resistance (ESR). Aluminum electrolytic capacitors are the least expensive solution but both the value and ESR of this type of capacitor change considerably at low temperatures (−25°C or −40°C). The capacitor manufacturer’s data sheet must be consulted for this information. Stability under all load and temperature conditions is guaranteed by a capacitor value greater than or equal to 4.7 μF and ESR between 0.2 Ω and 5 Ω.

SMPS OPERATION

LDO OUTPUT UNDERVOLTAGE MONITOR

Besides requiring the input voltage to be above $\mathbf{V_{STRT}}$ and the EN input to be above $\mathbf{V_{ENSTHH}}$, either the 5P0 output voltage must exceed V_{5UVSTT} or the 8P5 output voltage must exceed V_{8UVSTT} before the SMPS will begin soft−start.

SOFT−START

Upon being enabled and released from all fault conditions, and after one of the LDO outputs reaches regulation, a soft−start circuit slowly raises the switching regulator error amplifier reference to V_{FBR} in order to avoid overloading the input supply.

VOLTAGE REFERENCE

An internal, temperature compensated Bandgap voltage reference provides the SMPS Error Amplifier and the 5P0 and 8P5 linear regulators with a stable, precision reference voltage.

SMPS ERROR AMPLIFIER

The error amplifier is an operational amplifier. The Voltage Mode control method employed by the NCV8881 requires Type III compensation for optimum regulator response to load and line transients.

The output voltage of the error amplifier controls the duty cycle of the power switch by controlling the moment at which the power switch shuts off (power switch turn−ons occur at a fixed rate).

SMPS OSCILLATOR

With no connections to the ROSC or SYNC pins, the NCV8881 switching frequency will be the factory−set default frequency f_{OSC} of the internal oscillator.

ROSC SMPS FREQUENCY CONTROL

Connection of a resistor between the ROSC pin and ground will raise the switching frequency above the factory−set default according to the following equation.

$$F_{SW} = 6840 \times R_{ROSC}^{-0.97} + 170$$

Connection of a resistor between the ROSC pin and 5P0 will lower the switching frequency below the default. The programmed switching frequency should be no higher than the highest synchronization frequency if synchronization is used.

SMPS SYNCHRONIZATION

Applying a clock signal to the SYNC pin will cause power switch turn−on edges to coincide with rising edges of the applied clock signal. When synchronization will be significantly higher than the default frequency, an ROSC resistor which sets the internal oscillator frequency at (but no higher than) the synchronization frequency can be used to maintain the switching frequency approximately the same as the synchronization frequency in the absence of the SYNC signal.

Besides controlling the switching frequency, the ROSC resistor controls the internal ramp slope, and can be used to adjust the gain of the pulse width modulator.

A steady low or high SYNC input will restore SMPS operation to the factory−set default or ROSC programmed frequency after the De−synchronization delay.

OUTPUT VOLTAGE REGULATION MONITOR

When the FB voltage is below V_{FBMONL}, RESB is pulled low, and the POR, BOOT and Watchdog Delays are initialized. When FB voltage exceeds V_{FBMONH} the POR Delay begins to time out. If, when the FB voltage is below V_{FBMONL}, the Soft−Start Timer has expired and the EN input is low, the NCV8881 will completely shut off (see Figures 46 through 48).

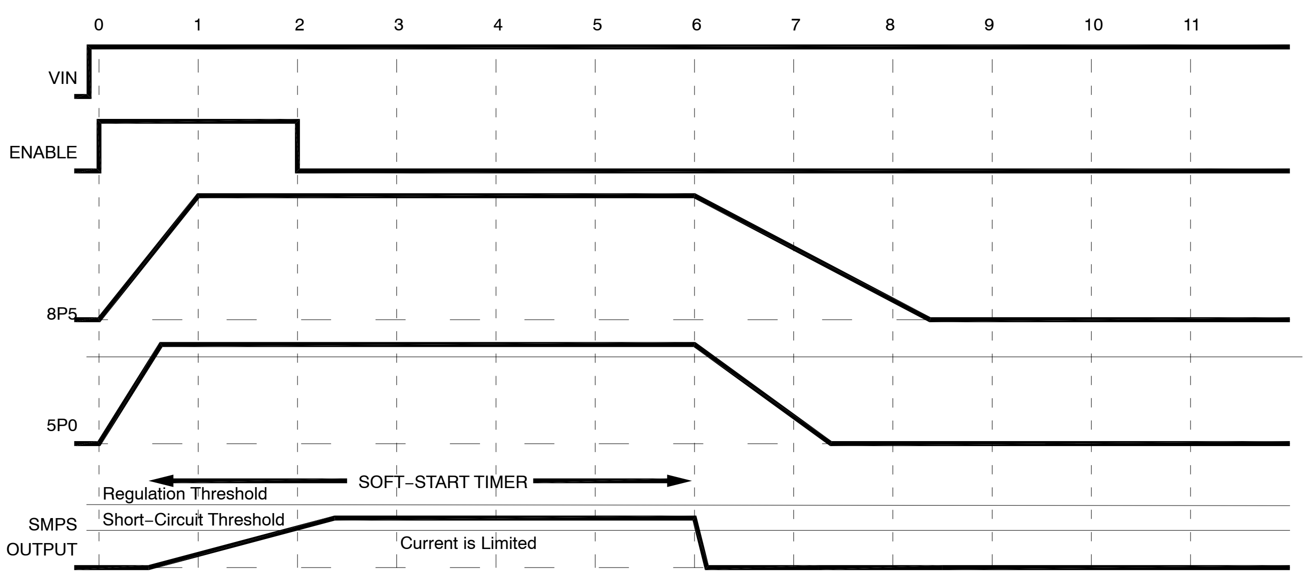


Figure 46. SMPS Overload During Startup

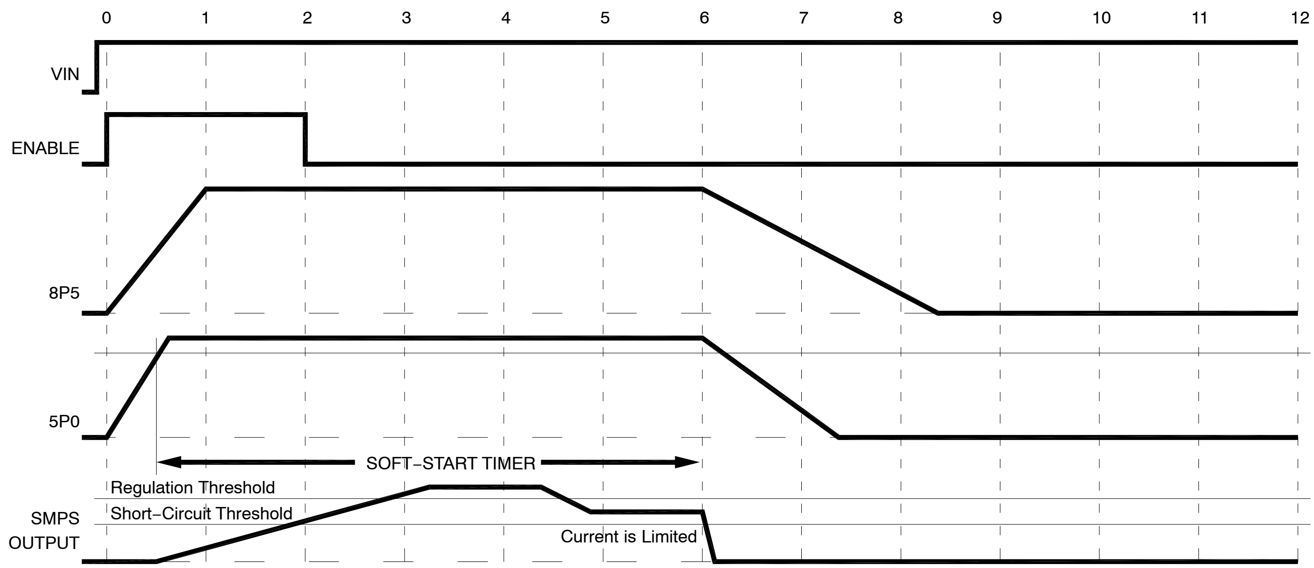


Figure 47. SMPS Overload after Successful Startup #1

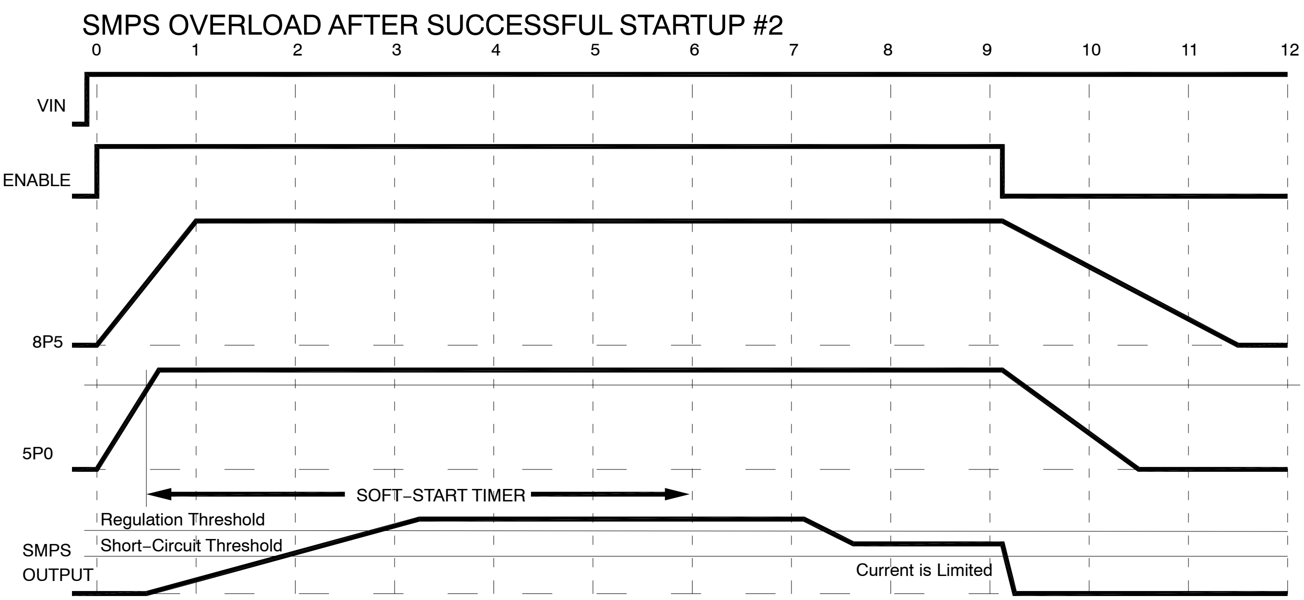


Figure 48. SMPS Overload after Successful Startup #2

SMPS CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

Every cycle, the power switch will be shut off if switch current exceeds the internal, fixed, current limit. After the Soft−Start Timer has expired, an extreme overload is prevented from producing switch current in excess of the current limit by detecting excessively low voltage at the FB pin and latching the SMPS regulator off. Toggling the EN input low then high, or cycling input voltage off and on is required to restart the SMPS (see bubble 5 of Figure 41, and Figures 49 − 51).

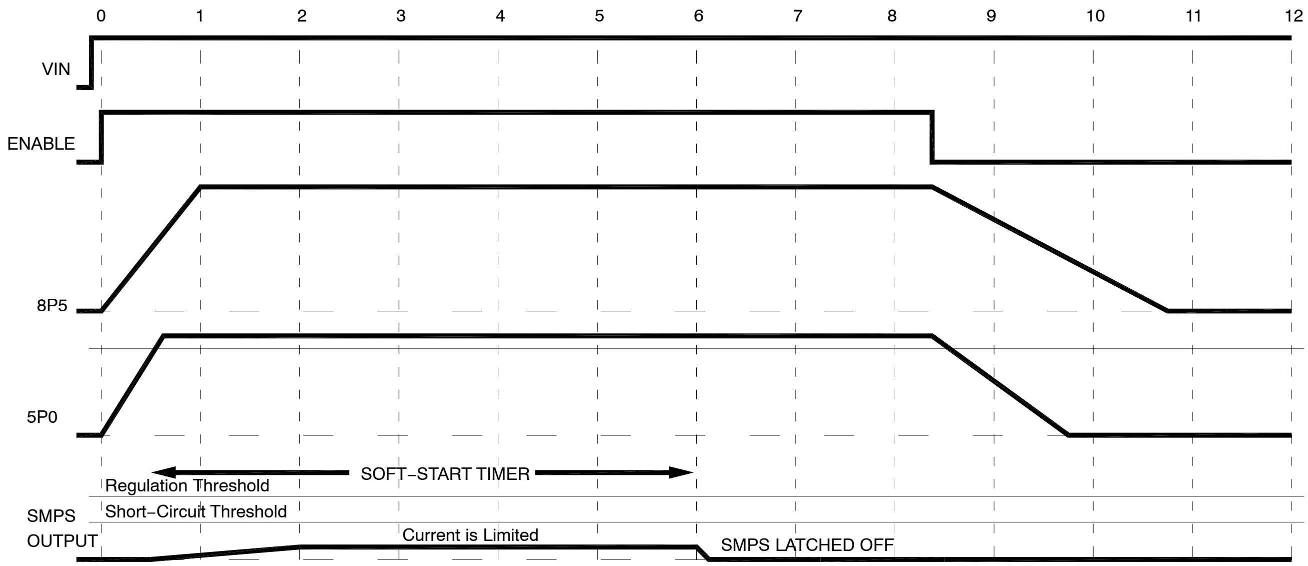


Figure 49. SMPS Short−Circuit during Startup

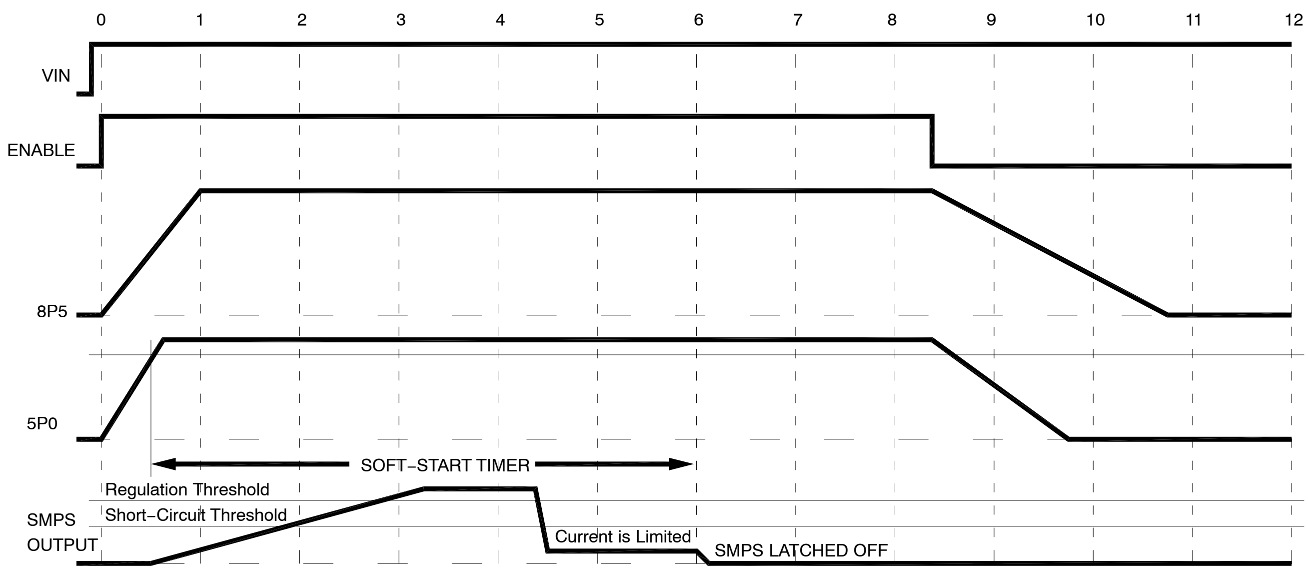


Figure 50. SMPS Short−Circuit after Successful Startup #1

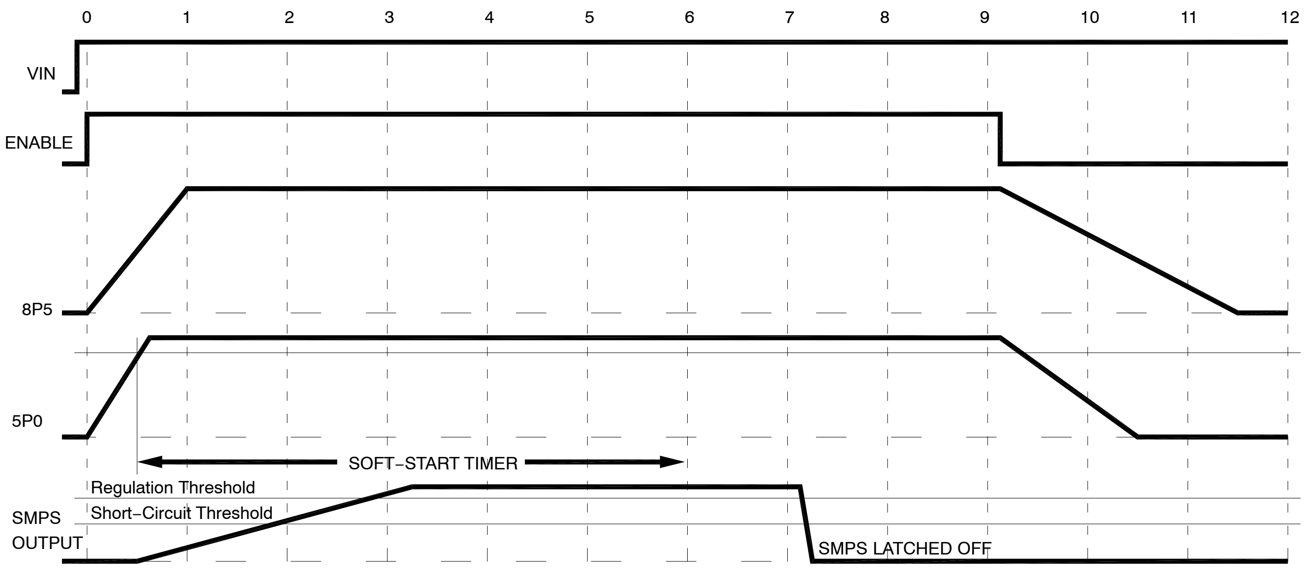


Figure 51. SMPS Short−Circuit After Successful Startup #2

WATCHDOG

WATCHDOG FUNCTION

The Watchdog function monitors the WDI input to check that WDI pulses arrive more frequently than the programmed minimum rate. Monitoring commences after two sequential time periods (the POR and BOOT Delays) which start when the SMPS output reaches regulation. After these initial time periods, time between WDI falling edges exceeding the Watchdog Delay indicates abnormal microcontroller activity, and the NCV8881 responds by pulling the open drain RESB output low. A single external resistor from the RDLY pin to ground programs the POR, BOOT and Watchdog Delays.

When enabled and upon the SMPS output reaching regulation, the NCV8881 enters the POR Delay period $\mathbf{t_{POR}}$, during which the RESB pin is held low. When the POR Delay expires, the NCV8881 enters the BOOT Delay period $\mathbf{t_{BD}}$ during which the RESB output is allowed to be pulled up by the external resistance. When the BOOT Delay expires, the Watchdog circuit begins monitoring the WDI pin for a falling edge (from a microprocessor or other signal source). If a falling edge arrives before the Watchdog Delay period $\mathbf{t_{WD}}$ expires, RESB remains high and a new Watchdog Delay period is initiated. Otherwise the NCV8881 enters another POR Delay period and the RESB pin is pulled low, while the SMPS and LDO outputs continue to regulate. If EN is low when the Watchdog Delay expires (no falling edge has occurred at the WDI input), RESB is pulled low and the NCV8881 shuts off all power outputs (SMPS and LDOs) and minimizes supply current.

In order to ensure that WDI pulses keep RESB from being pulled low, they must never occur further apart than the **minimum** specified $\mathbf{t_{WD}}$. However, RESB is not guaranteed to be pulled low unless pulses occur further apart than the **maximum** specified $\mathbf{t_{WD}}$.

Removal of other conditions that cause RESB to go low ($V_{IN} > V_{OVSTP}$, temperature > T_{TSD}, and SMPS output voltage low) also initiate POR and BOOT Delays prior to resumption of WDI monitoring.

Figures 52 through 57 illustrate the action of RESB and the POR, BOOT, and Watchdog Delays during start−up and shutdown.

The Watchdog Delay is internally limited to a maximum value proportional to the switching period in case the resistance at the RDLY pin becomes excessively high, such as would occur if the path from the RDLY pin through the RDLY resistance becomes an open circuit.

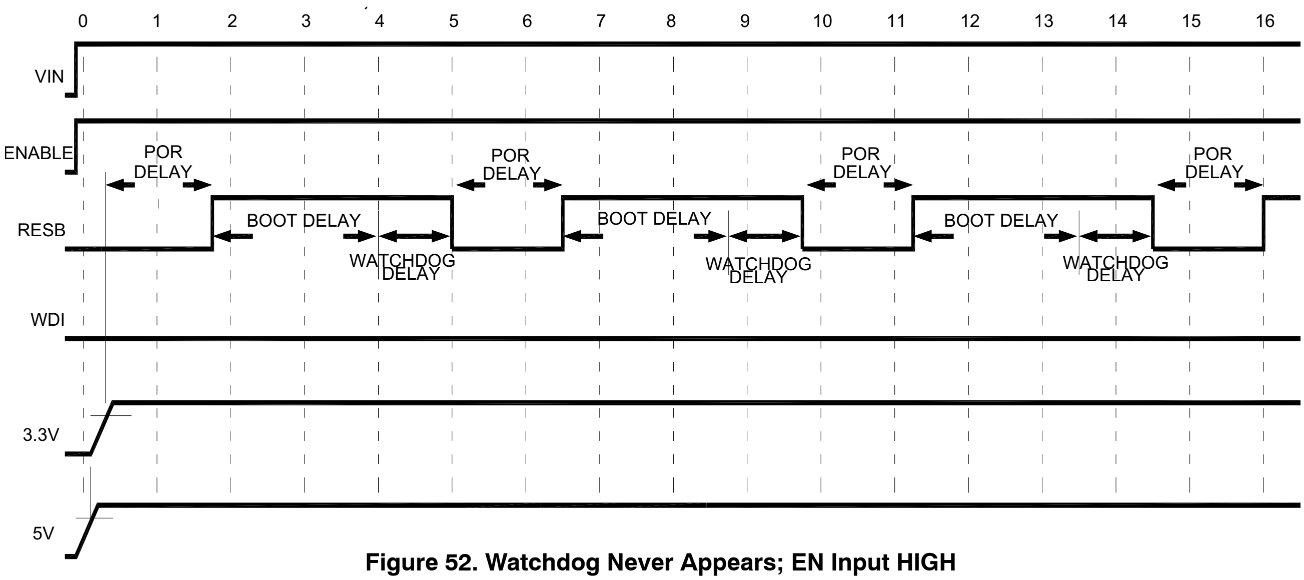


Figure 52. Watchdog Never Appears; EN Input HIGH

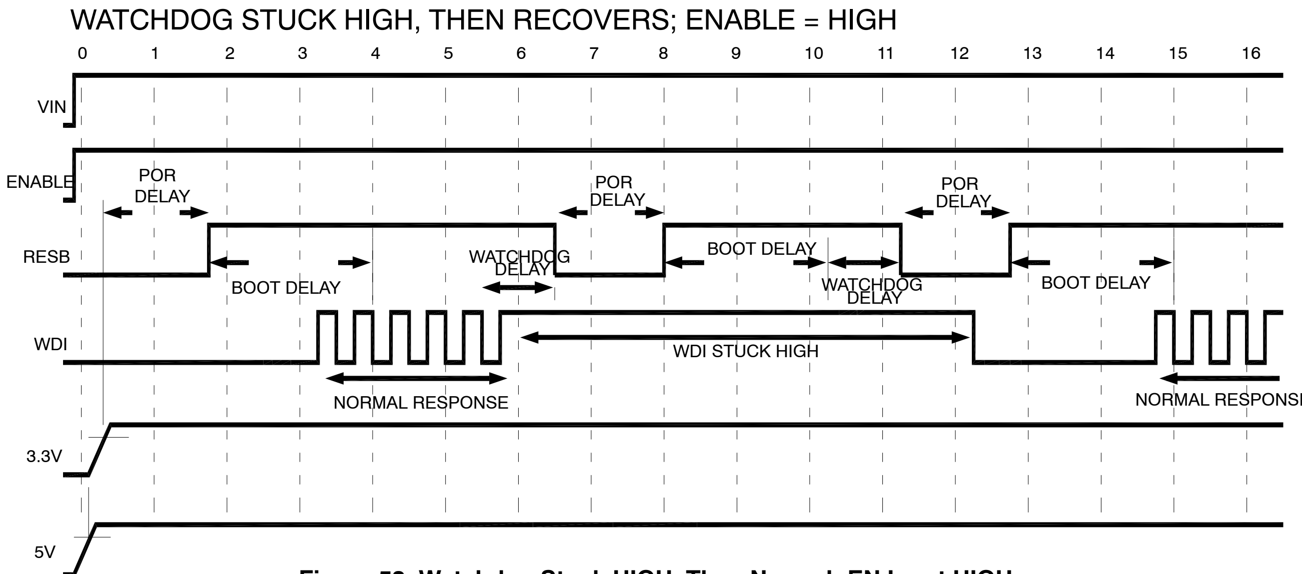


Figure 53. Watchdog Stuck HIGH, Then Normal; EN Input HIGH

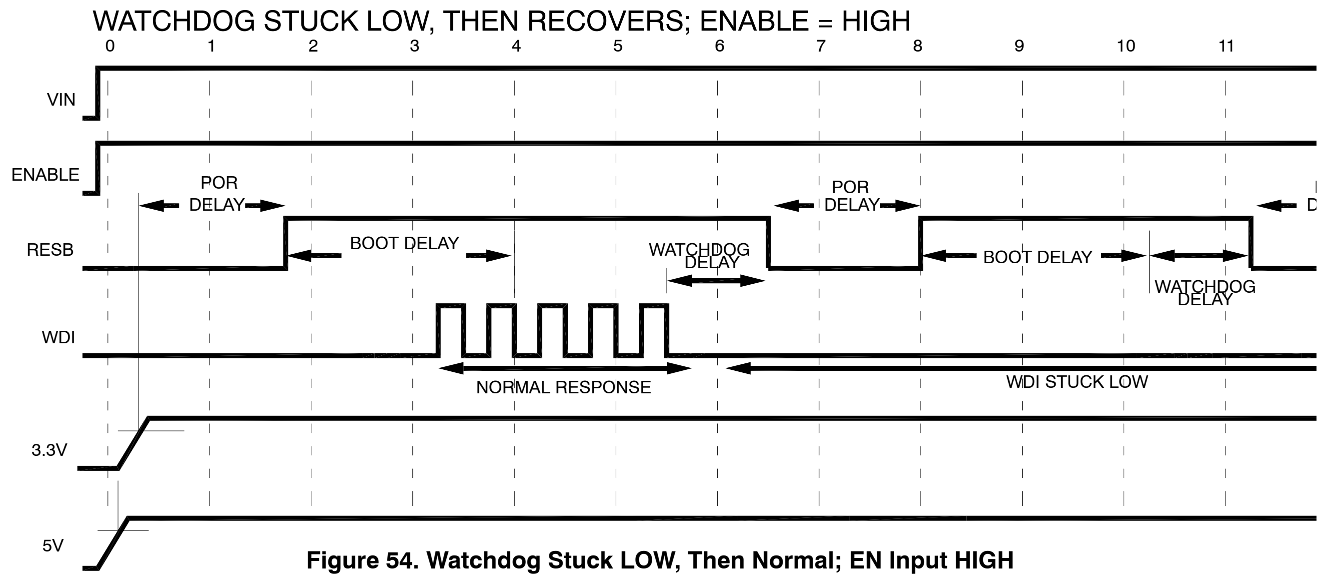


Figure 54. Watchdog Stuck LOW, Then Normal; EN Input HIGH

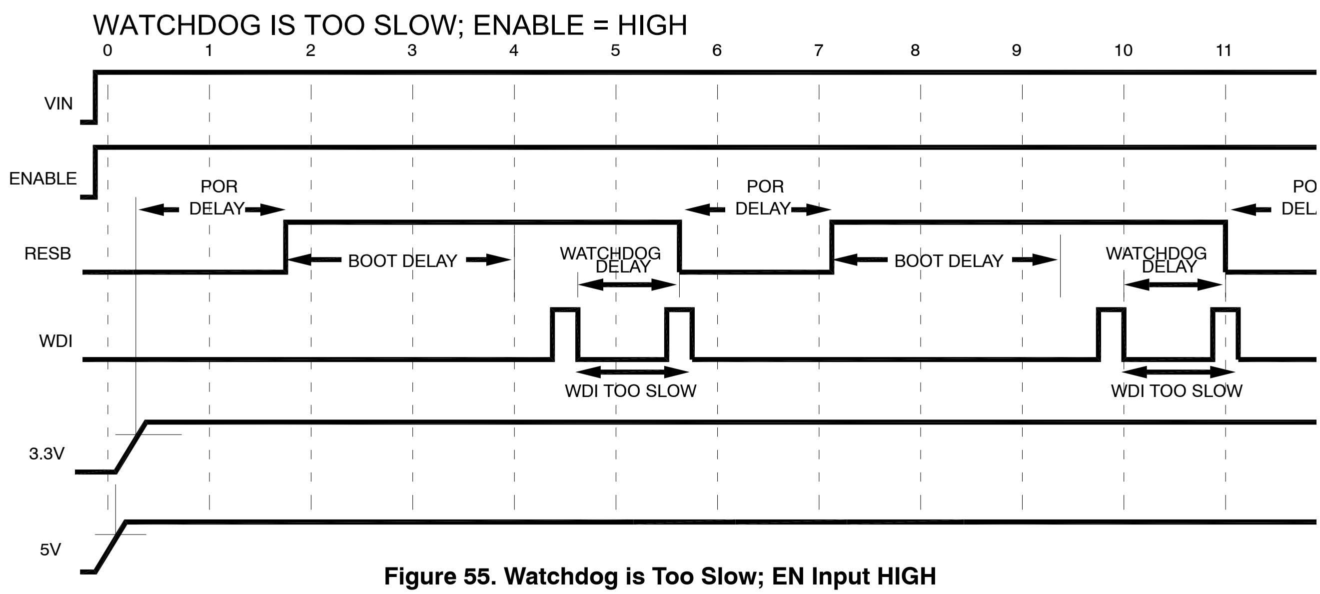


Figure 55. Watchdog is Too Slow; EN Input HIGH

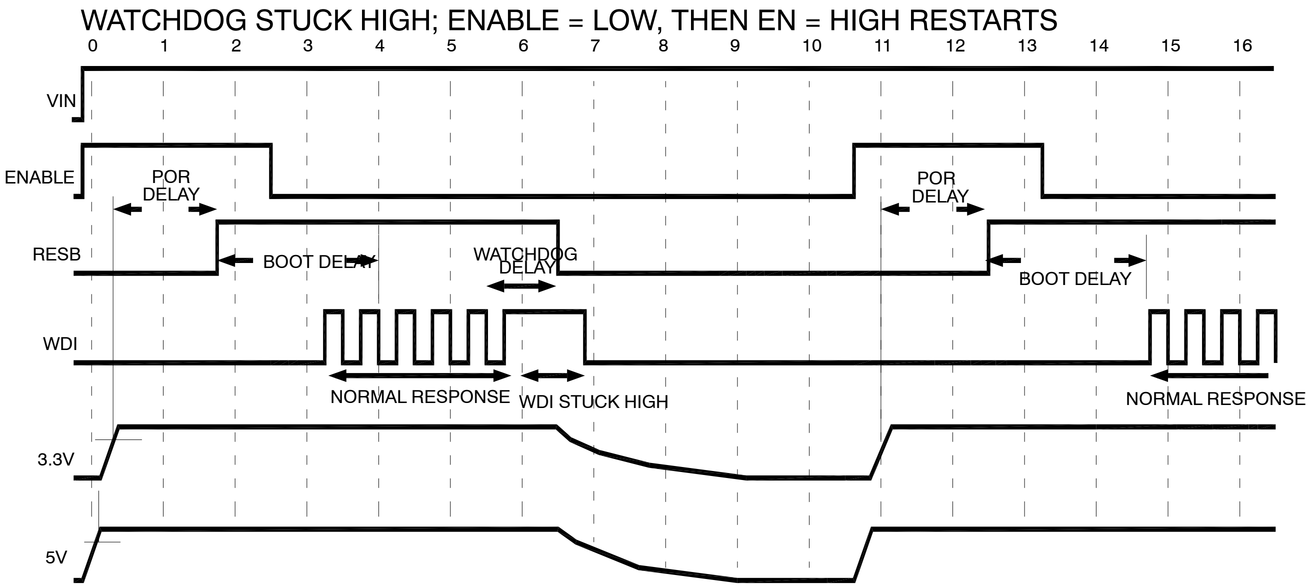


Figure 56. Watchdog Stuck HIGH, EN Input LOW; then EN Goes HIGH to Restart the Regulators

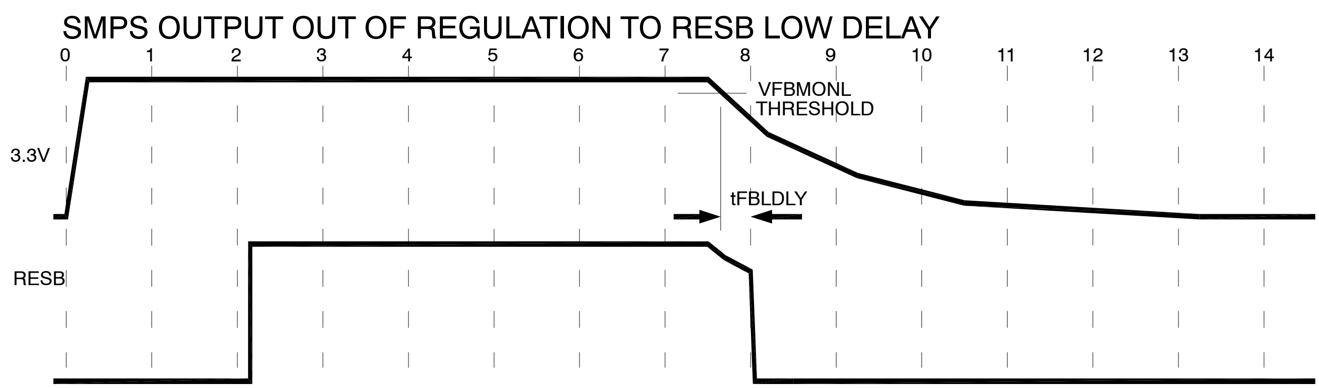


Figure 57. RESB Pulled Low as the SMPS Output Voltage (pullup source for RESB) Drops Out of Regulation

APPLICATION INFORMATION

Input Capacitors

The primary input capacitor should be a ceramic of at least 4.7 μF placed between the VIN pin and the ground terminal of the SMPS freewheeling diode in order to reduce input voltage perturbations present when the NCV8881 SMPS is heavily loaded. A secondary 0.1 μF ceramic capacitor positioned as closely as possible between the VIN and GND pins of the NCV8881 provides greater reduction of input perturbations than further increasing the value of the primary ceramic capacitor, and can be more effectively positioned than the larger 4.7 μF capacitor without compromising PCB thermal conductivity.

LDO Output Capacitor Selection

The LDOs have been compensated to work with output capacitors above 3.3 μF having an ESR from 200 mΩ up to 5 Ω over the full range of output current and temperature. Lower capacitance and ESR can be used for lighter load requirements. Tantalum, Aluminum or Polymer Electrolytic, capacitors can be used. Ceramic capacitors should have series resistance added to be within the recommended ESR range. There are many capacitor vendors which supply automotive rated parts that fall within these ranges. For example, the SUNCON EP−series Aluminum Electrolytic capacitors are well suited well for automotive radio applications.

Setting the SMPS Output Voltage

To set the output voltage of the switching regulator, use the following equation:

$$V_{SWOUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \qquad \text{(eq. 1)}$$

where V_{REF} is the Reference voltage, R1 is the resistor connected from V_{SWOUT} to the FB pin and R2 is the resistor connected from the FB pin to ground. To reduce the effect of input offset current error, it is customary to calculate R1 with R2 set at 1 kΩ.

SMPS Snubber

A resistor and ceramic capacitor must be connected in series between the SW pin and ground. Typical values are 10 Ω and 1 nF.

SMPS Freewheeling Diode Selection

The freewheeling diode in the SMPS provides the inductor current path when the power switch turns off, and is sometimes referred to as the commutation diode. The diode peak inverse voltage must exceed the maximum operating input voltage in order to accommodate any higher peak voltage produced by switchnode ringing. The peak conducting current is determined by the internal current limit. The average diode current can be calculated from the output current I_{OUT}, the input voltage V_{IN} and the output voltage V_{SWOUT} by:

$$I_{D(avg)} = I_{OUT} \times \left(1 - \frac{V_{SWOUT}}{V_{IN}}\right) \qquad \text{(eq. 2)}$$

The freewheeling diode should have a current rating equal to the maximum NCV8881 current limit, such as the MBRA340T3.

Inductor Selection

Mechanical and electrical considerations, as well as cost influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in SMPS system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, smaller inductor values correspond to faster transient response. The maximum current slew rate through the output inductor for a buck regulator is given by:

$$\text{Inductor Slew Rate} = \frac{dI_L}{dt} = \frac{V_L}{L} \qquad \text{(eq. 3)}$$

Where I_L is the inductor current, L is the output inductance, and V_L is the voltage drop across the inductor.

This equation indicates that larger inductor values limit the regulator’s ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply sufficient charge to maintain regulation while the inductor current “catches up” to the load. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator’s maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current.

In continuous conduction mode, the peak−to−peak ripple current is calculated using the following equation:

$$I_{PP} = T_{SW} \times \frac{V_{SWOUT}}{L} \times \left(1 - \frac{V_{SWOUT}}{V_{IN}}\right) \qquad \text{(eq. 4)}$$

Where T_{SW} is the switching period. From this equation it is clear that the ripple current increases as L decreases, emphasizing the trade−off between dynamic response and ripple current. For most applications, the inductor value falls in the range between 10 μH and 22 μH. There are many magnetic component suppliers providing energy storage inductor product lines suitable such as the Wurth TPC series or TOKO DSH104C series inductors, which are recommended for the automotive radio applications.

SMPS Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, it supplies the current to the load for first few microseconds, where after the controller recognizes the load transient and proceeds to increase the duty cycle. Neglecting the effect of the ESL, the output voltage has a first drop due to the ESR of the capacitor.

$$\Delta V_{SWOUT(ESR)} = \Delta I_{SWOUT} \times ESR \qquad \text{(eq. 5)}$$

A lower ESR produces a lower ΔV during load transient. In addition, a lower ESR produces a lower output voltage ripple. The voltage drop due to the output capacitance discharge can be approximated using the following equation:

$$\Delta V_{SWOUT(CHARGE)} = \frac{\left(\Delta I_{SWOUT}\right)^2 \times L}{2 \times C_{SWOUT} \times \left(V_{IN(MIN)} \times D_{MAX} - V_{SWOUT}\right)} \qquad \text{(eq. 6)}$$

Where, D_{MAX} is the maximum duty cycle value, which is 90%. Although the ESR effect is not in phase with the discharging of the output voltage, $\Delta V_{SWOUT(ESR)}$ can be added to $\Delta V_{SWOUT(CHARGE)}$ to give a rough indication of the maximum ΔV_{SWOUT} during a transient condition. Simulation can also help determine the maximum ΔV_{SWOUT}; however, it will ultimately have to be verified with the actual load since the ESL effect is dependent on layout and the actual load’s di/dt.

SMPS Input Capacitor Selection

Besides voltage rating, a primary consideration for selecting the input capacitor is input RMS current rating.

$$I_{IN(RMS)} = D \times \left((1 - D) \times I_{SWOUT} + \sqrt{(1 - D)^2 \times I_{SWOUT}{}^2 + \frac{\left((1 - D) \times \frac{T_{SW} \times (V_{SWOUT} + V_F)}{L} \right)^2}{12}} \right) \quad \text{(eq. 7)}$$

Where D is the Duty Cycle = $t_{ON}/(t_{ON}+t_{OFF})$, and V_F is the forward voltage of the freewheeling diode.

Another consideration for the value of the input capacitor is the ability to supply enough input charge to satisfy sudden increases in output current (such as produced at start−up, or upon maximum load step) without an unacceptable drop in input voltage. This is sometimes important when the input voltage initially rises past the Undervoltage Lockout threshold.

SMPS Compensation

The NCV8855 utilizes voltage mode control. The control loop regulates V_{SWOUT} by monitoring it and controlling the power switch duty cycle. Inherent with all voltage−mode control loops is a compensation network.

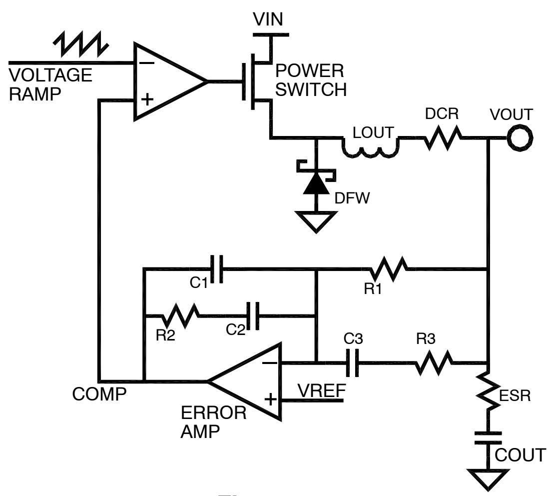


Figure 58.

The compensation network consists of the internal error amplifier and the impedance networks Z_{IN} (R1, R3 and C3) and Z_{FB} (R2, C1 and C2). The compensation network has to provide a loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions to minimize the load regulation. The open-loop gain magnitude versus frequency plot of a stable control loop crosses zero dB with close to −20 dB/decade slope and a phase margin greater than 45°.

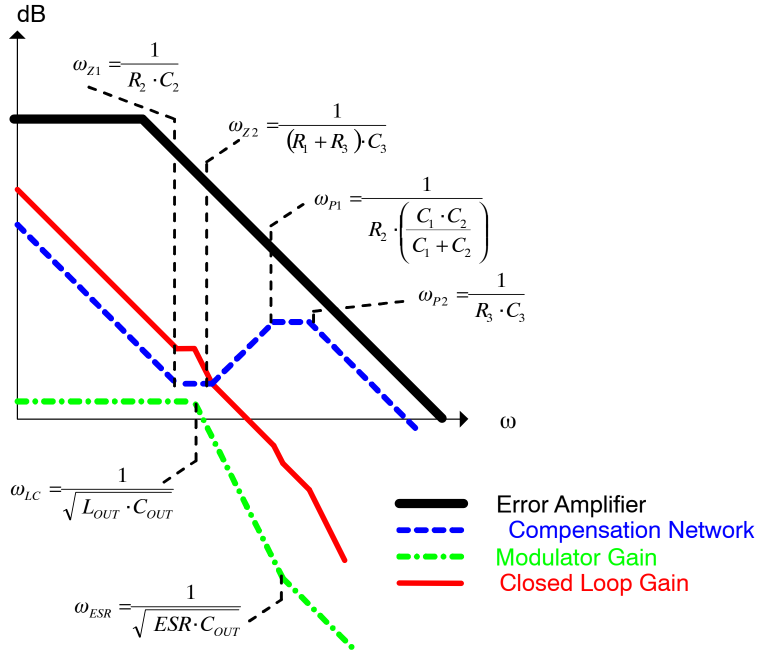


Figure 59.

To reiterate, there are 3 primary goals to compensating. Goal 1 is to have a high a unity gain bandwidth (UGB) that is greater than 1/10 the switching frequency F_{SW}, but less than 1/2 the switching frequency. UGB is also known as the crossover frequency. This is the point where the loop gain = 0 dB or a gain of 1. In the plot above, the UGB is the point where the red line crosses the TBD axis. Goal 2 is to have the loop gain cross 0 dB with a −20 dB/decade slope also known as a −1 slope. Goal 3 is to achieve over 45° of phase margin when the gain crosses 0 dB. These are just goals. Sometimes the crossover frequency is reduced below 1/10 F_{SW} in order to meet goal 3.

Conversely, some designs will push the crossover frequency as high as it can (as long as it is below 1/2 F_{SW}) with a reduced phase margin of 30° in order to get a faster transient response. The only two absolutes are that the crossover frequency cannot exceed 1/2 F_{SW} and the phase margin has to be greater than 0° at crossover. However, a SMPS operating towards these absolutes will experience severe ringing before it dampens out.

To achieve the above goals, the following guidelines should be adopted.

- Place ω_{Z1} at half the resonance of ω_{LC}
- Place ω_{Z2} at or around ω_{LC}
- Place ω_{P1} at ω_{ESR}
- Place ω_{P2} at half the switching frequency

Performing these calculations will take some amount of iteration and bench testing is needed to verify results. ON Semiconductor has developed a tool to speed up the design process tremendously with great ease and accuracy. This tool can be downloaded by following the link below: http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP

ORDERING INFORMATION

Device	Package	Shipping†
NCV8881PWR2G	SOIC−16W EP (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ADDITIONAL INFORMATION

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