19-4668; Rev 1; 12/09

Low-Power, Active Energy, Polyphase AFE

General Description

The MAXQ3181 is a dedicated electricity measurement front-end that collects and calculates polyphase voltage, current, active power and energy, and many other metering parameters of a polyphase load. The computed results can be retrieved by an external master through the on-chip serial peripheral interface (SPI™) bus. This bus is also used by the external master to configure the operation of the MAXQ3181 and monitor the status of operations.

The MAXQ3181 performs voltage and current measurements using an integrated ADC that can measure up to seven external differential signal pairs. An eighth differential signal pair is used to measure the die temperature. An internal amplifier automatically adjusts the current channel gain to compensate for low-current channel-signal levels.

Applications

3-Phase Active Energy Electricity Meters

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXQ3181-RAN+	-40°C to +85°C	28 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration and Typical Application Circuit appear at end of data sheet.

Features

- **Compatible with 3-Phase/3-Wire, 3-Phase/4-Wire, and Other 3-Phase Services**
- **0.1% Active Power and Energy Linearity Error**
- **0.5% Apparent Power and Energy Linearity Error**
- **0.5% Linearity Errors for RMS Voltage and RMS Current**
- **Neutral Line Current Measurement**
- **Line Frequency (Hz)**
- **Power Factors**
- **Phase Sequence Indication**
- **Phase Voltage Absence Detection**
- **Programmable Pulse Width**
- **Programmable No-Load Current Threshold**
- **Programmable Meter Constant**
- **Programmable Thresholds for Undervoltage and Overvoltage Detection**
- **Programmable Threshold for Overcurrent Detection**
- **Amp-Hours in Absence of Voltage Signals**
- **On-Chip Digital Temperature Sensor**
- **Precision Internal Voltage Reference 2.048V (30ppm/°C typical), Also Supports An External Voltage Reference**
- **Active Power and Energy of Each Phase and Combined 3-Phase (kWh), Positive and Negative**
- **Apparent Power and Energy of Each Phase and Combined 3-Phase**
- **Supports Software Meter Calibration**
- **Up to 3-Point Multipoint Calibration to Compensate for Transducer Nonlinearity**
- **Power-Fail Detection**
- **Bidirectional Reset Input/Output**
- **SPI-Compatible Serial Interface with Interrupt Request ($\overline{IRQ}$) Output**
- **Single 3.3V Supply, Low Power (35mW typical)**

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata****.*

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on DVDD Relative to DGND .....-0.3V to +4.0V
Voltage Range on AVDD Relative to AGND.....-0.3V to +4.0V
Voltage Range on AGND Relative to DGND.....-0.3V to +0.3V
Voltage Range on AVDD Relative to DVDD .....-0.3V to +0.3V
Voltage Range on Any Pin Relative to
DGND except VxP, IxN Pins.....-0.3V to +4.0V
Voltage Range on VxP, IxN Relative to AGND.....-0.3V to +4.0V
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Soldering Temperature.....Refer to the IPC/
JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

METERING SPECIFICATIONS

(V_{AVDD} = V_{DVDD} = V_{RST} to 3.6V, Current Channel Dynamic Range 1000:1 at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Active Energy Linearity Error	DR 1000:1		0.1		%
Apparent Energy Linearity Error	DR 1000:1		0.5		%
RMS Voltage Linearity Error	DR 20:1		0.5		%
RMS Current Linearity Error	DR 500:1		1.0		%
	DR 20:1		0.5		
Line Frequency Error			0.5		%
Power Factor Error			1.0		%

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY SPECIFICATIONS						
Digital Supply Voltage	V_{DVDD}		V_{RST}		3.6	V
Power-Fail Interrupt Trip Point	V_{PFW}	Active mode, EPWRF = 1	2.84		3.13	V
Power-Fail Reset Trip Point	V_{RST}	Active mode	2.70		2.99	V
Analog Supply Voltage	V_{AVDD}		V_{RST}		3.6	V
Analog Supply Current	I_{AVDD}	f_{CLK} = 8MHz		0.9	1.8	mA
Digital Supply Current	I_{DVDD}	f_{CLK} = 8MHz		8.5	13	mA
Low-Power Measurement Mode Current	I_{LOWPM}	LOWPM = 1 (Note 1)		4.2		mA
Stop-Mode Current				0.2	12	µA
DIGITAL I/O SPECIFICATIONS						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Hysteresis	V_{IHYS}	V_{DVDD} = 3.3V		500		mV
Input Leakage	I_L	V_{IN} = DGND or V_{DVDD}, pullup off		±0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Current	I_{IL}	V_{IN} = 0.4V, weak pullup on	-50			µA
$\overline{RESET}$ Pullup Resistance	R_{RESET}		50	150	200	kΩ
Output High Voltage (Except $\overline{RESET}$)	V_{OH}	I_{OH} = -4mA	V_{DVDD} - 0.4			V
		I_{OH} = -6mA	V_{DVDD} - 0.5			
Output Low Voltage	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.5	
SYSTEM CLOCK SOURCES						
External Clock Input Frequency			0		8.12	MHz
External Clock Input Duty Cycle			45		55	%
External HF Crystal Frequency		Fundamental mode			8.12	MHz
XTAL1, XTAL2 Internal Load Capacitance				16		pF
Internal RC Oscillator Frequency			7.4	7.6	8.6	MHz
Internal RC Oscillator Accuracy				±2		%
Internal RC Oscillator Current				50	120	µA
Internal RC Oscillator Startup Delay		(Note 1)		0.45		µs
ANALOG-TO-DIGITAL CONVERTER						
Input Voltage Range			0		V_{REF}	V
Common-Mode Bias	V_{COMM}			1.14		V
Offset Error				±2		mV
Offset Error Drift				±8		µV/°C
Gain Error (G = 1)				0.05		%
Spurious-Free Dynamic Range	SFDR			90		dB
Total Harmonic Distortion	THD			90		dB
Input Bandwidth (-3dB)		(Note 1)		7		kHz
INTERNAL VOLTAGE REFERENCE						
Temperature Coefficient		(Note 1)		30		ppm/°C
Output Voltage	V_{REF}			2.048		V
INTERNAL TEMPERATURE SENSOR						
Temperature Error		(Note 1)	-4		+4	°C
SPI SLAVE-MODE INTERFACE TIMING						
Maximum SPI Clock Rate		(Note 3)			f_{SYS}/4	MHz
SCLK Input Pulse-Width High	t_{SCH}	(Note 3)	4 x t_{SYS}			ns
SCLK Input Pulse-Width Low	t_{SCL}	(Note 3)	4 x t_{SYS}			ns

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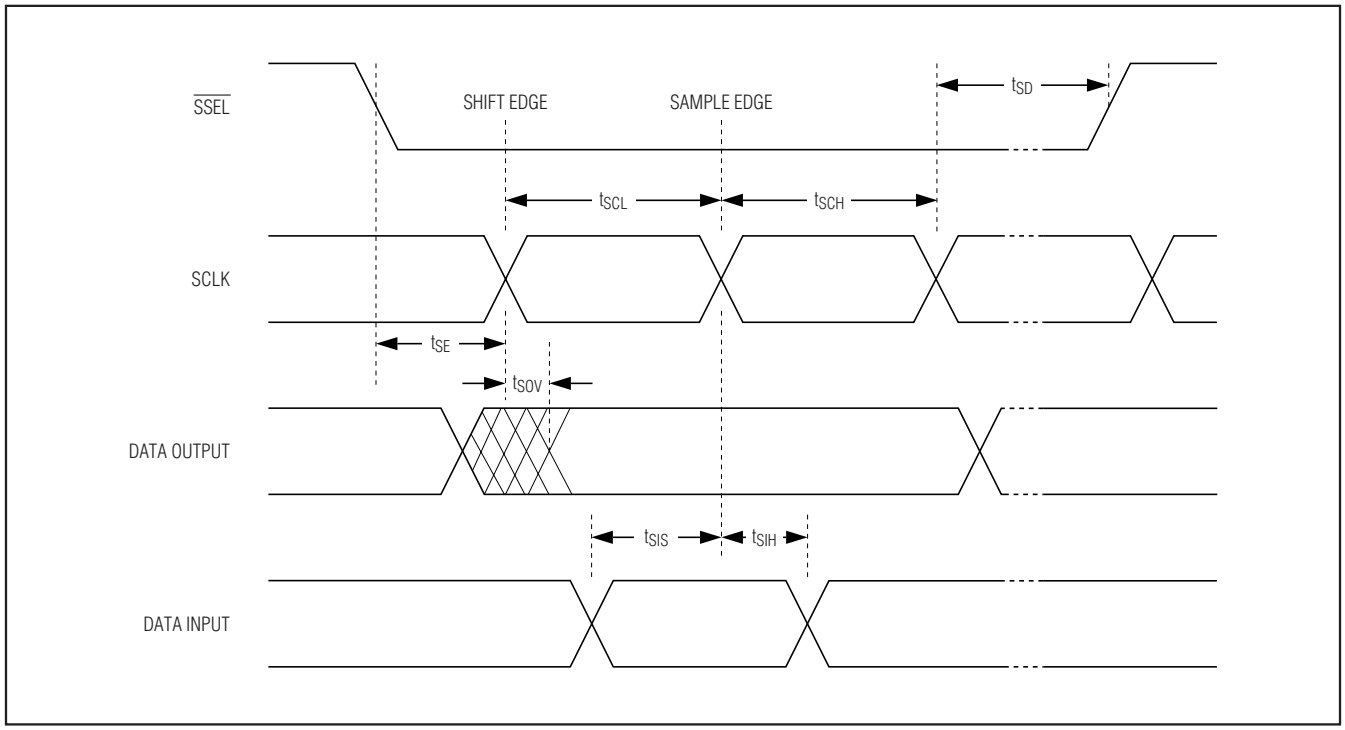
ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = V_{RST} to 3.6V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

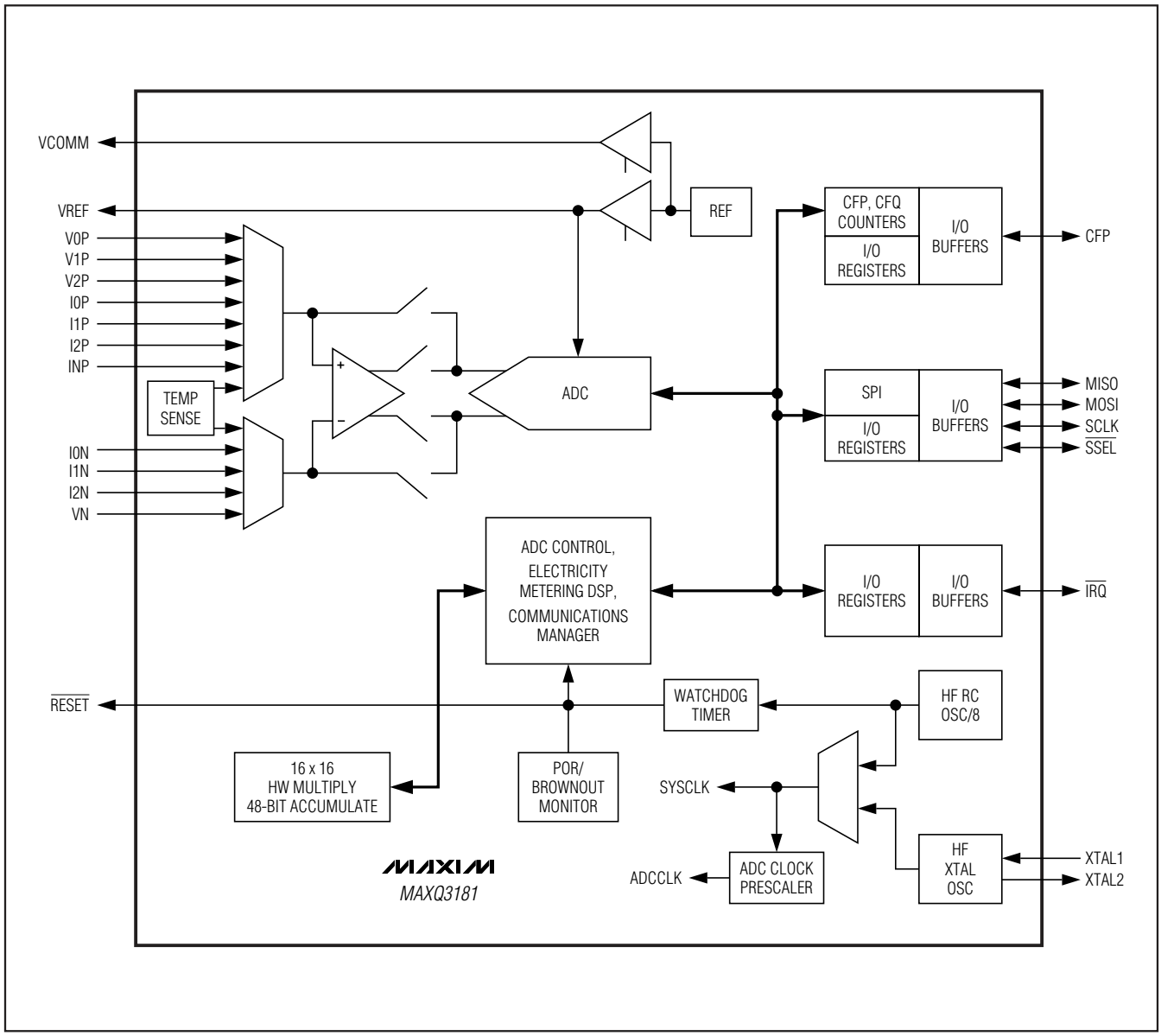
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SSEL}$ Low to First SCLK Edge (Slave Enable)	t_{SE}	(Note 3)	$4/t_{SYS}$			ns
Last SCLK Edge to $\overline{SSEL}$ High (Slave Disable)	t_{SD}		t_{SYS} + 5			ns
MOSI Valid to SCLK Sample Edge (MOSI Setup)	t_{SIS}		5			ns
SCLK Sample Edge to MOSI Change (MOSI Hold)	t_{SIH}		t_{SYS} + 5			ns
SCLK Shift Edge to MISO Valid (MISO Hold)	t_{SOV}				$3t_{SYS}$ + 5	ns

Note 1: Specifications guaranteed by design but not production tested.
Note 2: Specifications to -40°C are guaranteed by design and are not production tested.
Note 3: $t_{SYS} = 1/f_{SYS}$, where f_{SYS} is the system clock frequency, external or internal.

SPI Slave Mode Timing



Block Diagram



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Pin Description

PIN	NAME	FUNCTION
		POWER PINS
17, 22	DVDD	Digital Supply Voltage
25	AVDD	Analog Supply Voltage
18	DGND	Digital Ground
9	AGND	Analog Ground
23	VCOMM	Voltage Bias. This pin can be used to create an input common-mode DC offset for ADC channel conversions.
24	VREF	Voltage Reference. Reference voltage for the ADC. An external reference voltage can be connected to this pin when extremely high accuracy is required.
		VOLTAGE AND CURRENT PINS
26, 3, 4	V0P, I0P, I0N	Phase A Voltage and Current Analog Inputs
27, 5, 6	V1P, I1P, I1N	Phase B Voltage and Current Analog Inputs
28, 7, 8	V2P, I2P, I2N	Phase C Voltage and Current Analog Inputs
1	VN	Analog Input for Common Voltage
2	INP	Analog Input for Neutral Current
		CLOCK PINS
10	XTAL2	High-Frequency Crystal Input/Output. When using an external high-frequency crystal, the crystal oscillator circuit should be connected between XTAL1 and XTAL2. When using an externally driven clock (EXTCLK = 1), the clock should be input at XTAL1, with XTAL2 left unconnected.
11	XTAL1	
12	$\overline{IRQ}$	Interrupt Request Output. This line is driven low by the device to indicate to the master that an unmasked interrupt has occurred.
13	$\overline{SSEL}$	Slave Select Input. This line is the active-low slave select input for the SPI interface.
14	SCLK	Slave Clock Input. This line is the clock input for the SPI interface.
15	MOSI	Master Out-Slave In Input. This line is used by the master to transmit data to the slave (the MAXQ3181) over the SPI interface.
16	MISO	Master In-Slave Out Output. This line is used by the MAXQ3181 (the slave) to transmit data back to the master over the SPI interface.
19	CFP	Pulse Output. Configurable to represent energy or RMS voltage or current.
21	$\overline{RESET}$	Active-Low Reset Input/Output. An external master can reset the MAXQ3181 by driving this pin low. This pin includes a weak pullup resistor to allow for a combination of wired-OR external reset sources. An RC circuit is not required for power-up, as this function is provided internally. This pin also acts as a reset output when the source of the reset is internal to the device (power-fail, watchdog reset, etc.). In this case, the $\overline{RESET}$ pin is held low by the device until it exits the reset state, then the $\overline{RESET}$ pin is released.
		NO CONNECTION PINS
20	N.C.	No Connection

Detailed Description

The MAXQ3181 contains four major subsections: the analog front-end, the digital signal processor, the precision pulse generators, and an SPI peripheral for communication to the host processor.

Analog Front-End

The analog front-end (AFE) is an 8-channel analog-to-digital converter (ADC). It operates autonomously in the standard configuration, assigning three channels to phase A, B, and C voltage; three channels to phase A, B, and C current; one channel to neutral current; and the last channel to a temperature sensor.

Each channel also contains a programmable-gain amplifier capable of providing a gain of 1, 2, 4, 8, 16, or 32 incoming signals. Only the voltage channels permit gain scaling by the host processor. The MAXQ3181 DSP firmware automatically sets the gain on current channels.

Digital Signal Processor

The DSP code is permanently embedded in masked ROM and accepts raw current and voltage samples for each of three phases and continuously calculates a host of values including RMS volts, RMS amps, real energy, apparent energy, and power factor.

The MAXQ3181 DSP core processes incoming samples from the analog front-end according to user configurations. The host sets these operating parameters by specifying addresses within the device RAM space. When a calculation cycle is complete, the results are placed back into RAM as well. Thus, the DSP core uses the RAM block as both its input (for operating parameters) and output (for calculation results) medium. See the *SPI Peripheral* section for how the host writes operating parameters and reads results from the RAM.

The DSP also calculates certain values such as line frequency and active power only when demanded by the host.

Precision Pulse Generators

The MAXQ3181 includes a precision pulse generator that generates a pulse whenever certain conditions are met. In the MAXQ3181, many meter quantities can be selected for conversion to meter pulses including absolute energy, net energy, voltage, and current.

The pulse generator is an accumulator. On each DSP cycle, whatever quantity is being measured—real energy, current, or something else—is added to the pulse accumulator. The pulse accumulator is then tested to determine if the value in the accumulator is greater than the threshold. If it is greater, the threshold value is subtracted from the accumulator value and the meter pulse starts.

SPI Peripheral

The SPI controller is a slave-only device that can read or write any location in the data RAM. Additionally, it can request data from on-demand registers.

The MAXQ3181 implements a truly full-duplex communication, rather than the pseudo half-duplex mode used by other SPI peripherals. That is, each time a character is received by the MAXQ3181, a meaningful character is returned to the host. Often, this is a protocol character. In this way, the host can be assured that the command has been received and is valid. Optional error checking can also be enabled to further guarantee proper operation.

Operating Modes

The MAXQ3181 has two basic modes of operation, each of which is described in the following sections. The Initialization Mode is the default mode upon power-up or following reset; entry to and exit from the other operating modes is only performed as a result of commands sent by the master.

Run Mode

This mode is the normal operating mode for the MAXQ3181. In this mode, the MAXQ3181 continuously executes the following operations:

- Scans analog front-end channels and collects raw voltage and current samples.
- Processes voltage and current samples through DSP filters as enabled and configured.
- Calculates power, energy, and other required quantities and stores these values in RAM registers.
- Responds to register write and read commands from the master.
- Outputs power pulse on CFP as configured.
- Drives $\overline{IRQ}$ when an interrupt condition has been detected and the interrupt is not masked.

Stop Mode

This mode places the MAXQ3181 into a power-saving state where it consumes the least possible amount of current. In Stop Mode, all functions are suspended, including the ADC and power and voltage measurement and processing. The MAXQ3181 does not respond to any commands from the master in this operating state.

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Entry into Stop Mode only occurs at the request of the master. To place the MAXQ3181 into Stop Mode, the master must read the ENTER STOP (0xC02) register. Once this register has been read, the MAXQ3181 enters Stop Mode immediately, before the transmission of the final ACK byte by the MAXQ3181.

There are three possible ways to bring the MAXQ3181 back out of Stop Mode.

- **Power Cycle.** The MAXQ3181 automatically exits Stop Mode if a power-on reset occurs. Following exit from Stop Mode, all registers are cleared back to their default states, and the MAXQ3181 transitions to Initialization Mode.
- **External Reset.** The MAXQ3181 exits Stop Mode if an external reset is triggered by driving $\overline{\text{RESET}}$ low. Once the $\overline{\text{RESET}}$ pin is released and allowed to return to a high state, the MAXQ3181 comes out of reset and goes into Initialization Mode. All registers are cleared to their default states when exiting Stop Mode in this manner.
- **External Interrupt.** Driving the $\overline{\text{SSEL}}$ pin low causes the MAXQ3181 to exit Stop Mode without undergoing a reset cycle. When exiting Stop Mode in this manner, all register and configuration settings are retained, and the MAXQ3181 automatically resumes electric-metering functions and sample processing.

Note that when the master is communicating with the MAXQ3181, the $\overline{\text{SSEL}}$ line is normally driven low at the beginning of each SPI command. This means that if the master sends an SPI command after the MAXQ3181 enters Stop Mode, the MAXQ3181 automatically exits Stop Mode.

Reset Sources

There are several different sources that can cause the MAXQ3181 to undergo a reset cycle. For any type of hardware reset, the $\overline{\text{RESET}}$ pin is driven low when a reset occurs.

External Reset

This hardware reset is initiated by an external source (such as the master controller or a manual pushbutton press) driving the $\overline{\text{RESET}}$ pin on the MAXQ3181 low. The $\overline{\text{RESET}}$ line must be held low for at least four cycles of the currently selected clock for the external reset to take effect. Once the external reset takes effect, it remains in effect indefinitely as long as $\overline{\text{RESET}}$ is held low. Once the external reset has been released, the MAXQ3181 clears all registers to their default states and resumes execution in Initialization Mode.

When an external reset occurs outside of Stop Mode, execution (in Initialization Mode) resumes after four cycles of the currently selected clock (external high-frequency crystal for Run Mode, 1MHz internal RC oscillator for LOWPM Mode). As the MAXQ3181 enters Initialization Mode, the LOWPM bit is always cleared

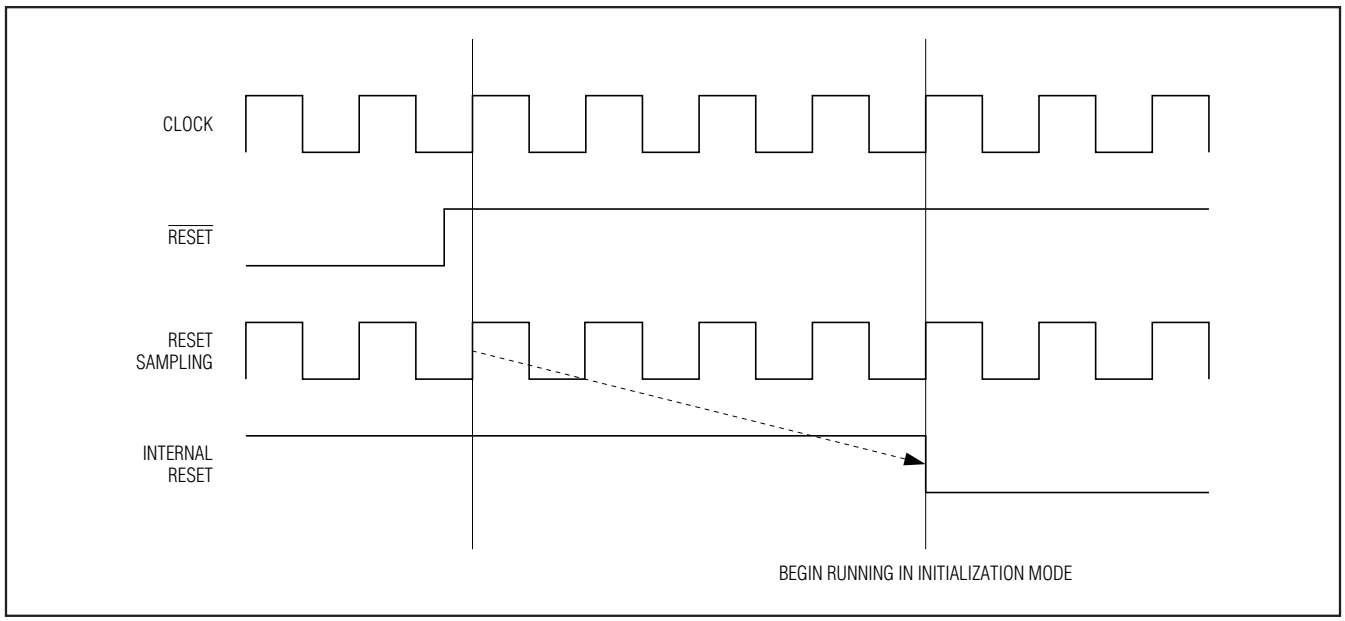

Figure 1. External Reset

to 0, meaning that the MAXQ3181 always switches to the high-frequency clock before it begins accepting commands in Initialization Mode.

When an external reset occurs from Stop Mode, execution (in Initialization Mode) resumes after 128 cycles of the internal RC oscillator (or approximately 128µs).

Power-On Reset

When the MAXQ3181 is first powered up, or when the power supply, V_{DVDD}, drops below the V_{RST} power-fail trip point (outside of Stop Mode), the MAXQ3181 is held in power-on reset. Once the power supply rises above the V_{RST} level, the power-on reset state is released and all registers are reset to their defaults and execution resumes in Initialization Mode. The high-frequency external crystal (LOWPM = 0) is always selected as the clock source following any power-on or brownout reset.

In Stop Mode brownout detection is disabled, so a power-on reset does not occur until V_{DVDD} drops to a lower level (V_{POR}). From the master's perspective, power-on resets and brownout resets both cause the MAXQ3181 to reset in the same way.

Watchdog Reset

The MAXQ3181 includes a hardware watchdog timer that is armed and periodically reset automatically during normal operation. Under normal circumstances, the MAXQ3181 always resets the watchdog timer often enough to prevent it from expiring. However, if an internal error of some kind causes the MAXQ3181 to lock up or enter an endless execution loop, the watchdog timer expires and triggers an automatic hardware reset. There is no register flag to indicate to the master that a watchdog reset has occurred, but the $\overline{\text{RESET}}$ line strobes low briefly.

The watchdog timer does not run during Stop Mode.

Software Reset

The master initiates a software reset by setting the SWRES (OPMODE0.3) bit to 1. When a software reset occurs, the MAXQ3181 clears all registers to their default states and returns to Initialization Mode, in the

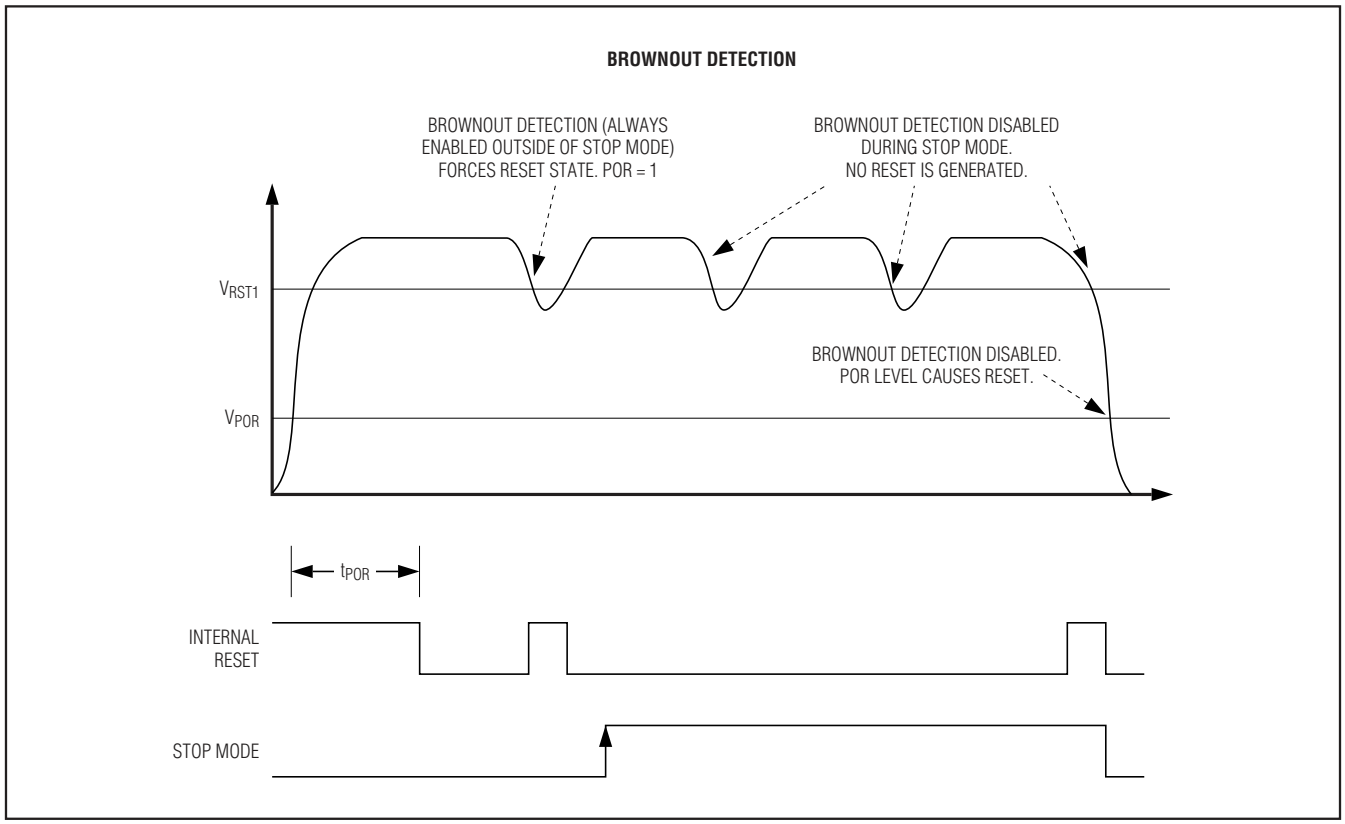

Figure 2. Brownout Reset

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same manner as if an external reset had taken place. Unlike a hardware reset, however, a software reset does not cause the MAXQ3181 to drive the RESET line low.

Power-Supply Monitoring

In addition to the hardware reset provided by the power-on reset and brownout reset circuits, the MAXQ3181 includes the capability to detect a low power supply on the DVDD pin and alert the master through the interrupt (IRQ) mechanism before a hardware reset occurs. This function, which is always enabled outside of Stop Mode, causes the RAM status register flag PWRF (IRQ_FLAG.0) to be set to 1 whenever V_{DVDD} drops below the V_{PFW} trip point. Once PWRF has been set to 1 by hardware, it can only be cleared by the master (or by a system reset). Whenever PWRF = 1, if the EPWRF interrupt masking bit is also set to 1, the MAXQ3181 drives IRQ low to signal to the master that an interrupt condition (in this case, a power-fail warning) exists and requires attention.

Clock Sources

All operations including ADC sampling and SPI communications are synchronized to a single system clock. This clock can be obtained from any one of three selectable sources, as shown in Figure 3.

External High-Frequency Crystal

The default system clock source for the MAXQ3181 is an external high-frequency crystal oscillator circuit connected between XTAL1 and XTAL2. When clocked with an external crystal, a parallel-resonant, AT-cut crystal oscillating in the fundamental mode is required.

When using a high-frequency crystal, the fundamental oscillation mode of the crystal operates as inductive reactance in parallel resonance with external capacitors C1 and C2. The typical values of these external capacitors vary with the type of crystal being used and should be selected based on the load capacitance as suggested by the crystal manufacturer.

Since noise at XTAL1 and XTAL2 can adversely affect device timing, the crystal and capacitors should always be placed as close as possible to the XTAL1 and XTAL2 pins, with connection traces between the crystal and the device kept as short and direct as possible. In multiple layer boards, avoid running other high-speed digital signals underneath the crystal oscillator circuit if possible, as this could inject unwanted noise into the clock circuit.

Following power-up or any system reset, the high-frequency clock is automatically selected as the system clock source. However, before this clock can be used

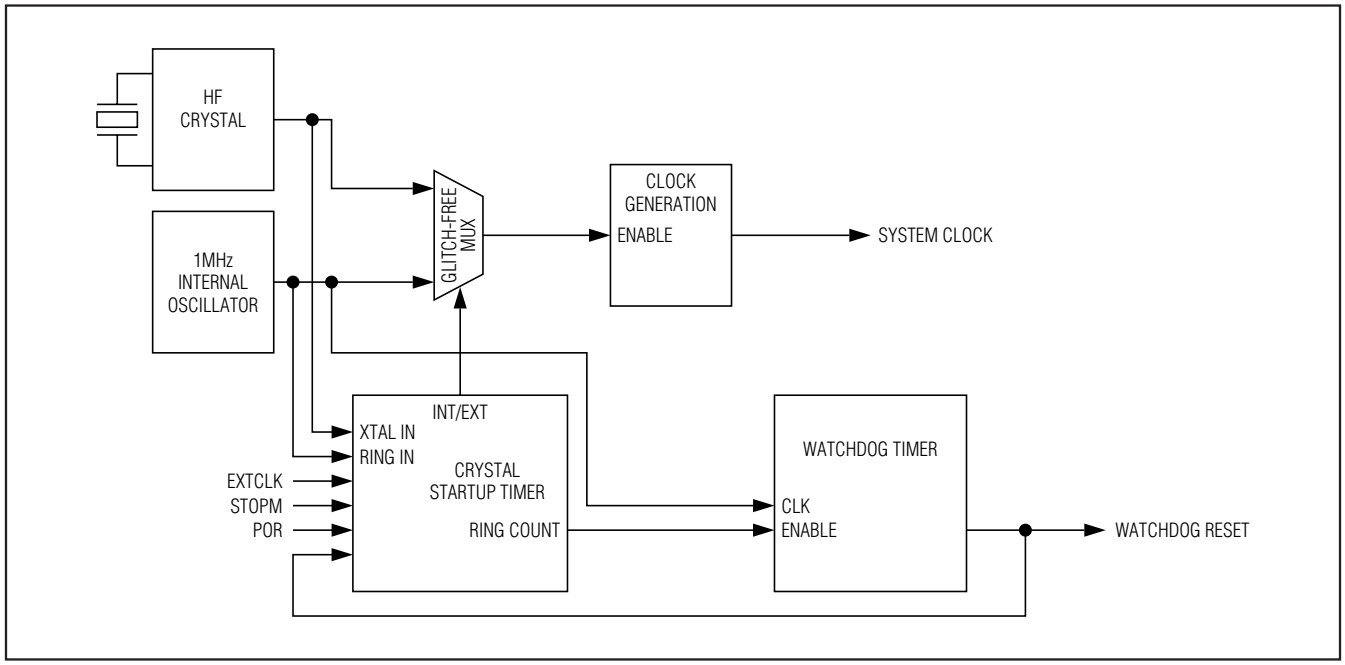

Figure 3. Simplified Clock Sources

for system execution, a crystal warmup timer must count 65,536 cycles of the high-frequency clock. While this warmup time period is in effect, execution continues using the internal 1MHz oscillator. Once the 65,536-cycle count completes (which requires approximately 8.2ms at 8MHz), the device automatically switches over to the high-frequency clock. This crystal warmup timer is also activated upon exit from Stop Mode, since the high-frequency crystal oscillator is shut down during Stop Mode.

External High-Frequency Clock

Instead of using a crystal oscillator to generate the high-frequency clock, it is also possible to input a high-frequency clock that has been generated by another source (such as a digital oscillator IC) directly into the XTAL1 pin of the MAXQ3181.

To use an external high-frequency clock as the system clock source, the XTAL1 pin should be used as the clock input and the XTAL2 pin should be left unconnected. The master should also shut down the internal crystal oscillator circuit by setting the EXTCLK bit (OPMODE0.4) to 1. This bit is only cleared by the MAXQ3181 if a power-on or brownout reset occurs and is unaffected by other resets.

When using an external high-frequency clock, the clock signal should be generated by a CMOS driver. If the clock driver is a TTL gate, its output must be connected to DVDD through a pullup resistor to ensure that the correct logic levels are generated. To minimize system noise in the clock circuitry, the external clock source must meet the maximum rise and fall times and the minimum high and low times specified for the clock source in the *Electrical Characteristics* table.

Internal RC Oscillator

When the external high-frequency crystal is warming up, or when the MAXQ3181 is placed into LOWPM mode, the system clock is sourced from an internal RC oscillator. This internal oscillator is designed to provide the system approximately 1MHz, although the exact frequency varies over temperature and supply voltage.

If no external crystal circuit or high-frequency clock will be used, the MAXQ3181 can be forced to operate infinitely from the internal oscillator by grounding XTAL1. This ensures that the crystal warmup count never completes, so the MAXQ3181 runs from the internal oscillator in all active modes.

Master Communications

Before the MAXQ3181 can begin performing electric-metering operations, the master must initialize a number of configuration parameters. Since the MAXQ3181 does not contain internal nonvolatile memory, these parameters (stored in internal registers) must be set by the master each time a power-up or reset cycle occurs, or each time a switch is made between LOWPM Mode and Run Mode.

The external master communicates with the MAXQ3181 over a standard SPI bus, using commands to read and write values to internal registers on the MAXQ3181. These registers include, among many other items:

- Operating mode settings (Stop Mode, LOWPM Mode, external clock mode, etc.)
- Status and interrupt flags (power-supply failure, overcurrent/overvoltage detection, etc.)
- Masking control for interrupts to determine which conditions cause $\overline{IRQ}$ to be driven low
- Configuration settings for analog channel scanning
- Power pulse output configuration
- Filter coefficients and configuration
- Read-only registers containing accumulated power and energy data

As the MAXQ3181 obtains voltage and current measurements in Run Mode or LOWPM Mode, it accumulates, filters, and performs a number of calculations on the collected data. Many of these operations (including the various filtering stages) are configured by settings in registers written by the master. The output results can then be read by the master from various read-only registers in parallel with the ongoing measurement and processing operations.

SPI Communications Rate and Format

The SPI is an interdevice bus protocol that provides fast, synchronous, full-duplex communications between a designated master device and one or more slave devices. In a MAXQ3181-based design, the MAXQ3181 would be the slave device connected to a designated master microcontroller.

The external master initiates all communications transfers. The interrupt request line $\overline{IRQ}$, while not technically part of the SPI bus interface, is also used for master/slave communications because it allows the MAXQ3181 to notify the master that an interrupt condition exists. Some SPI peripherals sacrifice speed in favor of simulating a half-duplex operation. This is not the case with the MAXQ3181; it is truly a full-duplex SPI slave.

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During an SPI transfer, data is simultaneously transmitted and received over two serial data lines (MISO and MOSI) with respect to a single serial shift clock (SCLK). The polarity and phase of the serial shift clock are the primary components in defining the SPI data transfer format. The polarity of the serial clock corresponds to the idle logic state of the clock line and, therefore, also defines which clock edge is the active edge. To define a serial shift clock signal that idles in a logic-low state (active clock edge = rising), the clock polarity select (CKPOL; R_SPICF.0) bit should be configured to a 0, while setting CKPOL = 1 causes the shift clock to idle in a logic-high state (active clock edge = falling). The phase of the serial clock selects which edge is used to sample the serial shift data. The clock phase select (CKPHA; R_SPICF.1) bit controls whether the active or inactive clock edge is used to latch the data. When CKPHA is set to a logic 1, data is sampled on the inactive clock edge (clock returning to the idle state). When CKPHA is set to a logic 0, data is sampled on the active clock edge (clock transition to the active state). Together, the CKPOL and CKPHA bits allow four possible SPI data transfer formats.

Transfers over the SPI interface always start with the most significant bit and end with the least significant bit. All SPI data transfers to and from the MAXQ3181 are always 8 bits (one byte) in length. The MAXQ3181 SPI interface does not support 16-bit character lengths.

The default format (upon power-up or system reset) for the MAXQ3181 SPI interface is represented in Figure 4a (CKPOL = 0; CKPHA = 0). In this format, the

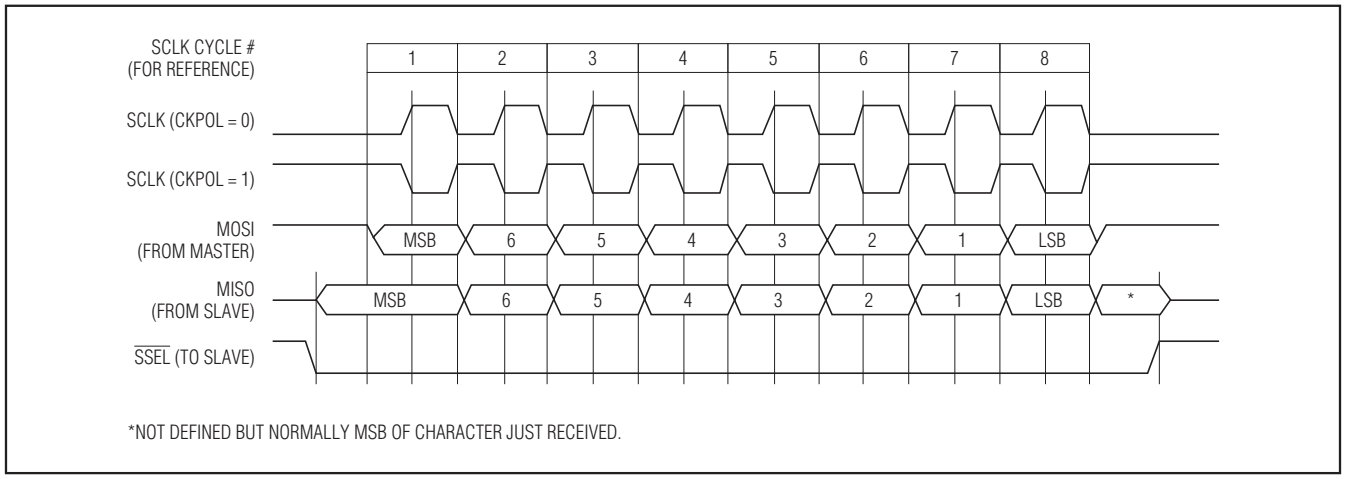

Figure 4a. SPI Interface Timing (CKPHA = 0)

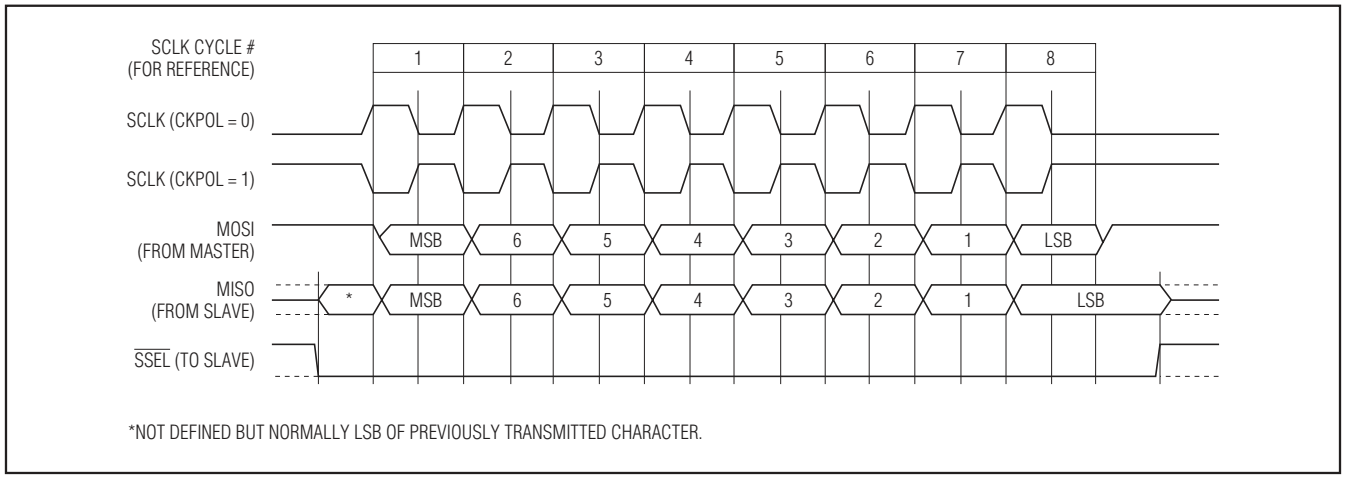

Figure 4b. SPI Interface Timing (CKPHA = 1)

SPI clock idle state is low, and data is shifted in and out on the rising edge of SCLK. Once SPI communication with the MAXQ3181 has been established, it is possible to alter the CKPOL and CKPHA format settings (as well as changing the $\overline{SSEL}$ signal from active low to active high) if desired by writing to the R_SPICF mirror register and then reading from the special command register UPD_SFR to copy the R_SPICF value into the internal SPI configuration register.

Whenever the active clock edge is used for sampling (CKPHA = 0), the transfer cycle must be started with assertion of the $\overline{SSEL}$ signal. This requirement means that the $\overline{SSEL}$ signal be deasserted and reasserted between successive transfers. Conversely, when the inactive edge is used for sampling (CKPHA = 1), the $\overline{SSEL}$ signal may remain low through successive transfers, allowing the active clock edge to signal the start of a new transfer.

The clock rate used for the SPI interface is determined by the bus master, since the MAXQ3181 always operates as an SPI slave device. However, the maximum clock rate is limited by the system clock frequency of the MAXQ3181. For proper communications operation, the SPI clock frequency used by the master must be less than or equal to the MAXQ3181's clock frequency divided by 4. For example, when the MAXQ3181 is running at 8MHz, the SPI clock frequency must be 2MHz or less. And if the MAXQ3181 is running in LOWPM Mode (or if the crystal is still warming up), the SPI clock frequency must remain at 250kHz or less for proper communications operation.

In addition to limiting the overall SPI bus clock rate, the master must also include a communications delay following each byte transmit/receive cycle. This delay, which provides the MAXQ3181 with time to process an ADC sample, should be a minimum of 400 system clocks. With default settings and running at 8MHz, this delay time is 50µs. Reducing the system clock frequency to 1MHz (LOWPM mode) would increase this delay period by a factor of 8 to 400µs.

SPI Communications Protocol

All transactions between the master and the MAXQ3181 consist of the master writing to or reading from one of the MAXQ3181's registers. To the host, the MAXQ3181 looks like a memory array that consists of both RAM and ROM. This is because the ROM firmware in the MAXQ3181 reads its operational parameters from RAM and places its results in RAM. Consequently, configuring a MAXQ3181 is as simple as performing a block write to its RAM locations.

Some read-only memory locations in the MAXQ3181 trigger actions within the device to calculate electricity-metering results on the fly. The specific function and purpose of RAM and virtual ROM locations are given in the register map. There are several different categories of internal registers on the MAXQ3181.

- **RAM Registers.** The values of these registers are stored in the internal RAM of the MAXQ3181. Some can be read and written by the master, while others are read-only. RAM registers are either 2 or 4 bytes long (16 or 32 bits), although in some registers not all the bits have defined values. Read/write registers are generally either status/flag registers (which can be written by either the MAXQ3181 or the master), configuration registers (which are written by the master and read by the MAXQ3181 firmware), or data registers (which are read-only and are written by the MAXQ3181 firmware and read by the master).
- **Virtual Registers.** These read-only registers are not stored in RAM; instead, they contain values that are calculated on the fly by the MAXQ3181 firmware when the master reads them. These registers are used by the master to obtain values such as phase A, B, and C active and apparent power; power factor; and RMS voltage and current, which are calculated from currently collected data on an as-needed basis. Most virtual registers are 8 bytes in length.
- **Hardware Registers.** These registers control core functions of the MAXQ3181 including the ADC and the SPI slave bus controller. Each of these registers (R_ACFG, R_ADCRATE, R_ADCACQ, R_SPICF, and OPMODE0 (bit 4, EXTCLK only)) has a register location in RAM that "shadows" the value of the hardware register. To read from a hardware register, the master must first read from the special command register UPD_MIR (A00h) to copy the values from the hardware registers to the mirror registers in RAM, and then the mirror register in RAM can be read. To write to a hardware register, the master reverses the process by writing to the mirror RAM register and then reading from the special command register UPD_SFR (900h) to copy the values from the mirror registers to the hardware registers.
- **Special Command Registers.** These registers (UPD_SFR and UPD_MIR) do not return meaningful data when read but instead trigger an operation. Reading UPD_SFR causes values to be copied from the mirror registers to hardware, and reading UPD_MIR causes values to be copied from the hardware to mirror registers.

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Every defined register on the MAXQ3181 has a 12-bit address (from 0 to 4095). This address is used when addressing the register for either a read or write operation. Addresses 0 to 1023 (000h to 3FFh) are used to address RAM registers. Registers with addresses from 1024 to 4095 (400h to FFFh) are used for virtual registers and special command registers.

Each command consists of a read/write command code, a data length (1, 2, 4, or 8 bytes), a 12-bit register address, and the specified number of data bytes followed optionally by a cyclic redundancy check (CRC). Since SPI is a full-duplex interface, the master and slave must both transmit the same number of bytes during the command. When a multiple-byte register is read or written (2/4/8 byte length), the least significant byte is read or written first in the command.

Every transaction begins with the master sending 2 bytes that contain the command (read or write), the address to access, and the number of bytes to transfer. Every SPI peripheral must return 1 byte for every byte it receives. If the master is reading 1 or more bytes from the MAXQ3181, it must send dummy bytes during the cycles when it is receiving a multibyte response to a request, meeting the "send a byte to get a byte" requirement. But the MAXQ3181 could require time to calculate the result, and thus might not have it ready when the master sends the dummy byte. For this reason, the MAXQ3181 always sends zero or more bytes of a NAK character (0x4E or ASCII 'N') followed by an ACK character (0x41, or ASCII 'A') before sending the data.

If the master is writing 1 or more bytes, it sends the data to be written immediately after sending the command. The MAXQ3181 returns ACK (0x41) for each data byte. It then returns NAK (0x4E) until the write cycle is complete, after which it returns a final ACK.

Immediately after the final ACK, the MAXQ3181 is ready to begin the next transaction; there is no need to wait for any other event. It is not even necessary to toggle $\overline{SSEL}$ to begin the next transaction. The MAXQ3181 knows that the first transaction is over and is ready for the next.

If, for whatever reason, it is necessary to reset the communications between the host and the MAXQ3181 (for

Table 1. Command Format for SPI Register Read

BYTE	TRANSFERS	BIT	DESCRIPTION
1st byte	Master sends command; Slave sends 0xC1 byte	7:6	Command Code: 00 Read 01 Reserved 10 Write 11 Reserved
		5:4	Data Length: 00 1 Byte 01 2 Bytes 10 4 Bytes 11 8 Bytes
		3:0	MSB portion of data address.
2nd byte	Master sends address; Slave sends 0xC2 byte	7:0	LSB portion of data address.
Sync bytes	Master sends dummy; Slave sends ACK (0x41) or NACK (0x4E) byte	7:0	Master sends dummy byte; Slave responds with NACK if busy, or with ACK when processing complete. Master must receive ACK, then receive data.
3rd byte (1st data byte)	Master sends dummy; Slave sends data	7:0	Data, LSB
...	...	...	...
Nth byte (Last data byte)	Master sends dummy; Slave sends data	7:0	Data, MSB
(N + 1) byte	Master sends dummy; Slave sends CRC	7:0	Optional CRC

Table 2. Command Format for SPI Register Write

BYTE	TRANSFERS	BIT	DESCRIPTION
1st byte	Master sends command; Slave sends 0xC1 byte	7:6	Command code: 00 Read 01 Reserved 10 Write 11 Reserved
		5:4	Data Length: 00 1 Byte 01 2 Bytes 10 4 Bytes 11 8 Bytes
		3:0	MSB portion of data address.
2nd byte	Master sends address; Slave sends 0xC2 byte	7:0	LSB portion of data address.
3rd byte (1st data byte)	Master sends data; Slave sends ACK (0x41)	7:0	Data, LSB
...	...	...	...
Nth byte (Last data byte)	Master sends data; Slave sends ACK (0x41)	7:0	Data, MSB
(N + 1) byte	Master sends CRC; Slave sends ACK (0x41)	7:0	Optional CRC
Sync bytes	Master sends dummy; Slave sends ACK (0x41) or NACK (0x4E) byte	7:0	Master sends dummy byte; Slave responds with NACK if busy, or with ACK when processing complete. Master must receive ACK before starting the next transaction.

example, if synchronization is lost), the host only needs to wait for the SPI to time out before restarting communication from the first command byte. SPI timeout count starts after receiving the first command byte from the master (after the 8th SPI clock of the first byte). The count stops and clears after receiving the last byte of a transaction (after the 8th SPI clock of the last byte).

If the timeout count expires (exceeds COM_TIMO) before the transaction completes, the MAXQ3181 abandons the unfinished transaction and resets the SPI logic to be ready for the next transaction. The default SPI timeout is 320ms.

Optionally, a CRC byte can be appended to each transaction. For write commands, the CRC byte is sent by the master, and for read commands the CRC byte is sent by the MAXQ3181. The CRC mode is enabled when the CRCEN bit is set to 1 in OPMODE1 register. Otherwise, the MAXQ3181 assumes no CRC byte is used. The 8-bit CRC is calculated for all bytes in a transaction, from the first command byte sent by the master through the last data byte excluding sync bytes, using the polynomial $P = x^8 + x^5 + x^4 + 1$. If the transmitted CRC byte does not match the calculated CRC byte (for a write command), the MAXQ3181 ignores the command.

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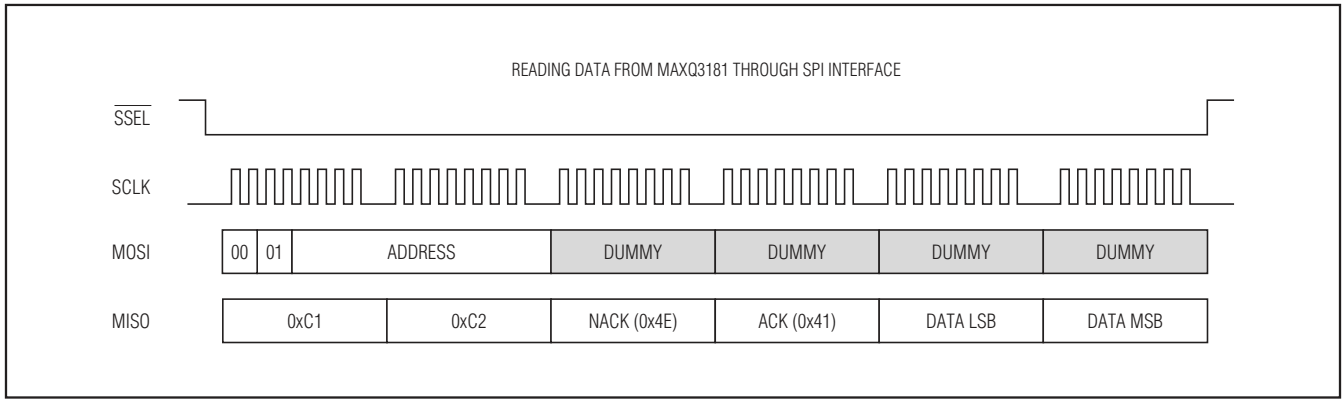

Figure 5. Read SPI Transfer

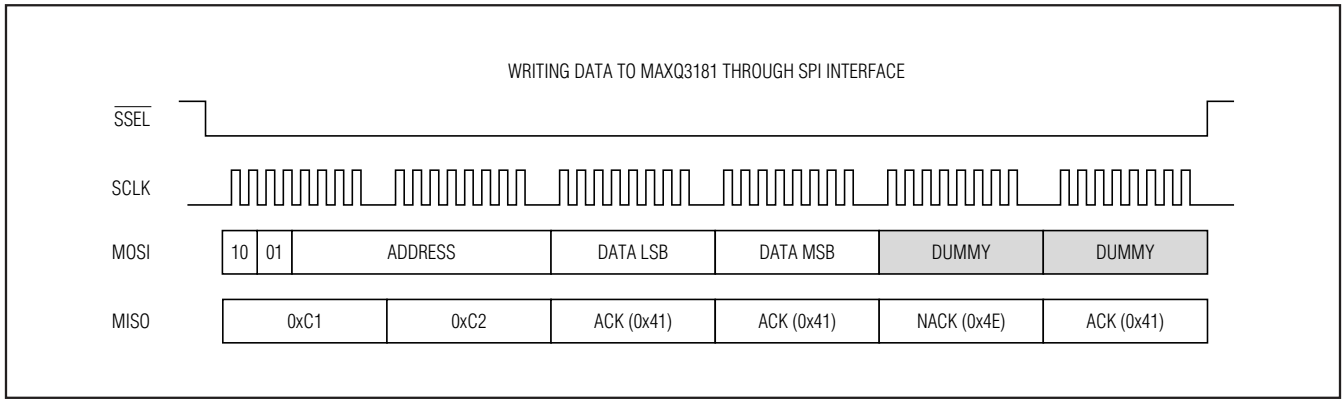

Figure 6. Write SPI Transfer

The length of the transfer is defined by the first command byte and the status of the CRCEN bit in the OPMODE1 register. There is no special synchronization mechanism provided in this simple protocol. Therefore, the master is responsible for sending/receiving the correct number of bytes. If the master mistakenly sends more bytes than are required by the current command, the extra bytes are either ignored (if the MAXQ3181 is busy processing the previous command) or are interpreted as the beginning of a new command. If the master sends fewer bytes than are required by the current command, the MAXQ3181 waits for SPI timeout, then drops the transaction and resets the communication channel. The duration of the timeout can be configured through the COM_TIMO register.

Figures 5 and 6 show typical 2-byte reading and writing transfers (without CRC byte).

Host Software Design

Individual message bytes sent through the SPI are processed in a software routine contained in the ROM firmware. For this reason, it is necessary to provide a delay between successive bytes. This byte spacing must be no less than 400 system clocks to ensure that the MAXQ3181 has a chance to read and process the byte before the arrival of the next one. It is strongly recommended that CRC be enabled for both read and write to achieve reliable communications.

Register Set

Data and device command and control information are located in internal registers. Registers range from 8 to 64 bits in length and are divided into RAM-based registers and virtual registers. The RAM-based registers contain both operating parameters and measurement results.

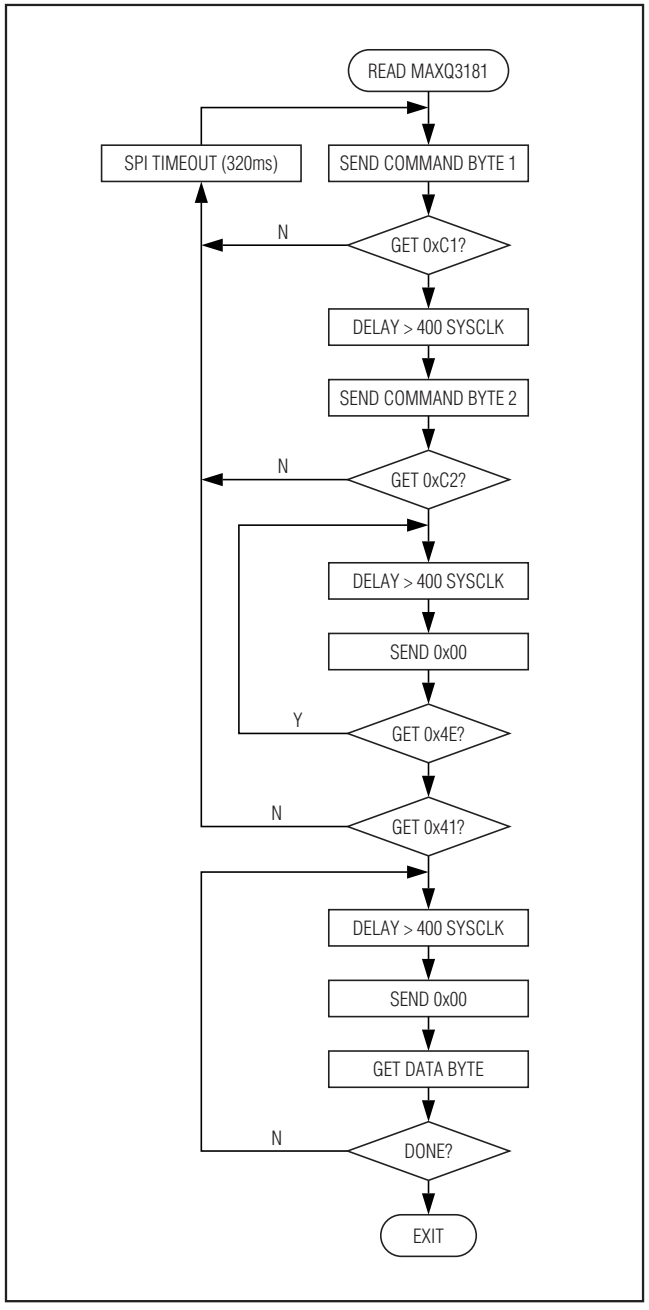

Figure 7. Flowchart for Reading from MAXQ3181

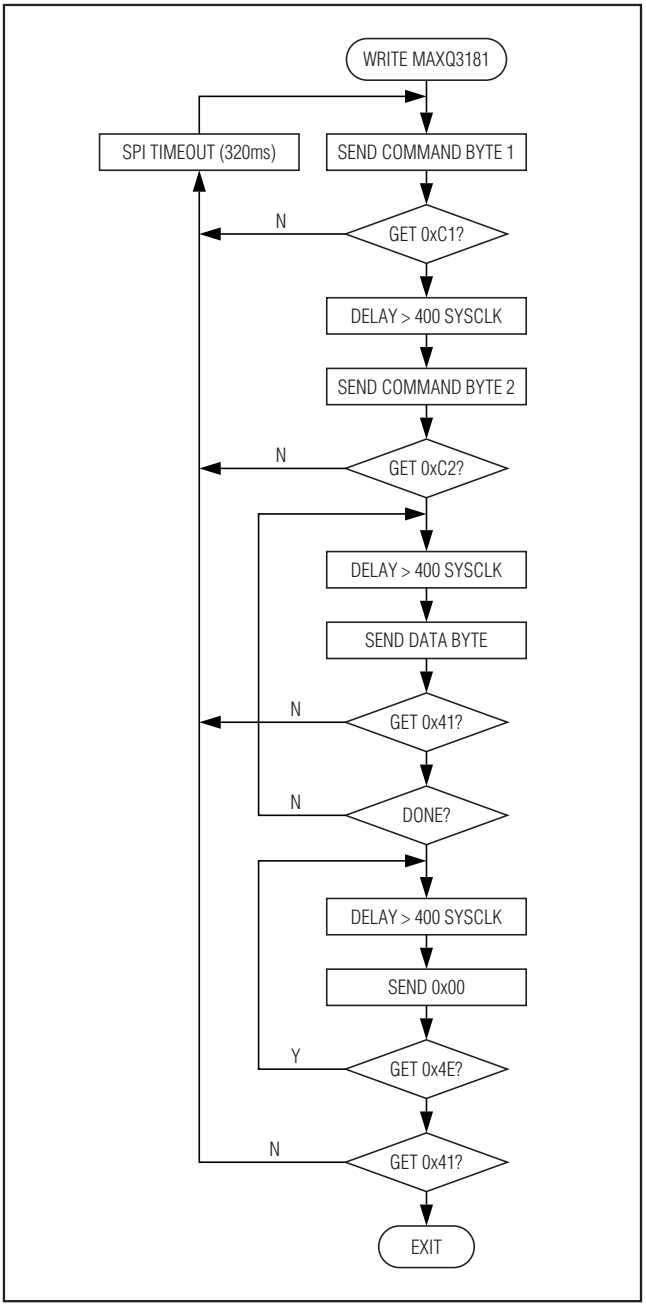

Figure 8. Flowchart for Writing to MAXQ3181

The virtual registers contain calculated values derived from one or more real registers. They are calculated at the time they are requested, and thus can involve additional time to return a value. Most virtual registers are 8 bytes in length and are delivered least significant byte first.

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Table 3. RAM Register Map

	x0h	x1h	x2h	x3h	x4h	x5h	x6h	x7h	x8h	x9h	xAh	xBh	xCh	xDh	xEh	xFh
0x00	STATUS	OP MODE1	OP MODE2	OP MODE3	IRQ_FLAG		IRQ_MASK		SCAN _IA	SCAN _VA	SCAN _IC	SCAN _VC	SCAN _IB	SCAN _VB	SCAN _IN	SCAN _TE
0x01	AUX_CFG		SYS_KHZ		VOLT_CC		AMP_CC		PWR_CC		ENR_CC		CYCNT		PLSCFG 1	
0x02	PLS1_WD		THR1										REJ_NS		AVG_NS	
0x03	AVG_C		HPF_C													
0x04	NS				OCLVL		OVLVL		UVLVL		NOLOAD		R_ACFG		R_ADCRATE	
0x05	R_ADCACQ		R_ SPICF		NZX_TIMO		COM_TIMO		ACC_TIMO		ZC_LPF		I1THR		I2THR	
0x06	CHKSUM		LINEFR													
0x11													N.IRMS			
0x12															N.I_GAIN	
PHASE A CONFIGURATION AND STATUS REGISTERS																
0x13	A.I_GAIN		A.V_GAIN		A.E_GAIN				A.OFFS_HI		A.GAIN_LO		A.OFFS_LO		A.PA0	
0x14	A.PA1		A.PA2		A. FLAGS	A. MASK	A. EOVER									
PHASE B CONFIGURATION AND STATUS REGISTERS																
0x21													B.I_GAIN		B.V_GAIN	
0x22	B.E_GAIN				B.OFFS_HI		B.GAIN_LO		B.OFFS_LO		B.PA0		B.PA1		B.PA2	
0x23	B. FLAGS	B. MASK	B. EOVER													
PHASE C CONFIGURATION AND STATUS REGISTERS																
0x30									C.I_GAIN		C.V_GAIN		C.E_GAIN			
0x31	C.OFFS_HI		C.GAIN_LO		C.OFFS_LO		C.PA0		C.PA1		C.PA2		C. FLAGS	C. MASK	C. EOVER	
0x32																
PHASE A MEASUREMENT REGISTERS*																
0x1C							A.PF		A.VRMS				A.IRMS			
0x1D	A.ACT								A.APP							
0x1E									A.EAPOS				A.EANEG			
0x1F									A.ES							
0x20																
PHASE B MEASUREMENT REGISTERS*																
0x2B			B.PF		B.VRMS				B.IRMS				B.ACT			
0x2C					B.APP											
0x2D					B.EAPOS				B.EANEG							
0x2E					B.ES											
0x2F																
PHASE C MEASUREMENT REGISTERS*																
0x39															C.PF	
0x3A	C.VRMS				C.IRMS				C.ACT							
0x3B	C.APP															
0x3C	C.EAPOS				C.EANEG											
0x3D	C.ES															
0x3E																

**Read-only.*

Table 4. Virtual Register Map

	x0	x1	x2	x3	x4	x5	x6	x7
0x80		PWRP.A	PWRP.B		PWRP.C			PWRP.T
0x81								
0x82		PWRS.A	PWRS.B		PWRS.C			PWRS.T
0x83		V.A	V.B		V.C			
0x84	I.N	I.A	I.B		I.C			
0x85								
0x86								PF.T
0x87		ENRS.A	ENRS.B		ENRS.C			ENRS.T
0x88								
0x89								
0x8A								
0x8B								
0x8C		ENRP.A	ENRP.B		ENRP.C			ENRP.T
0x8D								
0x8E								
0x8F								
SPECIAL FUNCTION REGISTERS								
0xC0	DSPVER	RAWTEMP	ENTER STOP	ENTER LOWPM	EXIT LOWPM			

Note: *All virtual registers are read-only.*

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RAM-Based Registers

The RAM-based registers contain both operating parameters and measurement results. They are divided into a number of categories that are described in the following sections.

General Operating Registers

Global Status Register (STATUS) (0x000)

Bit:	7	6	5	4	3	2	1	0
Name:	—	CROFF	PORF	WDTR	—	PHSEQ	—	REVCFP
Reset:	0	0	0	0	0	0	0	0

This register contains bits that reflect the global status of the device.

BIT	NAME	FUNCTION
7, 3, 1	—	Reserved.
6	CROFF	When set, the high-frequency crystal has failed and the MAXQ3181 is operating from its internal ring oscillator. Under these circumstances, energy accumulation is not accurate and the SPI bus does not operate at full speed.
5	PORF	When set, the last reset was due to power-on-reset. Host should clear this bit to allow the next POR detection.
4	WDTR	When set, the last reset was caused by expired watchdog. The bit should be cleared (set to 0) by the host to allow the next watchdog reset detection.
2	PHSEQ	0 = The sequence of voltages presented to the voltage inputs is (-A-B-C-). 1 = The sequence of voltages presented to the voltage inputs is reversed (-A-C-B-). This bit is meaningful only for connection systems that include all three voltages.
0	REVCFP	0 = The quantity being output on the CFP pin is positive (direct). 1 = The quantity being output on the CFP pin is negative (reverse).

Operating Mode Register 0 (OPMODE0) (0x001)

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	EXTCLK	SWRES	DSPDIS	LOWPM	—
Reset:	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
7:5, 0	—	Reserved.
4	EXTCLK	When set, the high-frequency crystal oscillator is disabled and the XTAL1 pin is configured to be a clock input for the device. This is used when it is desired to operate multiple devices from the same clock source for purposes of maintaining synchronization.
3	SWRES	When set, forces the internal software to restart from the reset vector. This has the same effect as a power-on reset, but does not specifically reset any hardware peripherals. This bit is automatically cleared after the reset.
2	DSPDIS	When set, disables the signal processing software routines. The CPU continues to run at full speed, but only to perform supervisory functions (such as servicing the SPI port).
1	LOWPM	When set, causes the CPU to switch its clock source from the external crystal to an internal ring oscillator that operates at a nominal frequency of 1MHz. In this mode, the CPU continues to run, but the host must reconfigure the parameters configured for crystal operation (such as filter settings, timeouts, and pulse widths).

Operating Mode Register 1 (OPMODE1) (0x002)

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	—	CRCEN	POPOL	CONCFG	
Reset:	0	0	0	0	0	0	0x0	

BIT	NAME	FUNCTION
7:4	—	Reserved.
3	CRCEN	If set, a 1-byte CRC is appended to the end of each SPI read and is expected at the end of each SPI write. See the *SPI Communications Protocol* section for details about how to use the CRC byte for error checking on the SPI bus.
2	POPOL	This bit sets the polarity of the output pulse generators. If clear, the pulse outputs are active low; that is, they remain in the high state until a pulse event occurs, at which time they switch low for one pulse-width interval before reverting to the high state. If set, the pulse outputs are active high; that is, they remain in the low state until a pulse event occurs, at which time they switch to the high state for one pulse-width interval before reverting to the low state.

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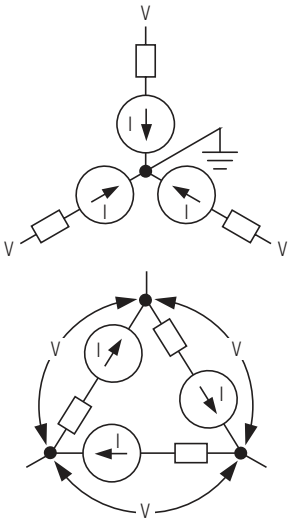
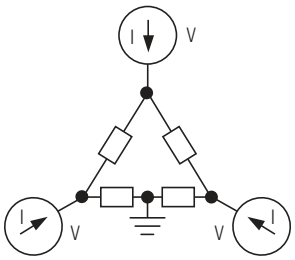
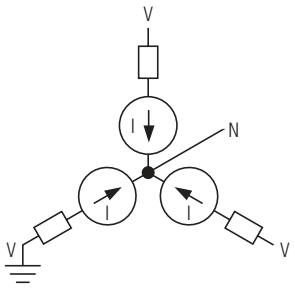
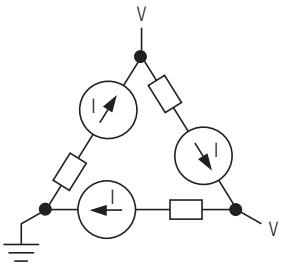
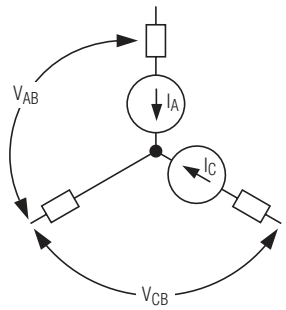
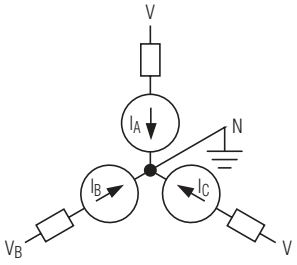
Operating Mode Register 1 (OPMODE1) (0x002) (continued)

BIT	NAME	FUNCTION			
1:0	CONCFG	These bits determine how power is calculated on each of the three phases.			
		00	$P_A = I_A \times V_A$ $P_B = I_B \times V_B$ $P_C = I_C \times V_C$	Use this configuration when the load is connected in a wye arrangement and neutral is connected to MAXQ3181 ground, or when the load is connected in a delta arrangement and isolated voltage and current sensors are used. This arrangement measures power in each load branch rather than power in each source branch.	
		01	$P_A = I_A \times V_A$ $P_B = I_B \times (-V_C)$ $P_C = I_C \times V_C$	Use this configuration when the load is connected in a four-wire delta arrangement. In this arrangement, the BC leg is split and V_{B-N} is expected to be equal to $-V_{C-N}$. Voltages are referenced to neutral.	
		10	$P_A = I_A \times V_A$ $P_B = I_B \times (-V_A - V_C)$ $P_C = I_C \times V_C$	Use this configuration when the load is connected in a four-wire wye arrangement, but only two voltage sensors are available. When connected in this way, phase B is assumed to be ground.	
		11	$P_A = I_A \times V_A$ $P_B = I_B \times (V_A - V_C)$ $P_C = I_C \times V_C$	Use this configuration when the load is connected as a three-wire delta and it is desired to measure the voltage and current inside the delta legs, but to calculate the power in each of the source circuits. When connected this way, source phase B is considered ground.	

Operating Mode Register 2 (OPMODE2) (0x003)

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	—	LINFRM	WIRSYS		APPSEL
Reset:	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION	
7:4	—	Reserved.	
3	LINFRM	Selects the current linearity offset calibration method. See the *Calibrating Current Offset* section for more information. 0 = $\sqrt{IRMS^2 + OFFS}$ 1 = IRMS + OFFS	
2:1	WIRSYS	These bits select the coefficient used in calculating apparent power. 00 = 1-phase, 3-wire (1P3W), or 3-phase, 4-wire (3P4W) (C = 1) 01 = 3-phase, 3-wire (3P3W) (C = √3/2) 10 = three voltages, three currents (3V3A) (C = √3/3)	
		3P3W Wiring (01)	
		3P4W Wiring (00)	

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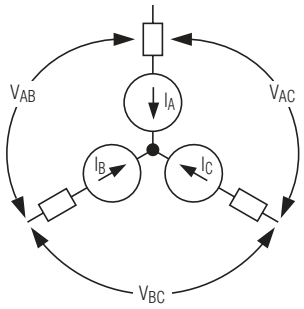
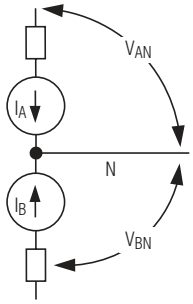
Operating Mode Register 2 (OPMODE2) (0x003) (continued)

BIT	NAME	FUNCTION	
2:1	WIRSYS	3V3A (10)	
		1P3W (00)	
0	APPSEL	Selects the mechanism to use for calculating apparent power.	
		0: $S = V_{RMS} \times I_{RMS}$	Apparent power is calculated by multiplying, on a per-DSP cycle basis, the product of the RMS volts and RMS amps. This bit must be set to 0.

Global Interrupt Registers

Interrupt Request Flag Register (IRQ_FLAG) (0x004)

Bit:	15	14	13	12	11	10	9	8
Name:	DSPOR	DSPRDY	—	DCHA	NOZX	UV	OV	OC
Reset:	0	0	0	0	0	0	0	0

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	—	—	EOVF	CHSCH	PWRF
Reset:	0	0	0	0	0	0	0	0

The interrupt request flag register contains bits that indicate the reason the $\overline{IRQ}$ pin has become active. The active bit must be cleared by the host to avoid continuing firing of the interrupt by the MAXQ3181.

BIT	NAME	FUNCTION
15	DSPOR	When set, the DSP was unable to complete processing one cycle when another cycle was due to begin. This indicates that the R_ADCRATE is set too low, and that samples are arriving more quickly than they can be processed. Increase the value of the R_ADCRATE register to reduce the load on the DSP.
14	DSPRDY	When set, the latest DSP cycle has just completed.
13, 7:3	—	Reserved.
12	DCHA	When set, the direction of real energy flow has changed (that is, from toward the load to away from the load, or from away from the load to toward the load).
11	NOZX	When set, the MAXQ3181 has failed to detect zero crossings on one or more voltage channels for the time defined by the NZX_TIMO register.
10	UV	When set, the absolute instantaneous voltage level in one or more voltage channels failed to exceed the trip level set in the UVLVL (Undervoltage Level) register for one DSP cycle.
9	OV	When set, the absolute instantaneous voltage level in one or more voltage channels has exceeded the trip level set in the OVLVL (Overvoltage Level) register.
8	OC	When set, the absolute instantaneous current in one or more current channels has exceeded the trip level set in the OCLVL (Overcurrent Level) register.
2	EOVF	When set, one or more energy accumulators have an MSB overflow condition.
1	CHSCH	When set, indicates a change of the CHKSUM. The CHKSUM is computed over the configuration and calibration data. The host should review a change in CHKSUM because any change in the configuration or calibration data affects the metering operation and accuracy.
0	PWRF	When set, a power-supply failure is imminent and the supervisory processor should begin taking steps to save its state and prepare for a loss of power.

Interrupt Mask Register (IRQ_MASK) (0x006)

Bit:	15	14	13	12	11	10	9	8
Name:	EDSPOR	EDSPRDY	—	EDCHA	ENOZX	EUV	EOV	EOC
Reset:	0	0	0	0	0	0	0	0

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	—	—	EEOVF	ECHSCH	EPWRF
Reset:	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
15	EDSPOR	When set, the DSPOR flag causes the $\overline{IRQ}$ pin to become active.
14	EDSPRDY	When set, this flag causes the $\overline{IRQ}$ pin to become active.
13, 7:3	—	Reserved.
12	EDCHA	When set, this flag causes the $\overline{IRQ}$ pin to become active when the direction of real energy flow has been observed to have changed (that is, from toward the load to away from the load, or from away from the load to toward the load).
11	ENOZX	When set, this flag causes the $\overline{IRQ}$ pin to become active when the MAXQ3181 has failed to detect zero crossings on one or more voltage channels for at least one DSP cycle.
10	EUV	When set, this flag causes the $\overline{IRQ}$ pin to become active when the absolute instantaneous voltage level in one or more voltage channels failed to exceed the trip level set in the UVLVL (Undervoltage Level) register for one DSP cycle.
9	EOV	When set, this flag causes the $\overline{IRQ}$ pin to become active when the absolute instantaneous voltage level in one or more voltage channels has exceeded the trip level set in the OVLVL (Overvoltage Level) register.
8	EOC	When set, this flag causes the $\overline{IRQ}$ pin to become active when absolute instantaneous current in one or more current channels has exceeded the trip level set in the OCLVL (Overcurrent Level) register.
2	EEOVF	When set, this flag causes the $\overline{IRQ}$ pin to become active when one or more energy accumulators have an overflow condition from their MSB.
1	ECHSCH	When set, this flag enables the $\overline{IRQ}$ pin to become active when a CHKSUM change is detected.
0	EPWRF	When set, this flag causes the $\overline{IRQ}$ pin to become active when a power-supply failure is imminent and the supervisory processor should begin taking steps to save its state and prepare for a loss of power.

Meter Pulse Configuration

Pulse Configuration—CFP Output (PLSCFG1) (0x01E)

Bit:	7	6	5	4	3	2	1	0
Name:	QNSEL					PHASEC	PHASEB	PHASEA
Reset:	0x0					0	0	0

This register selects which phases are included in the CFP pulse output and also selects which quantity is accumulated to drive the pulse output.

BIT	NAME	FUNCTION
7:3	QNSEL	CFP Pulse Output Source Select. This five-bit field determines what meter value will be accumulated in each of the phases to produce the CFP pulse output. All other values are reserved. 00000 = Net real energy 00001 = Absolute real energy 00100 = Apparent energy 00110 = I_{RMS} 00111 = V_{RMS} 01000 = Real energy delivered to load 01001 = Real energy delivered to line
2	PHASEC	CFP Phase C Inclusion. When this bit is set, phase C is included in CFP pulse generation.
1	PHASEB	CFP Phase B Inclusion. When this bit is set, phase B is included in CFP pulse generation.
0	PHASEA	CFP Phase A Inclusion. When this bit is set, phase A is included in CFP pulse generation.

CFP Pulse Width (PLS1_WD) (0x020)

Bit:	15	14	13	12	11	10	9	8
Name:	CFP Pulse-Width High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	CFP Pulse-Width Low Byte							
Reset:	0x9C							

This register designates the width of the CFP pulse, that is, the duration of the period that the CFP pulse is in the active state. This value is given in ADC frame times (about 320µs). The default value of 0x9C (156 decimal) provides a pulse width of about 50ms.

CFP Pulse Threshold (THR1) (0x022)

Bit:	31	30	29	28	27	26	25	24
Name:	THR1 Byte 3							
Reset:	0x00							

Bit:	23	22	21	20	19	18	17	16
Name:	THR1 Byte 2							
Reset:	0x10							

Bit:	15	14	13	12	11	10	9	8
Name:	THR1 Byte 1							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	THR1 Byte 0							
Reset:	0x00							

This register designates the threshold of the CFP pulse. This value is used to set the meter constant for the CFP pulse output. When the CFP pulse accumulator exceeds the value set in this register, the CFP pulse output is activated and the CFP pulse accumulator is reduced by the amount in this register.

Calibration Registers

Current Gain, Phase X = A/B/C/N (X.I_GAIN) (A: 0x130, B: 0x21C, C: 0x308, N: 0x12E)

Bit:	15	14	13	12	11	10	9	8
Name:	Current Gain Coefficient High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Current Gain Coefficient Low Byte							
Reset:	0x00							

This register contains gain coefficient for phase X current channel. The raw values are taken from the selected measurement quantity and scaled by the factor:

$$\frac{X.I\_GAIN}{2^{14}}$$

Note: Bit 15 of this register must be set to zero for correct operation.

Voltage Gain, Phase X = A/B/C (X.V_GAIN) (A: 0x132, B: 0x21E, C: 0x30A)

Bit:	15	14	13	12	11	10	9	8
Name:	Voltage Gain Coefficient High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Voltage Gain Coefficient Low Byte							
Reset:	0x00							

This register contains gain coefficient for phase X voltage channel. The raw values are taken from the selected measurement quantity and scaled by the factor:

$$\frac{X.V\_GAIN}{2^{14}}$$

Note: Bit 15 of this register must be set to zero for correct operation.

Energy Gain, Phase X = A/B/C (X.E_GAIN) (A: 0x134, B: 0x220, C: 0x30C)

Bit:	15	14	13	12	11	10	9	8
Name:	Energy Gain Coefficient High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Energy Gain Coefficient Low Byte							
Reset:	0x00							

This register contains gain coefficient for phase X energy. The raw values are taken from the selected measurement quantity and scaled by the factor:

$$\frac{X.E\_GAIN}{2^{14}}$$

Note: Bit 15 of this register must be set to zero for correct operation.

Phase-Angle Compensation, High Range, Phase X = A/B/C (X.PA0) (A: 0x13E, B: 0x22A, C: 0x316)

Bit:	15	14	13	12	11	10	9	8
Name:	Phase-Angle Offset High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Phase-Angle Offset Low Byte							
Reset:	0x00							

This signed register contains the angle as a fraction of one radian to add to the measured phase angle when the measured current is above the value given in I1THR. This signed value ranges from -0.5 radian (at a value of 0x8000) to +(0.5 - 2^{-16}) radian (at a value of 0x7FFF).

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Phase-Angle Compensation, Medium Range, Phase X = A/B/C (X.PA1) (A: 0x140, B: 0x22C, C: 0x318)

Bit:	15	14	13	12	11	10	9	8
Name:	Phase-Angle Offset High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Phase-Angle Offset Low Byte							
Reset:	0x00							

This signed register contains the angle, as a fraction of one radian, to add to the measured phase angle when the measured current is between the values given in I1THR and I2THR. This signed value ranges from -0.5 radian (at a value of 0x8000) to +(0.5 - 2^{-16}) radian (at a value of 0x7FFF).

Phase-Angle Compensation, Low Range, Phase X = A/B/C (X.PA2) (A: 0x142, B: 0x22E, C: 0x31A)

Bit:	15	14	13	12	11	10	9	8
Name:	Phase-Angle Offset High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Phase-Angle Offset Low Byte							
Reset:	0x00							

This signed register contains the angle, as a fraction of one radian, to add to the measured phase angle when the measured current is below the value given in I2THR. This signed value ranges from -0.5 radian (at a value of 0x8000) to +(0.5 - 2^{-16}) radian (at a value of 0x7FFF).

Limit Registers

Overcurrent Level (OCLVL) (0x044)

Bit:	15	14	13	12	11	10	9	8
Name:	Overcurrent Level High Byte							
Reset:	0xFF							

Bit:	7	6	5	4	3	2	1	0
Name:	Overcurrent Level Low Byte							
Reset:	0xFF							

This register specifies the fraction of full-scale current that is declared to be an overcurrent condition. When X.IRMS exceeds this level for one DSP cycle, the OCF flag in the X.FLAGS register is set. If the OCM flag is set in the X.MASK register, setting the OCF flag will cause the interrupt bit OC to be set in the IRQ_FLAG register. If the interrupt is enabled, the interrupt pin is driven active. Full scale is represented by 0x10000. The maximum value for this register is 0xFFFF.

Overvoltage Level (OVLVL) (0x046)

Bit:	15	14	13	12	11	10	9	8
Name:	Overvoltage Level High Byte							
Reset:	0xFF							

Bit:	7	6	5	4	3	2	1	0
Name:	Overvoltage Level Low Byte							
Reset:	0xFF							

This register specifies the fraction of full-scale voltage that is declared to be an overvoltage condition. When X.VRMS exceeds this level for one DSP cycle, the OVF flag in the X.FLAGS register is set. If the OVM flag is set in the X.MASK register, setting the OVF flag will cause the interrupt bit OV to be set in the IRQ_FLAG register. If the interrupt is enabled, the interrupt pin is driven active. Full scale is represented by 0x10000. The maximum value for this register is 0xFFFF.

Undervoltage Level (UVLVL) (0x048)

Bit:	15	14	13	12	11	10	9	8
Name:	Undervoltage Level High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Undervoltage Level Low Byte							
Reset:	0x00							

This register specifies the fraction of full-scale voltage below which an undervoltage condition is declared. When X.VRMS falls below this level for one DSP cycle, the UVF flag in the X.FLAGS register is set. If the UVM flag is set in the X.MASK register, setting the UVF flag will cause the interrupt bit UV to be set in the IRQ_FLAG register. If the interrupt is enabled, the interrupt pin is driven active. Full scale is represented by 0x10000. The maximum value for this register is 0xFFFF.

No-Load Level (NOLOAD) (0x04A)

Bit:	15	14	13	12	11	10	9	8
Name:	No-Load Level High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	No-Load Level Low Byte							
Reset:	0x03							

This register specifies the fraction of full-scale current below which a no-load condition is declared. When X.IRMS falls below this level, the MAXQ3181 no longer accumulates power for phase X. Full scale is represented by 0x10000. The maximum value for this register is 0xFFFF.

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Phase Status Registers

Interrupt Flags, Phase X = A/B/C (X.FLAGS) (A: 0x144, B: 0x230, C: 0x31C)

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	DCHAF	NOZXF	UVF	OVF	OCF
Reset:	0	0	0	0	0	0	0	0

The X.FLAGS register contains condition flags that relate to the function of phase X (A/B/C) measurements. Once set, these bits can be cleared only by the host.

BIT	NAME	FUNCTION
7:5	—	Reserved.
4	DCHAF	Real Energy Direction Change. Set when the direction of real power flow changes (from toward the load to toward the line, or from toward the line to toward the load). If the DCHAM bit is set, this bit sets the DCHA flag in the IRQ_FLAG register.
3	NOZXF	No-Zero Crossing. Set when the voltage waveform in phase X fails to exhibit a zero crossing during NZX_TIMO of the ADC sample periods. If the NOZXM bit is set, this bit sets the NOZX flag in the IRQ_FLAG register.
2	UVF	Undervoltage. Set when the RMS voltage in phase X falls below the undervoltage threshold set in UVLVL. If the UVM bit is set, this bit sets the UV flag in the IRQ_FLAG register.
1	OVF	Overvoltage. Set when the RMS voltage in phase X exceeds the overvoltage threshold set in OVLVL. If the OVM bit is set, this bit sets the OV flag in the IRQ_FLAG register.
0	OCF	Overcurrent. Set when the RMS current in phase X exceeds the overcurrent threshold set in OCLVL. If the OCM bit is set, this bit sets the OC flag in the IRQ_FLAG register.

Interrupt Mask, Phase X = A/B/C (X.MASK) (A: 0x145, B: 0x231, C: 0x31D)

Bit:	7	6	5	4	3	2	1	0
Name:	—	DIR_A	—	DCHAM	NOZXM	UVM	OVM	OCM
Reset:	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
7, 5	—	Reserved.
6	DIR_A	Active Energy Direction Status 0 = positive 1 = negative
4	DCHAM	Real Energy Direction Change Mask. If set, a change in real power direction on phase X causes the DCHA flag in the IRQ_FLAG register to be set.
3	NOZXM	No-Zero Crossing Mask. If set, a no-zero crossing on phase X causes the NOZX flag in the IRQ_FLAG register to be set.
2	UVM	Undervoltage Mask. If set, an undervoltage condition on phase X causes the UV flag in the IRQ_FLAG register to be set.
1	OVM	Overvoltage Mask. If set, an overvoltage condition on phase X causes the OV flag in the IRQ_FLAG register to be set.
0	OCM	Overcurrent Mask. If set, an overcurrent condition on phase X causes the OC flag in the IRQ_FLAG register to be set.

Energy Overflow Flags, Phase X = A/B/C (X.EOVER) (A: 0x146, B: 0x232, C: 0x31E)

Bit:	7	6	5	4	3	2	1	0
Name:	—	—	—	SOV	—	—	ANOV	APOV
Reset:	0	0	0	0	0	0	0	0

These bits indicate that an overflow condition has occurred on an energy accumulator. An overflow condition is **not** an error condition. Rather, it simply indicates that the value in the energy accumulator could be smaller than the previous reading due to the overflow in the counter. To obtain the actual energy usage since the previous reading, 0x100000000 must be added to the difference. These bits, once set, can be cleared only by the host.

BIT	NAME	FUNCTION
7:5, 3:2	—	Reserved.
4	SOV	When set, indicates an overflow condition on the apparent energy accumulator.
1	ANOV	When set, indicates an overflow condition on the real negative energy accumulator.
0	APOV	When set, indicates an overflow condition on the real positive energy accumulator.

Measurements

Line Frequency (LINEFR) (0x062)

Bit:	15	14	13	12	11	10	9	8
Name:	Line Frequency High Byte							
Reset:								

Bit:	7	6	5	4	3	2	1	0
Name:	Line Frequency Low Byte							
Reset:								

Line frequency, LSB = 0.001Hz.

Power Factor, Phase X = A/B/C (X.PF) (A: 0x1C6, B: 0x2B2, C: 0x39E)

Bit:	15	14	13	12	11	10	9	8
Name:	Power Factor High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Power Factor Low Byte							
Reset:	0x00							

Power factor of phase A/B/C, LSB = $1/2^{14}$. Note that the power factors are signed integers, and a negative value indicates a reversed power flow direction.

RMS Voltage, Phase X = A/B/C (X.VRMS) (A: 0x1C8, B: 0x2B4, C: 0x3A0)

Bit:	31	30	29	28	27	26	25	24
Name:	RMS Voltage Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	RMS Voltage Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	RMS Voltage Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	RMS Voltage Byte 0							

This register provides the raw RMS voltage over the most recent DSP cycle, LSB = $V_{FS}/2^{24}$.

RMS Current, Phase X = A/B/C (X.IRMS) (A: 0x1CC, B: 0x2B8, C: 0x3A4)

Bit:	31	30	29	28	27	26	25	24
Name:	RMS Current Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	RMS Current Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	RMS Current Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	RMS Current Byte 0							

This register provides the raw RMS current over the most recent DSP cycle, LSB = $I_{FS}/2^{24}$.

Energy, Real Positive, Phase X = A/B/C (X.EAPOS) (A: 0x1E8, B: 0x2D4, C: 0x3C0)

Bit:	31	30	29	28	27	26	25	24
Name:	Real Energy Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	Real Energy Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	Real Energy Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	Real Energy Byte 0							

On every DSP cycle, the contents of the X.ACT register are tested, and, if positive, are added to this register. When this register overflows, the APOV bit in the X.EOVER register is set.

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Energy, Real Negative, Phase X = A/B/C (X.EANEG) (A: 0x1EC, B: 0x2D8, C: 0x3C4)

Bit:	31	30	29	28	27	26	25	24
Name:	Real Energy Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	Real Energy Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	Real Energy Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	Real Energy Byte 0							

On every DSP cycle, the contents of the X.ACT register are tested, and, if negative, absolute values are added to this register. When this register overflows, the ANOV bit in the X.EOVER register is set.

Energy, Apparent, Phase X = A/B/C (X.ES) (A: 0x1F8, B: 0x2E4, C: 0x3D0)

Bit:	31	30	29	28	27	26	25	24
Name:	Apparent Energy Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	Apparent Energy Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	Apparent Energy Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	Apparent Energy Byte 0							

On every DSP cycle, the contents of the X.APP register are added to this register. When this register overflows, the SOV bit in the X.EOVER register is set.

Virtual Register Conversion Coefficients

Voltage Units Conversion Coefficient (VOLT_CC) (0x014)

Bit:	15	14	13	12	11	10	9	8
Name:	Voltage Units Conversion Coefficient High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Voltage Units Conversion Coefficient Low Byte							
Reset:	0x01							

This register contains the value by which the raw voltage value in each phase (A.VRMS, B.VRMS, and C.VRMS) is multiplied before being presented to the virtual RMS voltage registers (V.A, V.B, and V.C).

To determine the value of VOLT_CC, a voltage value for the least significant bit (VOLT_LSB) of the V.X registers must be selected. Typical values might range from 1mV to 1nV. To avoid significant conversion loss, VOLT_LSB should be chosen such that VOLT_CC is >1000. Once VOLT_LSB is determined, calculate VOLT_CC from the following equation:

$$VOLT\_CC = \frac{V_{FS}}{2^{24} \times VOLT\_LSB}$$

Current Units Conversion Coefficient (AMP_CC) (0x016)

Bit:	15	14	13	12	11	10	9	8
Name:	Current Units Conversion Coefficient High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Current Units Conversion Coefficient Low Byte							
Reset	0x01							

This register contains the value by which the raw current value in each phase (A.IRMS, B.IRMS, C.IRMS, and N.IRMS) is multiplied before being presented to the virtual RMS current registers (I.A, I.B, I.C, and I.N). To determine the value of AMP_CC, a current value for the least significant bit (AMP_LSB) of the I.X registers must be selected. Typical values might range from 1nA to 10µA. To avoid significant conversion loss, AMP_LSB should be chosen such that AMP_CC is >1000. Once determined, calculate AMP_CC from the following equation:

$$AMP\_CC = \frac{I_{FS}}{2^{24} \times AMP\_LSB}$$

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Power Units Conversion Coefficient (PWR_CC) (0x018)

Bit:	15	14	13	12	11	10	9	8
Name:	Power Units Conversion Coefficient High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Power Units Conversion Coefficient Low Byte							
Reset:	0x01							

This register contains the value by which the raw power value in each phase is multiplied before being presented to the virtual power registers. The table below lists the raw power registers and the corresponding virtual registers.

DESCRIPTION	RAW	VIRTUAL
Real power, phase A	A.ACT	PWRP.A
Real power, phase B	B.ACT	PWRP.B
Real power, phase C	C.ACT	PWRP.C
Real power, total	—	PWRP.T
Apparent power, phase A	A.APP	PWRS.A
Apparent power, phase B	B.APP	PWRS.B
Apparent power, phase C	C.APP	PWRS.C
Apparent power, total	—	PWRS.T

PWR_CC establishes the amount of power represented by one PWR_LSB of the power registers. To avoid significant conversion loss, PWR_LSB should be chosen such that PWR_CC is > 1000. Calculate the value of PWR_CC according to the following formula:

$$PWR\_CC = \frac{I_{FS} \times V_{FS}}{2^{32} \times PWR\_LSB}$$

Energy Units Conversion Coefficient (ENR_CC) (0x01A)

Bit:	15	14	13	12	11	10	9	8
Name:	Energy Units Conversion Coefficient High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Energy Units Conversion Coefficient Low Byte							
Reset:	0x01							

This register contains the value by which the raw accumulated energy value in each phase is multiplied before being presented to the virtual energy registers. The table below lists the raw energy accumulators and the corresponding virtual registers.

DESCRIPTION	RAW	VIRTUAL
Real energy, phase A, positive direction	A.EAPOS	ENRP.A*
Real energy, phase A, reverse direction	A.EANEG	
Real energy, phase B, positive direction	B.EAPOS	ENRP.B*
Real energy, phase B, reverse direction	B.EANEG	
Real energy, phase C, positive direction	C.EAPOS	ENRP.C*
Real energy, phase C, reverse direction	C.EANEG	
Real energy, total	—	ENRP.T
Apparent energy, phase A	A.ES	ENRS.A
Apparent energy, phase B	B.ES	ENRS.B
Apparent energy, phase C	C.ES	ENRS.C
Apparent energy, total	—	ENRS.T

**These registers represent the algebraic sum of the positive and reverse energy in the two "raw" registers noted. Thus, the energy returned in these virtual registers represents the net energy.*

To avoid significant conversion loss, ENR_LSB should be chosen such that ENR_CC is > 1000. Calculate the value of ENR_CC according to the following formula:

$$ENR\_CC = \frac{I_{FS} \times V_{FS} \times t_{FR}}{2^{16} \times ENR\_LSB}$$

Low-Power, Active Energy, Polyphase AFE

Virtual Registers

The virtual registers are calculated values derived from one or more real registers. They are calculated at the time they are requested, and thus could involve additional time to return a value. Most virtual registers are 8 bytes in length and are delivered least significant byte first.

Power

Real Power, Phase X = A/B/C/T (PWRP.X) (A: 0x801, B: 0x802, C: 0x804, T: 0x807)

This signed register contains the real instantaneous power delivered into phase A/B/C or total. Power is calculated from the instantaneous energy measurement according to the following equation:

$$PWRP.X = \frac{X.ACT \times PWR\_CC \times 2^{16}}{NS}$$

The register is 8 bytes long, but the most significant 2 bytes are not used. See the PWR_CC register description for more details.

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

Note that the sign bit is bit 47 for all 8-byte signed virtual registers.

Apparent Power, Phase X = A/B/C/T (PWRS.X) (A: 0x821, B: 0x822, C: 0x824, T: 0x827)

This register contains the apparent instantaneous power delivered into phase A/B/C or total. Power is calculated from the instantaneous energy measurement according to the following equation:

$$PWRS.X = \frac{X.APP \times PWR\_CC \times 2^{16}}{NS}$$

The register is 8 bytes long, but the most significant 2 bytes are not used. See the PWR_CC register description for more details.

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

Voltage and Current

RMS Volts, Phase X = A/B/C (V.X) (A: 0x831, B: 0x832, C: 0x834)

This register contains the RMS voltage on phase A/B/C. The units are defined by the VOLT_CC setting such that V.X = X.VRMS x VOLT_CC. In this equation, VOLT_CC is the conversion coefficient. See the VOLT_CC register for more information.

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

RMS Amps, Phase X = A/B/C/N (I.X) (A: 0x841, B: 0x842, C: 0x844, N: 0x840)

This register contains the RMS current on phase A/B/C or the neutral channel. The units are defined by the AMP_CC setting such that I.X = X.IRMS x AMP_CC. In this equation, AMP_CC is the conversion coefficient. See the AMP_CC register for more information.

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

Power Factor

Power Factor (PF.T) (0x867)

This signed register contains the power factor of the total power. The power factor is calculated as:

$$PF.T = \frac{A.ACT + B.ACT + C.ACT}{A.APP + B.APP + C.APP}$$

It is expressed in units of 0.00001; thus, unity power factor is expressed as decimal 100,000 (0x00000000000186A0). This register is presented as a two's complement value, so that a load delivering real power to the line (that is, reverse power) is seen as having a power factor of -1 (0x0000FFFFFFFE7960).

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

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Energy

Real Energy, Phase A/B/C/T (ENRP.X) (A: 0x8C1, B: 0x8C2, C: 0x8C4, T: 0x8C7)

This signed register contains the real accumulated energy delivered into phase A/B/C or total. The register is calculated according to the following formula:

ENRP.X = ENR_CC x (X.EAPOS - X.EANEG)

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

Apparent Energy, Phase A/B/C/T (ENRS.X) (A: 0x871, B: 0x872, C: 0x874, T: 0x877)

This register contains the apparent accumulated energy delivered into phase A/B/C or total. The register is the product of the ENR_CC and X.ES registers.

Byte 7 (MSByte unused)	Byte 6 (unused)
Byte 5	Byte 4
Byte 3	Byte 2
Byte 1	Byte 0 (LSByte)

Theory of Operation

Analog Front-End Operation

Whenever the MAXQ3181 is in one of the active operating modes (Run Mode or LOWPM Mode), the analog front-end operates continuously, scanning up to eight scan slots depending on the selected front-end configuration. For each analog scan slot that is enabled, one of the eight differential input pairs is measured.

The SCAN_IX and SCAN_VX (X = A/B/C), SCAN_IN, and SCAN_TE registers contain the settings for each slot, which include whether the slot is enabled and the differential input pair to measure during that scan slot. The logical mapping of the slots is fixed in following order:

- Slot 0—Phase A Current (IA)
- Slot 1—Phase A Voltage (VA)
- Slot 2—Phase C Current (IC)
- Slot 3—Phase C Voltage (VC)
- Slot 4—Phase B Current (IB)
- Slot 5—Phase B Voltage (VB)
- Slot 6—Neutral Current (IN)—disabled by default
- Slot 7—Temperature Measurement—disabled by default

The required time for each analog scan slot measurement (t_C) is determined by the MAXQ3181 system clock frequency and the setting of the R_ADCRATE hardware register, as shown below:

$$t_C = 1/f_{CLK} \times (R\_ADCRATE[8:0] + 1)$$

Using the default register settings (R_ADCRATE = 13Fh = 319d), the time for each analog slot measurement (t_C) is 40µs when the MAXQ3181 is running at 8MHz. Since there are eight analog scan slots in the measurement frame, the total time for all measurements (t_{FR}) is t_C x 8. Using the default settings with the MAXQ3181 running at 8MHz, the entire sequence of measurements takes 320µs to complete, which, in turn, means that 320µs will elapse, for example, between one phase A current measurement and the next.

Even if some of the analog measurement slots (such as neutral current or temperature measurement) are skipped by setting the DADCNV bit in that slot's register to 1, the time period for that slot will remain in the frame, ensuring that the total frame time is always t_C x 8, regardless of which individual slots are enabled or disabled.

Digital Signal Processing (DSP) Terminology

Establishing the precise definitions of some of the terms used in this document will assist in understanding how the DSP functions.

Sample Period: The amount of time required to measure a single data element; 40µs, by default.

ADC Frame Period: The amount of time required for the ADC to sample all analog inputs; always equal to 8 sample periods. The inverse of this value is the *frame rate*; by default 3125 samples per second. This is the rate at which any particular signal is sampled by the MAXQ3181.

Line Cycle: The period of time from one positive-going zero crossing on a voltage channel to the next positive-going zero crossing. At 50Hz, this is nominally 20ms; at 60Hz, this is nominally 16.67ms.

Cycle Count: The number of line cycles contained in a single DSP cycle. An integer, this is typically set to some value greater than one to minimize the effect of load variations that may not occur in every line cycle. By default, this value is 16.

DSP Cycle: The period of time over which line parameters are calculated. Energy and other parameters are accumulated once per DSP cycle. One DSP cycle is the time of a line cycle multiplied by the cycle count.

NS: This value represents the number of ADC frame periods in a DSP cycle. This is a noninteger calculated value. For example, if the cycle count is set to unity, and the line frequency is exactly 50Hz, the NS value would be 20ms/320µs = 62.5.

Digital Processing

As voltage and current samples are collected, the MAXQ3181 performs a variety of digital filtering, accumulation, and processing calculations to arrive at meter-reading values (such as line frequency, RMS voltage and current, and active power) that can then be read by the master. The MAXQ3181 calculates and detects values and conditions including the following:

- Zero-crossing detection
- Line frequency and line period calculation
- RMS voltage (phase A, phase B, phase C)
- RMS current (phase A, phase B, phase C, neutral current)
- Power (active and apparent) for each phase

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- Energy accumulation (including energy pulse output function)
- Overvoltage detection
- Overcurrent detection
- Undervoltage detection

Per Sample Operations

On every ADC frame, the input samples are processed as follows:

- The voltage and current samples are read. The current sample is shifted to account for the gain applied in the PGA. The phase- and gain-corrected samples are passed to the next stage.
- Both the current and voltage signals are passed through highpass filters (HPF) specified by the HPF_C variable.
- The current and voltage signals are now split into several components. The first of these components is squared and accumulated to begin the RMS current and voltage process. The second is processed and accumulated to begin the real power calculation.

The result is a set of accumulated values that represent squared voltage, squared current, and real (active) energy for both the entire usable spectrum and as filtered by the peak filter. The real energy at this point does not yet represent real power; to obtain usable power values further processing is required. Each of these values is further processed at the end of each DSP cycle.

Per DSP Cycle Operations

At the end of each DSP cycle, accumulated information is available that is used to calculate all other operational results in the meter. DSP cycles track the line frequency and have a duration of the number of cycles specified in the CYCNT register. On each phase, the time required for CYCNT cycles to complete is calculated and this value is used to update the duration of one DSP cycle, specified in the NS register.

NS contains the number of ADC frame periods in a single DSP cycle. Because line frequency varies slightly from cycle to cycle, and because the ADC frame clock is not synchronized to the line, the value of NS is not an integer, and varies slightly from DSP cycle to DSP cycle.

Because the value of NS is so critical to accurate calculation of energy, ensuring that it is correct on every cycle is essential. There are two ways to manage the slight variation of NS from cycle to cycle: first, one could simply replace the old value of NS with the newly calculated value on each DSP cycle. This means that NS (and every other value in the meter, since they depend on NS) would have a significant amount of uncertainty. A better method is to use each newly calculated value of NS as an input to a filter. The *output* of the filter is then the value of NS that is actually used in calculations. In the MAXQ3181, this filter is controlled by the AVG_NS register.

A second problem with updating NS on every line cycles is the fact that noise impulses that occur at nearly the same time as the zero crossing can shift the zero

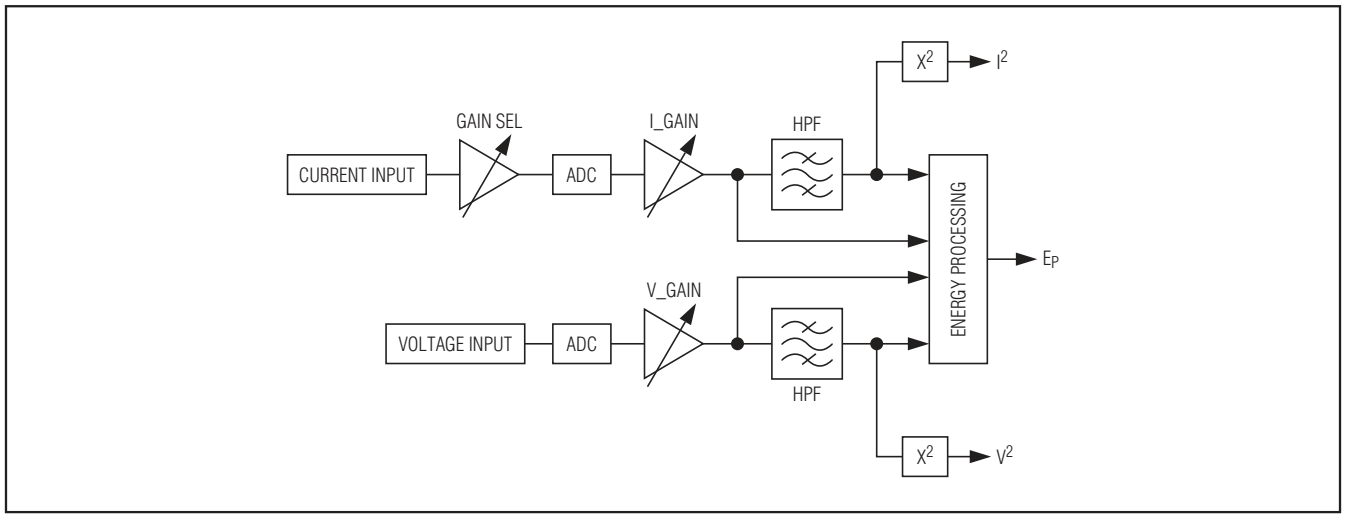

Figure 9. Per Sample Operations

crossing, affecting the accuracy of the energy measured during the preceding period. For this reason, a second register, REJ_NS contains a value that specifies how far a particular sample can deviate from the average and still be considered valid. If the period of the newly acquired DSP cycle differs from the previously accumulated average value by more than REJ_NS ADC frames, NS is not updated with the new period (but the energy is still accumulated).

With this discussion in mind, the signal path for the various reported parameters can be reviewed.

RMS Volts and RMS Amps: First, the squared voltage accumulation is divided by NS. This accomplishes the "mean" part of the "root-mean-square" calculation. Then, the square root of the result is taken, producing the raw RMS calculation value.

On the voltage channel, the signal is ready for gain compensation to be applied. But on the current channel, there is an additional twist: depending on the amplitude of the current, there may be a gain factor pre-applied before the raw sample is available. To compensate for inaccuracy in the gain factor for the amplifier and for noise seen in the channel at high gain settings, it may be necessary to provide linearity compensation.

There are three registers that manage the linearization of the current signal: the X.OFFS_HI (X = A/B/C) register contains a signed value that is added to the raw RMS current signal before further processing; the X.OFFS_LO register contains a signed value that is added to the raw RMS current signal when the current signal is below a low current threshold (1/32 of the full scale) value; and the X.GAIN_LO register contains a gain adjustment that is applied to the current signal when the current signal is below the threshold value.

The practical effect of this is to turn what may be a somewhat nonlinear response curve for the current sensor to a much more linear response by two-piece approximation.

The "high current" calibration term X.OFFS_HI is used so long as the instantaneous current exceeds the low-current threshold at some instant during a DSP cycle. As long as this threshold is crossed during a DSP cycle, the value in X.OFFS_HI controls the offset current.

When the input stays below the low-current threshold for one DSP cycle, the X.OFFS_LO and X.GAIN_LO are applied. The low-current calibration terms (X.GAIN_LO and X.OFFS_LO) remain in effect until the peak of input current waveform exceeds 1/32 of full-scale current at any time during a DSP cycle.

As a final step, both voltage and current are passed through an averaging filter that provides smoothing for the signals. The amount of filtering is given in AVG_C.

Energy: Current sensors and other external circuitry components could introduce a phase distortion to the current signal, and this phase distortion may not be constant at all current values. Consequently, for the most precise measurements, the phase between the voltage and current signals must be compensated. In the MAXQ3181, the energy signals are compensated for phase offset by performing a complex multiplication of the signal with the contents of the appropriate phase offset register.

Determining which phase offset register is appropriate is a matter of comparing the incoming RMS current for the phase with the contents of the I1THR and I2THR registers. It is the responsibility of the administrative software to ensure that I1THR is greater than or equal to I2THR. If the raw RMS current is greater than or equal to the con-

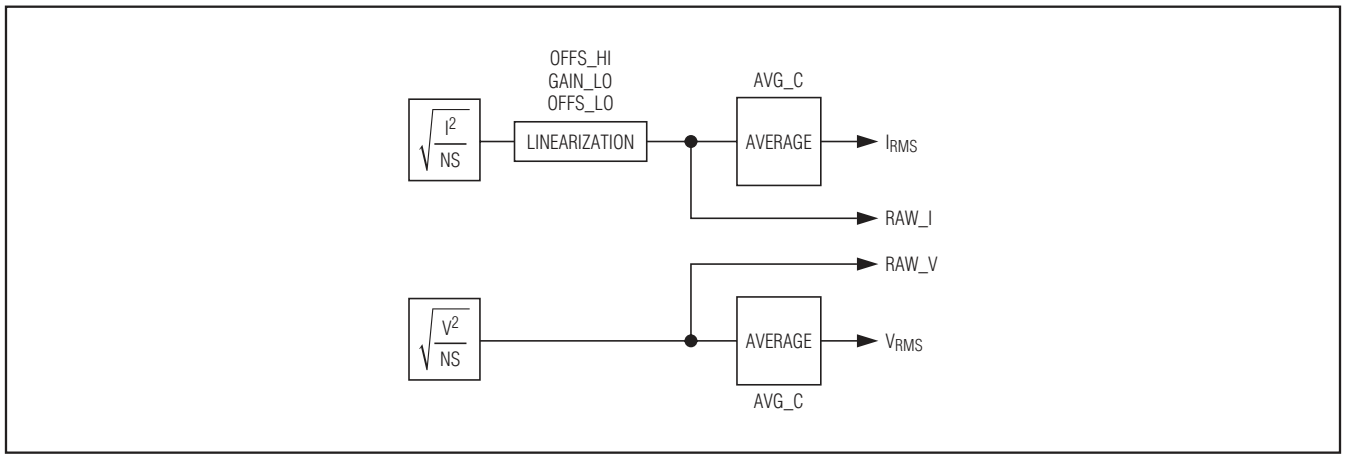

Figure 10. Computation of RMS Values

tents of I1THR, then the angle expressed in PA0 is used to compensate the phase angle. If the raw RMS current is less than I2THR, then the angle expressed in PA2 is used to compensate the phase angle. And if the raw RMS current falls between I1THR and I2THR then PA1 is used to compensate the phase angle. In this way, a three-piece stepwise approximation of the phase response of the current sensor is available.

$$PA = \begin{cases} PA0, I_{RMS} \geq I1THR \\ PA1, I1THR > I_{RMS} \geq I2THR) \\ PA2, I_{RMS} < I2THR \end{cases}$$

To use a constant phase compensation, set I1THR and I2THR to zero and insert the phase compensation value into PA0.

Apparent energy is calculated as the product of the raw RMS volts and amps.

Line Frequency: Line frequency can be taken directly from the NS value. Recall that NS is the number of frames in a DSP cycle. Since each frame is 320µs, simply multiply NS by 320µs and divide by CYCNT to obtain the line period. The reciprocal of this is the line frequency.

Energy Accumulation

Once real energy over the most recent DSP cycle has been calculated, it is necessary to accumulate the result.

The result accumulated during any DSP cycle can be positive (that is, energy is delivered to the load) or negative (that is, energy is driven back into the line). These values are separately accumulated.

Apparent energy is also accumulated, but since this value is always positive or zero, there is only one apparent energy accumulator.

From time to time, the accumulators generate an overflow. When this occurs, the appropriate bit is set in the overflow status register X.EOVER.

When an overflow occurs, supervisory code running on the host processor must make the appropriate adjustments in the reported energy. In many cases, this could simply involve incrementing an overflow counter. The host processor must then clear the overflow indication.

No-Zero-Crossing Detection

The MAXQ3181 monitors the voltage signal on each phase for zero-crossing events. If no ascending zero crossings are detected within a specified number (NZX_TIMO) of analog scan sample periods, the NOZXF (X.FLAGS) flag is set by the MAXQ3181 to notify the master of this condition. If the NOZXM bit is set, this flag sets the NOZX bit in the IRQ_FLAG. If the interrupt enable bit ENOZX is set to 1, the interrupt signal $\overline{IRQ}$ is driven low by the MAXQ3181 whenever NOZX = 1. The master can clear NOZXF and NOZX back to 0 to remove the interrupt condition.

Phase Sequence Status

A phase sequence status bit PHSEQ indicates the order in which zero crossings are detected. When a zero-crossing event occurs on the phase A voltage signal, followed by phase B, phase C, and then phase A

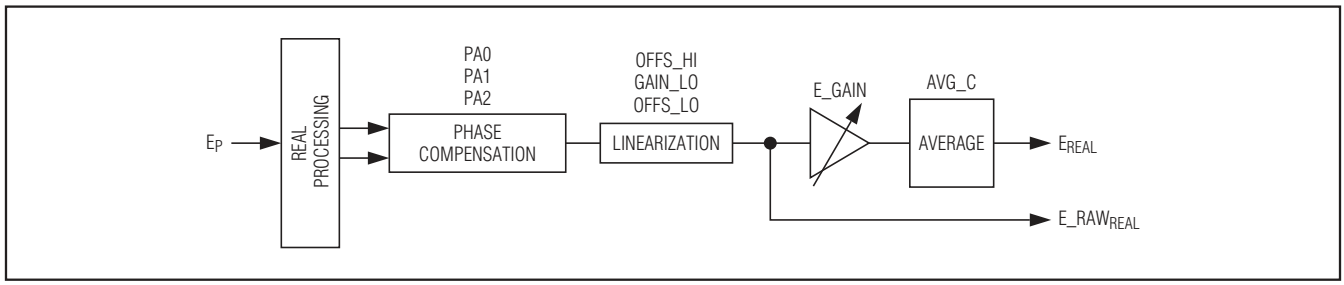

Figure 11. Phase Compensation for Energy Calculations

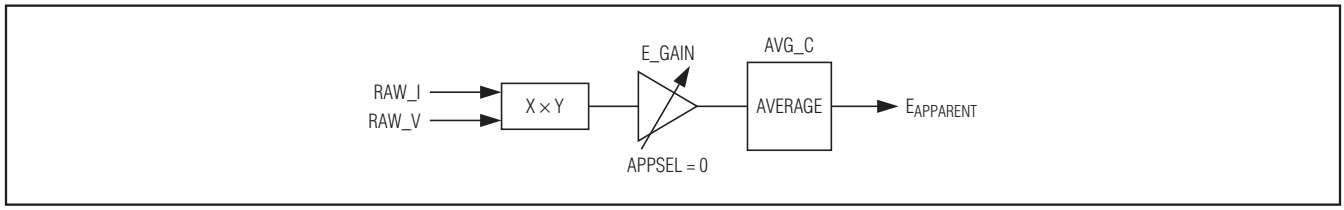

Figure 12. Apparent Energy Calculations

again, this bit cleared. If a zero crossing on phase A is then followed by a zero crossing on phase C, then phase B, this bit set to 1.

Power Calculation (Active and Apparent)

The power, energy, and RMS calculation process consists of two tasks: continuous accumulation and postprocessing triggered every CYCNT line cycles. The accumulation task accumulates raw data obtained from the AFE during CYCNT line cycles. This task is performed continuously in the background by the MAXQ3181. When a CYCNT line cycles accumulation stage has completed, which is determined by a dedicated frame counter exceeding the NS level, the raw integral accumulator values are saved for postprocessing and cleared, beginning the next cycle of accumulation task. Then, the DSP postprocessing is triggered to process saved integrals and calculate energy, power, etc., values. Note that the background accumulation task continues while foreground postprocessing is taking place, i.e., both tasks are executed simultaneously sharing CPU time. It is essential that the DSP postprocessing calculations be completed before the next DSP trigger to avoid losing accumulated data. The master should allow enough processing time by adjusting the R_ADCRATE register. Default settings provide plenty of CPU time for both tasks.

The MAXQ3181 accumulates raw sums and calculates line-cycle integrals for each voltage-current pair separately. The individual power accumulators are:

- $PA = V_A \times I_A$
- $PB = I_B \times V_B$ or $-I_B \times V_C$ or $-I_B \times (V_A + V_C)$ or $-I_B \times (V_A - V_C)$
- $PC = V_C \times I_C$

The PA and PC accumulators always operate in a single mode: ($V_A \times I_A$) for the PA accumulator, ($V_C \times I_C$) for the PC accumulator. Alternately, the operating mode of the PB accumulator is defined by setting the CONCFG[1:0] bits in the OPMODE1 register.

Energy Accumulation Start Delay

All filters have a certain settling time before accurate energy readings can be accumulated. To avoid accumulation of invalid data from filters that are still settling, an energy accumulation timeout period can be set in the ACC_TIMO register. When ACC_TIMO > 0, computed energy is not accumulated for ACC_TIMO of DSP cycles. The MAXQ3181 will decrement the ACC_TIMO register every DSP cycle until it becomes 0. When ACC_TIMO reaches 0 value, energy accumulation begins (or resumes, if ACC_TIMO was set to nonzero value by the master). Pulse outputs are also disabled when ACC_TIMO > 0. The default value of ACC_TIMO is 0x05.

No-Load Feature

To avoid “meter creep,” no energy accumulation should take place when measured current is less than a certain threshold. The NOLOAD register can be programmed to enable and configure this feature. If the measured X.IRMS value for a phase (A, B, or C) falls below the NOLOAD threshold, the energy accumulators for this phase are not incremented. Setting NOLOAD = 0 disables this feature. Full scale is represented by 0x10000.

On Demand Calculations

So far in this discussion, the values being calculated and managed in the MAXQ3181 have been based on fundamental units meaningful to the device itself: voltage as a binary fraction of full-scale voltage; current as a binary fraction of full-scale current, and time as a noninteger multiple of the ADC frame time.

But a practical electricity meter must report its results in standard units, such as volts, amperes, and watts. The MAXQ3181 contains a mechanism to convert the internal units (“meter units”) to real world units (“display units”). This conversion is performed in the conversion constant (CC) registers.

For some of these values (voltage, current) the calculation is simple: multiply by the conversion constant. For other values (power, energy) the calculation is more complex. In any case, the value in the CC register affects only the conversion from a meter unit to a display unit; calibration is handled separately in the gain adjustment registers for each recorded value.

The results of all on-demand calculations are reported as 8-byte (64-bit) values of which no more than 6 bytes (48 bits) are significant. Eight bytes are used as a common length; however, fewer bytes can be requested for those registers known to have smaller maximum values. For example, the power factor virtual register has a maximum value that is expressed in only 3 bytes; consequently, the register can be requested with a length of 4 bytes without loss of data.

RMS Volts, RMS Amps

These registers (V.A, V.B, V.C, I.A, I.B, I.C) are calculated by simply multiplying the calculated RMS value (A.VRMS, B.VRMS, C.VRMS, A.IRMS, B.IRMS, C.IRMS) by the contents of the VOLT_CC or AMP_CC register. Since the RMS voltage and RMS current are given in 32-bit registers and the conversion coefficients are given in 16-bit registers, the result of the product is 48 bits.

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Regardless of the internal units used, VOLT_CC and AMP_CC can be tailored so that the LSB of the virtual register can be any value. For example, if one wished to have a 32-bit value representing milliamps, one could multiply by a value that scaled the register such that the LSB was 2^{-16}mA. Then, discard the low-order 16 bits. The result is milliamps with 32 bits of precision; thus, the maximum current that could be represented would be 4,294,967,296mA, or just over 4MA.

The VOLT_CC and AMP_CC values can be calculated from the full-scale voltage or full-scale current and the desired value of one LSB in the display register:

$$AMP\_CC = \frac{I_{FS}}{2^{24} \times AMP\_LSB}$$

$$VOLT\_CC = \frac{V_{FS}}{2^{24} \times VOLT\_LSB}$$

Example: Assume the full-scale current is 102.4A, and that we desire a 1nA LSB. The calculation would provide an AMP_CC value of:

$$102.4/(2^{24} \times 10^{-9}) = 6104 = 0x17D8$$

Power

The MAXQ3181 measures energy. But power is just energy per unit time, and the MAXQ3181 keeps track of the time unit over which energy is accumulated. This is simply the NS value, the fractional number of samples that comprises one DSP cycle. So converting energy to power is as simple as dividing the accumulated energy over one DSP cycle by NS. Multiplying by a conversion constant (PWR_CC) gives power in user-established units.

The power registers (PWRP.A, PWRP.B, PWRP.C, PWRS.A, PWRS.B, PWRS.C) are calculated by multiplying the accumulated energy (A.ACT, A.APP, B.ACT, B.APP, C.ACT, C.APP) by the conversion coefficient (PWR_CC) and then dividing by NS. The result is the 48-bit average power over the most recent DSP cycle, in units established by the conversion coefficient.

The PWR_CC value can be calculated from the full-scale voltage, the full-scale current, and the desired value of one LSB in the display register:

$$PWR\_CC = \frac{I_{FS} \times V_{FS}}{2^{32} \times PWR\_LSB}$$

Example: For this example, assume the full-scale current is 102.4A, the full-scale voltage is 558.1V, and that the desired LSB is milliwatts after discarding the 16 LSB; that is, the desired LSB is 2^{-16} milliwatts. Perform the following calculation:

$$102.4 \times 558.1/(2^{32} \times 2^{-16} \times 10^{-3}) = 872 = 0x0368$$

Power Factor

Power factor is calculated as real power divided by apparent power. Apparent power is computed as the product of the RMS voltage and current measurement.

The power factor is multiplied by 2^{14} before it is reported; thus, unity power factor is given by 16,384 decimal (0x4000).

Line Frequency

The line frequency is derived directly from the mean NS values over the three phases. It is reported as millihertz; thus, a 50Hz line frequency is reported as decimal 50,000 (0xC350).

Energy

Energy is read as the net energy directly scaled from the appropriate registers. For example, the energy read from the ENRP.A register (real energy, phase A) is composed of the difference between the A.EAPOS (real energy, positive direction, phase A) and A.EANEG (real energy, negative direction, phase A) registers scaled by the ENR_CC register.

Note that the energy registers (ENRP.A, ENRP.B, ENRP.C, ENRP.T, ENRS.A, ENRS.B, ENRS.C, ENRS.T) represent the energy, in every case, since the last overflow event. For this reason, software must keep track of overflow and make adjustments accordingly when using this register set.

To calculate the ENR_CC register value, begin with the full-scale voltage and full-scale current, the frame time, and the desired LSB value for energy. Then perform the following calculation:

$$ENR\_CC = \frac{I_{FS} \times V_{FS} \times t_{FR}}{2^{16} \times ENR\_LSB}$$

Example: It is essential to ensure that the correct units are maintained throughout the calculation. In this example, assume that the full-scale voltage is 558.1V, the full-scale current is 102.4A, the frame time is the default of 320µs, and the desired LSB is 100 milliwatt-hours after the 32 bits are discarded; that is, the LSB is 0.1 x 2^{-32} watt-hours. Notice, however, that the frame time is given in microseconds *and must be converted to hours* before the calculation can be performed: 320µs is 88.9 x 10^{-9} hours. So the calculation proceeds as follows:

$$102.4 \times 558.1 \times 88.9 \times 10^{-9}/(2^{16} \times 0.1 \times 2^{-32}) = 3329 = 0x0D01$$

Meter Pulse

The purpose of a meter pulse is generally to advance a mechanical counter when such a device is used as a display. Meter pulses are also used during calibration since time intervals can be measured with great precision.

The MAXQ3181 supports one meter pulse output. This output can be configured for either active positive or active negative pulses by means of the POPOL bit in the OPMODE1 register. When triggered, the pulse goes to its active state and remains there for a period of time defined by the PLS1_WD register, and then returns to the inactive state (unless triggered again).

The PLS1_WD register contains the time in ADC frame periods that the pulses remain in the active state when triggered. By default, this register contains decimal 156 (0x9C) giving, at the default frame rate, a pulse width of 50ms.

Among the quantities that can be accumulated by the pulse subsystem are the arithmetic active energy (that is, the accumulated positive real energy minus the accumulated negative real energy) and the absolute active energy (that is, accumulated positive real energy plus accumulated negative real energy). Other quantities include RMS voltage and current, positive and negative real energy. Select the desired accumulation value in the QNSEL field of the PLSCFG1 register.

Also in the pulse configuration registers you can select which phases to include in the accumulation. Set any or all the PHASEA, PHASEB, and PHASEC bits in the PLSCFG1 register to include them in the accumulation.

Generating Pulses

On every DSP cycle, the MAXQ3181 adds the value in the selected register (or set of registers) to the pulse accumulator. If the value in the pulse accumulator exceeds the value in the associated threshold register (THR1), then a pulse is started and the value in the threshold register is subtracted from the value in the pulse accumulator.

Meter Constant

A meter constant is the number of pulses that are generated during a standard measurement interval; for example, a meter might specify a meter constant of 1600 pulses per kilowatt-hour. The THR1 register is used to specify the meter constant according to the following formula:

$$THR = \frac{2^{16}}{K_M \times I_{FS} \times V_{FS} \times t_{FR}}$$

In this formula, THR is the value to be written to the threshold register, K_M is the desired meter constant (in pulses per kilowatt hour), I_{FS} and V_{FS} are the full-scale voltage and current, respectively, and t_{FR} is the frame period in units of hours, as in the previous calculation.

As an example, assume once again a full-scale voltage value of 558.1V = 0.5581kV, a full-scale current value of 102.4A, a desired meter constant of 1600 pulses per kilowatt hour, and a default frame time of 320µs (88.9 x 10^{-9} hours). The threshold register value can be calculated as:

$$65{,}536/(1600 \times 102.4 \times 0.5581 \times 88.9 \times 10^{-9}) = 8{,}063{,}071 = 0x7B085F$$

Increasing the value of the threshold register *reduces* the meter constant (that is, there are fewer pulses per kilowatt-hour); reducing the threshold register *increases* the meter constant (that is, there are more pulses per kilowatt-hour.)

Interrupts

The MAXQ3181 contains an interrupt subsystem to relieve the host processor of the burden of constantly polling the device for status. Instead, under certain circumstances, the MAXQ3181 can activate an external pin to alert the host processor that some condition requiring host attention has occurred.

Interrupts are managed globally by the IRQ_MASK and IRQ_FLAG registers. In general, when a bit becomes set in the IRQ_FLAG register, an interrupt is generated if the corresponding bit is set in the IRQ_MASK register.

Interrupts can be configured for the following conditions:

PWRF: This flag indicates the V_{DVDD} to the MAXQ3181 has fallen below its nominal operating threshold (about 2.85V). This can be taken as an indication that power failure is imminent and that the host processor should begin taking steps to ensure an orderly shutdown.

CHSCH: This flag indicates that the CHKSUM register changed its value.

EOVF: Energy overflow. This flag indicates that one or more energy accumulators (X.EAPOS, X.EANEG, etc.) have overflowed. In a traditional meter, the host processor would poll the MAXQ3181 to determine which of the energy accumulators have overflowed and adjust its internal accounting registers accordingly.

OC: The RMS current value on one or more of the phases over the most recent DSP cycle has exceeded the value set in the OCLVL register.

OV: The RMS voltage on one or more of the phases over the most recent DSP cycle has exceeded the value set in the OVLVL register.

UV: The RMS voltage on one or more of the phases over the most recent DSP cycle has failed to exceed the value set in the UVLVL register.

NOZX: Zero crossings were not detected on one or more of the phases. The detection time is defined in the NZX_TIMO register. The resolution for the NZX_TIMO register is the duration of one ADC sample time (nominally 40µs).

DCHA: Tells the host processor that the direction of net real energy flow on one of the three phases has changed during the current DSP cycle as compared to the previous DSP cycle.

DSPRDY: Indicates the latest DSP cycle has just completed.

DSPOR: Indicates that the processing for the previous DSP cycle had not been completed before the current DSP cycle became available for processing. This overflow indication should never be seen in the default configuration; however, under some conditions (faster ADC rate, slower CPU clock) the processing requirements may exceed the number of CPU cycles available for DSP processing. Under these circumstances, the clock rate may be increased, the ADC rate may be reduced (that is, the R_ADCRATE register may be increased).

Note that when DSPOR becomes set, all DSP calculations as well as the pulse output are invalidated. The appropriate host response is to take the remedial action described above and discard the current set of DSP result values.

Each phase has a local register that contains copies of the OC, OV, UV, NOZX, and DCHA bits. Thus, to determine which phase(s) have exception conditions requires four reads: the IRQ_FLAG register to determine which conditions are active that are causing the interrupt to occur, and then a read to A.FLAGS, B.FLAGS, and C.FLAGS to determine which of the phases have the indicated condition.

Finally, each phase has a pair of local registers that contain overflow flags for each energy accumulator. If the EOVF bit is set in the IRQ_FLAG register, the host should then read the A.EOVER, B.EOVER, and C.EOVER registers to determine which of the phases have overflow conditions.

Overvoltage and Overcurrent Detection

The MAXQ3181 detects overvoltage and overcurrent events and can issue interrupt request signals to the master when these events occur. The overvoltage level can be programmed into the OVLVL register, while the overcurrent level is determined by the OCLVL register. Both OVLVL and OCLVL registers represent the bits 23:8 of the VRMS or IRMS registers. Any time the MAXQ3181 detects the RMS-value exceeding a threshold level, the OV or OC interrupt flag is set. If enabled, any of these flags issues an interrupt request. All interrupt flags are "sticky" bits—the MAXQ3181 never clears them on its own unless a reset occurs. The interrupt flags should be cleared by the master by writing the appropriate register.

Meter Units to Real Units Conversion

All energy calculations, including various threshold checks, are performed internally in fixed format in meter units. Therefore, the threshold values must be supplied by the user in meter units as well. This section summarizes how to convert real units (V, A, kWh, W, and kAh) into meter units and vice versa.

The conversion factors are based on the settings of t_{FR}, V_{FS}, and I_{FS}, defined by the user's design.

t_{FR} is analog scan frame timing. This parameter is defined by the R_ADCRATE setting and system clock frequency f_{SYS}:

$$t_{FR} = (R\_ADCRATE + 1) \times 8/f_{SYS}$$

Default conditions are R_ADCRATE = 319, f_{SYS} = 8MHz.

V_{FS} is full-scale voltage. This is the input voltage that produces full-scale ADC output; defined by the hardware voltage transducer ratio V_{TR} and ADC full-scale input voltage V_{FSADC}:

$$V_{FS} = V_{FSADC} \times V_{TR}$$

Default conditions are V_{FSADC} = 1.024V. V_{TR} is design dependent.

I_{FS} is full-scale current. This is the input current that produces full-scale ADC output; defined by the hardware current transducer ratio I_{TR} and ADC full-scale input voltage V_{FSADC}:

$$I_{FS} = V_{FSADC} \times I_{TR}$$

Default conditions are V_{FSADC} = 1.024V. I_{TR} is design dependent.

Meter units are defined with respect to the base parameters as shown in Table 5.

When reading virtual registers, the MAXQ3181 uses the configurable conversion coefficients AMP_CC, VOLT_CC, PWR_CC, and ENR_CC to return meaningful data. Table 6 describes how to set the coefficients.

Table 5. Meter Unit Definitions

REGISTER OR ACCUMULATOR	METER UNIT (1 LSB)
Current RMS: X.IRMS	$MU\_AMP = I_{FS}/2^{24}$
Pulse output current RMS	
THR1, when pulse output configured to IRMS	
Voltage RMS: X.VRMS	$MU\_VOLT = V_{FS}/2^{24}$
Pulse output RMS voltage	
THR1, when pulse output configured to VRMS	
Energy: X.ACT, X.APP, X.EAPOS, X.EANEG, X.ES Pulse Output Energy: THR1	$MU\_ENR = V_{FS} \times I_{FS} \times t_{FR}/2^{16}$
Power: PWRP.X, PWRS.X	$MU\_PWR = V_{FS} \times I_{FS}/2^{32}$
When X.ESF Contains Amp-Hours: X.ESF	$MU\_AH = I_{FS} \times t_{FR}/2^{16}$
OCLVL, NOLOAD, I1THR, I2THR	$I_{FS}/2^{16}$
OVLVL, UVLVL	$V_{FS}/2^{16}$

Table 6. Virtual Register Coefficients

VIRTUAL REGISTER	OUTPUT RESOLUTION (1 LSB), DEFINED BY USER	COEFFICIENT
Power: PWRP.X, PWRS.X	PWR_LSB	PWR_CC = MU_PWR/PWR_LSB
Voltage: V.X	VOLT_LSB	VOLT_CC = MU_VOLT/VOLT_LSB
Current: I.X	AMP_LSB	AMP_CC = MU_AMP/AMP_LSB
Energy: ENRP.X, ENRS.X	ENR_LSB	ENR_CC = MU_ENR/ENR_LSB

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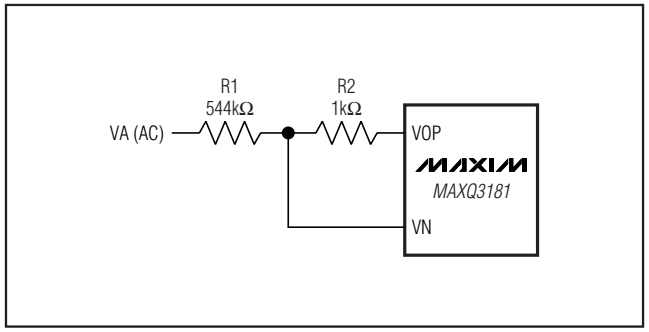

Figure 13. Sample Voltage Input Circuit

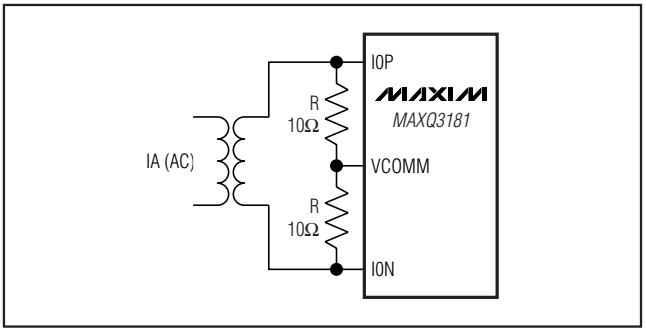

Figure 14. Sample Current Input Circuit

Units Conversion Examples

The conversions from meter units to physical units are illustrated with the simplified input circuits in Figures 13 and 14. The voltage input circuit is a voltage-divider. Current input is through a current transfer with turn ratio of 2000:1.

The voltage transducer ratio (V_{TR}) = (R1 + R2)/R2 = 545, V_{FS} = 558.1V.

The current transducer ratio (I_{TR}) = CT_N/(2 x R) = 2000/(2 x 10) =100 (A/V), I_{FS} = 102.4A.

The input circuits should be designed to avoid getting too close to the ADC input full sale at the specified maximum ratings. So for the above circuits, we would specify the maximum input current = 70A (RMS) and maximum voltage = 390V (RMS), to ensure that peak of sinusoudal waveform never exceeds I_{FS} or V_{FS}.

Use the default ADC timing t_{FR} = 320µs, we get the following meter unit to physical unit conversion coefficients (these coefficients are not part of the MAXQ3181 registers):

$$MU\_AMP = I_{FS}/2^{24} = 6.1E\text{-}6\ (A)$$

$$MU\_VOLT = V_{FS}/2^{24} = 33.3E\text{-}6\ (V)$$

$$MU\_PWR = V_{FS} \times I_{FS}/2^{32} = 13.3E\text{-}6\ (W)$$

$$MU\_ENR = V_{FS} \times I_{FS} \times t_{FR}/2^{16} = 77.5E\text{-}9\ (Wh)$$

For example, if we get 0x07654AF0 from reading 0x1CC register (phase A current RMS), the current value it represents is

$$0x07654AF0 \times MU\_AMP = 47.33\ (A)$$

For some low-end host microcontrollers, doing the above math multiplication above could be difficult. For this reason, the MAXQ3181 provides conversions for some commonly needed parameters through the VOLT_CC, AMP_CC, PWR_CC, and ENR_CC registers.

For example, if you want to display current in the resolution of 1mA, without having to use a multiplication operation to convert from the meter unit value 0x07654AF0, you would set AMP_CC to 0x0190, and read from virtual register 0x831 (phase A RMS current). The output would be 0xB8E45170. Dropping the lower 2 bytes (right shifting 16 bits) gives 0xB8E4, or 47332 decimal (47332mA).

AMP_CC is computed as follows:

$$AMP\_CC = (I_{FS}/2^{24})/AMP\_LSB = MU\_AMP/AMP\_LSB$$

$$AMP\_LSB = 0.001/2^{16}\ (A)$$

$$I_{FS} = 102.4A$$

$$AMP\_CC = (102.4/2^{24})/(0.001/2^{16}) = 400d = 0x0190$$

Calibration Procedure

Calibration Overview

Calibration ensures that the recorded voltage, current, energy, and power are in accordance with the design criteria. Before creating a calibration regimen, establish the fundamental units of the meter: the full-scale voltage and current. Then adjust the gain registers using calculated calibration constants to produce the expected reading in the raw current, voltage, energy, and power factor registers.

The calibration constants should be stored in non-volatile memory by the host microcontroller. Upon any reset or loss of power, the host microcontroller must reload the MAXQ3181 with the constants.

Calibration always follows a set of fundamental steps:

- Apply a known signal (voltage/current/power) to the meter.
- Read the meter.
- Calculate the correction factor based on the difference between the applied signal level and the meter reading.
- Write the correction factor to the appropriate register.

- Read the meter quantity again to verify the calibration.

Note that these steps can occur more than once for a given signal type to verify readings at different signal levels.

There are two methods to read the meter in the above second step. The first is to read the raw register associated with the value under calibration, for example, A.VRMS for the phase A voltage channel; A.IRMS for the phase A current channel, and A.ACT for phase A real power.

The second calibration method assigns a pulse output to the value being calibrated and measures the pulse period. In practical use, the method chosen depends on the specific application and the available equipment. For example, in some applications the voltage and current are of no concern, but the energy accumulation must be very accurate. For these applications, meter calibration sets with built-in pulse measurement facilities can make the most sense.

The calibration procedure involves the following general steps:

- Calibrate voltage for a given phase by applying a known voltage and adjusting the voltage gain (A.V_GAIN for phase A) until the RMS voltage (A.VRMS for phase A) reads the applied voltage in the designated units.
- Calibrate current by applying a known current and adjusting the current gain (A.I_GAIN for phase A) until the RMS current (A.IRMS for phase A) reads the applied current in the designated units. If desired, the current can be calibrated at two points (low range and high range) for more accuracy.
- Once the current gain and voltage gain are calibrated, the power/energy should not require any additional adjustment for most situations. Although, a separate power gain register is available for further fine-tuning of the power/energy accuracy. One must keep in mind that anytime voltage or current is recalibrated, the power or energy accuracy is naturally affected. So the power gain should be recalibrated to achieve the desired accumulative effect of voltage, current, and power gains.
- Calibrate the phase offset by applying a power factor load and adjusting the phase angle offset accordingly. If desired, the phase offset can be calibrated at up to three points for more accuracy.

Once these elements are calibrated for each phase, all other information (power factor, apparent power, etc.) is also properly calibrated. The descriptions in the following sections deal specifically with phase A, but the same procedure is followed with phases B and C.

Calibrating Voltage

Ensure that there is no previous value in the gain register, A.V_GAIN, by setting this register to 0x4000.

- Apply a known voltage with RMS value close to the desired maximum operating voltage (and less than $V_{FS}/\sqrt{2}$).
- Read the A.VRMS register. Note the value.
- Convert the known value to meter units by dividing it by MU_VOLT (= $V_{FS}/2^{24}$).
- Divide the applied value (in meter unit) by the value read from the MAXQ3181. The result should be a value between 0 and 2. If the value falls outside of this range, you have probably miscalculated V_{FS}.
- Multiply the calculated value by 2^{14}. The result is the gain value to be programmed into A.V_GAIN. Ensure the most significant bit is 0.

When the gain value is programmed, wait for 2 to 3 seconds, reread the RMS value from A.VRMS. Check that the measured value is correct by comparing A.VRMS against the applied voltage in meter unit.

Voltage Calibration Example

Assumptions: V_{FS} is 558.1V. The applied voltage is 240 VRMS.

- Convert the applied voltage to meter units. This calculation gives 240 x 2^{24}/558.1 = 7,214,714 = 0x006E1679.
- Read the A.VRMS register. You read 0x0708029. This is 7,372,841 decimal.
- Divide the applied voltage by the voltage read from the meter. The result is 7,214,714/7,372,841 = 0.97855.
- Convert to integer by multiplying 2^{14}: 16,384 x 0.97855 = 16,033 = 0x3EA1. Write this value to the A.V_GAIN register.

Calibrating Current

Ensure that there is no previous value in the gain register, A.I_GAIN, by setting this register to 0x4000.

- Apply a known current with RMS value close to the desired maximum operating current (and much lower than $I_{FS}/\sqrt{2}$).
- Read the A.IRMS register. Note the value.
- Convert the known value to meter units by dividing it by MU_AMP (= $I_{FS}/2^{24}$).

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- Divide the applied value (in meter unit) by the value read from the MAXQ3181. The result should be a value between 0 and 2. If the value falls outside of this range, you have probably miscalculated I_{FS}.
- Multiply the calculated value by 2^{14}. The result is the gain value to be programmed into A.I_GAIN. Ensure the most significant bit is 0.

When the gain value is programmed, wait for approximately 2 to 3 seconds, then reread the RMS value from A.IRMS. Check that the measured value is correct by comparing A.IRMS against the applied current in meter unit.

Calibrating Phase Offset

Phase offset calibration should be performed after the voltage and current gains have been calibrated. To calibrate the phase offset, it is first necessary to measure the power reported by the meter at two different phase points. The best way to do this is to rely on the pulse output of the meter; use a precise counter to determine the power reported by the meter by counting the pulse period. A load of power factor 0.5L or 0.5C is a good choice for calibrating phase offset.

1) Apply a known pure resistive load to the meter. Read the measured power, as $P_{1.0}$.
2) Shift the phase of the current by +60° (power factor of 0.5C). Read the measured power, as $P_{0.5C}$.
3) The phase offset $PA_{0.5C}$ is computed from the equation:

$$\tan(PA_{0.5C}) = (1 - 2P_{0.5C}/P_{1.0})/\sqrt{3}$$

If an inductive load (PF = 0.5L) is applied, the phase offset equation becomes:

$$\tan(PA_{0.5L}) = (2P_{0.5L}/P_{1.0} - 1)/\sqrt{3}$$

These equations can be expressed in terms of relative errors, where $E_{1.0}$, $E_{0.5C}$, and $E_{0.5L}$ are the power relative errors at PF = 1.0, 0.5C, and 0.5L respectively.

$$\tan(PA_{0.5C}) = \frac{E_{1.0} - E_{0.5C}}{\sqrt{3}(1+E_{1.0})}$$

$$\tan(PA_{0.5L}) = \frac{-E_{1.0} + E_{0.5L}}{\sqrt{3}(1+E_{1.0})}$$

4) Solve for PA from one of the above equations.
5) Convert PA into integer number, by multiplying it by 2^{16}.
6) Convert to hex value and write to the appropriate register.

Note that MAXQ3181 supports three offset values—X.PA2, X.PA1, and X.PA0—corresponding to the low, mid, and high range of the input signals, respectively. Calibrating at the three loading levels could become necessary if the phase error introduced by the current sensors varies significantly with the input levels. Registers I1THR and I2THR define the limits of the ranges. If I1THR and I2THR are left at their default values of 0x0000, X.PA0 is applied to the full input range.

Phase Offset Calibration Example

Make sure X.PA0, X.PA1, and X.PA2 are cleared before proceeding with calibrations. Assume the phase A has been calibrated for A.VGAIN and A.IGAIN at Ib (= 10A). At PF = 1.0, the active power relative error is $E_{1.0}$ = -0.4%. Set input to I = Ib and PF = 0.5L. The relative error reported by the meter tester is $E_{0.5L}$ = 1.2%. Solve for $PA_{0.5L}$ from the following equation:

$$\tan(PA_{0.5L}) = \frac{-E_{1.0} + E_{0.5L}}{\sqrt{3}(1+E_{1.0})} = \frac{0.4/100 + 1.2/100}{(1-0.4/100)\sqrt{3}} = 0.009274703$$

where $PA_{0.5L}$ = 0.009274437 (radians) = 0.53° and X.PA0 = 0.009274437 x 2^{16} = 607.8095 = 0x0260.

Write 0x260 to A.PA0 (address 0x13E). If multirange calibration is required, repeat the above procedure at the desired input levels. The input levels for calibration should be selected based the phase error characteristics of the current sensors.

Interfacing the MAXQ3181 to External Hardware

The MAXQ3181 has all the internal circuitry that is needed for a sophisticated electricity meter, but specific external hardware is required when configuring the meter for a particular application. The most critical decision that must be made is how the load will be connected to the power source, and how the meter will be connected to measure power consumed in the load. This section covers how to select hardware components for a MAXQ3181 electricity meter.

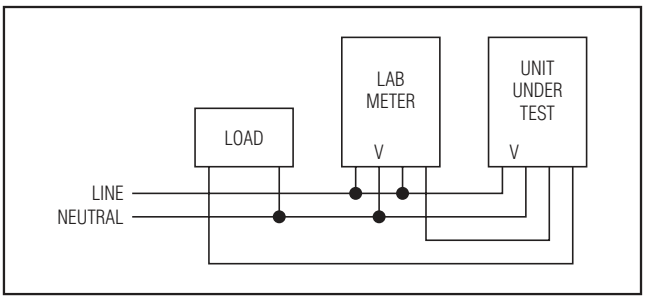

Figure 15. Offset Testing Setup

Connections to the Power Source

Generally, three-phase power as delivered from the utility consists of four wires: three voltage phases and a neutral wire. In one typical three-phase delivery system, measuring from neutral to any phase would read 120V, while measuring from any phase to any other phase would read 208V. Connecting a load so that load current is taken from phase lines and returned to neutral is called a wye-connected load. Connecting a load so that load current is provided by one phase and returned on another phase is called a delta-connected load. The MAXQ3181 can measure power consumed in either a wye-connected or a delta-connected load.

If the load is connected in a wye fashion, the voltage is measured from the neutral lead to each of the phases, and the current measuring device is placed in series with the load, most often in the hot lead. The sensor is not placed in the neutral lead to prevent a customer from defrauding the utility by returning the current to ground rather than neutral. A current sensor placed in the hot lead makes fraud even more difficult.

A delta-connected load can have current measured in two possible ways. If it is primarily desirable to know how much power is delivered to the load, one can place the current sensor in the load circuit between two phases. But if it is more important to know how much current is being drawn from each supply phase, each current sensor is placed in the line circuit of each single phase.

Most utilities are only concerned with the total amount of energy being consumed. If individually accounting for the power delivered by each phase is not a requirement, it is not necessary to measure all three voltages. Instead, knowing only two voltages and the three currents is all that is necessary to measure total energy usage.

There are several ways of doing this. In a wye arrangement, one of the phases—usually phase B—can be considered the voltage reference point instead of neutral. Then the voltage measurements can be made from phase A to phase B and from phase C to phase B. By using some simple arithmetic, the power delivered by phase A, phase B, and phase C can be calculated even though only two voltages are available.

A second mechanism is to have a delta-connected load, but with one leg—usually the BC leg—split into two equal loads. The point where the load is split is defined as the reference. In this arrangement, it is only necessary to know the voltage between phase C and the split and phase A and the split, since $V_C = -V_A$.

Finally, there is the connection arrangement in which the load is in a delta configuration with the current sensor at each load, but it is still desired to determine how much current is in each supply branch. The MAXQ3181 supports all of these connection arrangements.

Sensor Selection

The MAXQ3181 supports a variety of voltage and current sense elements. This section describes the properties of many of these sensing devices.

Voltage Sensors

Voltage-Divider

A voltage-divider is an ideal voltage-sensing element when there is no need for voltage isolation. Modern resistors have virtually no parasitic capacitance or inductance at the frequencies of interest in an electricity meter and have extremely low variation with temperature. When selecting resistors for a voltage-divider, keep the division ratio high enough so that the peak voltage value cannot exceed the maximum allowable input voltage. In the MAXQ3181, the peak input voltage is about 1V; consequently, a divider in the range of 400:1 to 600:1 is ideal.

The second consideration is the total power dissipation and voltage hold-off requirements of the resistor. It is tempting to design a 400:1 divider with a 400kΩ resistor in series with a 1kΩ resistor, but that would force the 400kΩ resistor to dissipate about 140mW. This is not an excessive amount of power, but if the design is to use small SMT parts, it can handle greater than a 1/10W SMT resistor. It is better to use a series of several smaller components to improve system reliability.

Voltage Transformer

If isolation is required between the meter electronics and the line, a voltage transformer is required. A voltage transformer is designed to faithfully transfer an AC voltage applied on the primary side to a sensor on the secondary side. On the primary side, a voltage-divider is used to reduce the voltage to a workable level. On the secondary side, a load resistor is selected so that the current in the transformer windings is safely within the transformer's linear operating region.

Because the impedance seen in the primary side of the transformer is equal to the impedance of the load resistor in the secondary circuit plus impedance of the transformer secondary winding at the operating frequency, it is easy to calculate the value of the required voltage-divider resistors in the primary side. For example, assume we want a 500:1 divider ratio and assume

the load resistor is 600Ω and that the impedance of the transformer secondary is 200Ω. The resistor required in the primary is

$$(600 + 200) \times 500 = 400k\Omega$$

Often, this resistor is constructed from multiple instances of a smaller value resistor; in this case, one might use eight 50kΩ resistors. Doing so minimizes the voltage requirements for the resistor chain and reduces the possibility that a single point of failure will cause a catastrophic failure.

Current Sensors

Current Shunt

A current shunt is a low-value (approximately 100µΩ to a 100mΩ) resistor that converts a large-value current into a small voltage. Shunts make good current sensors because the output is an extremely linear representation of the measured current, current shunts can have very low temperature coefficients, and they are inexpensive.

The power dissipated by a current shunt is inversely proportional to its resistance and proportional to the square of the output voltage. Consequently, there is great incentive to reduce the resistance (and hence, the output voltage) of a shunt. Often, full-scale current in a shunt produces only a few millivolts of output, making a front-end amplifier essential. The MAXQ3181 includes a gain-of-32 amplifier in the current channels that is automatically cycled in and out, depending on the input voltage of the current channels.

Current shunts operate at line voltage, thus, the AFE must be isolated from the line. That means that in a wye-connected meter, the current sensing must be performed in the neutral return circuit (so that all voltages into the current-sense amplifiers are referenced to neutral). It also means that the use of a shunt is precluded for delta-connected meters; the MAXQ3181 cannot tolerate the line-voltage differential between channels.

Current Transformer

In a current transformer, the primary is usually one turn of thick wire or buss bar and the secondary is often 1000 turns or more of magnet wire. A ferrite core magnetically couples the two. Thus, a large current in the primary turn creates a small current but large voltage in the secondary winding.

For example, assume a current transformer with a 1000 turn secondary. A 10A current in the primary winding induces a 10mA current in the secondary. This current is made to flow through a so-called "burden" resistor, usually 10Ω to 20Ω. Assuming a 20Ω burden, our 10A current thus produces a 200mV signal in the secondary.

Advanced Operation

Modifying the ADC Operation

There are several other registers that directly affect the AFE function. These registers directly affect the hardware functionality, and should be modified only when it is explicitly required. For example, if the MAXQ3181 is operated at some frequency other than the nominal 8MHz system clock, modification of these registers by supervisory code becomes necessary to maintain a 320µs frame time.

- **R_ACFG:** This register contains bits that disable the ADC entirely, disable the voltage reference buffer amplifier, and disable the ADC interrupt. Modifying this register will likely disable or impair operation of the MAXQ3181 internal firmware.
- **R_ADCRATE:** Modify this register to change the rate at which the MAXQ3181 acquires samples. By default, R_ADCRATE contains 319 decimal, which means that the ADC acquires a sample every 320 system clocks. With an 8MHz clock, this translates to 40µs. If the system clock is slower, it may be advantageous to reduce this value to keep a 40µs per sample time constant.
- **R_ADCACQ:** Modify this register to change the acquisition time. The acquisition time is the time from ADC power-on until conversion starts, and is provided to allow the input amplifiers to settle. By default this is set to 47 decimal, or 6µs at an 8MHz system clock. If the system clock rate is changed, then R_ADCACQ should change so that this value remains about 6µs.

Fine-Tuning the DSP Controls

Fine-Tuning the Line Frequency Measurement

Line frequency measurement is based on zero-crossing detection. For that purpose each voltage signal is passed through a digital lowpass filter, controlled by the ZC_LPF register. This register specifies the b_0 coefficient of a first-order LPF using following formula:

$$b_0 = \frac{ZC\_LPF}{2^{16}}$$

The MSB of this register must be zero.

For each phase A, B, and C, the MAXQ3181 counts the number of scan frames (NS) between zero crossings within a DSP cycle. Each individual phase A, B, or C zero-crossing event contributes the raw NS count that plugs as input to lowpass filter:

$$Y_n = Y_{n-1} + (AVG\_NS/65,536) \times (X_n - Y_{n-1})$$

The filter coefficient is a signed 16-bit value and can be configured by master. Here Y denotes the global NS value, X denotes individual NS measurements produced by zero-crossing events detected on the phase A, B, or C voltage channel. Note that if all three phase voltages present, the filter above receives three inputs each DSP cycle. The global NS value is used to generate the trigger for DSP processing. Note that the NS value can be configured by the master, which could be necessary if all three voltage signals are lost and no zero-crossings are detected. The line period is then calculated as a product of NS and the scan frame t_{FR}. The reciprocal of this value is the line frequency, which can be obtained as a fixed-point value with 1 LSB = 0.001Hz by reading the LINEFR register.

Low-Power Measurement Mode (LOWPM)

This mode enables a subset of metering functions while operating from the lower frequency internal RC oscillator to conserve power. The actual system clock frequency used is the RC oscillator output frequency divided by 8, which results in a system clock frequency of approximately 1MHz.

The parameters provided in the LOWPM are:

- Voltage RMS
- Current RMS
- Ampere-Hour

The ampere-hour value is readable from the X.ESF registers (X = A/B/C). Entry to LOWPM mode only occurs at the request of the master. The master must set the LOWPM_E bit (register address 0xC03) to 1 to place the MAXQ3181 into LOWPM mode. Entering LOWPM mode changes the clock frequency, thereby invalidating a number of configuration registers. As a result, the master must immediately reload the configuration registers and filter with new, updated values before metering measurement operations can continue.

The master instructs the MAXQ3181 to exit LOWPM mode by reading the LOWPM_X bit (register address 0xC04).

Temperature

The MAXQ3181 contains a temperature sensor that can be used by host software for any purpose, including compensating power readings for temperature effects.

Use the virtual register command (RAWTEMP, 0xC01) to perform a temperature conversion. The MAXQ3181 returns raw ADC reading of voltage produced by the temperature sensor.

Conversion from the arbitrary units to useful units (such as degrees Celsius) requires taking one calibration point and storing a conversion constant in the host processor. The conversion constant is simply the value (in absolute degrees) of one LSB.

To calculate the LSB value, take a reading at a known temperature and divide the known temperature by the reading. For example, assume you take a reading at room temperature (23°C), and the reading is 0x7F00. The degrees per LSB are then:

$$(23 + 273.15)/0x7F00 = 0.00911K$$

Now, assume at a later time you read the temperature and see it is 0x84F0. To find the temperature in Celsius, multiply by the degrees per LSB and subtract 273.15:

$$0x84F0 \times 0.00911 - 273.15 = 36.8°C$$

Advanced Calibrations

Calibrating Current Offset

Ideal hardware should produce a current reading linearly proportional to the input current. However, due to noise or other factors, the RMS current read by the meter might not be precisely linear. The current offset (X.OFFS_HI, X = A/B/C) can be used to compensate the current channel nonlinearity.

Since the MAXQ3181 tracks the input current to determine what linearity compensation factors to use, the user must choose two points (i_{lo} and i_{hi}) comfortably above the low current threshold, and get the X.IRMS current readings (r_{lo} and r_{hi}). Then calculate the Y-intercept of the line drawn between the two points, that is, the offset. To calculate the value for the offset register, use the following formula. If LINFRM = 0:

$$offs = \frac{r_{hi}^2 i_{lo}^2 - i_{hi}^2 r_{lo}^2}{2^{24}(i_{hi}^2 - i_{lo}^2)}$$

If LINFRM = 1:

$$offs = \frac{r_{hi} i_{lo} - i_{hi} r_{lo}}{2^4(i_{lo} - i_{hi})}$$

In this equation, i_{hi} and r_{hi} are the applied current and the current reading, respectively, in meter units at the higher of the two reference currents; i_{lo} and r_{lo} are the applied current and the current reading, respectively, in meter units at the lower of the two reference currents.

The gain (X.I_GAIN) may require recalibration after the offset register updated.

Calibrating Linearity

The current channel includes a variable-gain amplifier that introduces a gain of 32 when the current falls below the low current threshold (about 1/32 of full-scale current I_{FS}). Because the gain of the amplifier cannot

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be controlled with arbitrary precision, and because high gain implies increased noise, it may be necessary to calibrate the MAXQ3181 to maintain linearity at the lowest inputs.

There are two settings that manage low-current linearity: an offset setting, OFFS_LO; and a gain setting, GAIN_LO. Setting the offset is simple. Ensure no current is flowing in the current circuit. Read X.IRMS. To calculate offset use following formula:

If LINFRM = 0:

$$offs = -\frac{(X.IRMS)^2}{2^{16}}$$

If LINFRM = 1:

$$offs = -X.IRMS$$

Program the offs into the OFFS_LO register.

So, if the user reads 0x0113 from the X.IRMS register and LINFRM = 1, program 0xFEED into the OFFS_LO register. Setting the GAIN_LO register means applying a current below the low-current threshold, reading the value from the MAXQ3181, and adjusting the gain accordingly. Note that, unlike offset, the low-end gain is *added* to the overall gain provided in the I_GAIN register.

Apply a known current with peak value less than the low-current threshold. Ensure that there is no previous value in the low-current gain register, A.GAIN_LO, by setting this register to 0x4000. Read the A.IRMS register (0x1CC). Note the value. Convert the known value to meter units by multiplying the known value (in amperes) by 2^{24} and dividing by I_{FS}. Divide the results of this calculation by the value read from the MAXQ3181. The result should be a value between 0 and 2. Convert the integer by multiplying 2^{14}, and ensure MSB is zero. The result is the gain value to be programmed into A.GAIN_LO.

Calibrating Power/Energy Gain

Once voltage and current have been calibrated, the energy and power calculation automatically reflects the calibrated voltage and current. However the energy gain factor (X.E_GAIN, X = A/B/C) can be further tuned to achieve even more accurate power and energy result if necessary. For example, if the voltage and current calibration sources are not as accurate as the power/energy calibration source, then the additional gain calibration may be necessary. The following procedure for power/energy gain calibration is outlined for phase A.

- Apply a precision unity power factor power (applied value) that is close to the desired normal operating point.
- Read the PWRP.A register. Note the value.
- Convert the applied value to meter units by dividing it by MU_PWR.
- Divide the applied value (in meter unit) by the value read from the MAXQ3181. The result should be a value between 0 and 2. If the value falls outside of this range, I_{FS} and/or V_{FS} have probably been miscalculated.
- Multiply the calculated value by 2^{14}, and ensure the MSB is zero. The result is the gain value to be programmed into A.E_GAIN.
- When the gain value is programmed, wait for 1 to 2 seconds, then reread the power value from PWRP.A. Check that the measured value is correct by comparing PWRP.A against the applied power in meter unit.

Multipoint Phase Offset Calibration

To perform the calibration at three current levels, note the raw current value (X.IRMS) at each point. Label the current values, from highest to lowest, I_0, I_1, and I_2. Program X.PA0, X.PA1, and X.PA2 with the phase offset values calculated at I_0, I_1, and I_2, respectively, as described in the *Calibrating Phase Offset* section. Finally, program I1THR with the average of I_0 and I_1, and program I2THR with the geometric average of I_1 and I_2. Now as the current changes the phase offset is adjusted accordingly. See Figure 16.

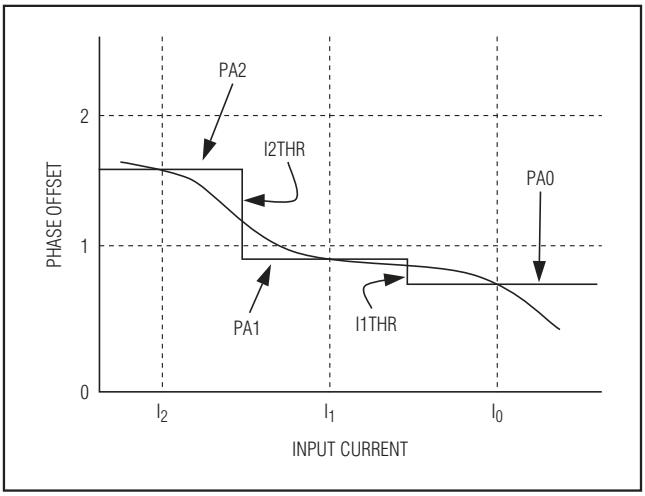

Figure 16. Phase Offset vs. Input Current Calibration

Advanced Register Configurations

Analog Scan Configuration Registers

Time Slot Assignment—Current Channel X = A/B/C (SCAN_IX) (A: 0x008, B: 0x00C, C: 0x00A)

Bit:	7	6	5	4	3	2	1	0
Name:	ADCMX				DADCNV	—	—	—
Reset A:	0x3				0	0	0	0
Reset B:	0x4				0	0	0	0
Reset C:	0x5				0	0	0	0

These registers configure the time slot normally assigned to current channels A/B/C. We recommend leaving these registers at their default values. If they must be reassigned, one must ensure that all the current and voltage channels are reassigned properly so that the MAXQ3181 computes the power/energy parameters as intended by your setup.

BIT	NAME	FUNCTION
7:4	ADCMX	Analog Input Select. This four-bit field determines which of the following analog inputs are sampled during this time slot. 0000 = V0P - VN 0001 = V1P - VN 0010 = V2P - VN 0011 = I0P - I0N (Phase A Current: 0011) 0100 = I1P - I1N (Phase B Current: 0100) 0101 = I2P - I2N (Phase C Current: 0101) 0110 = INP - VN 1xxx = Temperature All other values are reserved.
3	DADCNV	ADC Disable. When set, disables the ADC for this time slot.
2:0	—	Reserved.

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Time Slot Assignment—Voltage Channel X = A/B/C (SCAN_VX) (A: 0x009, B: 0x00D, C: 0x00B)

Bit:	7	6	5	4	3	2	1	0
Name:	ADCMX				DADCNV	PGG		
Reset A:	0x0				0	0x0		
Reset B:	0x1				0	0x0		
Reset C:	0x2				0	0x0		

These registers configure the time slot normally assigned to voltage channels A/B/C. The user may wish to change the PGG settings to match the voltage sensor. However, it is recommended that the user not modify the ADCMX settings.

BIT	NAME	FUNCTION
7:4	ADCMX	Analog Input Select. This four-bit field determines which of the following analog inputs are sampled during this time slot. 0000 = V0P - VN (Phase A Voltage: 0000) 0001 = V1P - VN (Phase B Voltage: 0001) 0010 = V2P - VN (Phase C Voltage: 0010) 0011 = I0P - I0N 0100 = I1P - I1N 0101 = I2P - I2N 0110 = INP - VN 1xxx = Temperature
3	DADCNV	ADC Disable. When set, disables the ADC for this time slot.
2:0	PGG	Programmable Gain Amplifier Select. This three-bit field configures the programmable-gain amplifier at the front-end of the analog input. The field has the following values: 000 = Gain of 1 001 = Gain of 2 010 = Gain of 4 011 = Gain of 8 100 = Gain of 16 101 = Gain of 32 All other values are reserved and can cause unpredictable behavior if selected.

Time Slot Assignment—Neutral Current Channel (SCAN_IN) (0x00E)

Bit:	7	6	5	4	3	2	1	0
Name:	ADCMX				DADCNV	—	—	—
Reset:	0x6				1	0	0	0

This register configures the time slot normally assigned to the neutral current channel. The user can change the DADCNV bit to enable/disable neutral current sampling. It is recommended that the other bits of this register be left at their default values.

BIT	NAME	FUNCTION
7:4	ADCMX	Analog Input Select. This four-bit field determines which of the following analog inputs are sampled during this time slot. All other values are reserved. By default, this register is set to 0110. 0000 = V0P - VN 0001 = V1P - VN 0010 = V2P - VN 0011 = I0P - I0N 0100 = I1P - I1N 0101 = I2P - I2N 0110 = INP - VN 1xxx = Temperature
3	DADCNV	ADC Disable. When set, disables the ADC for this time slot.
2:0	—	Reserved.

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Time Slot Assignment—Temperature Channel (SCAN_TE) (0x00F)

Bit:	7	6	5	4	3	2	1	0
Name:	ADCMX				DADCNV	PGG		
Reset:	0x8				1	0x2		

This register configures the time slot normally assigned to the temperature measurement device. This register is managed by the firmware and should not be modified by the host. Changing this register can result in unpredictable results.

BIT	NAME	FUNCTION
7:4	ADCMX	Analog Input Select. This four-bit field determines which of the following analog inputs are sampled during this time slot. 0000 = V0P - VN 0001 = V1P - VN 0010 = V2P - VN 0011 = I0P - I0N 0100 = I1P - I1N 0101 = I2P - I2N 0110 = INP - VN 0111 = Auto-zero ADC 1xxx = Temperature By default, this register is set to 1000.
3	DADCNV	ADC Disable. When set, disables the ADC for this time slot.
2:0	PGG	Programmable Gain Amplifier Select. This three-bit field configures the programmable-gain amplifier at the front end of the analog input. The field has the following values: 000 = Gain of 1 001 = Gain of 2 010 = Gain of 4 011 = Gain of 8 100 = Gain of 16 101 = Gain of 32 All other values are reserved and can cause unpredictable behavior if selected. This register is managed by the firmware and should not be modified by the host.

Neutral Current
Auxiliary Channel Configuration (AUX_CFG) (0x010)

Bit:	15	14	13	12	11	10	9	8
Name:	—	—	—	—	—	—	—	—
Reset:	0	0	0	0	0	0	0	0

Bit:	7	6	5	4	3	2	1	0
Name:	—	ENAUX	—	—	—	AUX_MUX		
Reset:	0	0	0	0	0	0	0	0

The MAXQ3181 can monitor the RMS value of one auxiliary channel in addition to its normal processing. The Auxiliary Channel Configuration register selects which input the auxiliary channel processes and what processing is applied to the auxiliary channel.

BIT	NAME	FUNCTION
15:7	—	Reserved.
6	ENAUX	Enable Auxiliary Channel. When set, enables auxiliary channel processing.
2:0	AUX_MUX	Auxiliary Channel Input Select. This three-bit field selects the input to be processed by the auxiliary channel. 001 = I_N

DSP System Configuration
System Clock Frequency (SYS_KHZ) (0x012)

Bit:	15	14	13	12	11	10	9	8
Name:	System Clock Frequency High Byte							
Reset:	0x1F							

Bit:	7	6	5	4	3	2	1	0
Name:	System Clock Frequency Low Byte							
Reset:	0x40							

This register contains the system clock frequency in kHz units. Because the default frequency is 8MHz, this register defaults to 0x1F40.

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Cycle Count (CYCNT) (0x01C)

Bit:	15	14	13	12	11	10	9	8
Name:	Cycle Count High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Cycle Count Low Byte							
Reset:	0x10							

This register contains the number of line cycles that will be accumulated in a single DSP cycle. When CYCNT line cycles have been accumulated, the DSP performs power, power factor, and energy calculations. By default, the cycle count is 0x10 (16 decimal).

Number of Scan Frames per DSP Cycle (NS) (0x040)

Bit:	31	30	29	28	27	26	25	24
Name:	Integer Portion, High Byte							
Reset:	0x03							

Bit:	23	22	21	20	19	18	17	16
Name:	Integer Portion, Low Byte							
Reset:	0xE8							

Bit:	15	14	13	12	11	10	9	8
Name:	Fractional Portion, High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Fractional Portion, Low Byte							
Reset:	0x00							

The NS register defines the fundamental timing for the electricity meter. It defines a DSP cycle in terms the period of the ADC scan frame. Generally, this register is calculated and updated automatically by the MAXQ3181 firmware based on the zero-crossing detection, and whether noise rejection (REJ_NS) and averaging (AVG_NS) are enabled. Host code can write to this register in order to set the desired DSP cycle duration. The duration of one scan frame (t_{FR}) is represented as 0x00010000.

Filter Coefficients

Line Cycle Noise Rejection Filter (REJ_NS) (0x02C)

Bit:	15	14	13	12	11	10	9	8
Name:	Line Cycle Noise Rejection Filter High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Line Cycle Noise Rejection Filter Low Byte							
Reset:	0xC8							

This register establishes the sensitivity of the NS rejection filter setting. NS is a measure of the line frequency. If a line cycle occurs that is shorter or longer than the line cycle represented in the NS register, this filter determines whether the cycle is used to update the NS value. For more information, see the NS register description. If this register is zero, noise rejection is disabled for the line cycle counter.

Line Cycle Averaging Filter (AVG_NS) (0x02E)

Bit:	15	14	13	12	11	10	9	8
Name:	Line Cycle Averaging Filter High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Line Cycle Averaging Filter Low Byte							
Reset:	0x00							

This register determines whether the NS value is averaged over previous values or whether the most recently measured value is used directly. If the value of this register is nonzero, the NS value is averaged using the following formula:

$$y_n = y_{n-1} + AVG\_NS\frac{x_n - y_{n-1}}{2^{16}}$$

If the value of this register is zero, NS is not averaged. The MSB of this register must be zero.

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Meter Measurement Averaging Filter (AVG_C) (0x030)

Bit:	15	14	13	12	11	10	9	8
Name:	Meter Measurement Averaging Filter High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Meter Measurement Averaging Filter Low Byte							
Reset:	0x00							

This register determines whether the all other measured values in the electricity meter are averaged over time. If the value of this register is nonzero, all measured meter values are averaged using the following formula:

$$y_n = y_{n-1} + AVG\_C\frac{x_n - y_{n-1}}{2^{16}}$$

If the value of this register is zero, no averaging is performed. The MSB of this register must be zero.

Meter Measurement Highpass Filter (HPF_C) (0x032)

Bit:	15	14	13	12	11	10	9	8
Name:	Meter Measurement Highpass Filter High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Meter Measurement Highpass Filter Low Byte							
Reset:	0xC8							

This register specifies the b_0 coefficient of a first-order Butterworth filter using the following formula:

$$b_0 = \frac{HPF\_C}{2^{16}}$$

The MSB of this register must be zero.

Zero-Cross Lowpass Filter (ZC_LPF) (0x05A)

Bit:	15	14	13	12	11	10	9	8
Name:	Zero-Cross Lowpass Filter High Byte							
Reset:	0x0B							

Bit:	7	6	5	4	3	2	1	0
Name:	Zero-Cross Lowpass Filter Low Byte							
Reset:	0x00							

This register specifies the lowpass filter applied for zero-cross detection. The MSB of this register must be zero.

Hardware Mirror Registers

ADC Configuration (R_ACFG) (0x04C)

Bit:	7	6	5	4	3	2	1	0
Name:	ADCASD	ADCRY	ADCCD		ADCBY	ADCIE	ARBE	ADCE
Reset:	0	0	0x0		0	1	1	1

This register is a mirror of a CPU register in the MAXQ3181. This register should not be modified by supervisory code.

BIT	NAME	FUNCTION
7	ADCASD	Disable ADC Automatic Shutdown. Normally, the ADC analog section is powered off following a conversion to conserve power. If this bit is set, the ADC leaves the analog section powered on following a conversion.
6	ADCRY	ADC Data Ready. When a conversion is complete, this bit is set to indicate that data is available. This bit generates an interrupt if ADCIE is set.
5:4	ADCCD	ADC Clock Divider. Sets the division ratio between the CPU master and ADC clock. 00 = divide by 1 01 = divide by 2 10 = divide by 4 11 = reserved
3	ADCBY	ADC Busy. When set, a single ADC conversion cycle is in progress. The bit is cleared on the conclusion of the conversion cycle.
2	ADCIE	ADC Interrupt Enable. If set, the ADC interrupts the CPU at the completion of a conversion cycle.
1	ARBE	Reference Buffer Enable. If set, the reference buffer is enabled to drive the REFO pin.
0	ADCE	ADC Enable. If set, the ADC hardware is activated.

ADC Conversion Rate (R_ADCRATE) (0x04E)

Bit:	15	14	13	12	11	10	9	8
Name:	ADC Conversion Rate High Byte							
Reset:	—	—	—	—	—	—	—	1

Bit:	7	6	5	4	3	2	1	0
Name:	ADC Conversion Rate Low Byte							
Reset:	0x3F							

This register specifies the number of system clock cycles between consecutive ADC conversions. It defaults to 0x13F (319 decimal), which specifies 320 CPU clock cycles between conversions. This register is a mirror of a CPU register in the MAXQ3181.

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ADC Settling Time (R_ADCACQ) (0x050)

Bit:	15	14	13	12	11	10	9	8
Name:	ADC Settling Time High Byte							
Reset:	—	—	—	—	—	—	—	—

Bit:	7	6	5	4	3	2	1	0
Name:	ADC Settling Time Low Byte							
Reset:	—	0x2F						

This register is a mirror of a CPU register in the MAXQ3181. This register should not be modified by supervisory code. This register specifies the time, in CPU clocks, that the ADC must wait after switching analog mux inputs before beginning its conversion. This register defaults to 0x2F (47 decimal), which specifies a 48 CPU clock-cycle delay from analog mux switching to the start of conversion.

SPI Configuration (R_SPICF) (0x052)

Bit:	7	6	5	4	3	2	1	0
Name:	ESPII	SAS	—	—	—	CHR	CKPHA	CKPOL
Reset:	1	0	0	0	0	0	0	0

This register is a mirror of a CPU register in the MAXQ3181. This register configures the SPI port of the MAXQ3181.

BIT	NAME	FUNCTION
7	ESPII	Enable SPI Interrupt. If set, arrival of a character on the SPI bus causes a CPU interrupt.
6	SAS	SPI Slave Select Polarity. If clear, $\overline{SSEL}$ is assumed to be active low; if set, $\overline{SSEL}$ is assumed to be active high.
5:3	—	Reserved.
2	CHR	SPI Character Length. If clear, characters on the SPI bus are assumed to be 8 bits; if set, characters on the SPI bus are assumed to be 16 bits.
1	CKPHA	SPI Clock Phase. If clear, data is sampled on the leading edge of the clock (low-to-high if the clock is active high, and high-to-low if the clock is active low). If set, data is sampled on the trailing edge of the clock (high-to-low if the clock is active high, and low-to-high if the clock is active low).
0	CKPOL	SPI Clock Polarity. If clear, the clock is assumed to be active high; if set, the clock is assumed to be active low.

Timeouts

Zero-Crossing Timeout (NZX_TIMO) (0x054)

Bit:	15	14	13	12	11	10	9	8
Name:	Zero-Crossing Timeout High Byte							
Reset:	0x23							

Bit:	7	6	5	4	3	2	1	0
Name:	Zero-Crossing Timeout Low Byte							
Reset:	0x28							

This register specifies the time in ADC sample periods (default 40µs) that must elapse following a zero-crossing event before the MAXQ3181 declares a “no-zero crossing” fault. When this fault is declared, the NOZXF bit in the X.FLAGS register is set.

Communications Timeout (COM_TIMO) (0x056)

Bit:	15	14	13	12	11	10	9	8
Name:	Communications Timeout High Byte							
Reset:	0x03							

Bit:	7	6	5	4	3	2	1	0
Name:	Communications Timeout Low Byte							
Reset:	0xE8							

This register specifies the duration of SPI timeout in ADC frames (default 320µs).

Energy Accumulation Timeout (ACC_TIMO) (0x058)

Bit:	15	14	13	12	11	10	9	8
Name:	Energy Accumulation Timeout High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Energy Accumulation Timeout Low Byte							
Reset:	0x05							

This register specifies the time in DSP cycles that the MAXQ3181 waits before accumulating energy. If this register is nonzero, it is decremented on each DSP cycle. If the result of the decrement is nonzero, the results of the DSP cycle are discarded and are not accumulated to the energy registers. This register is useful for delaying the initiation of energy accumulation on startup or after some hardware function has been modified.

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Phase-Angle Compensation

Phase Offset Current Threshold 1 (I1THR) (0x05C)

Bit:	15	14	13	12	11	10	9	8
Name:	Phase Accumulator Current Threshold 1 High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Phase Accumulator Current Threshold 1 Low Byte							
Reset:	0x00							

This register specifies the fraction of full-scale current that causes the MAXQ3181 to switch from PA0 to PA1 to provide phase-angle compensation. For more information, see the PA0, PA1, and PA2 register descriptions. The full-scale current is represented by 0x10000.

Phase Offset Current Threshold 2 (I2THR) (0x05E)

Bit:	15	14	13	12	11	10	9	8
Name:	Phase Accumulator Current Threshold 2 High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Phase Accumulator Current Threshold 2 Low Byte							
Reset:	0x00							

This register specifies the fraction of full-scale current that causes the MAXQ3181 to switch from PA1 to PA2 to provide phase-angle compensation. For more information, see the PA0, PA1, and PA2 register descriptions. The full-scale current is represented by 0x10000.

Miscellaneous Gain

Neutral Current Gain (N.I_GAIN) (0x12E)

Bit:	15	14	13	12	11	10	9	8
Name:	Compensation Coefficient High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Compensation Coefficient Low Byte							
Reset:	0x00							

This register contains gain compensation coefficient for the neutral current channel measurement. The raw values are taken from the selected measurement quantity and scaled by $N.I\_GAIN/2^{14}$.

Linearity Compensation

Linearity Offset, High Range, Phase X = A/B/C (X.OFFS_HI) (A: 0x138, B: 0x224, C: 0x310)

Bit:	15	14	13	12	11	10	9	8
Name:	Linearity Offset High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Linearity Offset Low Byte							
Reset:	0x00							

This signed register contains the linearity offset for phase X current channel when the programmable gain amplifier is set to unity gain (that is, the measured current is above the low current threshold). The signed value represented by this register is added to the current value according to following formula:

$$\text{if LINFRM = 0: } \sqrt{X.IRMS^2 + X.OFFS\_HI \times 2^{24}}$$

$$\text{if LINFRM = 1: } X.IRMS + X.OFFS\_HI \times 2^4$$

Linearity Gain Coefficient, Low Range, Phase X = A/B/C (X.GAIN_LO) (A: 0x13A, B: 0x226, C: 0x312)

Bit:	15	14	13	12	11	10	9	8
Name:	Linearity Coefficient High Byte							
Reset:	0x40							

Bit:	7	6	5	4	3	2	1	0
Name:	Linearity Coefficient Low Byte							
Reset:	0x00							

This register contains the linearity coefficient for phase X current channel when the programmable gain amplifier is set to gain of 32 (that is, the measured current is below the low current threshold). The effective gain is given by the equation:

$$\frac{X.GAIN\_LO}{2^{14}}$$

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Linearity Offset, Low Range, Phase X = A/B/C (X.OFFS_LO) (A: 0x13C, B: 0x228, C: 0x314)

Bit:	15	14	13	12	11	10	9	8
Name:	Linearity Offset High Byte							
Reset:	0x00							

Bit:	7	6	5	4	3	2	1	0
Name:	Linearity Offset Low Byte							
Reset:	0x00							

This signed register contains the linearity offset for phase X current channel when the programmable gain amplifier is set to gain of 32 (that is, the measured current is below the low current threshold). The signed value represented by this register is added to the current value. The total linearity compensation is applied as follows:

$$\text{if LINFRM = 0: X.GAIN\_LO}/2^{14} \times \sqrt{\text{X.IRMS}^2 + \text{X.OFFS\_LO} \times 2^{16}}$$

$$\text{if LINFRM = 1: X.GAIN\_LO}/2^{14} \times (\text{X.IRMS} + \text{X.OFFS\_LO})$$

Measurements—RAM Registers

On-Demand RMS Result (N.IRMS) (0x11C)

Bit:	31	30	29	28	27	26	25	24
Name:	RMS Result, Byte 3							
Reset:								

Bit:	23	22	21	20	19	18	17	16
Name:	RMS Result, Byte 2							
Reset:								

Bit:	15	14	13	12	11	10	9	8
Name:	RMS Result, Byte 1							
Reset:								

Bit:	7	6	5	4	3	2	1	0
Name:	RMS Result, Byte 0							
Reset:								

This register contains the result of the RMS calculation on the AUX channel. Usually, this is the neutral current channel.

Energy Accumulated in the Last DSP Cycle

Real Energy, Phase X = A/B/C (X.ACT) (A: 0x1D0, B: 0x2BC, C: 0x3A8)

Bit:	31	30	29	28	27	26	25	24
Name:	Real Energy Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	Real Energy Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	Real Energy Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	Real Energy Byte 0							

This signed register provides the raw real energy accumulated over the most recent DSP cycle. For each ADC sample period, the real instantaneous power calculated from the instantaneous voltage and current is accumulated. At the end of each DSP cycle, the result of the accumulation over the DSP cycle is copied to this register and is accumulated in X.EAPOS or X.EANEG, depending on the sign of the accumulated energy.

LSB of the energy registers is $V_{FS} \times I_{FS} \times t_{FR}/2^{16}$.

Apparent Energy, Phase X = A/B/C (X.APP) (A: 0x1D8, B: 0x2C4, C: 0x3B0)

Bit:	31	30	29	28	27	26	25	24
Name:	Apparent Energy Byte 3							

Bit:	23	22	21	20	19	18	17	16
Name:	Apparent Energy Byte 2							

Bit:	15	14	13	12	11	10	9	8
Name:	Apparent Energy Byte 1							

Bit:	7	6	5	4	3	2	1	0
Name:	Apparent Energy Byte 0							

This signed register provides the raw apparent energy accumulated over the most recent DSP cycle.

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Checksum (CHKSUM) (0x060)

Bit:	15	14	13	12	11	10	9	8
Name:	Checksum High Byte							
Reset:								

Bit:	7	6	5	4	3	2	1	0
Name:	Checksum Low Byte							
Reset:								

This register contains the calculated 16-bit arithmetic checksum over critical configuration and calibration registers. It is updated on every DSP cycle. In use, the administrative processor records the value in the CHKSUM register and then checks it periodically to verify that no configuration or calibration registers have changed. The MAXQ3181 sets the CHSCH bit when this register's value changes.

The registers included in the checksum calculation include the following:

SYS_KHZ		R_ADCRATE	A.I_GAIN	B.I_GAIN	C.I_GAIN
VOLT_CC	REJ_NS	R_ADCACQ	A.V_GAIN	B.V_GAIN	C.V_GAIN
AMP_CC	AVG_NS	R_SPICF	A.E_GAIN	B.E_GAIN	C.E_GAIN
PWR_CC	AVG_C	NZX_TIMO			
ENR_CC	HPF_C	COM_TIMO	A.OFFS_HI	B.OFFS_HI	C.OFFS_HI
CYCNT		ACC_TIMO	A.GAIN_LO	B.GAIN_LO	C.GAIN_LO
PLSCFG1	OCLVL	I1THR	A.OFFS_LO	B.OFFS_LO	C.OFFS_LO
	OVLVL	I2THR	A.PA0	B.PA0	C.PA0
PLS1_WD	UVLVL	ZC_LPF	A.PA1	B.PA1	C.PA1
THR1	NOLOAD		A.PA2	B.PA2	C.PA2
	R_ACFG				

Neutral Current

RMS Current, Neutral (I.N) (0x840)

This register reports the RMS current of the neutral current channel. The units are defined by the AMP_CC setting.

Special Commands

Table 7 shows the read-only virtual registers that activate special commands when read by the master. Some commands return dummy values.

Applications Information

Grounds and Bypassing

Careful PCB layout significantly minimizes noise on the analog inputs, resulting in less noise on the digital I/O that could cause improper operation. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

The MAXQ3181 must have separate ground areas for the analog (AGND) and digital (DGND) portions, connected together at a single point.

CMOS design guidelines for any semiconductor require that no pin be taken above DVDD or below DGND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Specific Design Considerations for MAXQ3181-Based Systems

To reduce the possibility of coupling noise into the microcontroller, the system should be designed with a crystal or oscillator in a metal case that is grounded to the digital plane. Doing so reduces the susceptibility of the design to fast transient noise.

Because the MAXQ3181 is designed for use in systems where high voltages are present, care must be taken to route all signal paths, both analog and digital, as far away as possible from the high-voltage components.

It is possible to construct more elaborate metering designs using multiple MAXQ3181 devices. This can be accomplished by using a single SPI bus to connect all

Table 7. Virtual Registers That Activate Special Commands

NAME	ADDRESS	DESCRIPTION	DATA LENGTH (BYTES)
UPD_SFR	0x900	Reading this register copies the mirror registers (R_ADCF, R_ADCRATE, R_ADCACQ, R_SPICF) into hardware SFR registers. The read returns dummy data.	1
UPD_MIR	0xA00	Reading this register copies hardware SFR registers into mirror registers (R_ADCF, R_ADCRATE, R_ADCACQ, R_SPICF). The read returns dummy data.	1
DSPVER	0xC00	Reading this register returns the DSP firmware version number.	2
RAWTEMP	0xC01	Reading this register initiates the sampling and averaging of two internal temperature readings. The result in internal temperature units is read from this register LSB first. Use the following equation to convert a raw temperature reading to Celsius: T[c] = T[raw] x TempFactor - 273.15 where TempFactor is a value to be determined by calibration. Note that the final value may be slightly higher than ambient due to internal die heating.	2
ENTER STOP	0xC02	Reading this register places the device into Stop Mode.	1
ENTER LOWPM	0xC03	Reading this register places the device into LOWPM Mode.	1
EXIT LOWPM	0xC04	Reading this register exits LOWPM Mode.	1

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the MAXQ3181 devices together but using separate slave select lines to individually select each MAXQ3181.

Additional Documentation

Designers must ensure they have the latest MAXQ3181 errata documents. Errata sheets contain deviations from published specifications. A MAXQ3181 errata sheet for any specific device revision is available at **www.maxim-ic.com/errata**.

Technical Support

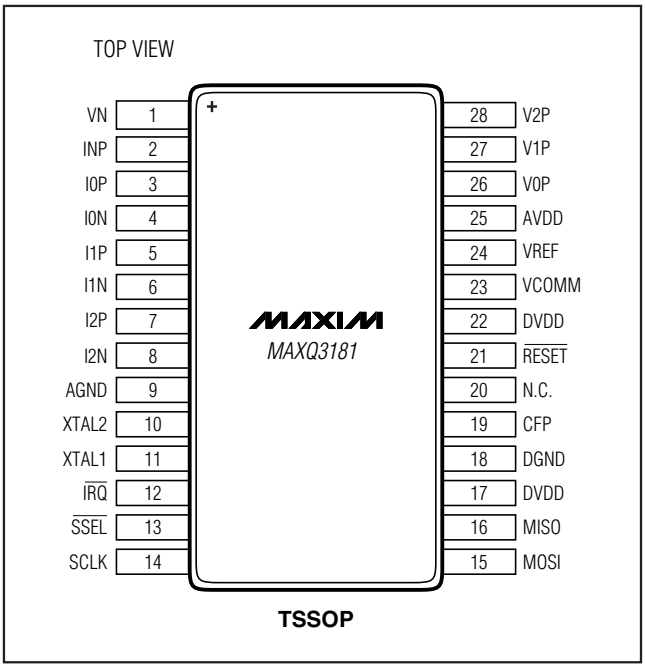
For technical support, go to **https://support.maxim-ic.com/micro**.

Package Information

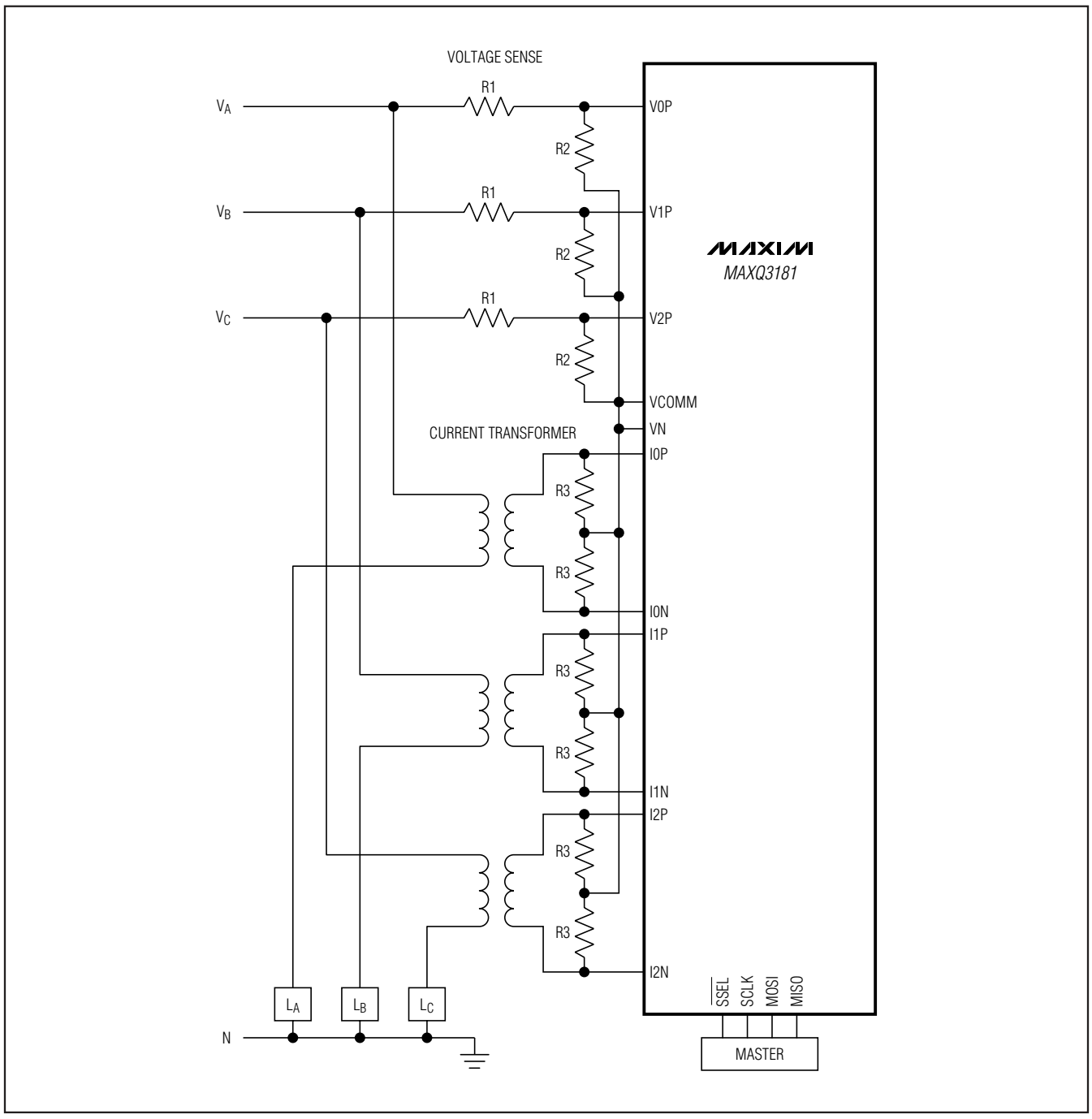
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	U28+3	**21-0066**

Pin Configuration



Typical Application Circuit



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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release.	—
1	12/09	Changed the voltage range on VxP, IxN relative to AGND to -0.3V to +4.0V in the *Absolute Maximum Ratings* section.	8
		Added a statement that the CRC be enabled for read and write in the *Host Software Design* section.	22