TUSB1002 USB3.1 10 Gbps Dual-Channel Linear Redriver

1 Features

- Supports USB3.1 SuperSpeed (5 Gbps) and SuperSpeedPlus (10 Gbps)
- Supports PCI Express Gen3, SATA Express, and SATA Gen3.
- Ultra Low-Power Architecture
  - Active: < 340 mW
  - U2/U3: < 8 mW
  - Disconnected: < 2 mW
- Adjustable Voltage Output Swing Linear Range up to 1200 mVpp
- No Host/Device Side Requirement
- 16 Settings for up to 16 dB at 10 Gbps of Linear Equalization
- Adjustable DC Equalization Gain
- Hot-Plug Capable
- Pin-to-Pin Compatible With LVPE502A and LVPE512 USB 3.0 Redriver
- Temperature Range: 0°C to 70°C
- ±6 KV HBM ESD
- Available in Single 3.3 V Supply.
- Available in 4 mm x 4 mm VQFN

2 Applications

- Notebook and Desktop PC
- TVs
- Tablets
- Cell Phones
- Active Cable
- Docking Stations

3 Description

The TUSB1002 is the industry's first dual-channel USB 3.1 SuperSpeedPlus (SSP) redriver and signal conditioner. The device offers low power consumption on a 3.3-V supply with its ultra-low-power architecture. It supports the USB3.1 low power modes which further reduces idle power consumption.

The TUSB1002 implements a linear equalizer, supporting up to 16 dB of loss due to Inter-Symbol Interference (ISI). When USB signals travel across a PCB or cable, signal integrity degrades due to loss and inter-symbol interference. The linear equalizer compensates for the channel loss, and thereby, extends the channel length and enables systems to pass USB compliance. The dual lane implementation and small package size provides flexibility in the placement of the TUSB1002 in the USB3.1 path.

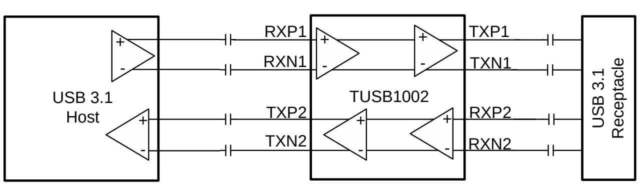
The TUSB1002 is available in either a a 24-pin 4 mm x 4 mm VQFN. It is also available in a commercial grade (TUSB1002).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB1002	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision D (October 2017) to Revision E	Page
• Deleted TUSB1002I industrial from the *Feature*, *Description*, and *Device Information*	1
• Deleted TUSB1002I Operating free-air temperature from the *Recommended Operating Conditions*	6
• Deleted TUSB1002I from the *Thermal Information* table	6

Changes from Revision C (August 2017) to Revision D	Page
• Changed pin 8 From: RXIN To: RX1N in the RGE pin image	4

Changes from Revision B (August 2017) to Revision C	Page
• Changed *Feature* From: 14 Settings for up to 15 dB at 10 Gbps of Linear Equalization To: 16 Settings for up to 16 dB at 10 Gbps of Linear Equalization	1
• Deleted the RMQ package option from the *Pin Configuration and Functions* section	4
• Deleted the RMQ package from the *Pin Functions* table	4
• Changed the description of pin 7 From: R = Test Mode To: R = PCIe / Test Mode. in the *Pin Functions* table	5
• Deleted the RMQ column from *Thermal Information* table	6
• Added Differential crosstalk between TX and RX signal pairs.	7
• From: $E_{Q(GAIN\text{-}10Gbps)}$ 15dB To: $E_{Q(GAIN\text{-}10Gbps)}$ 16dB	7
• EQ setting 15 changed from Reserved to 10.4 / 16.0	16
• EQ setting 16 changed from Reserved to 10.6 / 16.3	16
• Added the *PCIe/SATA/SATA Express Redriver Operation* section.	17
• Added the *Typical SATA, PCIe, and SATA Express Application* section	22

Changes from Revision A (May 2016) to Revision B **Page**

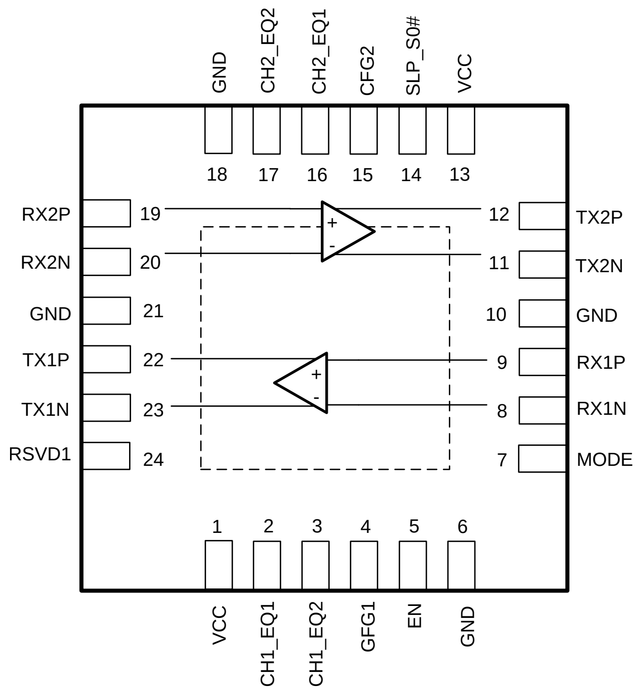
- Added a capacitor to the RXP2 and RXN2 pins of the Simplified Schematic ... 1
- Added a capacitor to the RXP2 and RXN2 pins of Figure 17 ... 19
- Updated the A/C coupling Capacitor section of Table 4 ... 19
- Changed text in the *Detailed Design Procedure* From: No A/C coupling capacitors are placed on the RX2P/N. To: 330nF A/C coupling capacitors along with 220k resistors are placed on the RX2P and RX2N. Inclusion of these 330nF capacitors and 220k resistors is optional but highly recommended. If not implemented, then RX2P/N should be DC-coupled to the USB receptacle. ... 20
- Added 330nF AC capacitors (C12 and C13) on RX2P and RX2N in Figure 18 ... 20

Changes from Original (May 2016) to Revision A **Page**

- Changed device status From: Preview To: Production ... 1

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	**RGE**			
RX1P	9	90Ω Differential Input		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1
RX1N	8			Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1
RX2P	19	90Ω Differential Input		Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2
RX2N	20			Differential input for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2.
TX1P	22	90Ω Differential Output		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 1.
TX1N	23			Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 1.
TX2P	12	90Ω Differential Output		Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) positive signals for Channel 2.
TX2N	11			Differential output for SuperSpeed (SS) and SuperSpeedPlus (SSP) negative signals for Channel 2.
CH1_EQ1	2	I (4-level)	PU (approx 45K) PD (approx 95K)	CH1_EQ1. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. This pin along with CH1_EQ2 allows for up to 16 equalization settings.
CH1_EQ2	3	I (4-level)		CH1_EQ2. Configuration pin used to control Rx EQ level for RX1P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. This pin along with CH1_EQ1 allows for up to 16 equalization settings.
CH2_EQ1	16	I (4-level)		CH2_EQ1. Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. This pin along with CH2_EQ2 allows for up to 16 equalization settings.
CH2_EQ2	17	I (4-level)		CH2_EQ2. Configuration pin used to control Rx EQ level for RX2P/N. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. This pin along with CH2_EQ1 allows for up to 16 equalization settings.

Pin Functions (continued)

PIN		TYPE	INTERNAL PULLUP PULLDOWN	DESCRIPTION
NAME	RGE			
EN	5	I (2-level)	PU (approx 400 K)	EN. Places TUSB1002 into shutdown mode when asserted low. Normal operation when pin is asserted high. When in shutdown, TUSB1002's receiver terminations will be high impedance and tx/rx channels will be disabled.
CFG1	4	I (4-level)	PU (approx 45K) PD (approx 95K)	CFG1. This pin along with CFG2 will select VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. Refer to Table 3 for VOD linearity range and DC gain options.
CFG2	15	I (4-level)		CFG2. This pin along with CFG1 will set VOD linearity range and DC gain for both channels 1 and 2. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. Refer to Table 3 for VOD linearity range and DC gain options.
MODE	7	I (4-level)	PU (approx 45 K) PD (approx 95K)	MODE. This pin is for selecting different modes of operation. The state of this pin is sampled after the rising edge of EN. Refer to Figure 2 for details of timing. 0 = Test Mode. TI Internal Use Only. R = PCIe / Test Mode. PCIe Mode and TI Internal use only F = USB3.1 Dual Channel Operation enabled (TUSB1002 normal mode). 1 = USB3.1 Single-channel operation.
RSVD1	24	O		RSVD1. Under normal operation, this pin will be driven low by TUSB1002. Recommend leaving this pin unconnected on PCB.
SLP_S0#	14	I (2-level)	PU (approx 400 K)	SLP_S0#. This pin when asserted low will disable Receiver Detect functionality. While this pin low and TUSB1002 is in U2/U3, TUSB1002 disables LOS and LFPS detection circuitry and Rx termination for both channels will remain enabled. If this pin is low and TUSB1002 is in Disconnect state, the Rx detect functionality is disabled and Rx termination for both channels will be disabled. If the system SoC does not support a GPIO that indicates system sleep state, then it is recommended to leave this pin unconnected. 0 – Rx Detect disabled 1 – Rx Detect enabled
NC				No Connect. Leave unconnected on PCB.
VCC	1, 13	Power		3.3 V (±10%) Supply.
GND	6, 10, 18, 21	GND		Ground
Thermal pad				Thermal pad. Recommend connecting to a solid ground plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range(2), V_{CC}		–0.3	4	V
IO Voltage Range	Differential Voltage between RX1P/N and RX2P/N.		±2.5	V
	Voltage at RX1P/N and RX2P/N.	–0.5	V_{CC} + 0.5	V
	Voltage on Control IO pins	–0.5	V_{CC} + 0.5	V
Maximum junction temperature, T_J			105	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	3.3 V Supply Voltage	3	3.3	3.6	V
	Supply Ramp requirement			50	ms
$V_{(PSN)}$	Supply Noise on V_{CC} pins			100	mV
T_A	Operating free-air temperature	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB1002 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics, Power Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(U0\_SSP\_1200mV)}$	TUSB1002 power under normal operation in U0 operating a SuperSpeedPlus datarate with linear range set to 1200mV.	At 10 Gbps; V_{CC} supply stable; V_{CC} = 3.3 V; V_{OD} = 1200 mVpp; Pattern = CP9		340		mW
$P_{(U0\_SSP\_1000mV)}$	TUSB1002 power under normal operation in U0 operating a SuperSpeedPlus datarate with linear range set to 1000mV.	At 10 Gbps; V_{CC} supply stable; V_{CC} = 3.3 V; V_{OD} = 1000 mVpp; Pattern = CP9		325		mW
$P_{(U0\_SSP\_900mV)}$	TUSB1002 power under normal operation in U0 operating a SuperSpeedPlus datarate with linear range set to 900mV.	At 10 Gbps; V_{CC} supply stable; V_{CC} = 3.3 V; V_{OD} = 900 mVpp; Pattern = CP9		298		mW
$P_{(U0\_SS\_1200mV)}$	TUSB1002 power under normal operation in U0 operating a SuperSpeed datarate.	At 5 Gbps; V_{CC} supply stable; V_{CC} = 3.3 V; V_{OD} = 1200 mVpp; Pattern = CP0.		340		mW
$P_{(U1)}$	TUSB1002 power when U1.	In U1; VCC supply stable; V_{CC} = 3.3 V; V_{OD} = 1200 mVpp		340		mW
$P_{(U2U3)}$	TUSB1002 power when in U2/U3.	Both channels 1 and 2 in U2/U3; VCC supply stable; V_{CC} = 3.3 V;		8		mW
$P_{(U2U3\_SLP)}$	TUSB1002 power when in U2/U3 and SLP_S0# is low.	Both channels 1 and 2 in U2/U3; VCC supply stable; V_{CC} = 3.3 V;		0.850		mW
$P_{(DISCONNECT\_NONE)}$	TUSB1002 power when no USB device detected on both TX1P/N or TX2P/N.	RX1 and RX2 termination disabled; VCC supply stable; V_{CC} = 3.3 V		2		mW
$P_{(DISCONNECT\_ONE)}$	TUSB1002 power when a USB device detected on either TX1P/N or TX2P/N but not both.	Either RX1 or RX2 termination enabled both not both enabled; VCC supply stable; V_{CC} = 3.3 V		5		mW
$P_{(DISCONNECT\_SLP)}$	TUSB1002 power when no USB device detected on either TX1P/N or TX2P/N and SLP_S0# is low..	RX1 and RX2 termination disabled; VCC supply stable; V_{CC} = 3.3 V		0.850		mW
$P_{(SHUTDOWN)}$	TUSB1002 power when EN is asserted low.;	VCC supply stable; V_{CC} = 3.3 V, EN = 0		0.6		mW

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-Level Inputs (MODE, CFG1, CFG2,CH1_EQ1, CH1_EQ2, CH2_EQ1, CH2_EQ2)						
I_{IH}	High level input current	V_{CC} = 3.6 V; V_{IN} = 3.6 V	20		80	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V; V_{IN} = 0 V	–160		–40	µA
V_{TH}	Threshold 0 / R	V_{CC} = 3.3 V		0.55		V
	Threshold R/ Float			1.65		V
	Threshold Float / 1			2.8		V
R_{PU}	Internal pull-up resistance			45		kΩ
R_{PD}	Internal pull-down resistance			95		kΩ
EN, SLP_S0# Input						
V_{IH}	High level input voltage	V_{CC} = 3. V	1.7		VCC	V
V_{IL}	Low level input voltage	V_{CC} = 3.3 V	0		0.7	V
I_{IH}	High level input current	V_{CC} = 3.6 V, EN = 3.6 V	–10		10	µA
I_{IL}	Low level input current	V_{CC} = 3.6 V, EN = 0 V	–15		15	µA
$R_{(EN-PU)}$	Internal pull-up resistance for EN and SLP_S0#.			400		kΩ
USB3.1 RECEIVER INTERFACE (RX1P/N AND RX2P/N)						
$R_{L(RX-DIFF)}$	RX Differential return loss	SDD11 10 MHz at 90 Ω		–19		dB
		SDD11 2 GHz at 90 Ω		–14		dB
		SDD11 5 – 10 GHz at 90 Ω		–7		dB
$R_{L(RX-CM)}$	RX Common mode return loss	0.5 – 5 GHz at 90 Ω		–10		dB
X-TALK	Differential crosstalk between TX and RX signal pairs.			-50		dB
$E_{Q(GAIN-10Gbps)}$	Equalization Gain	50 mVpp At 5 GHz		16		dB
$E_{Q(DC0)}$	DC Equalization Gain at 0dB setting.	500 mVpp V_{ID} at 100 MHz; 1200mV Linear Range Setting; Refer to Table 3		-0.15		dB

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$E_{Q(DC1)}$	DC Equalization Gain at +1dB setting.	500 mVpp V_{ID} at 100 MHz; 1200mV Linear Range Setting;		0.80		dB
$E_{Q(DC2)}$	DC Equalization Gain at +2dB setting.	500 mVpp V_{ID} at 100 MHz; 1000mV Linear Range Setting;		1.5		dB
$E_{Q(DC-1)}$	DC Equalization Gain at -1dB setting.	500 mVpp V_{ID} at 100 MHz; 1200mV Linear Range Setting;		–1.1		dB
$E_{Q(DC-2)}$	DC Equalization Gain at -2dB setting.	500 mVpp V_{ID} at 100 MHz; 1200mV Linear Range Setting;		–2.05		dB
$V_{(DIFF\_IN)}$	Input differential peak-peak voltage swing range.			2000		mV
$V_{(RX-DC-CM)}$	RX DC common mode voltage		1.65	1.85	2.0	V
$R_{(RX-CM-DC)}$	Receiver DC common mode impedance	Measured at connector. Present when SuperSpeed USB device detected on TXP/N	18		30	Ω
$R_{(RX-DIFF-DC)}$	Receiver DC differential impedance	Measured at connector. Present when SuperSpeed USB device detected on TXP/N; SLP_S0# = 1;	72		120	Ω
$Z_{(RX-HIGH-IMP-DC-POS)}$	DC input CM input impedance when termination is disabled.	Measured at connector. Present when no SuperSpeed USB device detected on TXP/N or while V_{CC} is ramping	30			KΩ
$V_{(RX-SIGNAL\_DET\_DIFF-PP)}$	Input differential peak-to-peak Signal Detect Assert level	at 10 Gbps. No loss input channel and PRBS7 pattern		92		mV
$V_{(RX-IDLE\_DET\_DIFF-PP)}$	Input differential peak-to-peak Signal Detect De-assert Level	at 10 Gbps. No loss input channel and PRBS7 pattern		62		mV
$V_{(RX-LFPS-DET-DIFF-P-P)}$	LFPS Detect threshold. Below min is noise.	Measured at connector. Below min is squelched	100		300	mV
$V_{(RX-CM-AC-P)}$	Peak RX AC common mode voltage	Measured at package pin			150	mV
$C_{(RX-PARASITIC)}$	Rx Input capacitance for return loss	At package pin			0.5	pF
USB3.1 Transmitter Interface (TX1P/N and TX2P/N)						
$R_{L(TX-DIFF)}$	TX Differential return loss	SDD22 10MHz – 2 GHz at 90 Ω		–15		dB
		SDD22 5 GHz at 90 Ω		–11		dB
		SDD22 5 - 10 GHz at 90 Ω		–7		dB
$R_{L(TX-CM)}$	TX Common Mode return loss	0.05 – 5 GHz at 90 Ω		–9		dB
$V_{(TX-DIFF-PP\_1200)}$	Differential peak-to-peak TX voltage swing linear dynamic range	CFG1 pin = F or 1; Refer to Table 3 Measured at -1dB compression point = 20log (VOD/VOD_linear)	1200	1450		mV
$V_{(TX-DIFF-PP\_1000)}$	Differential peak-to-peak TX voltage swing linear dynamic range	CFG1 pin = R; Refer to Table 3 Measured at -1dB compression point = 20log (VOD/VOD_linear)	1000			mV
$V_{(TX-DIFF-PP\_900)}$	Differential peak-to-peak TX voltage swing linear dynamic range	CFG1 pin = 0; Refer to Table 3Measured at -1dB compression point = 20log (VOD/VOD_linear)	900			mV
$V_{(TX-RCV-DETECT)}$	The amount of voltage change allowed during Receiver Detection.				600	mV
$V_{(TX-CM-IDLE-DELTA)}$	Transmitter idle common-mode voltage change while in U2/3 and not actively transmitting LFPS.		–600		600	mV
$V_{(TX-DC-CM)}$	TX DC common mode voltage	1200mVpp Linear Range setting.	0	1.85	2	V
$V_{(TX-IDLE-DIFF-AC-PP)}$	AC Electrical Idle differential peak-to-peak output voltage	At package pin.	0		10	mV
$V_{(TX-IDLE-DIFF\_DC)}$	DC Electrical Idle differential output voltage	At package pin. After low pass filter to remove AC component.	0		14	mV
$V_{(TX-CM-AC-PP)}$	Transmitter AC common mode peak-peak voltage in U0	1200mVpp linear range; CHx_EQ setting matches input channel insertion loss;			80	mV
$V_{(TX-CM-DC-ACTIVE-IDLE-DELTA)}$	Absolute DC common mode voltage between U1 and U0.	At package pin.			200	mV
$I_{(TX-SHORT)}$	TX short-circuit current limit				106	mA
$R_{(TX-DC)}$	TX DC common mode impedance	At package pin	18		30	Ω

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(TX-DIFF-DC)}$	TX DC differential impedance		72	90	120	Ω
$C_{(TX-PARASTIC)}$	TX input capacitance for return loss	At package pin			0.7	pF
$C_{(AC-COUPLING)}$	External AC Coupling capacitor on differential pairs.		75		265	nF

6.7 Power-Up Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
t_{d_pg}	Internal Power Good asserted high when V_{CC} is at 2.5 V	See Figure 2		5	µs
t_{cfg_su}	CFG(1) pins setup before internal Reset(2) high	See Figure 2	0		s
t_{cfg_hd}	CFG(1) pins hold after internal Reset(2) high	See Figure 2	500		µs
t_{VCC_RAMP}	V_{CC} supply ramp requirement	See Figure 2		50	ms

(1) Following pins comprise CFG pins: MODE, CFG1, CFG2, CH1_EQ1, CH1_EQ2, CH2_EQ1, and CH2_EQ2.
(2) Internal reset is the AND of EN pin and internal Power Good.

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SuperSpeed (SS) and SuperSpeedPlus(SSP)						
$t_{IDLEEntry}$	Delay from U0 to electrical idle.	See Figure 1			150	ps
$t_{IDLEExit\_U1}$	U1 exit time: break in electrical idle to the transmission of LFPS.	See Figure 1			150	ps
$t_{IDLEExit\_U2U3}$	U2/U3 exit time: break in electrical idle to transmission of LFPS	See Figure 1		2.3	3.75	µs
$t_{DIFF-DLY}$	Differential propagation delay				150	ps
$t_{PWRUPACTIVE}$	Time when V_{CC} reach 2.5 V to device active and performing Rx.Detect.	EN = H			7	ms

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB3.1 Transmitter Interface (TX1P/N, TX2P/N)						
$t_{TX-RISE-FALL}$	Transmitter rise/fall time	20% to 80% of differential output; 1200mVpp linear range setting		40		ps
$t_{RF-MISMATCH}$	Transmitter rise/fall mismatch	20% to 80% of differential output; 1200mVpp linear range setting; 1000mVpp VID;		0.01		UI
t_{TX-DJ}	Residual deterministic jitter	@10Gbps; 1200mVpp Linear Range Setting		0.08		UI

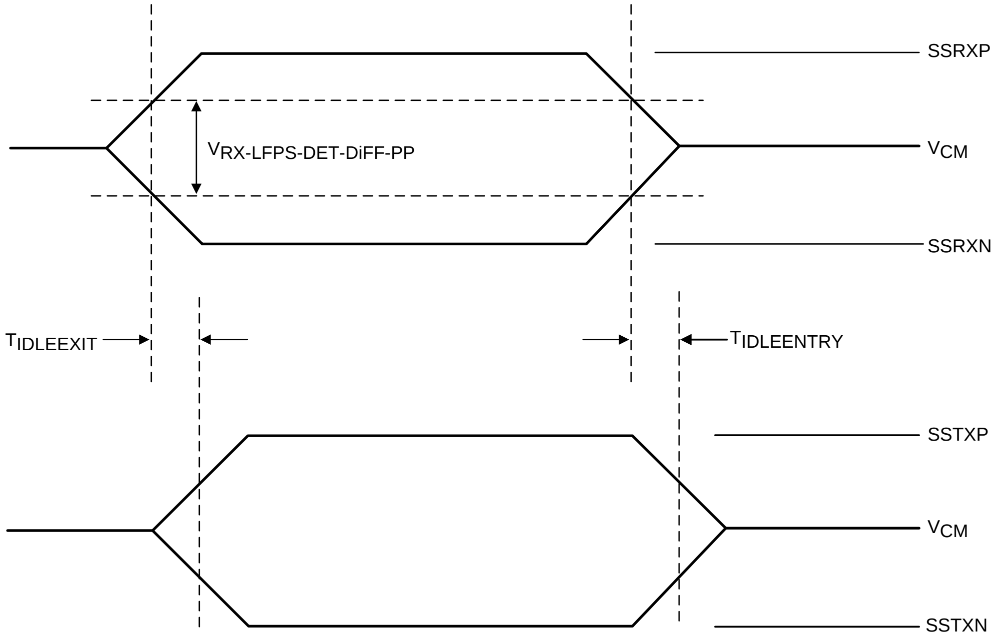


Figure 1. Idle Entry and Exit Latency

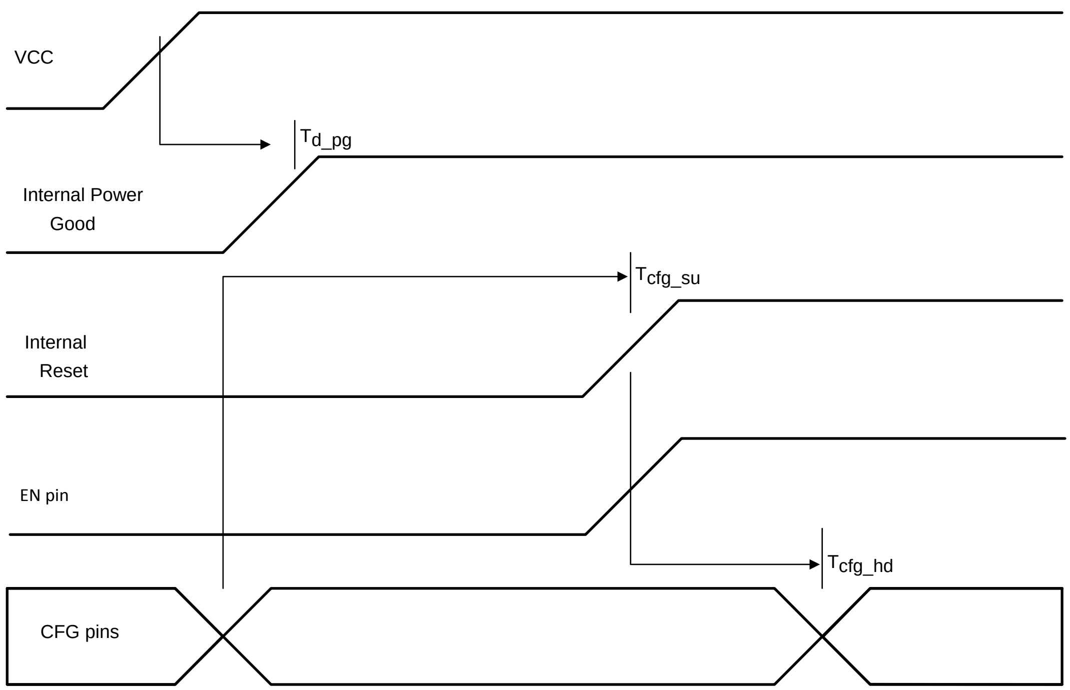


Figure 2. Power-Up Diagram

6.10 Typical Characteristics

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

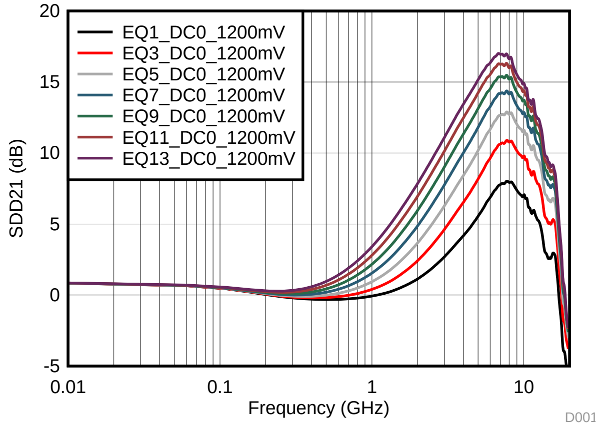


Figure 3. 1200 mV DC0 Gain Odd EQ Settings Curves

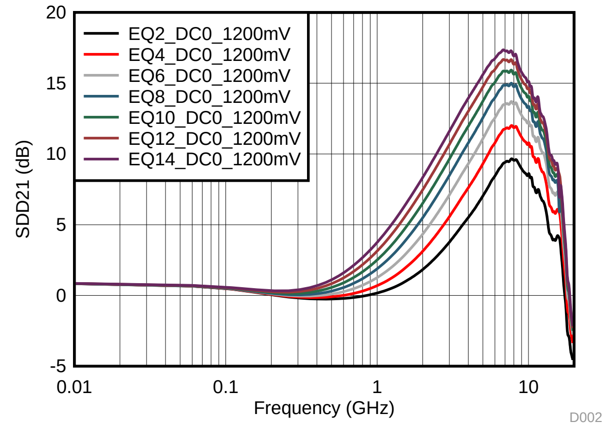


Figure 4. 1200 mV DC0 Even EQ Settings Curves

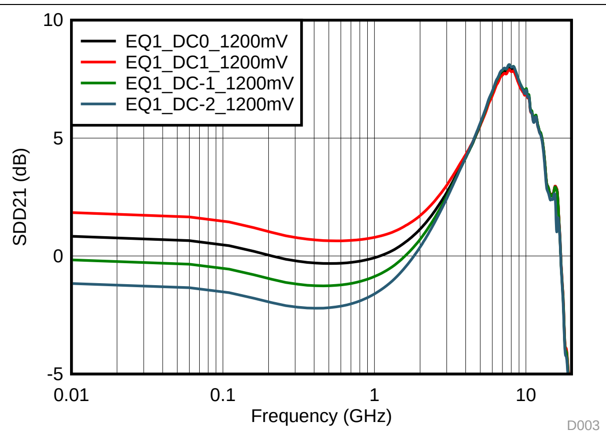


Figure 5. 1200 mV DC Gain Adjustments Curves

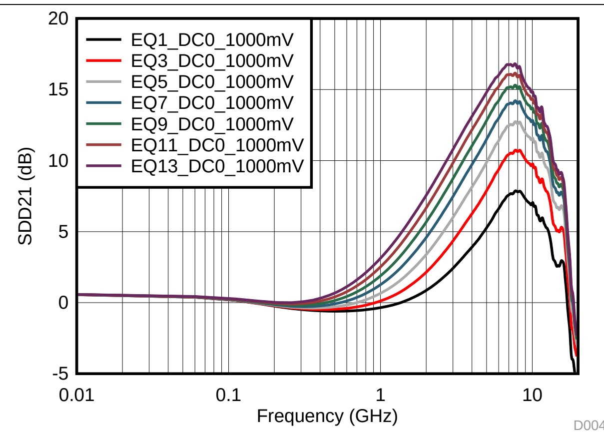


Figure 6. 1000 mV DC0 Gain Odd EQ Settings Curves

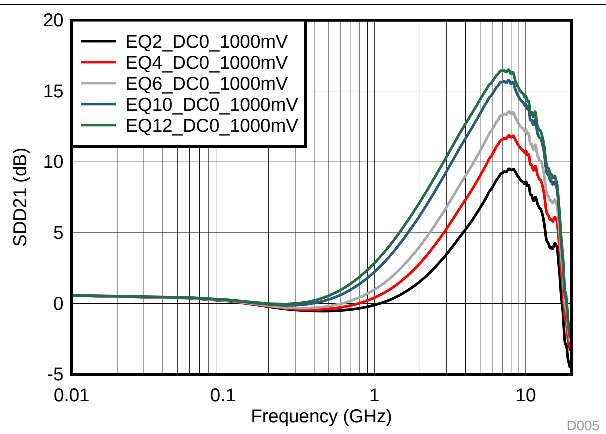


Figure 7. 1000 mV DC0 Gain Even EQ Settings Curves

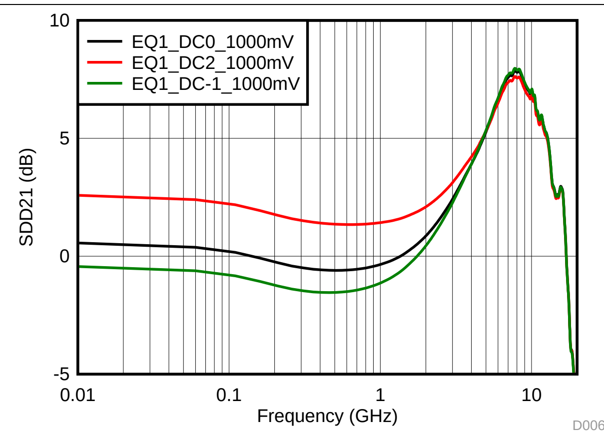


Figure 8. 1000 mV DC Gain Adjustments Curves

Typical Characteristics (continued)

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

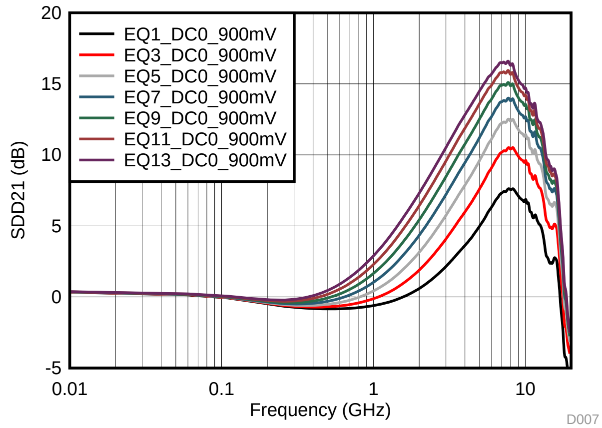


Figure 9. 900 mV DC0 Gain Odd EQ Settings Curves

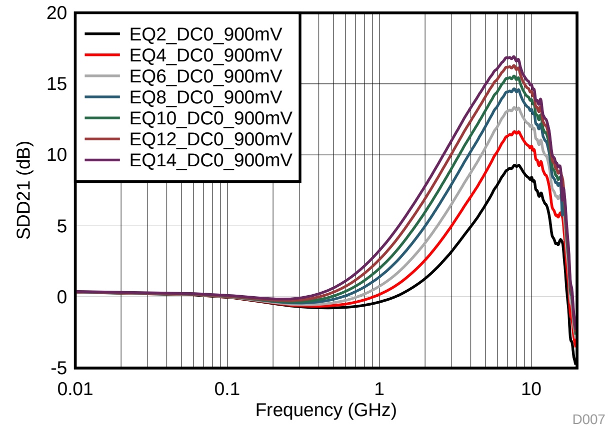


Figure 10. 900 mV DC0 Gain Even EQ Settings Curves

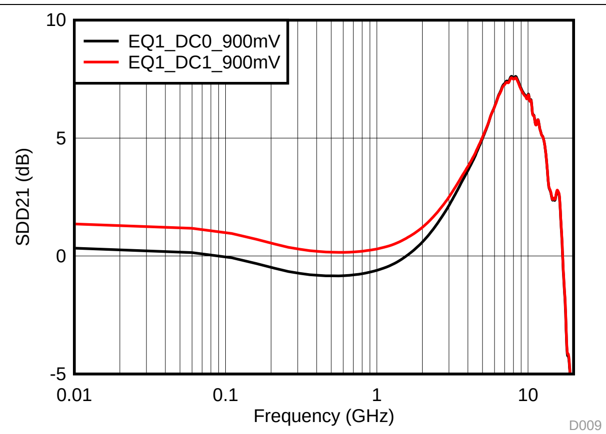


Figure 11. 900 mV DC Gain Adjustment Curves

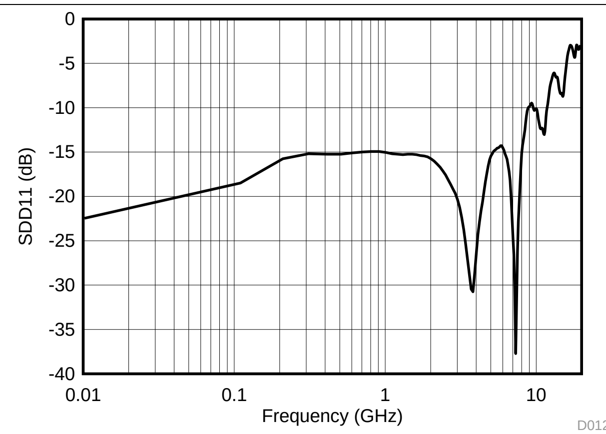


Figure 12. SDD11 Return Loss

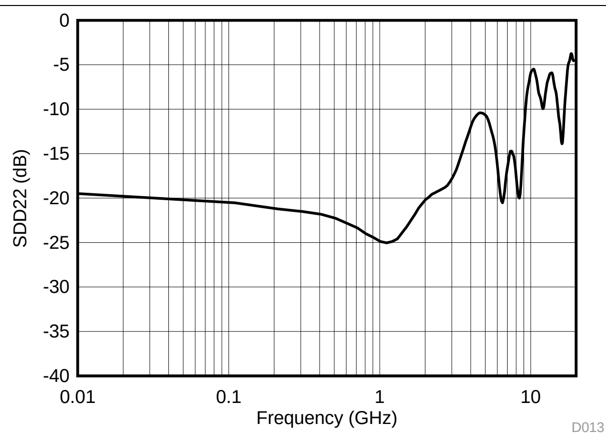


Figure 13. SDD22 Return Loss

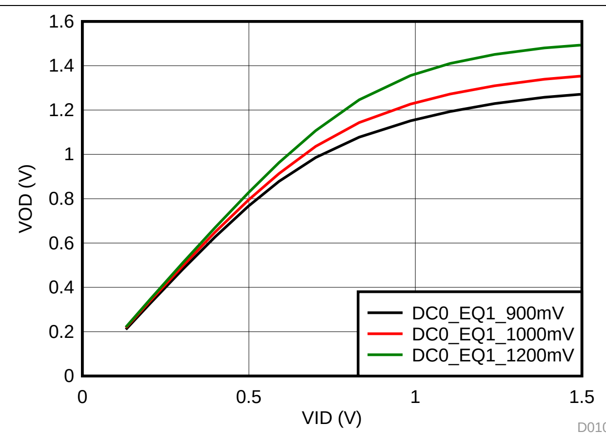


Figure 14. 5-GHz Sine Wave VID vs VOD Linearity Range Setting

Typical Characteristics (continued)

V_{CC} = 3.3V , 25°C, 200 mVpp V_{ID} sine wave, Z_O = 100 Ω, RGE package

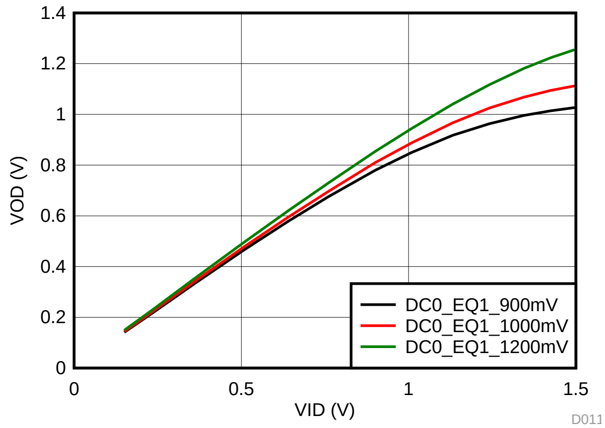


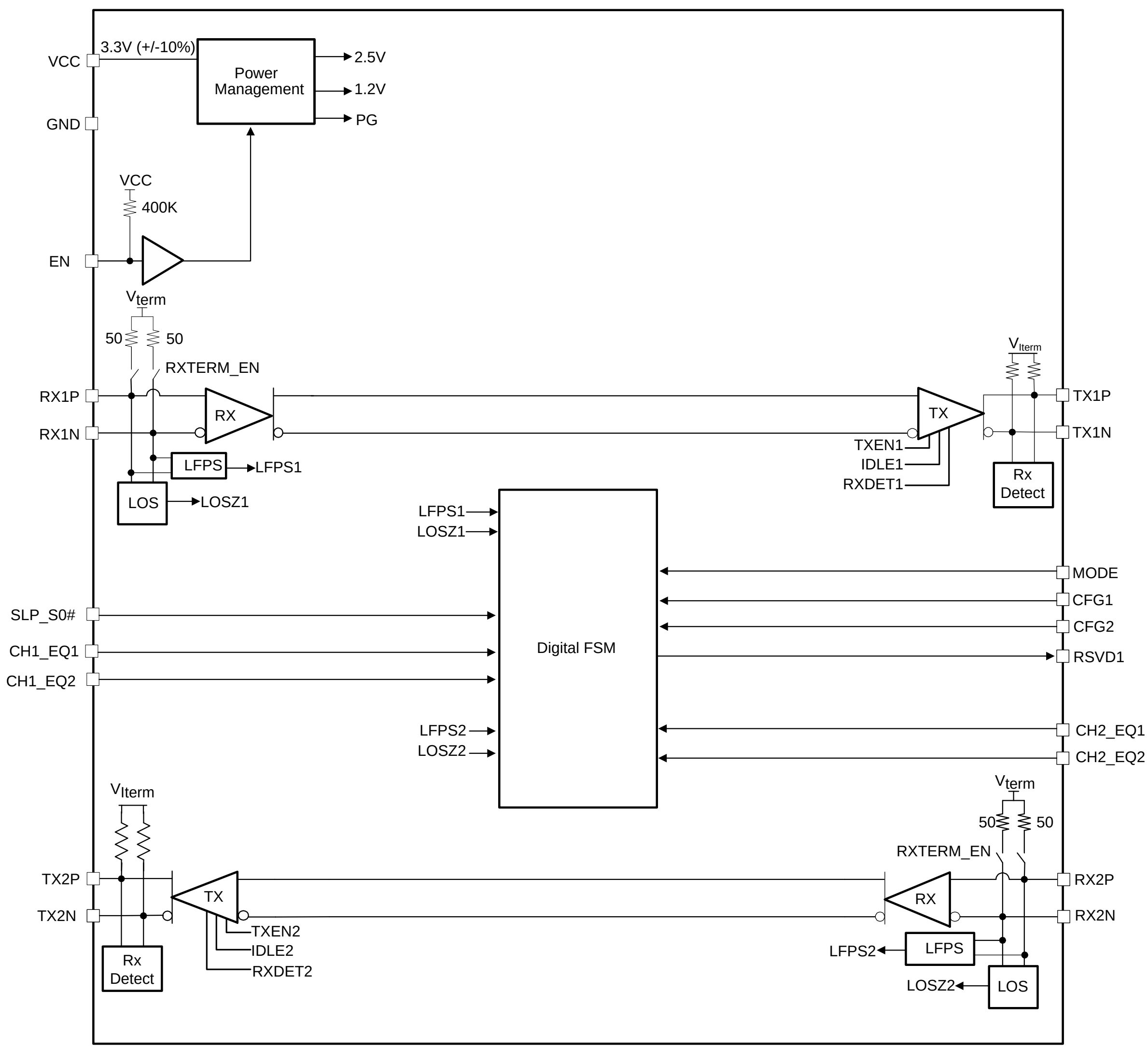
Figure 15. 100-MHz Sine Wave VID vs VOD Linearity Range Setting

7 Detailed Description

7.1 Overview

The TUSB1002 is the industry's first, dual lane USB 3.1 SuperSpeedPlus redriver. As signals traverse through a channel (like FR4 trace) the amplitude of the signal is attenuated. The attenuation varies depending on the frequency content of the signal. Depending the length of the channel this attenuation could be large enough resulting in signal integrity issues at a USB 3.1 receiver. By placing a TUSB1002 between USB3.1 host and device the attenuation effect of the channel can eliminated or minimized. The result is a USB3.1 compatible eye at the devices receiver. With up to 16 receiver equalization settings, the TUSB1002 can support many different channel loss combinations. The TUSB1002 offers low power consumption on a single 3.3 V supply with its ultra low power architecture. It supports the USB3.1 low power modes which further reduces idle power consumption. The TUSB1002 settings are configured through pins. In addition to equalization adjustment, the TUSB1002 provides knobs for adjusting DC gain and voltage output linearity range.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 4-Level Control Inputs

The TUSB1002 has (MODE, CFG1, CFG2, CH1_EQ1, CH1_EQ2, CH2_EQ1, and CH2_EQ2) 4-level inputs pins that are used to control the equalization gain and the output voltage swing dynamic range. These 4-level inputs use a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 45 kΩ pull-up and a 95 kΩ pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 KΩ 5% to V_{CC}. Option 2: Tie directly to V_{CC}.

NOTE

In order to conserve power, the TUSB1002 disables 4-level input's internal pull-up/pull-down resistors after the state of 4-level pins have been sampled on rising edge of EN. A change of state for any four level input pin is not applied to TUSB1002 until after EN pin transitions from low to high.

7.3.2 Linear Equalization

With a linear equalizer, the TUSB1002 can electrically shorten a particular channel allowing for longer run lengths.

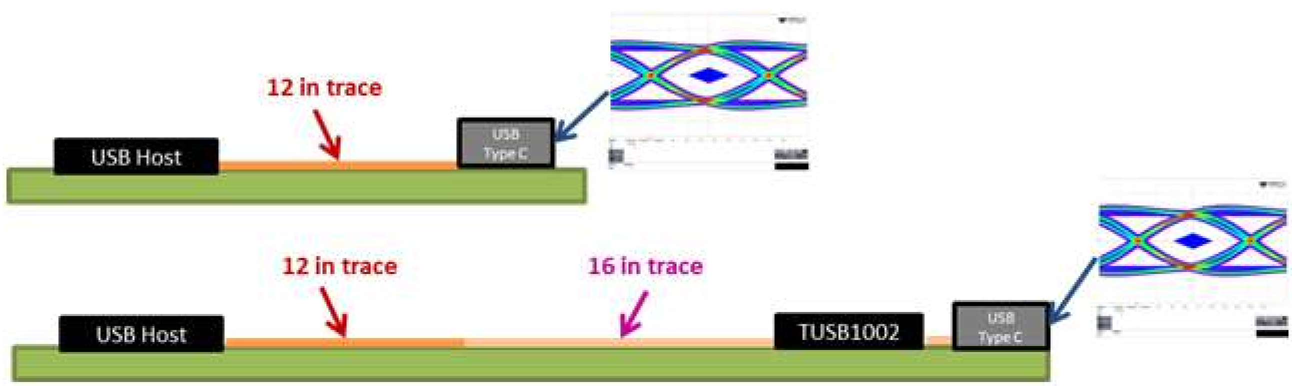


Figure 16. Linear Equalizer

With a TUSB1002, the 28 in trace can be made to have similar insertion loss as the 12 inch trace.

The receiver equalization level for each channel is determined by the state of the CHx_EQ1 and CHx_EQ2 pins, where x = 1 or 2.

Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHx_EQ2 PIN LEVEL	CHx_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.9 / 5.5
2	0	R	2.8 / 7.1
3	0	F	3.5 / 8.2
4	0	1	4.4 / 9.3
5	R	0	5.0 / 10.2
6	R	R	5.8 / 11.1
7	R	F	6.4 / 11.8
8	R	1	7.1 / 12.6
9	F	0	7.6 / 13.1
10	F	R	8.2 / 13.8
11	F	F	8.7 / 14.3
12	F	1	9.2 / 14.8
13	1	0	9.6 / 15.2
14	1	R	10.1 / 15.6
15	1	F	10.4 / 16.0
16	1	1	10.6 / 16.3

7.3.3 Adjustable VOD Linear Range and DC Gain

The CFG1 and CFG2 pins can be used to adjust the TUSB1002 output voltage swing linear range and receiver equalization DC gain. Table 3 details the available options.

For best performance, the TUSB1002 should be operated within its defined VOD linearity range. The gain of the incoming VID should be kept to less than or equal to the TUSB1002 VOD linear range setting. The can be determined by Equation 1:

$$\text{VID at 5 GHz} = \text{VOD} \times (10^{-(Gv/20)})$$

where

- Gv = TUSB1002 Gain and VOD = TUSB100 VOD linearity setting. (1)

For example, for a VOD linearity range setting of 1200 mV, the maximum incoming VID signal at 5 GHz with a CHx_EQ[1:0] setting of 1 (5.5 dB) is 1200 x $(10^{-(5.5/20)})$ = 637 mVpp. The TUSB1002 can be operated outside its VOD linear range but jitter will be higher.

Table 3. VOD Linear Range and DC Gain

SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V_{OD} LINEAR RANGE (mVpp)	CH2 V_{OD} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	-2	-2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	-1	0	1200	1200
14	1	R	0	-1	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

7.3.4 Receiver Detect Control

The SLP_S0# pin offers system designers the ability to control the TUSB1002 Rx.Detect functionality during Disconnect and U2/U3 states and therefore achieving lower consumption in these states. When the system is in a low power state (Sx where x = 1, 2, 3, 4, or 5), system can assert SLP_S0# low to disable TUSB1002 receiver detect functionality. While SLP_S0# is asserted low and USB 3.1 interface is in U3, the TUSB1002 keeps receiver termination active. The TUSB1002 will not respond to any LFPS signaling while in this state. This means that system wake from U3 is not supported while SLP_S0# is asserted low. If the TUSB1002 is in Disconnect state when SLP_S0# is asserted low, then TUSB1002 disables both channels receiver termination. When SLP_S0# is asserted high, the TUSB1002 resumes normal operation of performing far-end receiver termination detection.

7.3.5 USB3.1 Dual Channel Operation (MODE = “F”)

The TUSB1002 in dual-channel operation waits for far-end terminations on both channels 1 and 2 before transitioning to fully active state (U0 mode). This mode of operation, defined as MODE pin = ‘F’, is the most common configuration for USB3.1 Source (DFP) and Sink (UFP) applications.

7.3.6 USB3.1 Single Channel Operation (MODE = “1”)

In some applications, like Type-C USB3.1 active cables, only one of the two channels may be active. For this application, setting MODE pin = ‘1’, enables single-channel operation. In this mode of operation, the TUSB1002 attempts far-end termination on both channels 1 and 2. The channel which has a far-end termination detected will be enabled while the remaining channel will be disabled. If far-end termination is detected on both channels, then TUSB1002 behaves in dual channel operation (both channels enabled).

7.3.7 PCIe/SATA/SATA Express Redriver Operation (MODE = “R”; CFG1 = "0"; CFG2 = "0")

The TUSB1002 can be used as a PCI Express (PCIe) Gen3, SATA Gen3, or SATA Express redriver. When TUSB1002's MODE pin = “R”, CFG1 pin = "0", and CFG2 pin = "0", the TUSB1002 will enable both channels (upstream and downstream) receiver and transmitter paths upon detecting far-end termination on both TX1 and TX2. Both upstream and downstream paths will remain enabled until EN pin is de-asserted low. All USB3.1 power management functionality is disabled in this mode. In this mode the TUSB1002 is transparent to PCIe link power management (L0s, L1) and SATA interface power states. Once far-end termination is detected on both TX1 and TX2, the TUSB1002 power will be at $P_{(U0\_SSP\_1200mV)}$ regardless of the PCIe or SATA power state. To save power during system S3/S4/S5 states it is suggested to de-assert the EN pin to conserve power.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The Shutdown mode is entered when EN pin is low and VCC is active and stable. This mode is the lowest power state of the TUSB1002. While in this mode, the TUSB1002 receiver terminations is disabled.

7.4.2 Disconnect Mode

Next to Shutdown Mode, the Disconnect mode is the lowest power state of the TUSB1002. The TUSB1002 enters this mode when exiting Shutdown mode. In this state, the TUSB1002 periodically checks for far-end receiver termination on both SSTX1 and SSTX2. Upon detection of the far-end receiver’s termination on both ports, the TUSB1002 transitions to a fully active mode called U0 mode.

When SLP_S0# is asserted low and the TUSB1002 is in Disconnect mode, the TUSB1002 remains in Disconnect mode and never perform far-end receiver detection. This allows even lower TUSB1002 power consumption while in the Disconnect mode. Once SLP_S0# is asserted high, the TUSB1002 again starts performing far-end receiver detection so it can know when to exit the Disconnect mode.

7.5 U0 Mode

The U0 mode is the highest power state of the TUSB1002. Anytime high-speed traffic (SuperSpeed or SuperSpeedPlus) is being received, the TUSB1002 remains in this mode. The TUSB1002 only exits this mode if electrical idle is detected on both SSRX1 and SSRX2. While in this mode, the TUSB1002 hs speed receivers and transmitters are powered and active.

7.6 U1 Mode

The U1 mode is the intermediate mode between U0 mode and U2/U3 mode. In U1 mode, the TUSB1002's receiver termination remains enabled and the TXP/N DC common mode is maintained.

7.7 U2/U3 Mode

Next to the disconnect mode, the U2/U3 mode is next lowest power state. While in this mode, the TUSB1002 periodically performs far-end receiver detection. Anytime the far-end receiver termination is not detected on either CH1 or CH2, the TUSB1002 leaves the U2/U3 mode and transition to the Disconnect mode. It also monitors the SSRX1 and SSRX2 for a valid LFPS. Upon detection of a valid LFPS, the TUSB1002 immediately transitions to the U0 mode.

When SLP_S0# is asserted low and the TUSB1002 is in U2/U3 mode, the TUSB1002 remains in U2/U3 state and never perform far-end receiver detection. While in this state, the TUSB1002 ignores LFPS signaling. This allows even lower TUSB1002 power consumption while in the U2/U3 mode. Once SLP_S0# is asserted high, the TUSB1002 again starts performing far-end receive as well as monitor LFPS so it can know when to exit the U2/U3 mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB1002 is a linear redriver designed specifically to compensation for ISI jitter caused by attenuation through a passive medium like traces and cables. Because the TUSB1002 has two independent channels, it can be optimized to correct ISI in both the upstream and downstream direction through 16 different equalization choices. Placing the TUSB1002 between a USB3.1 Host/device controller and a USB3.1 receptacle can correct signal integrity issues resulting in a more robust system.

8.2 Typical USB3.1 Application

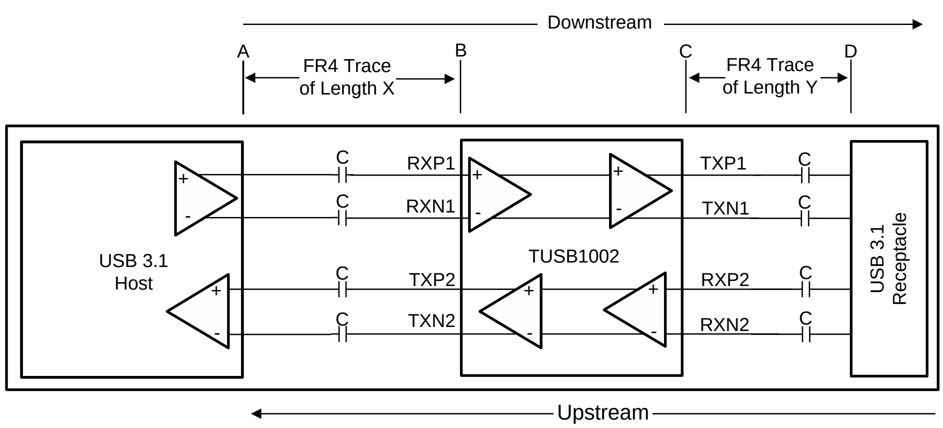


Figure 17. TUSB1002 in USB3.1 Host Application

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 4.

Table 4. Design Parameters

PARAMETER	VALUE
VCC supply (3 V to 3.6 V)	3.3 V
Mode of Operation (Dual or Half Channel)	MODE = F (Floating) for USB3.1 Dual Channel
TX1, TX2, RX1 A/C coupling Capacitor (75 nF to 265 nF)	100 nF
RX2 A/C coupling Capacitor (297 nF to 363 nF)	Suggest 330 nF ±10%
RX2 pull-down resistors on USB receptacle side of AC capacitor (200K to 242K ohms)	220k
A to B FR4 Length (inches)	8
A to B FR4 Trace Width (mils)	4
C to D FR4 length (inches)	2
C to D FR4 Trace Width (mils)	4
USB3.1 Host Sleep GPIO Support	No (SLP_S0# pin floating)
DC Gain (-2, -1, 0, +1, +2)	0 dB (CFG[2:1] pins floating)
Linear Range (900 mV, 1000 mV, or 1200 mV)	1200 mV (CFG[2:1] pins floating)

8.2.2 Detailed Design Procedure

The TUSB1002 differential receivers and transmitters have internal BIAS and termination. For this reason, the TUSB1002 must be connected to the USB3.1 host and receptacle through external A/C coupling capacitors. In this example as depicted in Table 4, 100 nF capacitors are placed on TX2P and TX2N, RX1P and RX1N, and TX1P and TX1N. 330 nF A/C coupling capacitors along with 220k resistors are placed on the RX2P and RX2N. Inclusion of these 330nF capacitors and 220k resistors is optional but highly recommended. If not implemented, then RX2P/N should be DC-coupled to the USB receptacle.

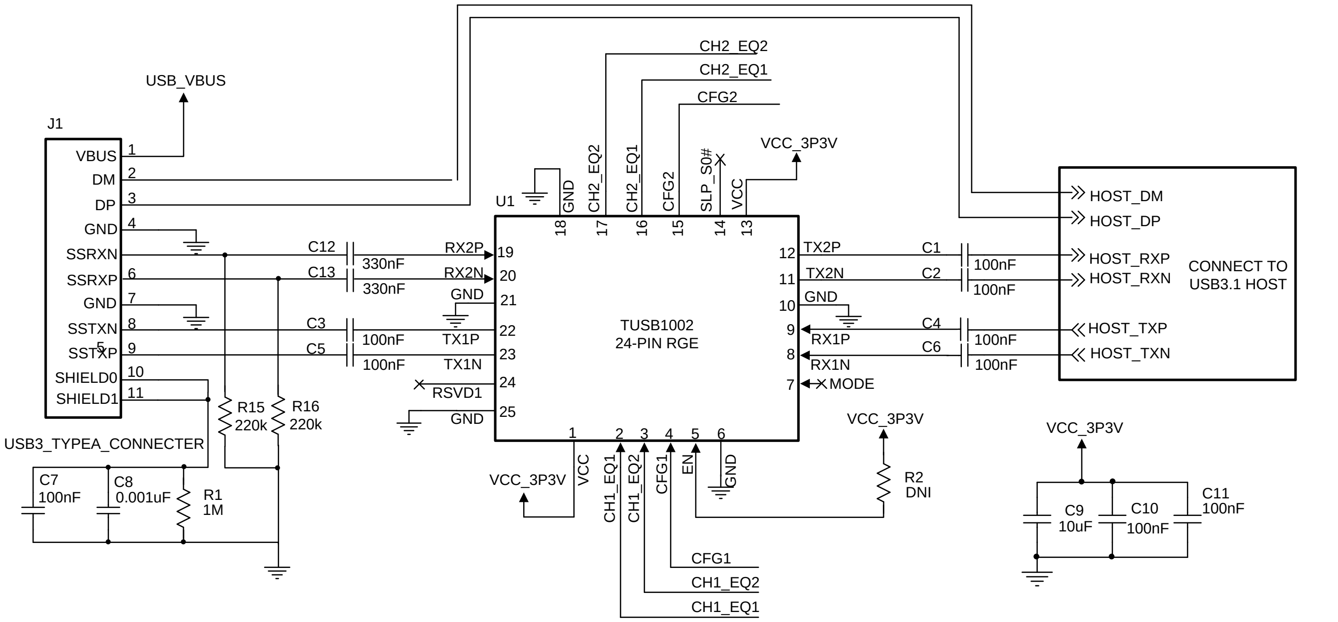


Figure 18. Host Implementation Schematic

The USB3.1 Dual channel operation is used in this example. Mode pin should be left floating (unconnected) when using this mode.

In this example, the USB3.1 Host does not support a GPIO for indicating system Sx state or low power states and therefore the SLP_S0# pin can be left floating.

The TUSB1002 compensates for channel loss in both the upstream (D to C) and downstream direction (A to B). This is done by configuring the CH1_EQ[2:1] and CH2_EQ[2:1] pins to the equalization setting that matches as close possible to the channel insertion loss. In this particular example, CH1_EQ[2:1] is for path A to B which is the channel between USB3.1 host and the TUSB1002, and CH2_EQ[2:1] is for path C to D which is the channel between TUSB1002 and the USB3.1 receptacle.

The TUSB1002 supports 5 levels of DC gain that are selected by the CFG[2:1] pins. Typically, the DC gain should be set to 0 dB but may need to be adjusted to correct any one of the following conditions:

1. Input V_{ID} too high resulting in V_{OD} being greater than USB 3.1 defined swing. For this case, a negative DC gain should be used.
2. Input V_{ID} too low resulting in V_{OD} being less than USB 3.1 defined swing. For this case, a positive DC gain should be used.
3. Low frequency discontinuities in the channel resulting in DC component of the signal clipping the vertical eye mask. For this case, a positive DC gain should be used.

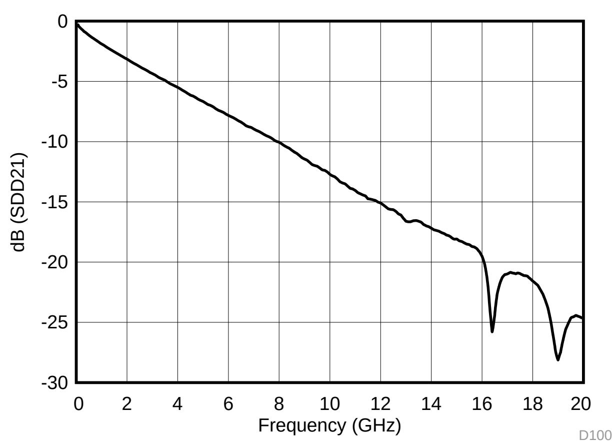
It is assumed in this example the incoming V_{ID} is at the nominal defined USB3.1 range and the channel is linear across frequency. The CFG1 and CFG2 pins can both be left floating if these assumptions are true.

In this particular example, the channel A-B has a trace length of 8 inches with a 4 mil trace width. This particular channel has about 0.83 dB per inch of insertion loss at 5 GHz. This equates to approximately 6.7 dB of loss for the entire 8 inches of trace. An additional 1.5 dB of loss is added due to package of the USB3.1 Host, TUSB1002, and the A/C coupling capacitor. This brings the entire channel loss at 5 GHz to 6.7 dB + 1.5 dB = 8.2 dB. A typical USB 3.1 host/device will have around 3 dB of transmitter de-emphasis. Transmitter de-emphasis pre-compensates for the loss of the output channel. With 3 dB of de-emphasis, the total equalization required by the TUSB1002 is in the 5.2 dB (8.2 dB - 3 dB) range. The channel A-B for this example is connected to TUSB1002's RX1P/N input and therefore CH1_EQ[2:1] pins are used for adjusting TUSB1002 RX1P/N equalization settings. The CH1_EQ[2:1] pins should be set such that TUSB1002 equalization is between 5dB and 8dB.

The channel C-D has a trace length of 4 inches with a 4mil trace width. Assuming 0.83 dB per inch of insertion loss, the 4 inch trace will equate to about 3.32 dB of loss at 5 GHz. An additional 2dB of loss needs to be added due to package, A/C coupling capacitor, and the USB 3.1 receptacle. The total loss is around 5.32 dB. Because channel C-D includes a USB 3.1 receptacle, the actual total loss could be much greater than 5.32dB due to the fact that devices plugged into the receptacle will also have loss. The device plugged into receptacle will have either a short or long channel. USB3.1 standard defines total loss limit of 23dB that is distributed as 8.5 dB for Host, 8.5dB for device, and 6.0dB for cable. With variable channel of devices plugged into the USB3.1 receptacle, configuring TUSB1002's RX2P/N equalization settings is not as straight forward as Channel A-B.

Engineer can not set TUSB1002 CH2_EQ[2:1] pins to the largest equalization setting to accommodate the largest allowed USB3.1 device/cable loss of 14.5 dB. Doing so will result in TUSB1002 operating outside its linear range when a device with short channel is plugged into the receptacle. For this reason, it is recommended to configure TUSB1002 CH2_EQ[2:1] pins to equalize a shorter device channel. This will result in requiring USB3.1 host to compensate for remaining channel loss for the worse case USB3.1 channel of 14.5 dB. The definition of a short device channel is not specified in USB 3.1 specification. Therefore, an engineer must make their own loss estimate of what constitutes a short device channel. For particular example, we will assume the short channel is around 3 to 5 dB. The device's channel loss will need to be added to estimated Channel C-D loss minus the typical 3db of de-emphasis. This means CH2_EQ[2:1] pins should be configured to handle a loss of 5 to 7 db.

8.2.3 Application Curves



Freq = 5 GHz dB(SDD21) = –6.666

Figure 19. Insertion Loss for 8inch 4 mil FR4 Trace

8.3 Typical SATA, PCIe and SATA Express Application

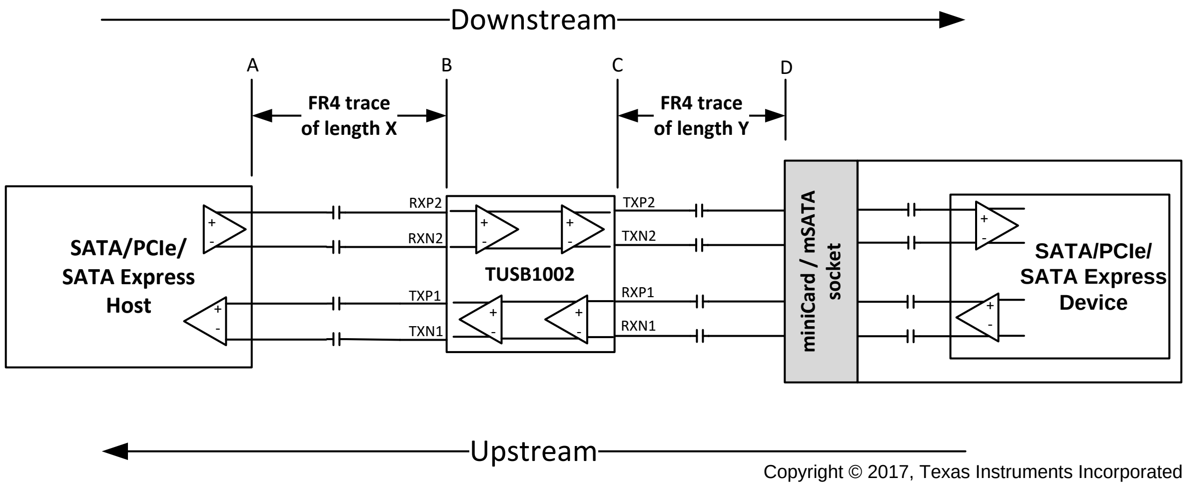


Figure 20. SATA/PCIe/SATA Express Typical Application

8.3.1 Design Requirements

Table 5. Design Parameters

PARAMETER	VALUE
VCC supply (3 V to 3.6 V)	3.3 V
PCIe Support Required (Yes/No)	Yes
SATA Express Support Required (Yes/No)	Yes
SATA Support Required (Yes/No)	Yes, then ferrite beads (FB1 and FB2) and 49.9-ohm required. No, then ferrite bead (FB1 and FB2) and 49.9-ohm not required.
TX1, TX2, RX2 A/C coupling Capacitor (176 nF to 265 nF)	220 nF ±10%
RX1 A/C coupling Capacitor (297 nF to 363 nF)	Optional. But if implemented suggest 330 nF ±10%
A to B FR4 Length (inches)	8
A to B FR4 Trace Width (mils)	4
C to D FR4 length (inches)	2
C to D FR4 Trace Width (mils)	4
USB3.1 Host Sleep GPIO Support	This feature not supported when MODE = "R", CFG1 = "0", and CFG2 = "0".
DC Gain (-2, -1, 0, +1, +2)	Not configurable when MODE = "R", CFG1 = "0", and CFG2 = "0". Will always default to 0 dB
Linear Range (900 mV, 1000 mV, or 1200 mV)	Not configurable when MODE = "R", CFG1 = "0", and CFG2 = "0". Will always default to 1200mV

8.3.2 Detailed Design Procedure

The MODE pin = "R", CFG1 = "0", and CFG2 = "0" will place the TUSB1002 into PCIe mode. In this mode, the TUSB1002 will have its DC gain fixed at 0dB and its linearity range fixed at 1200mV. The TUSB1002 will perform far-end receiver termination detection and enable both upstream and downstream paths when far-end termination is detected on both TX1 and TX2.

The AC coupling capacitor range defined for a SATA device is a lot smaller than the AC-coupling capacitor range defined for SATA Express and PCI Express (PCIe) as indicated by Figure 21. The AC-coupling capacitor range defined for SATA Express and PCI Express is within the same range as the AC-coupling capacitor range defined by USB 3.1. The TUSB1002 will be able to detect PCIe and SATA Express device's receiver termination. But the SATA's 12nF (max) AC-coupling capacitor will prevent TUSB1002 from detecting the SATA device's receiver termination. To correct this problem, a ferrite bead along with 49.9 ohm resistor must be placed between C_{TX2} and miniCard/mSATA socket. These components can be isolated from the high-speed channel when PCIe or

SATA Express is active by using an NFET as shown in Figure 22. The NFET should be enabled whenever a SATA device is present. The ferrite bead chosen must present at least 600 ohms impedance at 100MHz so as to not impact high-speed signalling. It is recommended to use Murata BLM03AG601SN1 or BLM03HD601SN1D or a ferrite bead with similar characteristics from a different vendor. For applications which only require support for PCIe and SATA Express and do not need to support SATA, the ferrite beads and 49.9 ohm resistors are not needed.

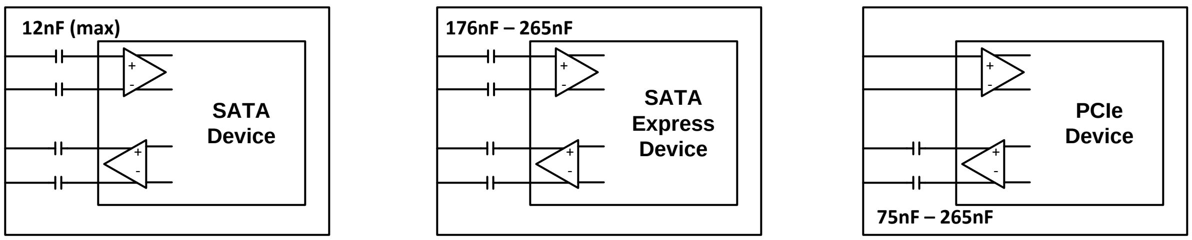


Figure 21. AC-Coupling capacitor Implementation for SATA, SATA Express, and PCIe Devices

The TUSB1002's power will be at $P_{(U0\_SSP\_1200mV)}$ when both its upstream and downstream paths are enabled. In order to save system power in system S3/S4/S5 states, it is suggested to control TUSB1002's EN pin. Anytime the system enters a low power state (S3, S4, or S5), it is suggested to de-assert the EN pin. While EN pin is de-asserted, the TUSB1002 will consume $P_{(SHUTDOWN)}$. Assertion of this pin is necessary anytime the system exits a lower power state.

The TUSB1002 compensates for channel loss in both the upstream (C to D) and downstream direction (A to B). This is done by configuring the CH1_EQ[2:1] and CH2_EQ[2:1] pins to the equalization setting that matches as close possible to the channel insertion loss. In this particular example, CH2_EQ[2:1] is for path A to B which is the channel between PCIe/SATA/SATA Express host and the TUSB1002, and CH1_EQ[2:1] is for path C to D which is the channel between TUSB1002 and the miniCard/mSATA socket.

In this particular example, the channel A-B has a trace length of 8 inches with a 4 mil trace width. This particular channel has about 0.83 dB per inch of insertion loss at 5 GHz. This equates to approximately 6.7 dB of loss for the entire 8 inches of trace as depicted in Figure 19. An additional 1.5 dB of loss is added due to package of the PCIe/SATA/SATA Express Host, TUSB1002, and the A/C coupling capacitor. This brings the entire channel loss at 5 GHz to 6.7 dB + 1.5 dB = 8.2 dB. The channel A-B for this example is connected to TUSB1002 RX2P/N input and therefore CH2_EQ[2:1] pins are used for adjusting TUSB1002 RX2P/N equalization settings. The CH2_EQ[2:1] pins should be set such that TUSB1002 equalization is between 5dB and 8dB. A value closer to 5 dB maybe best if Host has transmitter de-emphasis.

A similar method should be used for the upstream path (C to D). In this particular example, C to D has a trace length of 2 inches with a 4-mil trace width. This equates to approximately 1.5 dB at 5 GHz. The SATA/SATA Express/PCIe device will have its own channel loss. This loss can be added to the C to D channel loss. For this example, we will assume a value of 5dB is acceptable to compensate for C to D channel loss as well as loss associated with the SATA/SATA Express/PCIe device. The CH1_EQ[2:1] pins should be set such that TUSB1002 equalization is 5dB.

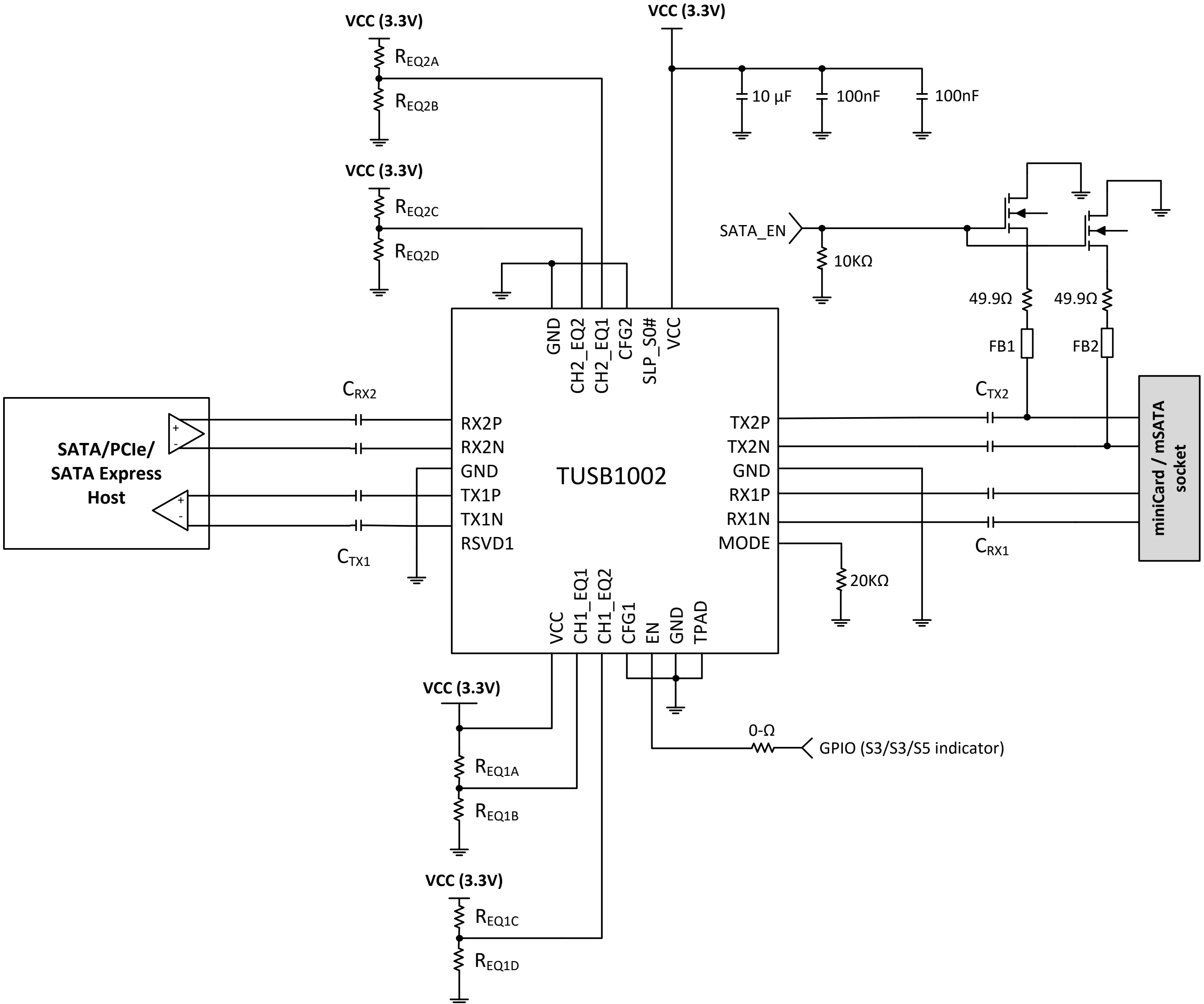


Figure 22. Example SATA/PCIe/SATA Express Schematic

8.3.3 Application Curves

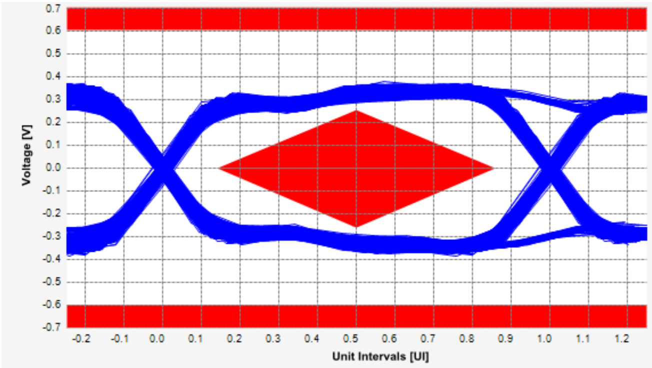


Figure 23. PCIe Gen1 TX Eye Diagram

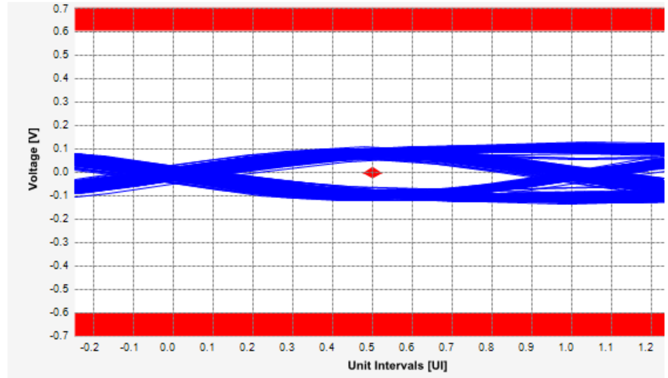


Figure 24. PCIe Gen 3 TX Eye Diagram

9 Power Supply Recommendations

The TUSB1002 has two V_{CC} supply pins. It is recommended to place a 100 nF de-coupling capacitor near each of the V_{CC} pins. It is also recommended to have at least one bulk capacitor of at least 10 µF on the V_{CC} plane near the TUSB1002.

10 Layout

10.1 Layout Guidelines

- RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
- Keep away from other high speed signals.
- Intra-pair routing should be kept to within 2 mils.
- Length matching should be near the location of mismatch
- Each pair should be separated at least by 3 times the signal trace width.
- The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This minimizes any length mismatch causes by the bends; ad therefore, minimize the impact bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of VIAS should be kept to a minimum. It is recommended to keep the VIAS count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points causes impedance discontinuity; and therefore, negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

10.2 Layout Example

Example 4 layer PCB Stackup

Top Layer 1 (Signal)
Inner Layer 2 (GND)
Inner Layer 3 (VCC)
Bottom Layer 4 (Signal)

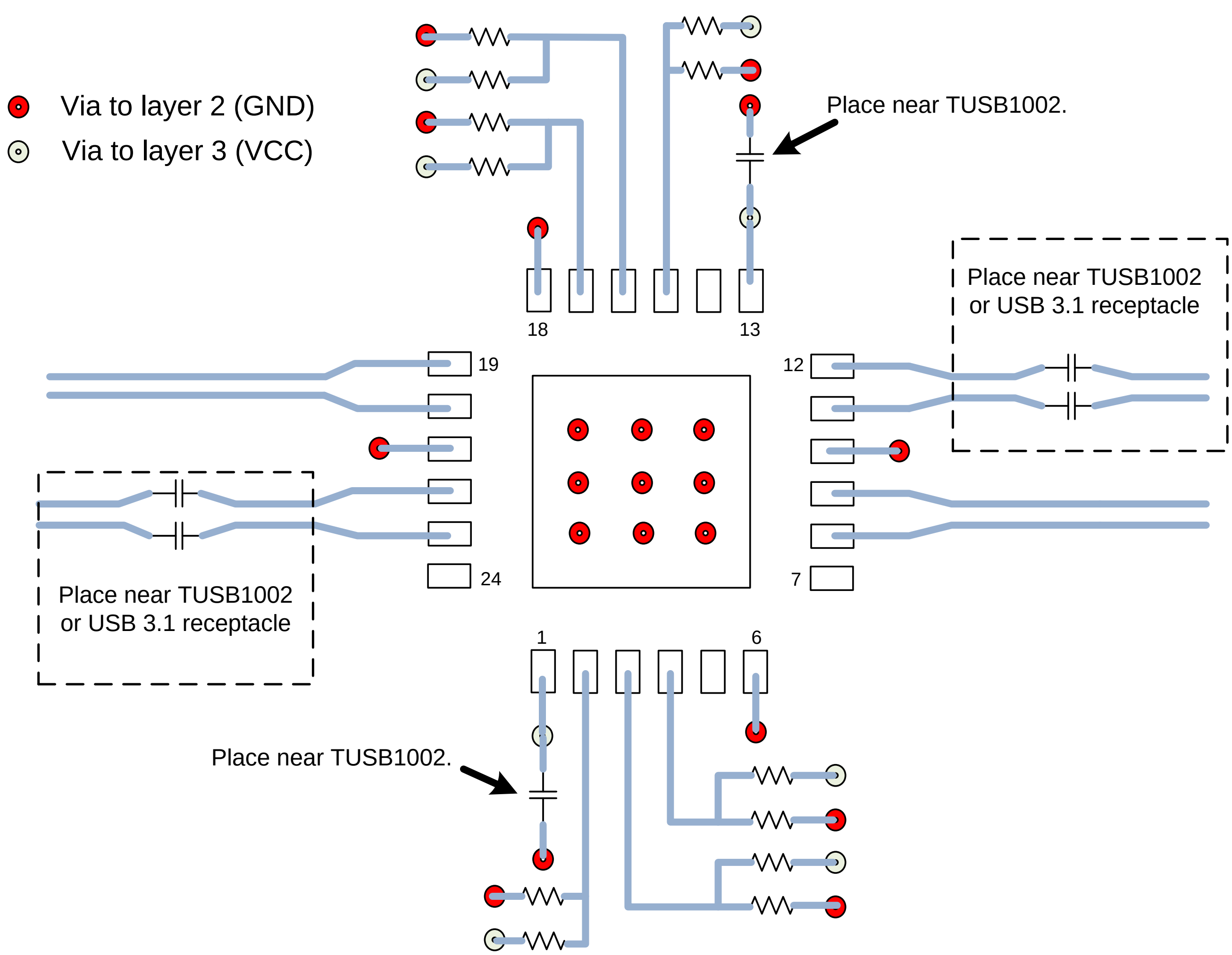


Figure 25. Example Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB1002RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TUSB 1002	Samples
TUSB1002RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TUSB 1002	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

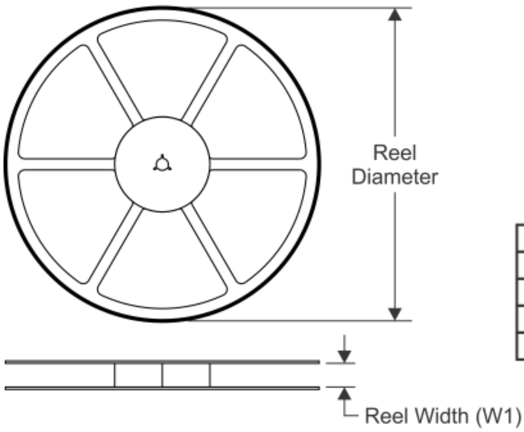
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

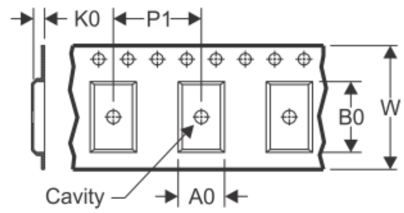
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

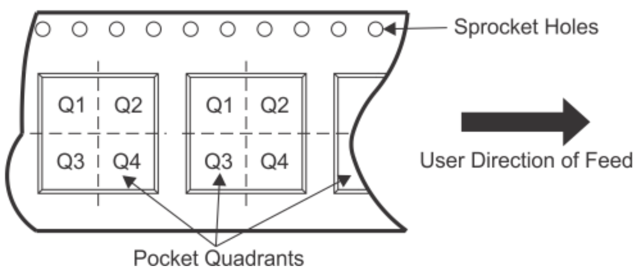
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





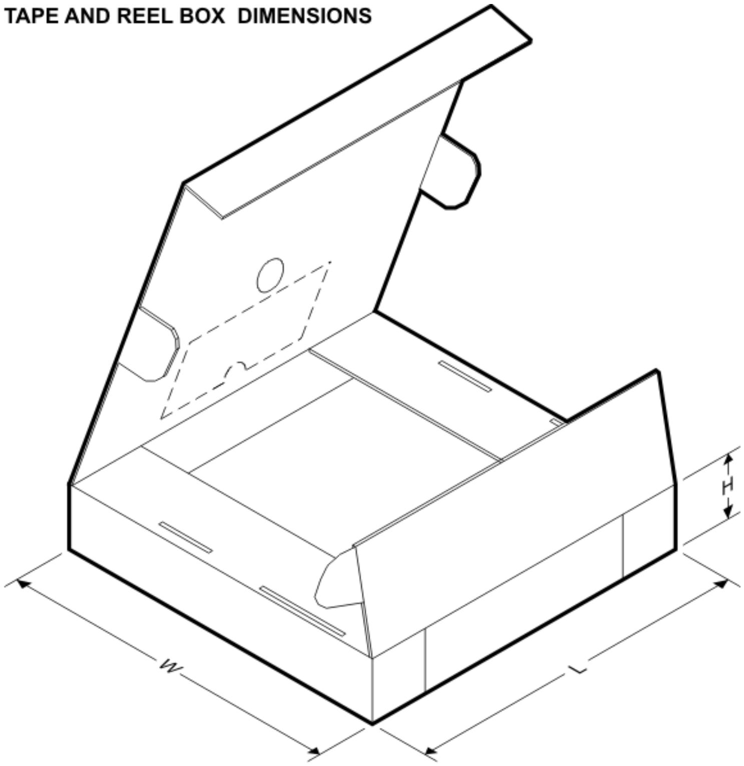
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

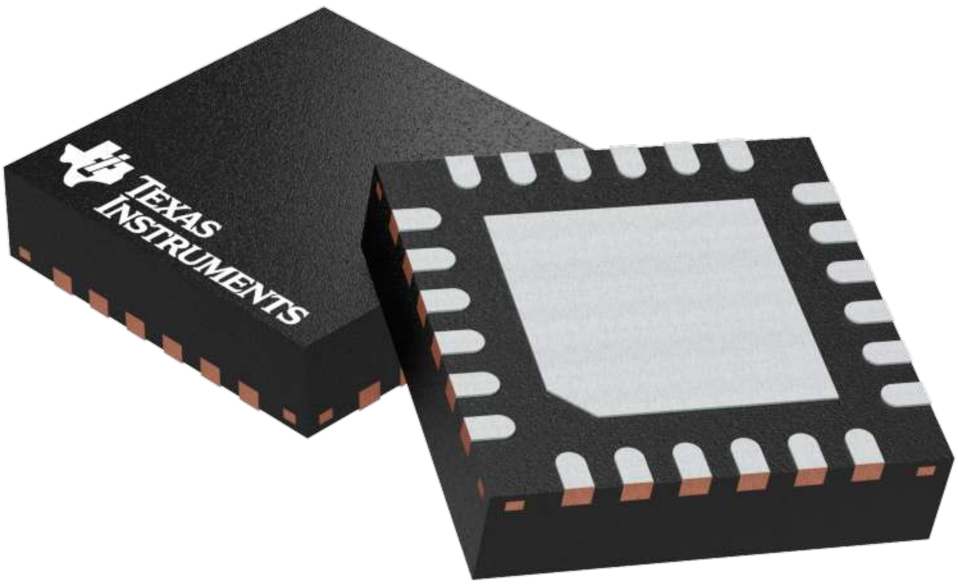
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB1002RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSB1002RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

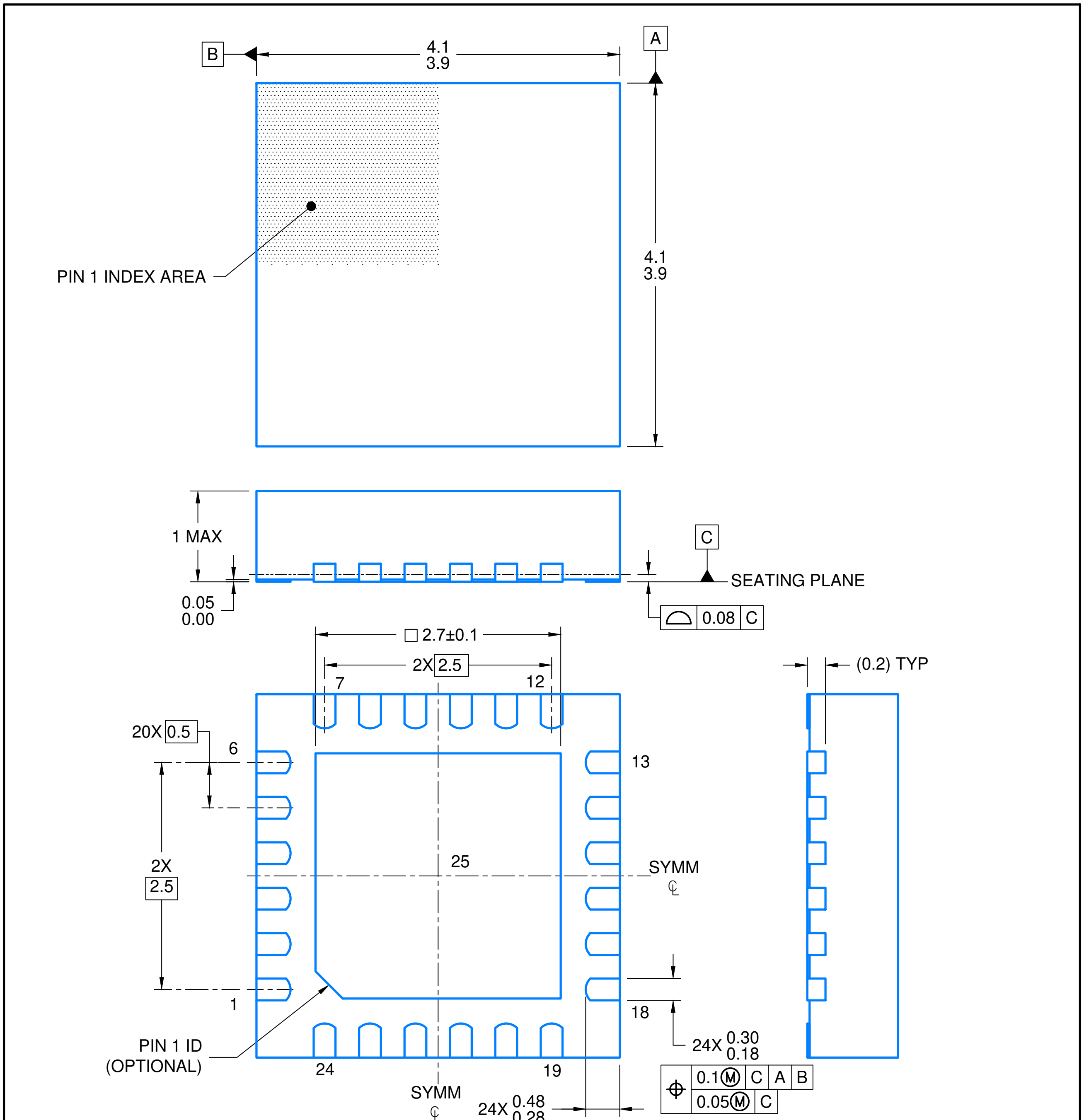


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB1002RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TUSB1002RGET	VQFN	RGE	24	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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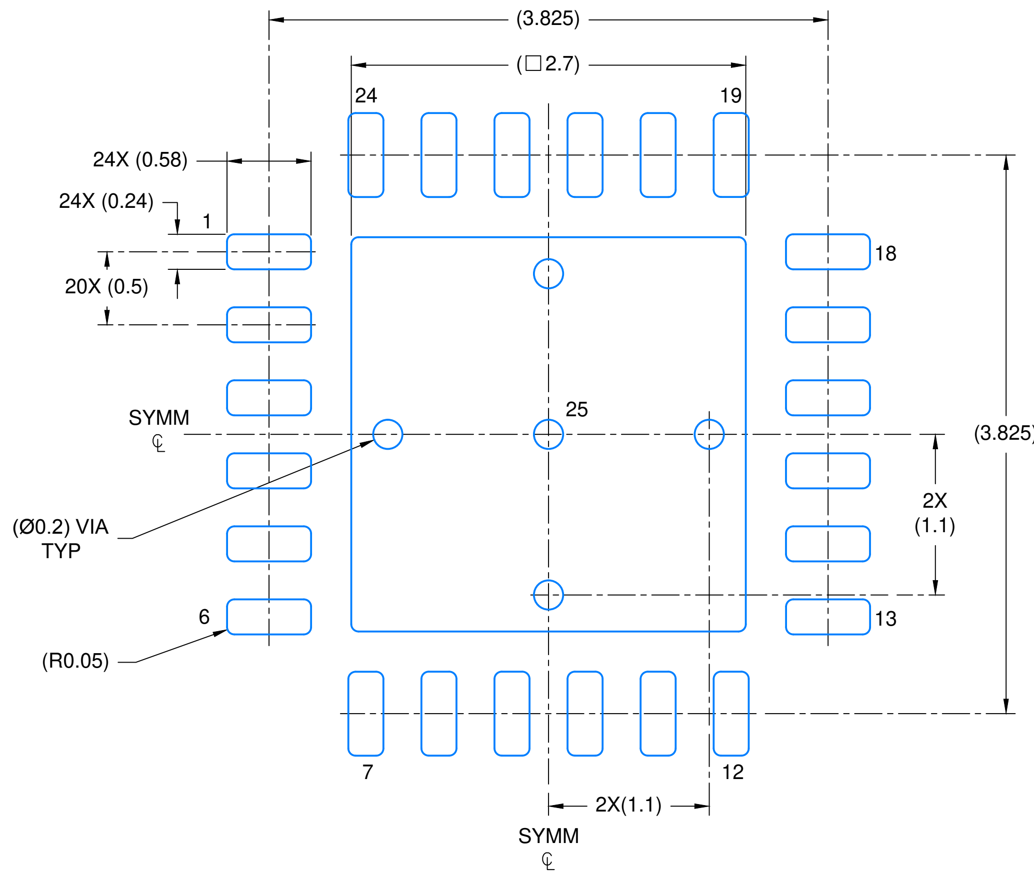
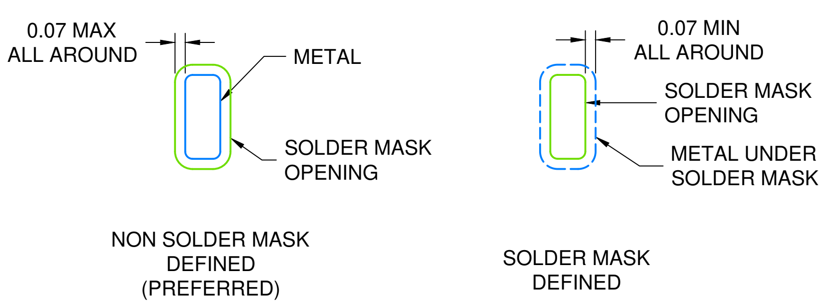
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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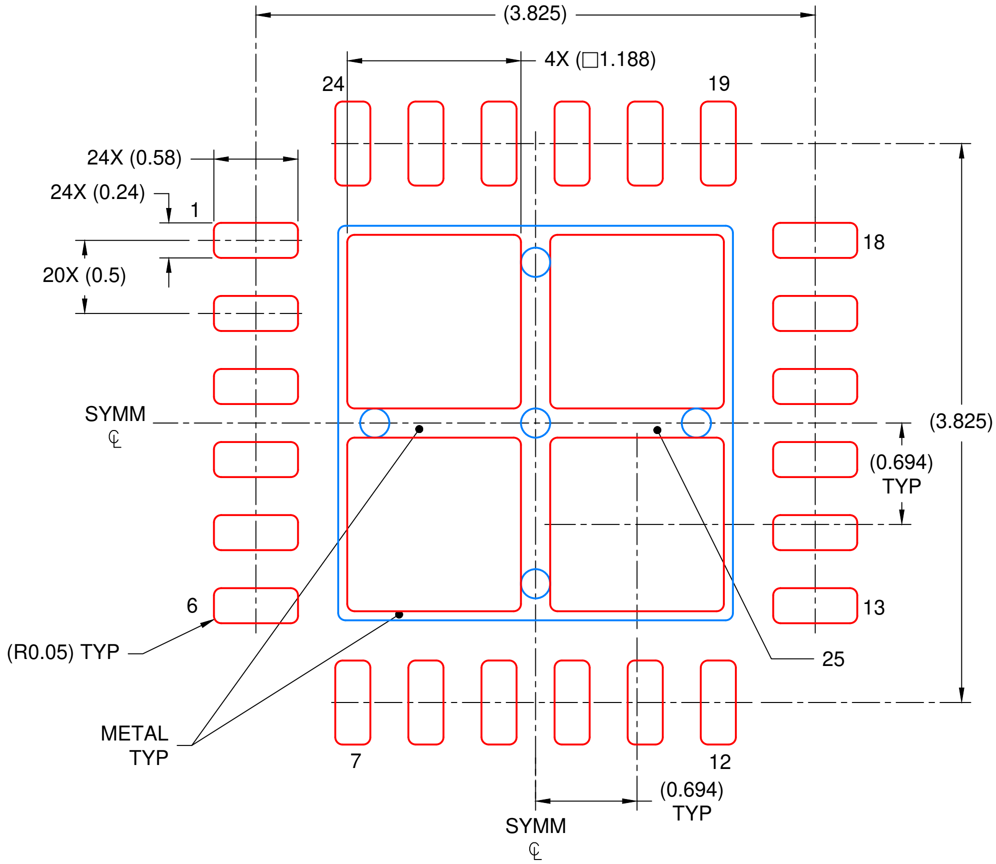
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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