2ch Half-Bridge Gate Driver

BD16950EFV-C

General Description

The BD16950EFV is an AEC-Q100 automotive qualified 2-channel Half-Bridge Gate Driver, controlled by an external MCU through a 16-bit Serial Peripheral Interface (SPI). Independent control of low-side and high-side N-MOSFETS allows for several MCU controlled modes. A programmable drive current is available to adjust slew-rates, in order to meet EMI and power dissipation requirements. Diagnostics can be read and reset by an external MCU.

Features

- AEC-Q100 Qualified(Note1)
- 2ch Half-Bridge Gate Drivers
- 4 external MOSFETs are Controlled Independently
- Half-Bridge Control Modes are Selected by SPI
- Slew Rates are Controlled with Constant Source /Sink Current.
- 500 kHz Oscillation for Charge Pump.
- 16bit SPI

(Note1) Grade1

Applications

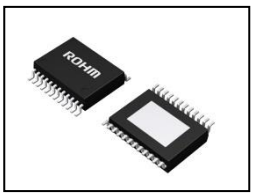
- 4WD Torque Distribution System, Power Window Lifter, Sun Roof Module, Wiper, Seat Belt Tensioner, Seat Positioning etc.

Key Specifications

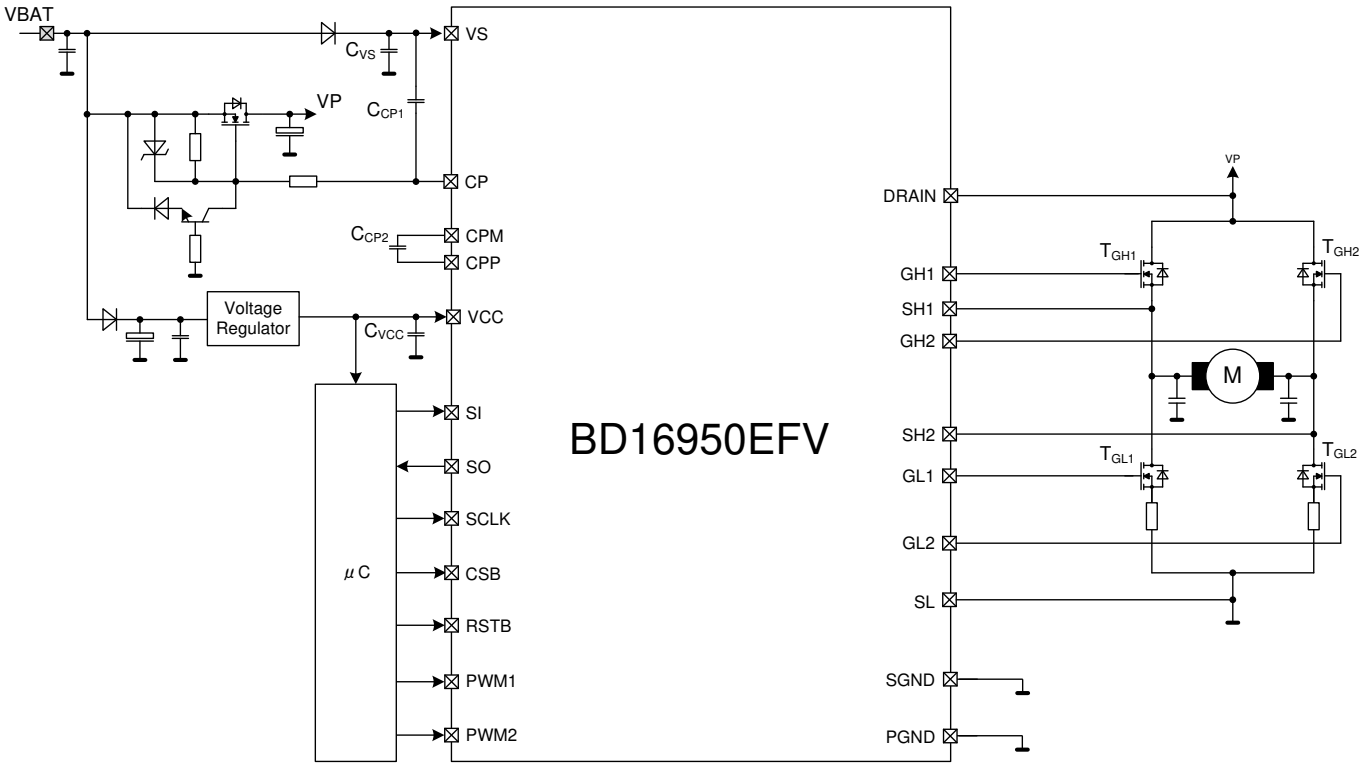
■ Input Voltage VS:	5.5V to 40V
■ Input Voltage VCC:	3.0V to 5.5V
■ Gate Drive Voltage for Half-Bridge:	11V(Typ)
■ VS Quiescent Supply Current:	0μA(Typ)
■ VCC Quiescent Supply Current:	2μA(Typ)
■ Gate Driver Current	1mA to 31mA with 1mA step
■ Cross Current Protection Time	0.25μs to 92μs
■ SPI clock	7MHz (Max)

Package

	W (Typ)	x D (Typ)	x H (Max)
HTSSOP-B24	7.8mm	× 7.6mm	× 1.00mm



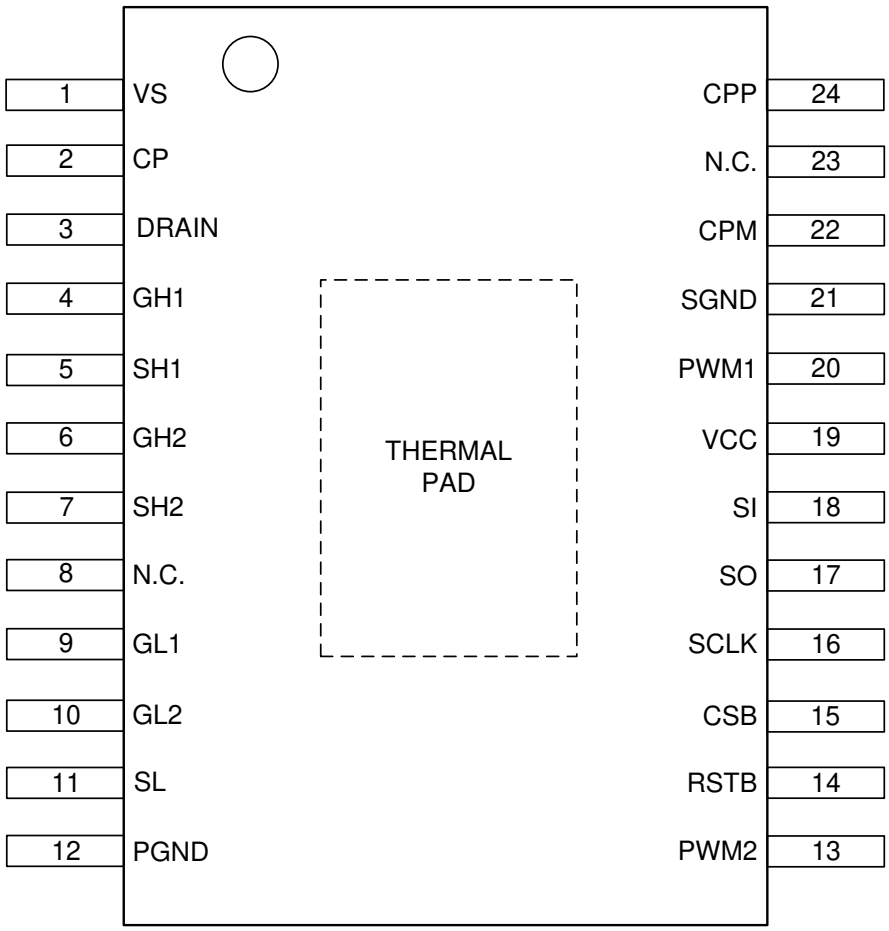
Typical Application Circuit



◯Product structure: Silicon monolithic integrated circuit ◯This product has no designed protection against radioactive rays.

Pin Configuration

(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	VS	Power supply terminal used for charge pump and low side driver. A capacitor (C_{VS} =1.0µF (Typ)) is recommended to be located as close as possible to this pin and PGND.
2	CP	Charge pump output. Connect C_{CP1}=0.1µF to VS.
3	DRAIN	High side monitor input from external MOSFET drain for over current and under voltage protection.
4	GH1	Gate driver output to external MOSFET high-side switch in half-bridge. Connect to Gate terminal of high-side external MOSFET.
5	SH1	Source/Drain of half-bridge. Connect to Source / Drain terminal of external MOSFET high/low-side.
6	GH2	Gate driver output to external MOSFET high-side switch in half-bridge. Connect to Gate terminal of high-side external MOSFET.
7	SH2	Source/Drain of half-bridge. Connect to Source / Drain terminal of external MOSFET high/low-side.
8	N.C.	Pin not connected internally.(Note1)
9	GL1	Gate driver output to external MOSFET low-side switch in half-bridge. Connect to Gate terminal of low-side external MOSFET.
10	GL2	Gate driver output to external MOSFET low-side switch in half-bridge. Connect to Gate terminal of low-side external MOSFET.
11	SL	Low-side monitor at external MOSFET Source for over current protection
12	PGND	Power Ground Connector. Connected to Charge pump, High side driver and Low side driver.
13	PWM2	PWM2 input for Half-bridge (GH2 and GL2) control. This input has a pull-down resister.
14	RSTB	Reset input. The Reset input has a pull-down resistor. RSTB=Low will put the BD16950EFV into Reset condition from any state.
15	CSB	Chip Select Bar: this input is low active and requires CMOS logic levels. The serial data transfer between BD16950EFV and MCU is enabled by pulling the input CSB to low-level. This input has a pull-up resister.
16	SCLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels. This input has a pull-down resister.
17	SO	Serial data out: SPI data sent to the MCU by the BD16950EFV. When CSB is High, the pin is in the high-impedance state.
18	SI	Serial data in: the input requires CMOS logic levels and receives serial data from the MCU. The communication is organized in 16bit control words and the most significant bit (MSB) is transferred first. This input has a pull-down resister.
19	VCC	Analog blocks and logic voltage supply 3.3V or 5V : for this input a C_{VCC} =0.1µF (Typ) capacitor as close as possible to SGND is recommended.
20	PWM1	PWM1 input for Half-bridge (GH1 and GL1) control. This input has a pull-down resister.
21	SGND	Ground terminal Connect to THERMAL PAD for heat dissipation. Connected to Logic and analog circuit.
22	CPM	Charge pump pin for capacitor, negative side. Connect C_{CP2} =0.1µF (Typ) to CPP terminal.
23	N.C.	Pin not connected internally.(Note1)
24	CPP	Charge pump pin for capacitor, positive side. Connect C_{CP2} =0.1µF (Typ) to CPM terminal.
THERMAL PAD		THERMAL PAD for heat dissipation. Connect to SGND terminal.

(Note1) Please be sure to floating at N.C. pin.

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may damage the IC. Avoid nearby pins being shorted to each other especially to ground, power supply or output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) or unintentional solder bridge deposited in between pins during assembly.

Selection of Components Externally Connected

Input Capacitor C_{VS}

The input capacitor (C_{VS}) lowers the power supply impedance and averages the input current. The C_{VS} value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. Although the capacitance requirement varies according to the impedance of the power supply that is used as well as the load current value, it is generally in the range of 1.0µF.

Input Capacitor C_{VCC}

The input capacitor (C_{VCC}) lowers the power supply impedance and averages the input current. The C_{VCC} value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. A capacitor value of 0.1µF is recommended.

Charge Pump Capacitor C_{CP1}

The Charge pump capacitor C_{CP1} is required for smoothing the ripple voltage. A capacitor value of 0.1µF is recommended. Using a capacitor with a capacitance lower than 0.1µF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1µF results in a larger rush current during start-up, but ripple voltage becomes lower.

Charge Pump Capacitor C_{CP2}

The charge pump capacitor C_{CP2} is required for charging up the voltage. A capacitor value of 0.1µF is recommended. Using a capacitor with a capacitance lower than 0.1µF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1µF results in a larger rush current during start-up, but ripple voltage becomes lower.

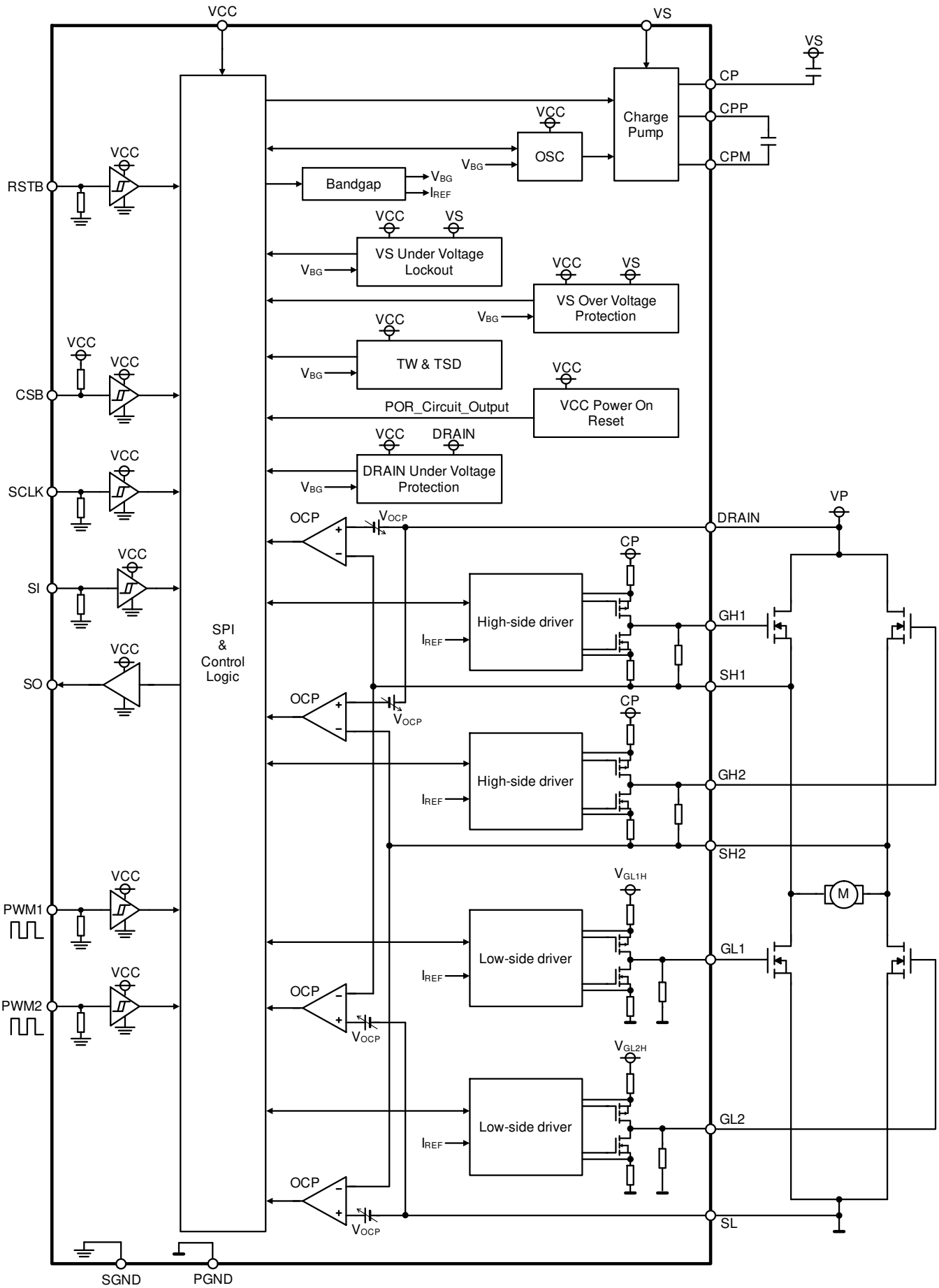
External N-ch MOSFET

BD16950EFV is the gate driver for high side and low side N-channel MOSFETs. Select MOSFETs with the required current capacity to drive the motor and a Gate-Source breakdown voltage ≥ 12V.

External Parts

Symbol	Part
C_{VS}	1.0µF, -/+10%
C_{VCC}	0.1µF, -/+10%
C_{CP1}	0.1µF, -/+10%
C_{CP2}	0.1µF, -/+10%
T_{GH1}, T_{GH2}, T_{GL1}, T_{GL2}	N-Channel MOSFET

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
VS Voltage	VS	-0.3 to 40	V
VCC Voltage	VCC	-0.3 to 7.0	V
Digital I/O Voltage (SI, SO, SCLK, CSB, RSTB, PWM1, PWM2)	V_{IO}	-0.3 to 7.0	V
CP Voltage	V_{CP}	VS to VS+20	V
CPM Voltage	V_{CPM}	-0.3 to +12V+0.3V (V_{CPM} < VS)	V
CPP Voltage	V_{CPP}	VS to VS+20	V
Gate Voltage for High Side (GH1,GH2)	V_{GH1}, V_{GH2}	-0.3 to 60 (CP-VS < 12V)	V
Gate Voltage for Low Side (GL1,GL2)	V_{GL1}, V_{GL2}	-0.3 to +12V+0.3V (V_{GL1}, V_{GL2} < VS)	V
Bridge output (SH1,SH2)	V_{SH1}, V_{SH2}	-4 to 40	V
Drain Voltage for High Side	V_{DRAIN}	-0.3 to 40	V
Source Voltage for Low Side	V_{SL}	-0.3 to 7.0	V
Operating Temperature Range (Ambient temperature range)	T_{amb}	-40 to 125	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C
Maximum Junction Temperature	T_{jmax}	150	°C
Human Body Model (HBM Global Pin) (Note1)	$V_{ESD,HBM}$	±4	kV
Human Body Model (HBM Local Pin) (Note2)	$V_{ESD,HBM}$	±2	kV
Charged Device Model (CDM Corner Pin) (Note3)	$V_{ESD,CDM}$	±750	V
Charged Device Model (CDM Other Pin) (Note 4)	$V_{ESD,CDM}$	±500	V

(Note 1)Global pins are VS, SH1 and SH2 (A 'global' pin carries signal or power, which enters or leaves the application board).
These voltages are guaranteed by design.
(Note 2)Local pins are except VS, SH1 and SH2 (A 'local' pin carries a signal or power, which does not leave the application board).
These voltages are guaranteed by design.
(Note 3)Corner pins are VS, PGND, PWM2 and CPP. These voltages are guaranteed by design.
(Note 4)Other pins are except VS, PGND, PWM2 and CPP. These voltages are guaranteed by design.

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	143.8	26.4	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	7	2	°C/W

(Note 1)Based on JESD51-2A(Still-Air)
(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via(NOTE 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5)This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage1	VS	5.5	13.5	40	V
Supply Voltage2	VCC	3.0	5	5.5	V
Digital Input Voltage	SI, SCLK, CSB, RSTB, PWM1, PWM2	-0.3	-	VCC	V
Junction Temperature Range	Tj	-40	-	150	°C

Electrical Characteristics

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Consumption Current						
VS Quiescent Supply Current1 (Reset / Sleep State) (Note 1)	I_{VS_qui1}	-	0	10	μA	0V ≤ VS ≤ V_{s_OVP1} -40 °C ≤ Tj ≤ +105 °C
VS Quiescent Supply Current2 (Reset / Sleep State) (Note 1)	I_{VS_qui2}	-	0	50	μA	0V ≤ VS ≤ V_{s_OVP1} -40 °C ≤ Tj ≤ +150 °C
VS Active Current (Normal State) (Note 1)	I_{VS_act}	-	3.2	6.4	mA	SH1=SH2=PGND CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
VCC Quiescent Supply Current1 (Reset / Sleep State) (Note 1)	$I_{VCC\ qui1}$	-	2	10	μA	V_{CC_POR1} ≤ VCC ≤ 5.5V -40 °C ≤ Tj ≤ +105 °C
VCC Quiescent Supply Current2 (Reset / Sleep state) (Note 1)	$I_{VCC\ qui2}$	-	2	100	μA	V_{CC_POR1} ≤ VCC ≤ 5.5V -40 °C ≤ Tj ≤ +150 °C
VCC Active Current (Normal state) (Note 1)	I_{VCC_act}	-	1.2	2.4	mA	SH1=SH2=PGND CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Input / Output Terminal						
Input High Voltage(PWM1, PWM2, SI, SCLK, CSB, RSTB)	V_{IH}	VCC x 0.7	-	-	V	
Input Low Voltage(PWM1, PWM2, SI, SCLK, CSB, RSTB)	V_{IL}	-	-	VCC x 0.3	V	
Hysteresis Width	V_{HYS}	-	VCC x 0.1	-	V	
Pull-Down Resistance (PWM1, PWM2, SI, SCLK, RSTB)	R_{In1}	40	100	160	kΩ	
Input Current (PWM1, PWM2, SI, SCLK, RSTB)	I_{IL}	-1	0	-	μA	PWM1, PWM2, SI, SCLK, RSTB=0V
Pull-Up Resistance at CSB	R_{In2}	40	100	160	kΩ	
Input Current at CSB	I_{IH}	-1	0	-	μA	CSB=VCC
Output Voltage High at SO	V_{OH}	VCC x 0.8	-	VCC	V	ISO=-1mA (into the pin)
Output Voltage Low at SO	V_{OL}	-	-	VCC x 0.2	V	ISO=1mA
PWM Frequency Range	f_{PWM}	-	-	25	kHz	
SH1,SH2 Output Current (Reset/Sleep state) (Note 1)	$I_{SH1,2\_LEAK}$	-10	0	-	μA	GH1-SH1,GH2-SH2=0V
SH1, SH2 Outflow Current1 (Normal state) (Note 1)	$I_{SH1,2\_out1}$	-280	-155	-70	μA	GH1=GH2=SH1=SH2=0 EN=CPEN=DRVEN=1 CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
SH1, SH2 Outflow Current2 (Normal state) (Note 1)	$I_{SH1,2\_out2}$	-280	-155	-70	μA	GH1=GH2=SH1=SH2=VS EN=CPEN=DRVEN=1 CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
GH1,GH2 Pull-Down Resistance (Gate-Source Pull-Down Current) (Reset/Sleep State) (Note 1)	$R_{GH1,2\_pulldown}$	6	15	24	kΩ	
SL Output Current (Reset/Sleep State) (Note 1)	$I_{SL1,2\_LEAK}$	-10	0	-	μA	GL1-SL,GL2-SL=0V
GL1,GL2 Pull Down Resistance (Gate-Source Pull-Down Current) (Reset/Sleep State) (Note 1)	$R_{GL1,2\_pulldown}$	6	15	24	kΩ	

(Note 1) Functional statement control is shown on the figure 13.

Electrical Characteristics(continued)

(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Charge Pump						
Output Voltage1 (Normal State) (Note 1)	V_{CP1}	V_S+10	V_S+11	V_S+12	V	VS = 13.5V, I_{CP}=0mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Output Voltage2 (Normal State) (Note 1)	V_{CP2}	V_S+5.0	-	V_S+6.0	V	VS = 6V, I_{CP}=0mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Voltage Drop of Charge Pump1 (Normal State) (Note 1)	V_{CP_Drop1}	-	-	1.0	V	VS = 13.5V, I_{CP}= -10mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Voltage Drop of Charge Pump2 (Normal State) (Note 1)	V_{CP_Drop2}	-	-	0.5	V	VS = 6V, I_{CP}= -2mA CUR_SOURCE[4:0]=00000 CUR_SINK[4:0]=00000
Charge Pump Operating Frequency (Normal State) (Note 1)	f_{CP}	400	500	667	kHz	Charge Pump operating frequency is divided by Clock frequency
Clock Frequency (Internal Oscillator)	f_{CLK}	3.20	4.00	5.34	MHz	
CP Input Current (Reset/Sleep State) (Note 1)	I_{CP_LEAK}	-	0	10	µA	EN=0, V_{CP}=25.5V, VS=13.5V

(Note 1) Functional statement control is shown on the figure 13.

Electrical Characteristics(continued)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Drivers for External MOSFETs						
Accuracy of Gate Driver Current	ACC_{ISR}	-25	-	+25	%	CUR_SOURCE[4:0]= 00001 to 11111 (Note 1) CUR_SINK[4:0]= 00001 to 11111 (Note 1) 1mA to 31mA setting with 1mA step
Pull Down Current (Note 2) (Reset/Sleep State) (Note 3)	$I_{pulldown}$	83	133	334	µA	GH1=SH1+2V, GH1=SH2+2V GL1=2V, GL2=2V
DNL of Gate Driver Current	ACC_{DNLISR}	-	-	1	LSB	
GH1/GH2 Output High Voltage for High Side(Normal State) (Note 3)	V_{GHxH}	V_S+10	V_S+11	V_S+12	V	VS = 13.5V, Icp=0mA
GL1/GL2 Output High Voltage for Low Side(Normal State) (Note 3)	V_{GLxH}	10	11	12	V	VS = 13.5V
Cross Current Protection Time	t_{CCPT}	-25	-	25	%	CCPT[5:0]=00000 to 111111 0.25µs to 92µs setting
DNL of Cross Current Protection Time	$t_{DNLCCPT}$	-	-	1	LSB	
Synchronization Delay Time (Note 4)	t_{syn}	0.56	-	1.25	µs	
Propagation Delay Time (Note 5)	t_{propa}	100	250	400	ns	SH1=SH2=VS CUR_SOURCE[4:0]=11111 CUR_SINK[4:0]=11111
Output on Resistance	$R_{ds\_on\_gate}$	-	10	20	Ω	Output on resistance CUR_SOURCE[4:0]=11111

(Note 1) High side source current : GH1=SH1, GH2=SH2, Low side source current : GL1=PGND, GL2=PGND
High side sink current : Isink(GH1=GH2=11V, SH1=SH2=PGND) - 15 kΩ pull down current(CPEN=0)
Low side sink current : Isink(GL1=GL2=11V) - 15 kΩ pull down current(CPEN=0)

(Note 2) (External MOSFET's gate driver current) = (Accuracy of gate driver current) – (Pull down current)
e.g. condition : CUR_SOURCE[4:0]=01010(10mA setting),GH1=SH1+2V,
(External MOSFET's gate driver current of GH1) = 10mA(Typ) – 133uA(Typ) = 9.867mA.
Maximum inflow current of pull down resistance is 2mA(12V/6kΩ).GH1/GH2/GL1/GL2 outputs do not rise high voltage in 1mA or 2mA setting.

(Note 3) Functional statement control is shown on the figure 13.

(Note 4) Synchronization delay time : Asynchronous internal delay between PWM signal and high-side or low side of logic signal.
This delay time is guaranteed by design.

(Note 5) Propagation delay time : internal delay between high-side or low side of logic signal and GHx or GLx outputs.
This delay time is guaranteed by design.

Electrical Characteristics(continued)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Protection						
UVLO Voltage Rising	V_{S_UVLO1}	4.5	5.0	5.5	V	VS UVLO
Under Voltage Hysteresis	$V_{S\_UV\_hys}$	300	500	700	mV	
OVP Voltage Rising	V_{S_OVP1}	20	22	24	V	VS OVP
Over Voltage Hysteresis	$V_{S\_OVP\_hys}$	0.6	1	1.4	V	
Power On Reset Rising	V_{CC_POR1}	0.75	2.00	2.95	V	VCC POR
Power On Reset Hysteresis	$V_{CC\_POR\_hys}$	0.03	0.1	0.25	V	
Thermal Warning Trigger(Note 1)	T_{TW_TR}	125	137.5	150	ºC	
Thermal Warning Release(Note 1)	T_{TW_RL}	105	117.5	130	ºC	
Thermal Warning Hysteresis(Note1)	T_{TWHYS}	15	20	25	ºC	
Thermal Shut Down Trigger(Note 1)	T_{TSD_TR}	150	175	200	ºC	
Thermal Shut Down Release(Note 1)	T_{TSD_RL}	135	160	185	ºC	
Thermal Shut Down Hysteresis(Note 1)	T_{TSDHYS}	-	15	-	ºC	
DRAIN Quiescent Current (Reset/Sleep State) (Note 1)	I_{DRAIN_qui}	-	-	1	µA	
DRAIN Active Current (Normal State)	I_{DRAIN_act}	-	120	180	µA	
DRAIN Under Voltage Protection Falling	V_{UVP}	4.4	4.9	5.4	V	
OCP Detect Voltage (Drain-SH and SH –SL)	V_{OCP}	-15	-	+15	%	OCPHD[2:0]=000 to 111 OCPLD[2:0]=000 to 111 0.2V, 0.3V, 0.4V, 0.5V, 0.75V, 1.0V, 1.25V and 1.5V setting
OCP Detect FILTER Time	t_{ocp_filter}	-25	-	+25	%	OCP_FILTER[5:0]=000000 to 111111 1µs and 63µs setting with 1µs step
POR Detect Blanking Time	$t_{por\_blanking}$	0.8	2	3.8	µs	
UVLO Detect Blanking Time	$t_{uvlo\_blanking}$	48	64	80	µs	
OVP Detect Blanking Time	$t_{ovp\_blanking}$	48	64	80	µs	

(Note 1) This temperature is guaranteed by design.

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

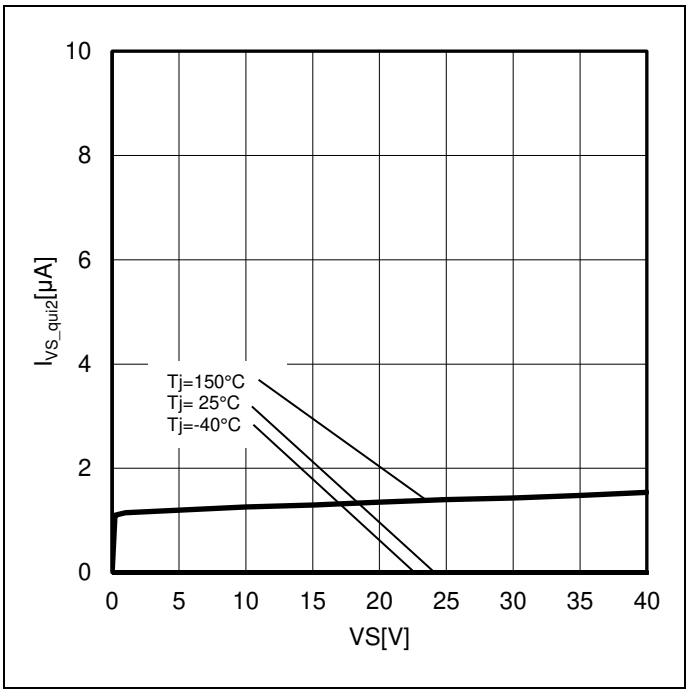


Figure 1. I_{VS_qui2} vs VS (Reset State)
(RSTB=0V)

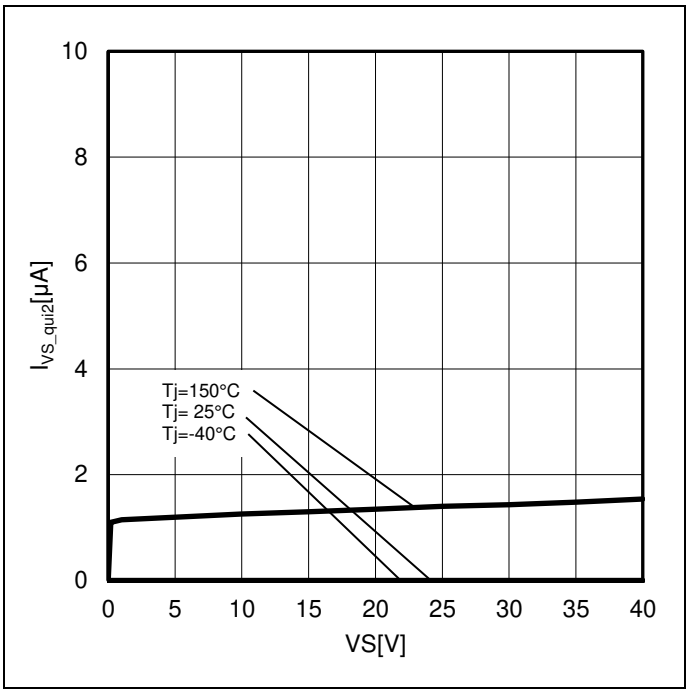


Figure 2. I_{VS_qui2} vs VS (Sleep State)
(RSTB=5V, Enable Register[2:0]=000)

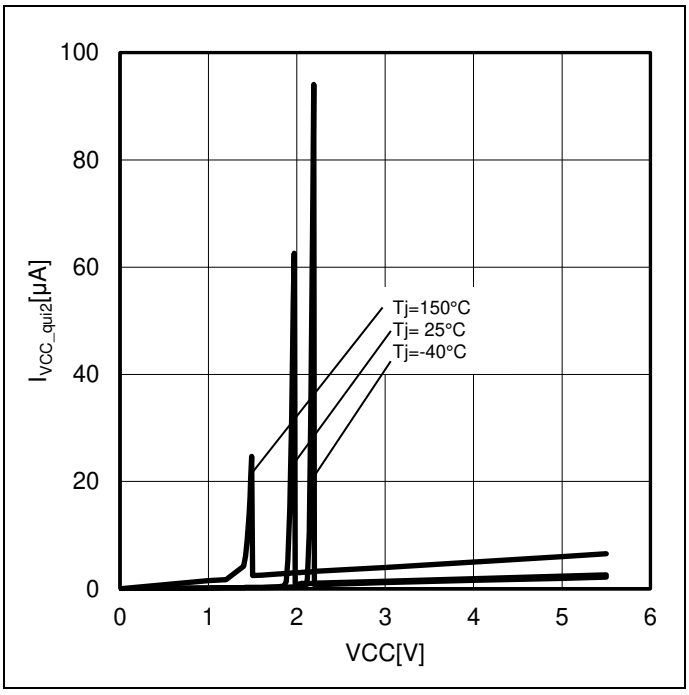


Figure 3. I_{VCC_qui2} vs VCC (Reset State)
(RSTB=0V)

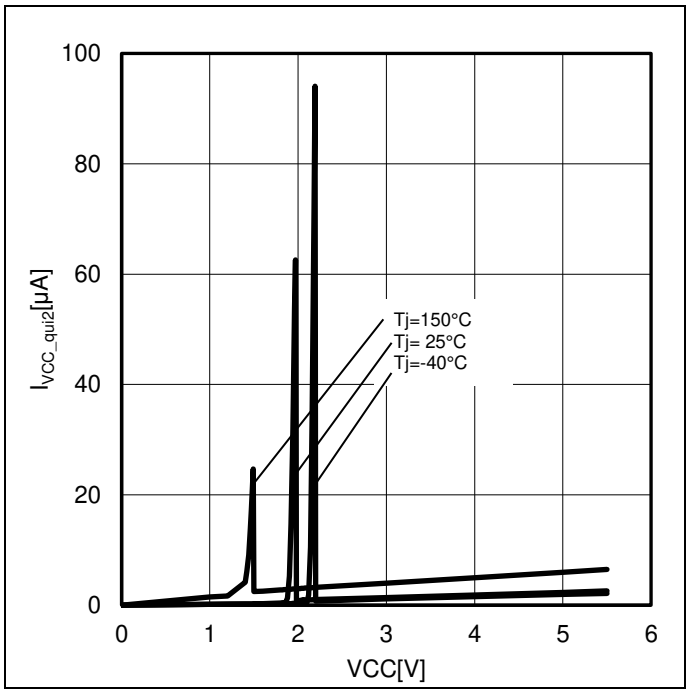


Figure 4. I_{VCC_qui2} vs VCC (Sleep State)
(RSTB=VCC, Enable Register[2:0]=000)

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

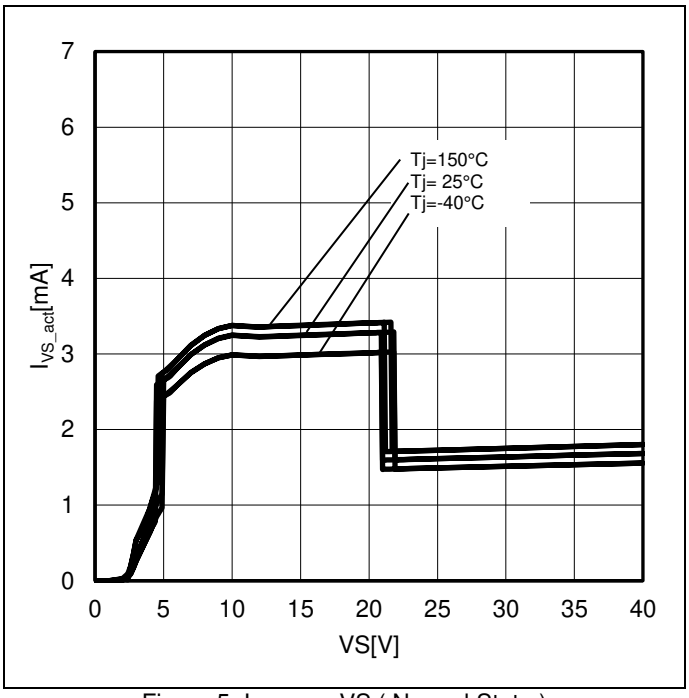


Figure 5. I_{VS_act} vs VS (Normal State)
(RSTB=VCC, SH1=SH2=PGND, Enable Register[2:0]=111,
CUR_SOURCE[4:0]=00000, CUR_SINK[4:0]=00000,
Protection Mode Setting[7:0]=00000000
Other address data is default value)

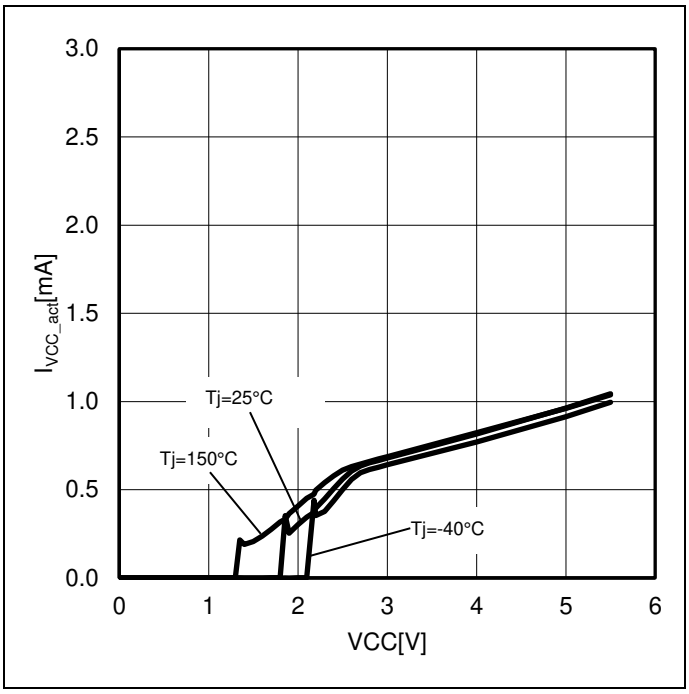


Figure 6. I_{VCC_act} vs VCC (Normal State)
(RSTB=VCC, SH1=SH2=PGND, Enable Register[2:0]=111,
CUR_SOURCE[4:0]=00000, CUR_SINK[4:0]=00000,
Other address data is default value)

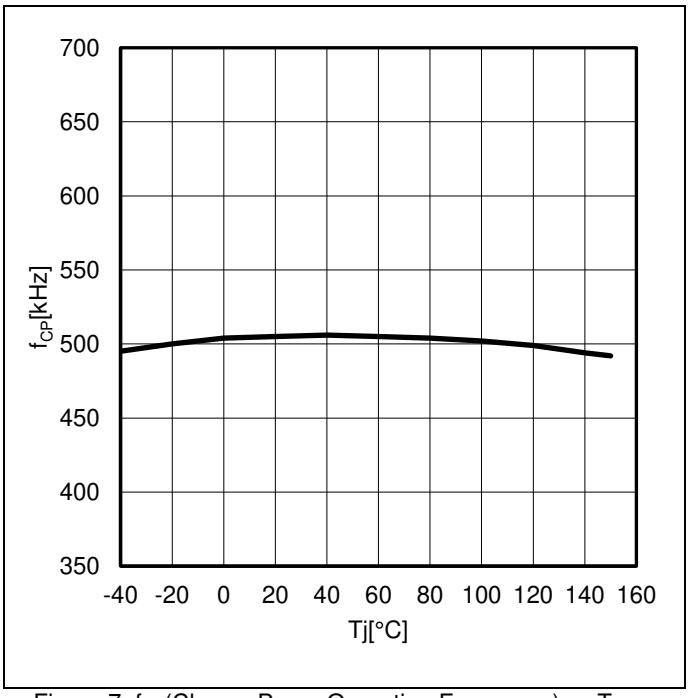


Figure 7. f_{CP}(Charge Pump Operating Frequency) vs Temp
(RSTB=VCC, Enable Register[2:0]=111,
Other address data is default value)

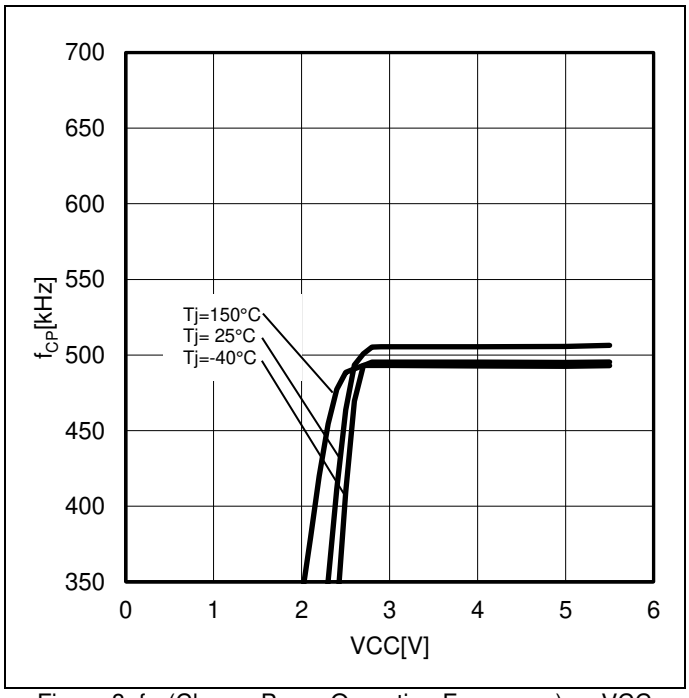


Figure 8. f_{CP}(Charge Pump Operating Frequency) vs VCC
(RSTB=VCC, Enable Register[2:0]=111,
Other address data is default value)

Typical Performance Curves (Reference Data)
(Unless otherwise specified, -40 °C ≤ Tj ≤ +150 °C, VS= 13.5 V, VCC= 5 V, The typical value is defined at Tj = 25 °C)

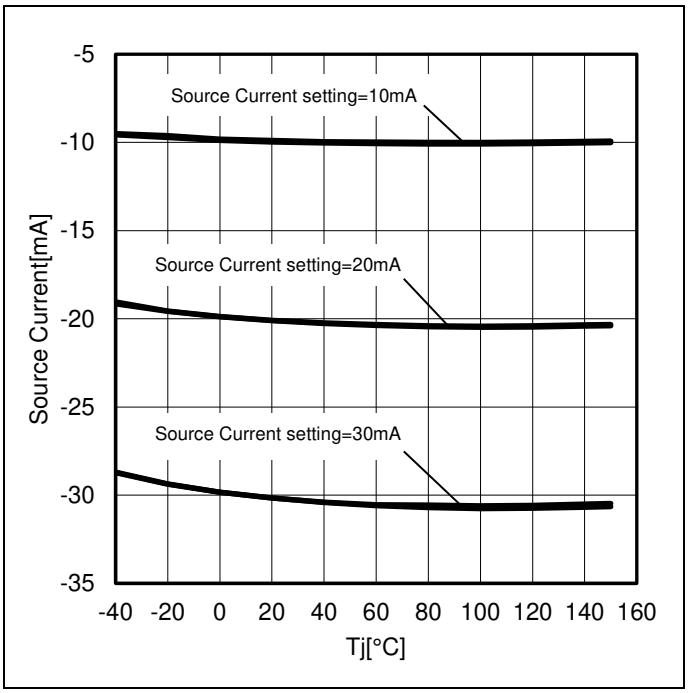


Figure 9. High Side Gate Driver Source Current vs Temp
(RSTB=VCC, PWM1=PWM2=VCC, GH1=SH1+2V,
GH2=SH2+2V, Enable Register[2:0]=111,
CH1_MODE[3:0]=1000, CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=01010, 10100, 11110
CUR_SINK[4:0]=00000, Other address data is default value)

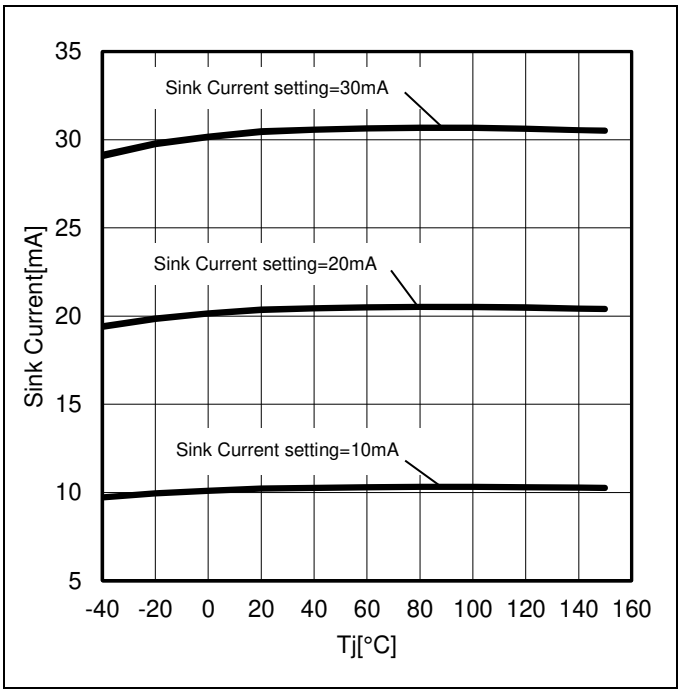


Figure 10. High Side Gate Driver Sink Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GH1=SH1+2V,
GH2=SH2+2V, Enable Register[2:0]=111,
CH1_MODE[3:0]=1000, CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=00000,
CUR_SINK[4:0]= 01010, 10100, 11110,
Other address data is default value)

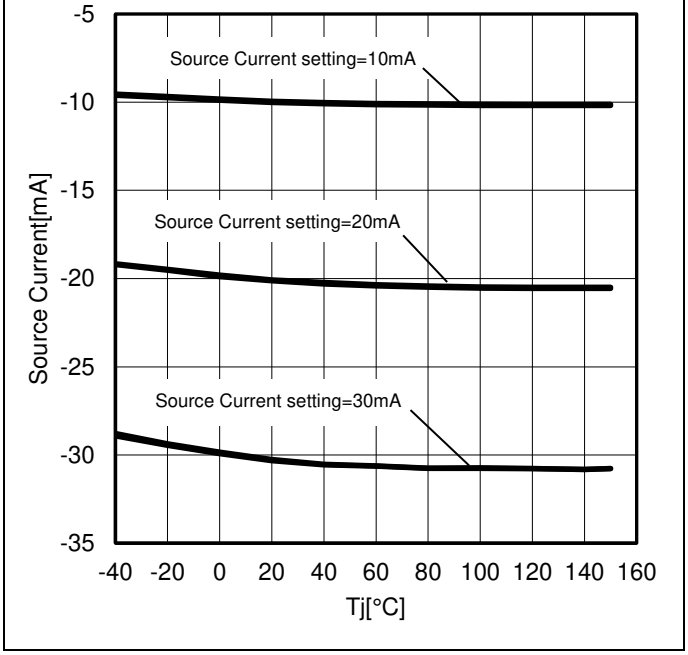


Figure 11. Low Side Gate Driver Source Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GL1=2V, GL2=2V,
Enable Register[2:0]=111, CH1_MODE[3:0]=1000,
CH2_MODE[3:0]=1000,
CUR_SOURCE[4:0]=01010, 10100, 11110
CUR_SINK[4:0]=00000, Other address data is default value)

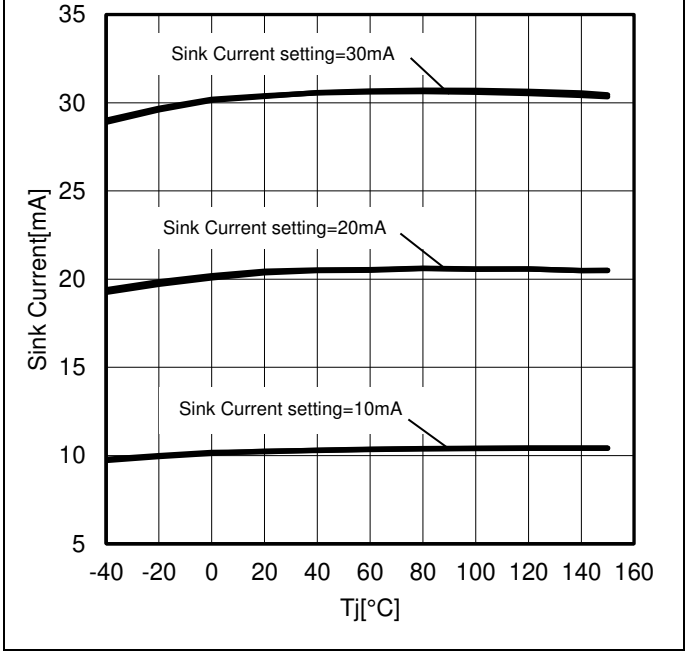
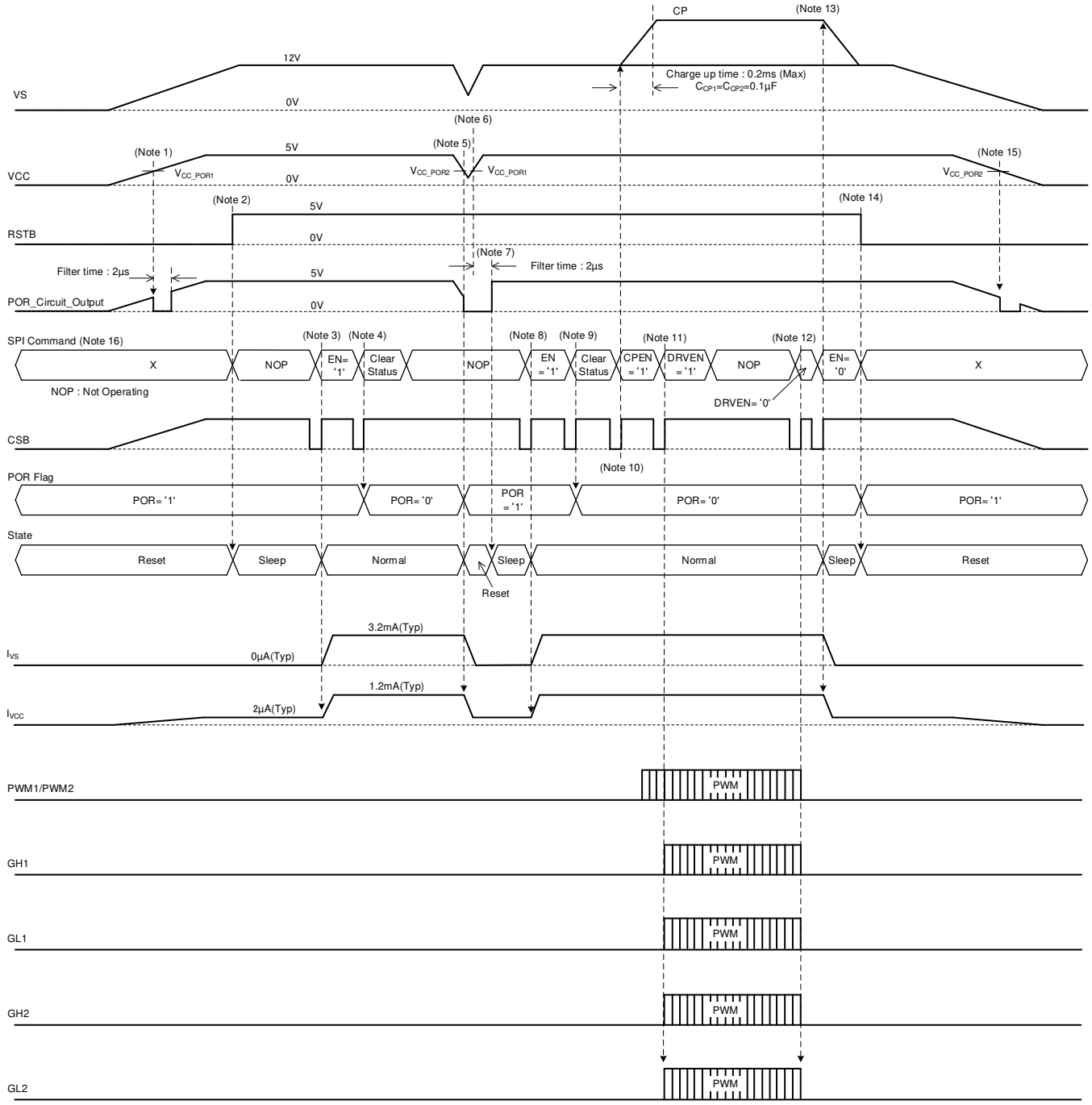


Figure 12. Low Side Gate Driver Sink Current vs Temp
(RSTB=VCC, PWM1=PWM2=0V, GL1=2V, GL2=2V,
Enable Register[2:0]=111, CH1_MODE[3:0]=1000,
CH2_MODE[3:0]=1000,CUR_SOURCE[4:0]=00000,
CUR_SINK[4:0]= 01010, 10100, 11110,
Other address data is default value)

Timing Chart



(Note 1) The Power-On-Reset circuit (POR) monitors the VCC voltage. At power-up, POR is released when VCC ≥ V_{CC_POR1} voltage. The POR circuit has a blanking time for 2µs (Typ) to reject noise.
The POR Flag in status resister is set to '1' in reset and is kept after recovery reset.

(Note 2) RSTB is set high by MCU. State is changed to Sleep state.

(Note 3) MCU sends the EN='1' command. State is changed to Normal state.
EN='1' command can be sent after 1µs(min) to change RSTB from "Low" to "High".
Consequently, analog circuit becomes active (I_{VS_act}=3.2mA Typ and I_{VCC_act}=1.2mA Typ).
Transition time is 50µs(Max) from "Sleep state" to "Normal state".

(Note 4) MCU sends "Clear Status" Command. Therefore, POR bit in status register is set to '0' (POR='1' to POR='0').

(Note 5) VCC voltage drops below $V_{CC\_POR1} - V_{CC\_POR\_hys}$. POR_Circuit_Output voltage is low (logic reset signal).
POR bit register is set to '1'. State is changed to Reset state.
Consequently, the analog circuit is OFF (I_{VS_qui1}=0μA Typ and I_{VCC_qui1}=2μA Typ).

(Note 6) VCC voltage rises above V_{CC_POR1}. POR_Circuit_Output level is high (logic reset release)
after filter time(2μs Typ).

(Note 7) POR_Circuit_Output level is high. Therefore, State is changed to Sleep state.

(Note 8) MCU sends the EN='1' command. State is changed to Normal state.
Therefore, analog circuit becomes active(I_{VS_act}=3.2mA Typ and I_{VCC_act}=1.2mA Typ).

(Note 9) MCU sends the "Clear Status" Command. Therefore, the POR bit register is set to '0'(POR='1' to POR='0').

(Note 10) MCU sends the CPEN='1' command. Charge pump circuit is activated. Charge time is 0.2ms(Max).

(Note 11) MCU sends the DRVEN='1' command. GH1, GL1, GH2 and GL2 outputs are active(Constant current driving).
Each register setting is set before DRVEN='1'.

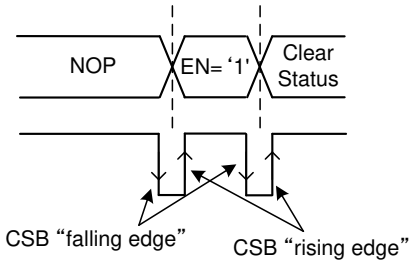
(Note 12) MCU sends the DRVEN='0' command. GH1, GL1, GH2 and GL2 outputs are pulled low with a 10Ω pull down.

(Note 13) MCU sends the EN='0' command. State is changed to Sleep state.
Therefore, analog circuit turns OFF(I_{VS_qui1}=0μA Typ, I_{VCC_qui1}=2μA Typ and charge pump circuit is OFF).

(Note 14) RSTB input is set to low level by MCU. State is changed to Reset state.
POR bit register is to '1'.Therefore, the SPI interface can't be communicable.

(Note 15) VCC voltage falls below $V_{CC\_POR1} - V_{CC\_POR\_hys}$. POR_Circuit_Output level is low (logic reset signal).

(Note 16) CSB falling edge and rising edge are described as below.



State Description

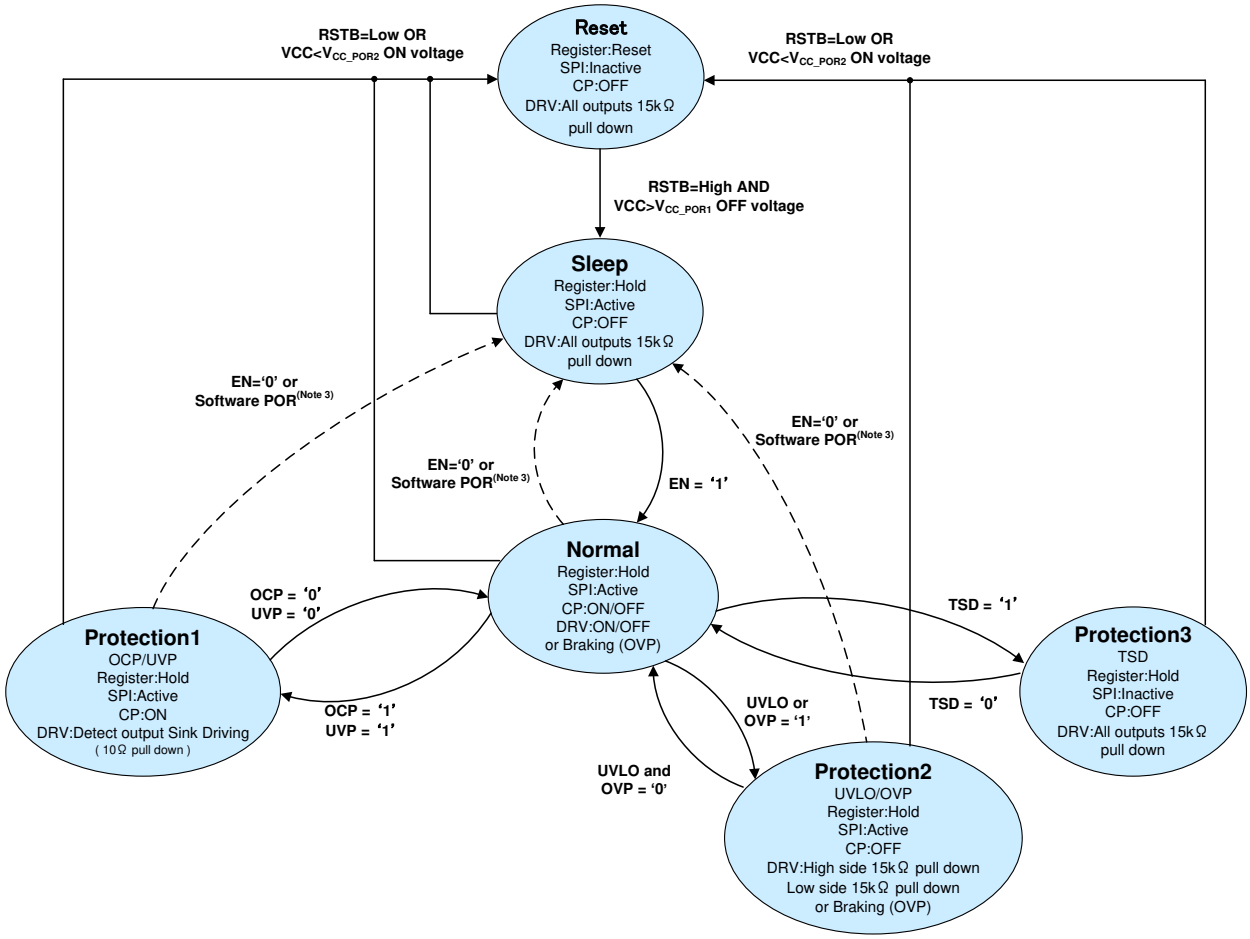
Table 1. State Description

State	CP	GH1,GH2	GL1,GL2	SPI
Reset	OFF	15kΩ pull down	15kΩ pull down	Inactive
Sleep	OFF	15kΩ pull down	15kΩ pull down	Active
Normal	ON	ON(DRVEN=1): Output is synchronous with PWM1(Note 1) or PWM2(Note 2) input	ON(DRVEN=1): Output is synchronous with PWM1(Note 1) or PWM2(Note 2) input	Active
		OFF(DRVEN=0): Outputs are Sink Driving Mode (10Ω pull down)	OFF(DRVEN=0): Outputs are Sink Driving Mode (10Ω pull down)	Active
	OFF	15kΩ pull down	15kΩ pull down / braking mode	Active
Protection1	ON	Output is Sink Driving Mode (10Ω pull down)	Output is Sink Driving Mode (10Ω pull down)	Active
Protection2	OFF	15kΩ pull down	15kΩ pull down / braking	Active
Protection3	OFF	15kΩ pull down	15kΩ pull down	Inactive

(Note 1) GH1 and GL1 outputs are synchronized to the PWM1 input.

(Note 2) GH2 and GL2 outputs are synchronized to the PWM2 input.

Functional Description State Control



(Note 3) This is Software POR command. It will set all register to default value. Note default value for POR register is 1.

Figure 13. Functional Description State Control

Transition time is 2μs(Typ) between each state. This does not include any relevant the blanking time. (e.g. UVLO detect blanking time, OVP detect blanking time etc.).

If settings are changed while IC is in one of the Protection states, the settings become valid except for those which can influence the transition to that particular protection state itself. Transition from Protection states to Reset state or Sleep state occurs immediately. Transition to normal state is only possible when the particular protection condition (e.g. OCP, OVP, UVLO or TSD) is no more existing. Furthermore, only the channels which are having over current move to OCP Protection state. Other channels with normal currents stay in Normal state.

The following table describes validity of individual command settings when changed in Protection states.

Command	Address	Protection1	Protection2
Software POR, Enable Register, Status Read/Clear Status	00h, 01h, 09h	Valid immediately	Valid immediately
Other Commands	02h, 03h, 04h, 05h, 06h, 07h	Valid immediately(note1)	Valid immediately(note2)

(note1) Settings become immediately valid except for the Channel which is in OCP. For those channel, settings would become effective only when they move out of OCP. E.g. if OCP threshold value is changed while a channel is in OCP, the new value would be effective only when the channel moves out of OCP.

(note2) Settings become immediately valid except for those which can influence the transition to protection mode itself. e.g. when state is Protection2 due to UVLO, it cannot be disabled by setting UVLOM as '0'.

Reset State (Refer to Table 1, Table 2, Figure 13 and Figure 16)

If RSTB=Low or VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$ Voltage, the state changes to Reset state.
Logic is in Reset state, therefore SPI communication is impossible. All register data is cleared. In the Reset State all analog circuits are OFF, therefore I_{VS_qui1}=0μA and I_{VCC_qui1}=2μA. The driver outputs of BD16950EFV are pulled down by a 15kΩ (Typ) internal resistor. The Reset state changes to Sleep state when RSTB=High and VCC > V_{CC_POR1} Voltage.

Transition to Reset State

Transition to Reset State can be made with 2 type of operation methods.

1. when RSTB=Low.
2. when VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$ Voltage.

Sleep State (Refer to Table 1, Table 2, Figure 13 and Figure 16)

When RSTB=High and VCC > V_{CC_POR1}, the state changes to the Sleep state. The logic is released from reset, therefore SPI communication is possible and all registers can be set. In the Sleep State, all analog circuits are OFF, therefore I_{VS_qui1}=0μA and I_{VCC_qui1}=2μA. The driver outputs of BD16950EFV are pulled down by a 15kΩ (Typ) internal resistor. However, the POR circuit remains active in Sleep State. When VCC < V_{CC_POR1} – $V_{CC\_POR\_hys}$, is detected, the logic is reset and the state changes to the Reset State.

Transition to Sleep State

Transition to the Sleep State can be made with 2 type of operation methods.

1. when EN=0 (RSTB=High and VCC > V_{CC_POR1})
2. by software reset (RSTB=High and VCC > V_{CC_POR1}).

Normal State (Refer to Table 1 and Figure 13)

The Normal State is the standard operating state for BD16950EFV. When the enable register EN is set to '1', the state changes from Sleep State to Normal State. In the Normal State, all analog circuits are active and SPI communication is possible. Additionally, ON/OFF control of the charge pump and the driver output is possible by setting the registers CPEN and DRVEN. The driver outputs are pulled down with 15kΩ (Typ) when CPEN=0. However, when both DRVEN=1 and DRVEN=0, the driver outputs are actively driven low with 10Ω (Typ). When CPEN='1' and DRVEN='1' the driver outputs are synchronized with the PWM1 or PWM2 input.

Protection1 State (Refer to Table 1, Table 2, Figure 13 and Figure 25 to 27)

When Over Current Protection (OCP) or DRAIN terminal Under Voltage Protection (UVP) event is detected, the state changes to Protection1 State. In this state, the SPI registers hold their values, SPI communication remains possible and the Charge pump is kept in charged-up state. The driver outputs are actively pulled low with 10Ω (Typ). For driver output OFF operation of the over current detection, a latch mode and auto recovery mode can be selected. Only the output at which an OCP event is detected will be turned OFF.

Protection2 State (Refer to Table 1, Table 2, Figure 13 and Figure 17 to 22)

When a UVLO or OVP event is detected at the VS terminal, the state changes to the Protection2 state. In this state, the SPI registers hold their values, SPI communication remains possible and the charge pump stops charging. The driver outputs can either be pulled down with 15kΩ (Typ) or operate in braking mode, which is controlled by the MCU in case of a user-generated over-voltage event that is detected by the MCU. Both (UVLO and OVP) detection functions can be disabled, but not during an already detected OVP or UVLO event.

Protection3 State (Refer to Table 1, Table 2, Figure 13 and Figure 23)

When a TSD event is detected, the state changes to Protection3 State. In Protection3 state SPI registers hold their values, but SPI is disabled and the charge pump stops charging. The driver outputs are pulled down with 15kΩ (Typ).

Dual Power Supply: VS and VCC

The supply voltage VS supplies the charge-pump and low-side driver. An internal charge-pump is used to drive the high-side switches. The supply voltage VCC (3.3V/5V) is used for analog blocks and digital core of the BD16950EFV. Due to the independent VCC supply voltage, the logic control and logic status information is not lost even if the VS supply voltage is switched OFF. In case of power-on (VCC increases above the POR threshold V_{CC_POR1} = 2.00V Typ), the circuit is initialized by an internally generated power-on reset (POR). If the VCC voltage decreases under the POR threshold V_{CC_POR1} – $V_{CC\_POR\_hys}$ = 1.90V(Typ), the driver outputs (GH1, GH2, GL1 and GL2) are switched-off and the logic registers are set to default values.

Constant Current Control

The controlled constant source and sink current values of the gate driver can be set individually by the SPI register. Setting ranges are ‘Drivers OFF’ and 1mA - 31mA in steps of 1mA. In the ‘Drivers OFF’ setting, the drivers are set to 0mA setting (CUR_SINK [4:0] = 5’b00000). They can be synchronized with PWM1 or PWM2 input signal depending on the Half-bridge driver mode.

In Figure 14, the high-side constant current circuit is shown. Figure 15 shows the low-side constant current circuit. The global reference current ‘IREF’ is mirrored into the channel current to generate a local reference voltage while amplifier A1 forces the voltage across the current sense resistor to match the local reference voltage.

The output device is scaled to give a 5 bit output range so that the source/sink current values can be achieved in range of 1mA to 31mA by steps of 1mA. The source /sink current values do not contain the 15 kΩ pull down current.

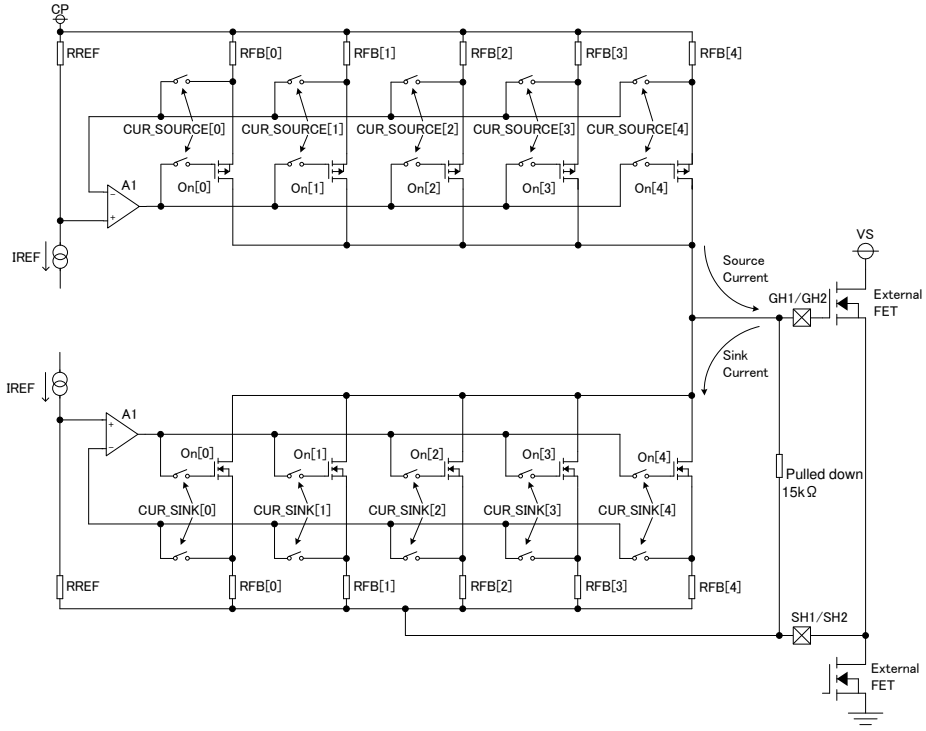


Figure 14. High Side Constant Current Circuit

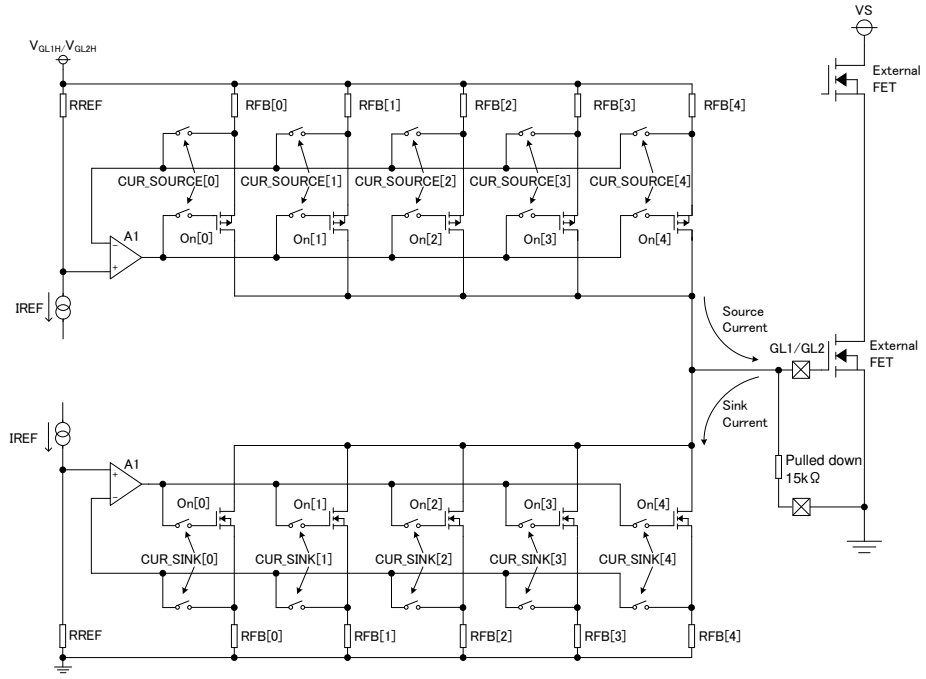
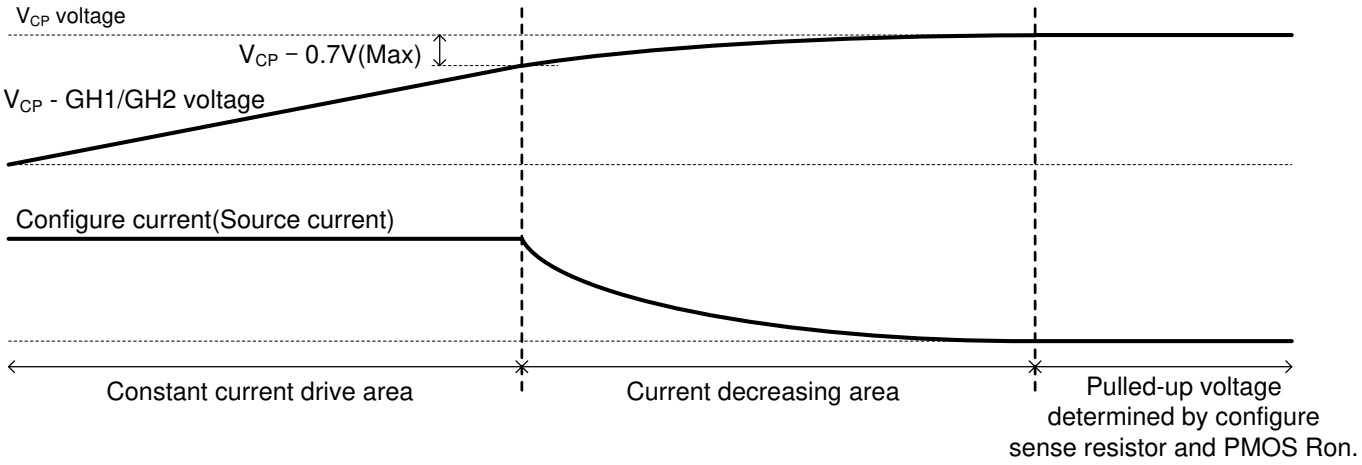


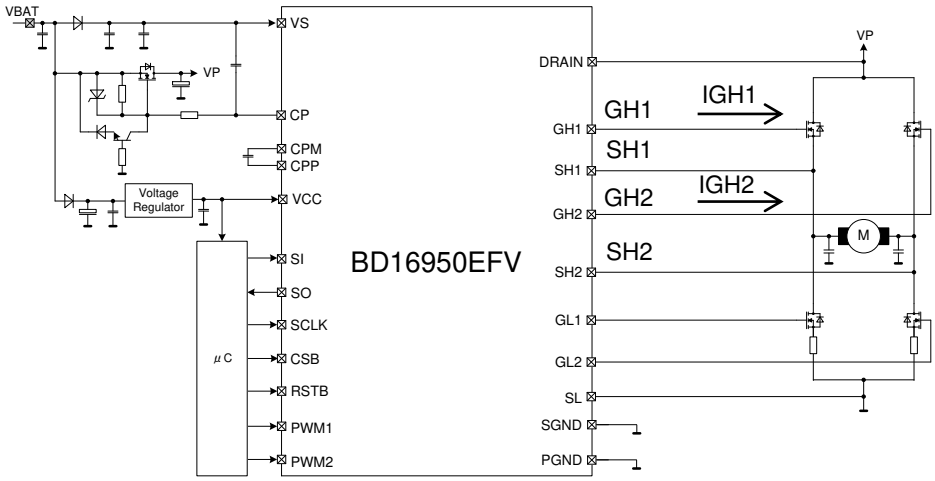
Figure 15. Low Side Constant Current Circuit

High Side Gate Driver Outputs at Saturation Source Current Control

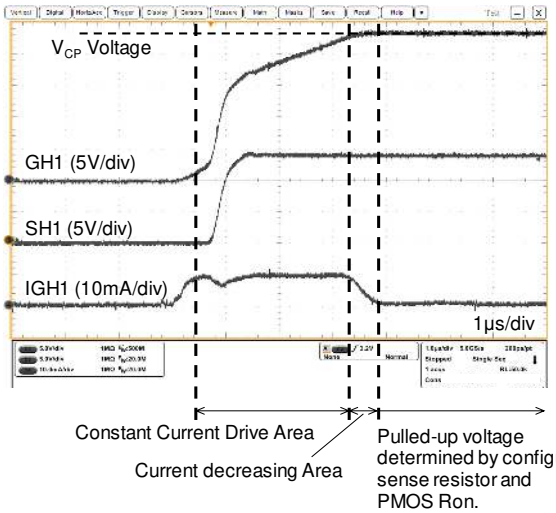
When the GH1/GH2 terminal voltage exceeds V_{CP}-0.7V (Max), the source current decreases from the setting value. Therefore, the constant current drive range is within GH1/GH2 terminal voltage < V_{CP}-0.7V(Max). After constant current drive, GH1 and GH2 terminals are pulled up by the current sense resistor and PMOS ON-resistance (current sense resistor(RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4]) and PMOS). The effective resistance value of the pulled-up is determined by current sense resistor and PMOS Ron.



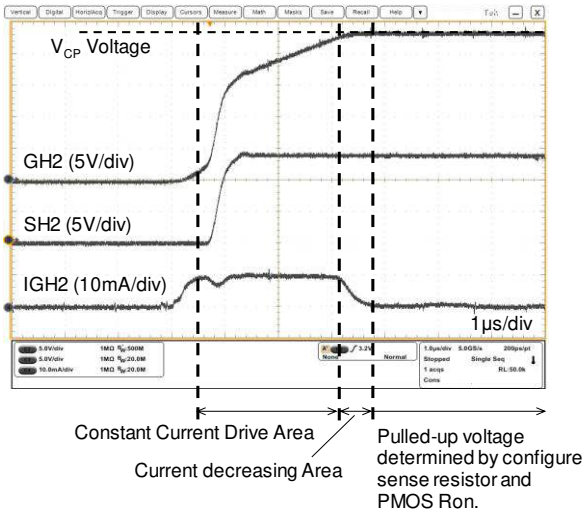
Evaluation Example (High Side Gate Voltage and Gate Current)



Channel 1 side waveform
(CUR_SOURCE[4:0]=01010)

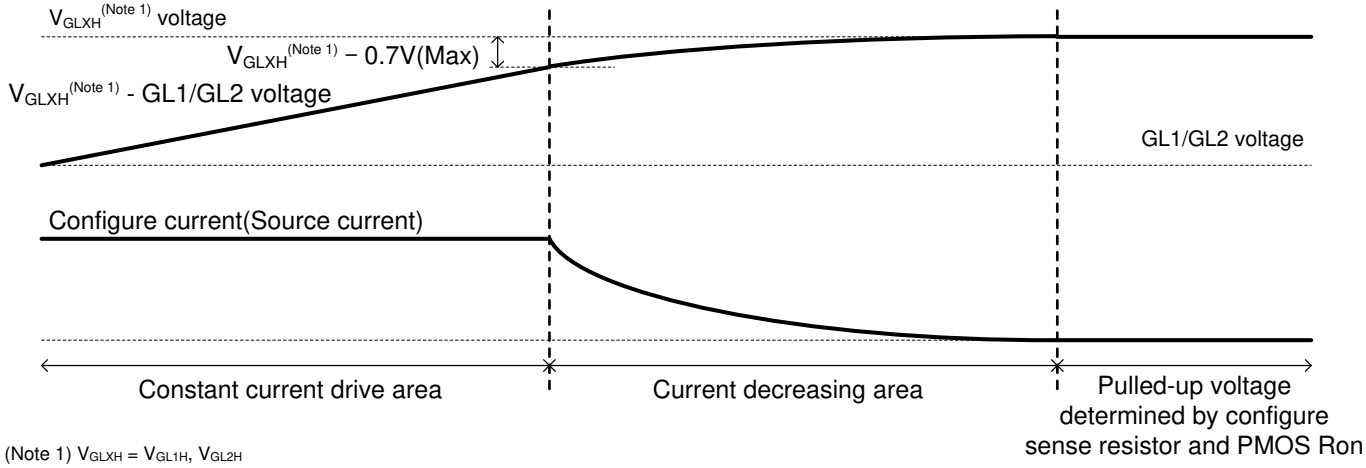


Channel 2 side waveform
(CUR_SOURCE[4:0]=01010)



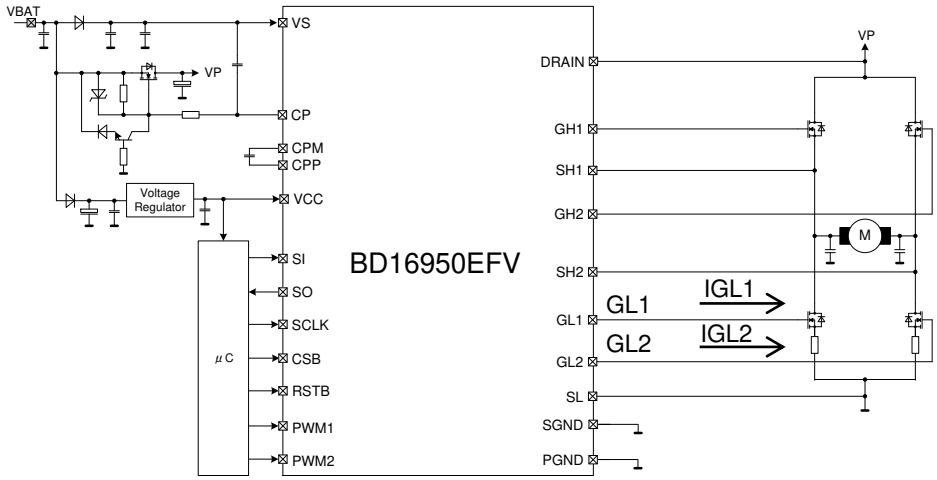
Low Side Gate Driver Outputs at Saturation Source Current Control

When the GL1/GL2 terminal voltage exceeds V_{CLAMP}-0.7V (Max), the source current decreases from the setting value. Therefore, the constant current drive range is within GL1/GL2 terminal voltage < V_{GLXH}-0.7V (Max). After constant current drive, GL1 and GL2 terminals are pulled up on a current sense resistor and PMOS Ron (current sense resistor(RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4]) and PMOS). The effective resistance value of the pulled-up is determined by current sense resistor and PMOS Ron.

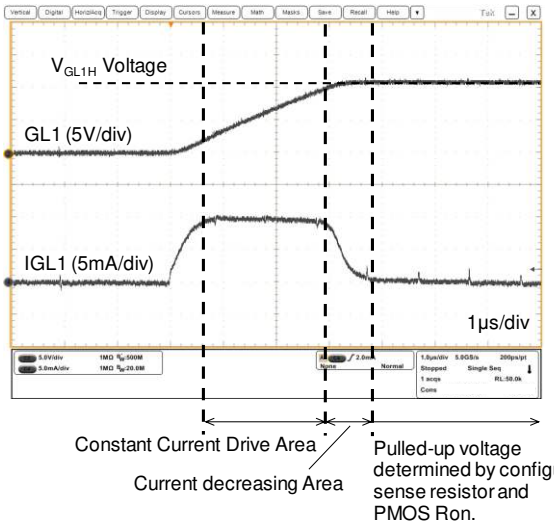


(Note 1) $V_{GLXH} = V_{GL1H}, V_{GL2H}$

Evaluation Example (High Side Gate Voltage and Gate Current)

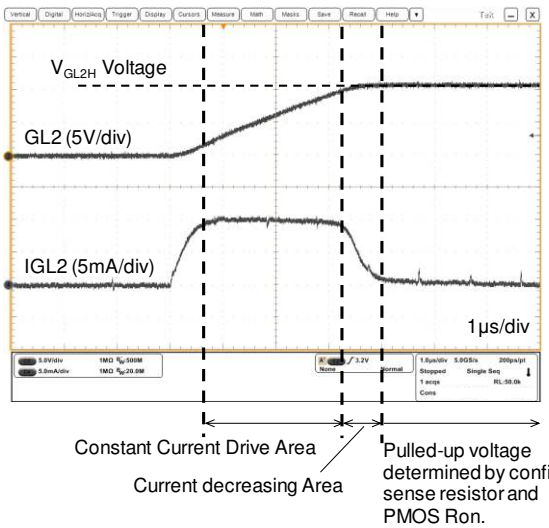


Channel 1 side waveform
(CUR_SOURCE[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and PMOS Ron.

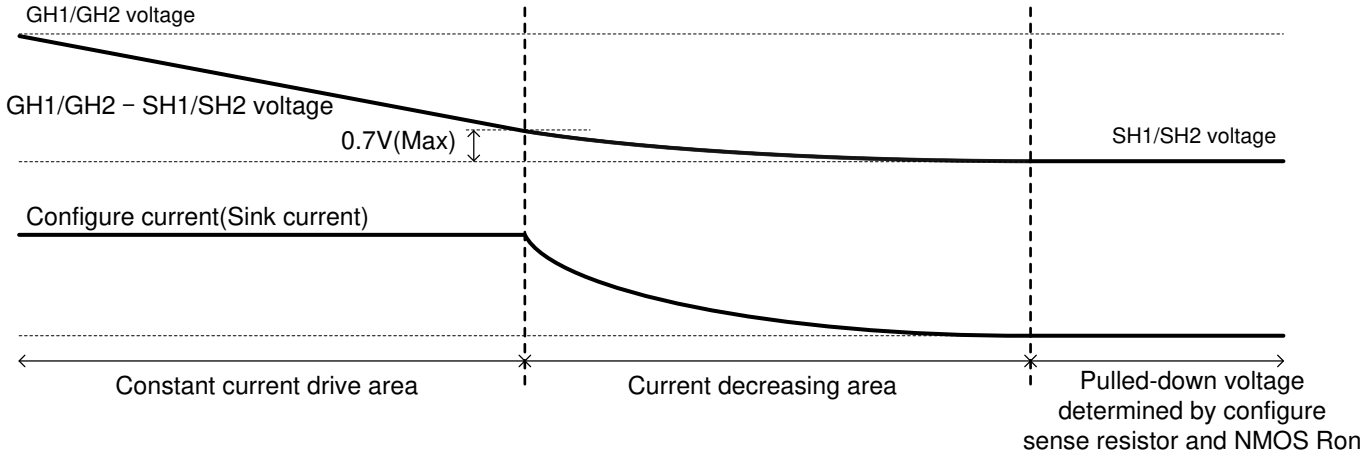
Channel 2 side waveform
(CUR_SOURCE[4:0]=01010)



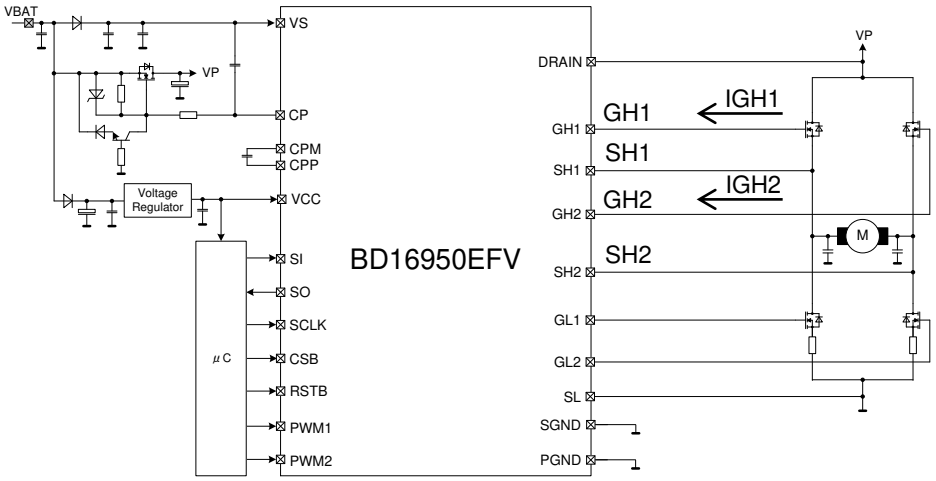
Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and PMOS Ron.

High Side Gate Driver Outputs at Saturation Sink Current Control

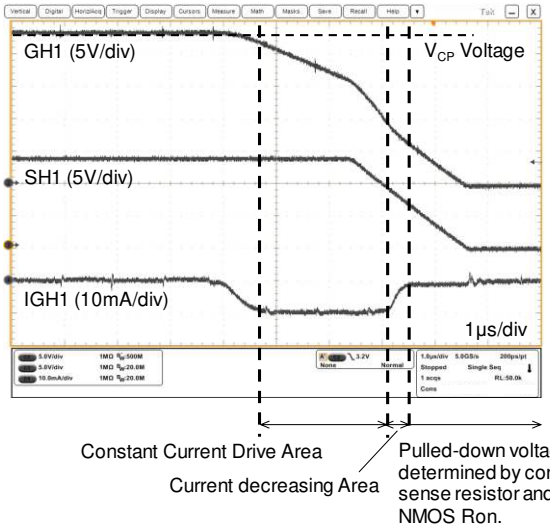
When GH1/GH2 terminal voltage falls below 0.7V (Max), the sink current decreases from the setting value. Therefore, constant current drive range is within GH1/GH2 terminal voltage > 0.7V (Max). Beyond this range, GH1 and GH2 terminals are pulled down on a current sense resistor and NMOS Ron (current sense resistors RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4] and NMOS). The effective resistance value of the pulled-down is determined by current sense resistor and NMOS Ron.



Evaluation Example (High Side Gate Voltage and Gate Current)

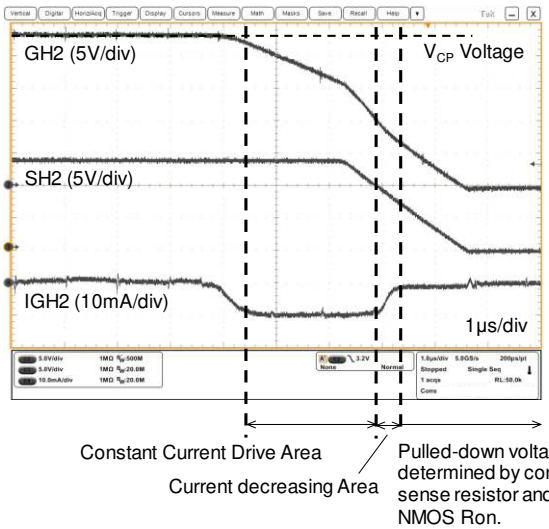


Channel 1 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-down voltage determined by configure sense resistor and NMOS Ron.

Channel 2 side waveform
(CUR_SINK[4:0]=01010)

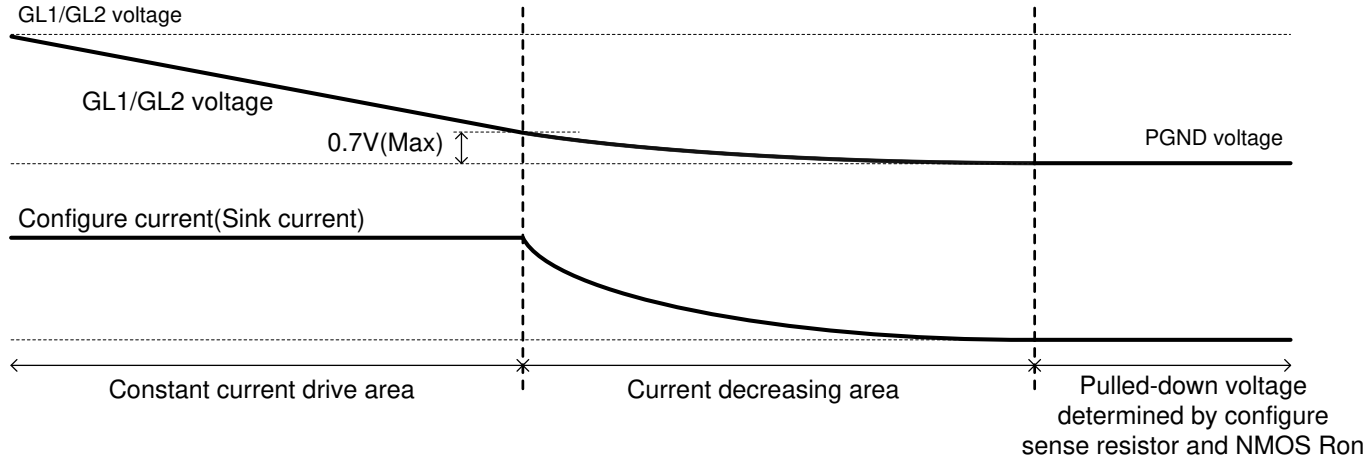


Constant Current Drive Area
Current decreasing Area
Pulled-down voltage determined by configure sense resistor and NMOS Ron.

Low Side Gate Driver Outputs at Saturation Sink Current Control

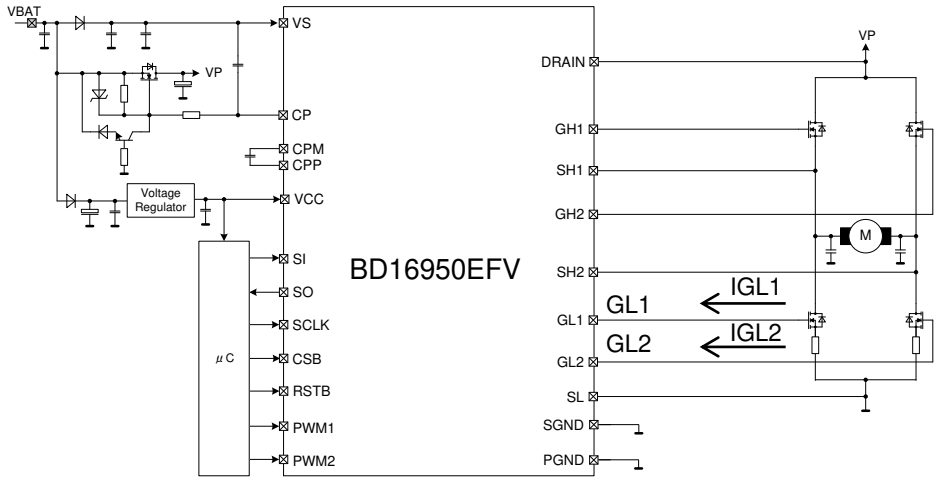
When GL1/GL2 terminal voltage falls below 0.7V (Max), the sink current decreases from the setting value. Therefore, constant current drive range is within GL1/GL2 terminal voltage > 0.7V (Max). Beyond this range, GL1 and GL2 terminals are pulled down on a current sense resistor and NMOS Ron (current sense resistors RFB[0], RFB[1], RFB[2], RFB[3] and RFB[4] and NMOS).

The effective resistance value of the pulled-down is determined by current sense resistor and NMOS Ron.

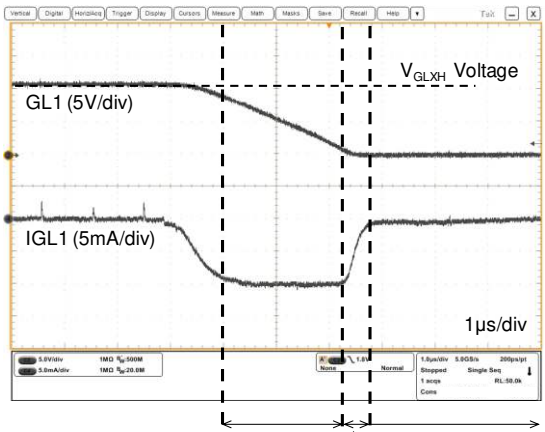


Evaluation Example (High Side Gate Voltage and Gate Current)

p

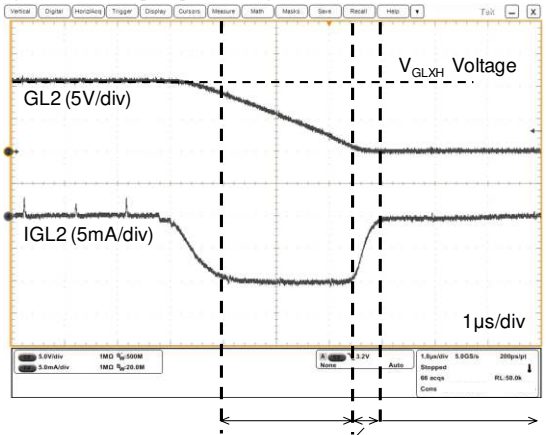


Channel 1 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and NMOS Ron.

Channel 2 side waveform
(CUR_SINK[4:0]=01010)



Constant Current Drive Area
Current decreasing Area
Pulled-up voltage determined by configure sense resistor and NMOS Ron.

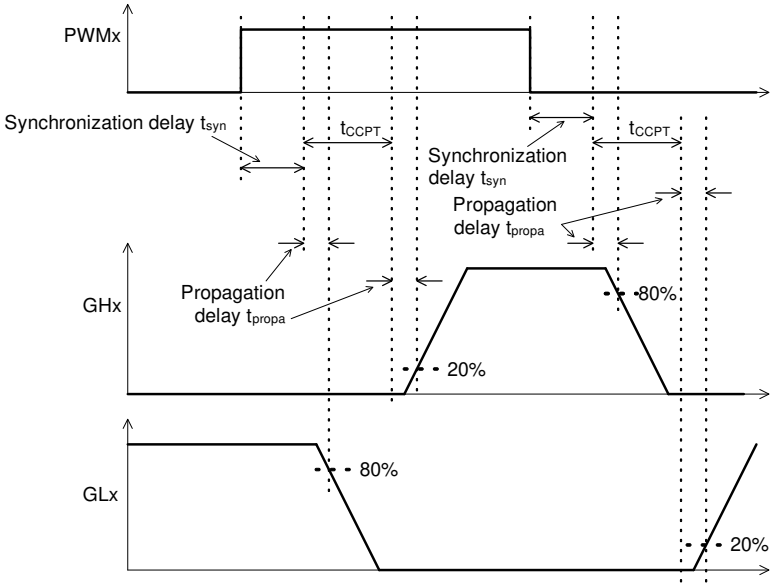
PWM Control

(Active Free Wheeling : Half-Bridge Control Mode=1000. See Mode Configuration on page 37)

The relationship of PWM, GHx and GLx outputs signal are as below. When the BD16950EFV detects the rising edge of the PWM signal, the GHx or GLx are turned on, after an asynchronous delay (Synchronization delay t_{syn}). There is also an internal delay time(Propagation delay t_{propa}). before GHx or GLx outputs are turned on.

The external MOSFETs in Half-bridge configuration are switched ON with an additional delay time t_{CCPT} (Cross Current Protection Time) between the sink current start of GL1 / GL2 and the source current start of GH1/GH2 to prevent cross current in the half-bridge. This value can be set by the SPI register in the range:

0.25µs…4µs (0.25µs steps)
4µs…12µs (1µs steps)
12µs…92µs (2µs steps)

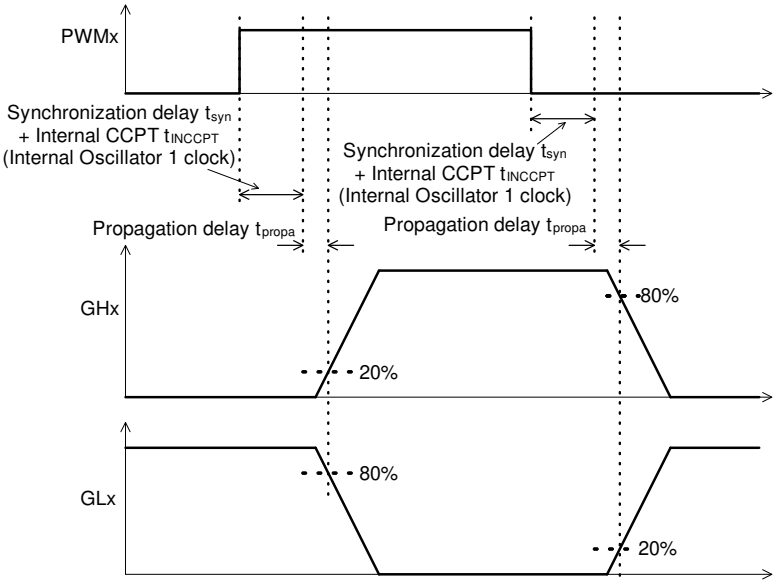


PWM Control

(Passive Free Wheeling : Independent Control Mode : PWM Control Mode. See Mode Configuration on page 37)

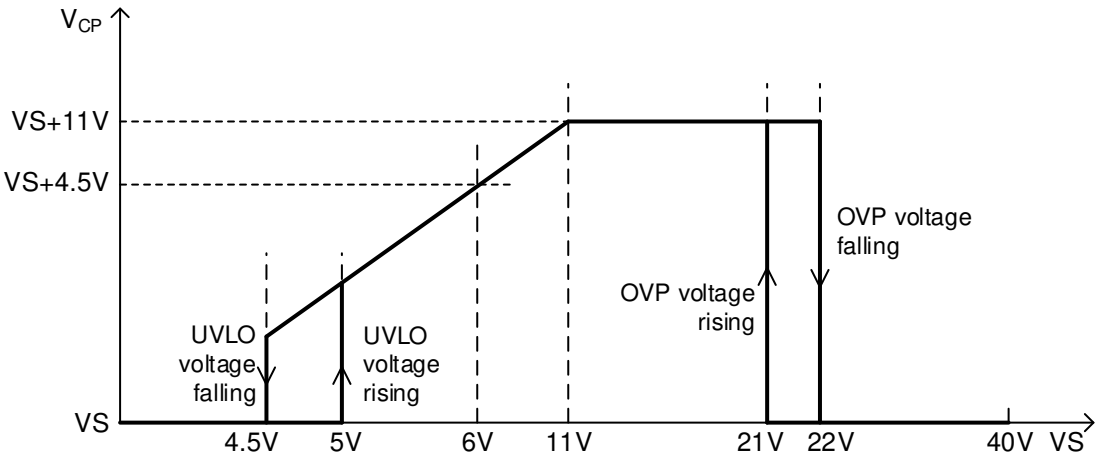
The relationship of PWM, GHx and GLx outputs signal are shown below. When the BD16950EFV is detecting the high edge of the PWM signal, an asynchronous delay is present (Synchronization delay t_{syn}) between the PWM signal and high-side source/sink or low-side source/sink of internal logic signal. Then, GHx or GLx are turned on. However, there is an internal delay time(Propagation delay t_{propa}) before GHx or GLx outputs are turned on.

The GHx or GLx are switched ON with an additional delay time t_{INCCPT} (Internal Cross Current Protection Time) between the sink current end of GHx / GLx and the source current start of GHx / GLx to prevent cross current.



Charge Pump

A charge pump is needed for driving the gates of the high-side external power MOS transistors. It requires a 0.1µF capacitor between the CPP and CPM terminals and another 0.1µF capacitor between the CP and VS terminals. Without load or when VS>13.5V, the voltage at the CP terminal is boosted up to VS+11V. The charge pump is clocked at 500kHz with a dedicated internal oscillator. The V_{CP} voltage decreases with a slope of 1V per 10mA of current load at VS=13.5V. It is also possible to use the V_{CP} voltage to drive external parts taking into account the mentioned load current range and V_{CP} drop voltage.



Protection

Table 2. Protection

State	Protection	Detect Conditions (Typical)		Detect Operation	Register Flag
		Detect	Release		
Reset	VCCPOR	V_{CC} < 1.90V	V_{CC} > 2.00V	All registers are reset CP : OFF DRV(GH1,GH2,GL1,GL2) : All outputs 15kΩ pull down	POR
Normal	TW	Tj > 137.5°C	Tj < 117.5°C	CP : ON DRV(GH1,GH2,GL1,GL2): Constant current operating	TW
Protection2	VS UVLO	V_S<4.5V	V_S>5.0V	CP : OFF DRV(GH1,GH2,GL1,GL2) : All outputs 15kΩ pull down	UVLO
Protection2	VS OVP	V_S>22V	V_S<21V	CP : OFF DRV(GH1,GH2,GL1,GL2) : High side outputs 15kΩ pull down. Low side outputs 15kΩ pull down or Braking mode.	OVP
Protection3	TSD	Tj > 175°C	Tj < 160°C	CP : OFF DRV(GH1,GH2,GL1,GL2) : All outputs 15kΩ pull down	TSD
Protection1	OCP UVP	V_{OCP} > Setting value(Note 1) V_{UVP} < 4.9V	V_{OCP} < Setting value(Note 1) V_{UVP} > 4.9V	CP : ON DRV(GH1,GH2,GL1,GL2) : OCP : Detection output only turn OFF(Note 2) UVP : GH1 and GH2 turn OFF(Note 2)	OCP_HS1 OCP_HS2 OCP_LS1 OCP_LS2

(Note 1) BD16950EFV be able to set the OCP threshold by SPI

(Note 2) BD16950EFV be able to set in the register the latching or auto recovery of OCP and UVP

VCC Power On Reset (POR)

When the VCC terminal voltage drops below 1.90V (Typ), all registers are reset, the driver outputs (GH1, GH2, GL1 and GL2) of BD16950EFV are pulled down with 15kΩ (Typ) and all analog circuits are OFF. In this case, the POR Status Flag register is set to '1' (initial value=1). Reading this SPI register is possible when VCC terminal voltage is above 2.00V (Typ). In order to clear the POR flag in this case, a 'clear status' command (clear POR bit) should be sent. In addition, POR Blanking time of 2μs (Typ) is programmed to avoid a malfunction caused by noise. The BD16950EFV starts counting the blanking time When the VCC terminal voltage drops below 1.90V (Typ). After that, the driver outputs are pulled down with the internal 15kΩ (Typ) resistor and the POR register is set to '1'.

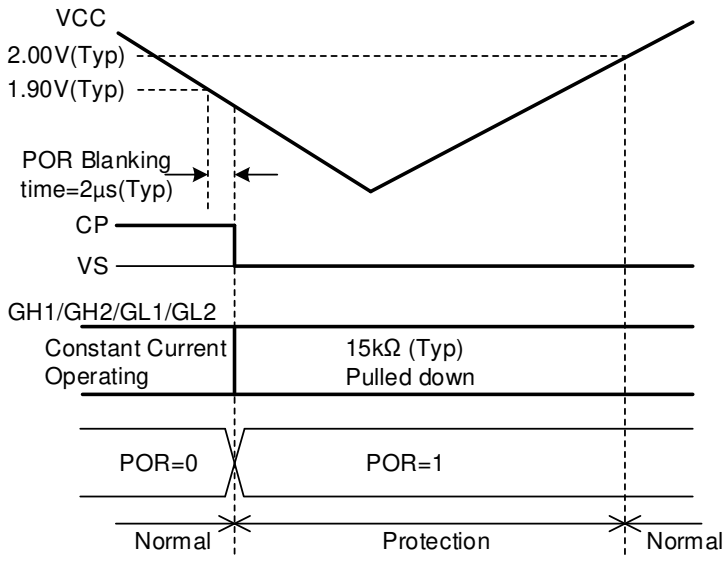


Figure 16. VCC POR Timing Chart

VS Under Voltage Lock Out (UVLO)

There are 3 modes for UVLO function: Auto recovery, Latch and UVLO disable. The UVLO setting can be set by the SPI register.

1. Auto Recovery

When VS terminal voltage is below 4.5V (Typ), all driver outputs (GH1, GH2, GL1 and GL2) of the BD16950EFV are pulled down with 15kΩ (Typ), the charge pump stops and the UVLO Status Read register is set to '1'. When the VS terminal voltage rises above 5.0V (Typ), the BD16950EFV returns to normal operation mode. The Status Read remains latched UVLO= 1 until it is cleared via the "Clear Status" command. In addition, a 64µs (Typ) UVLO Blanking time is programmed to reject noise. When the VS terminal voltage drops below 4.5V (Typ), BD16950EFV starts the blanking time. After that, the driver outputs are pulled low state with 15kΩ (Typ) and the UVLO register is set "1".

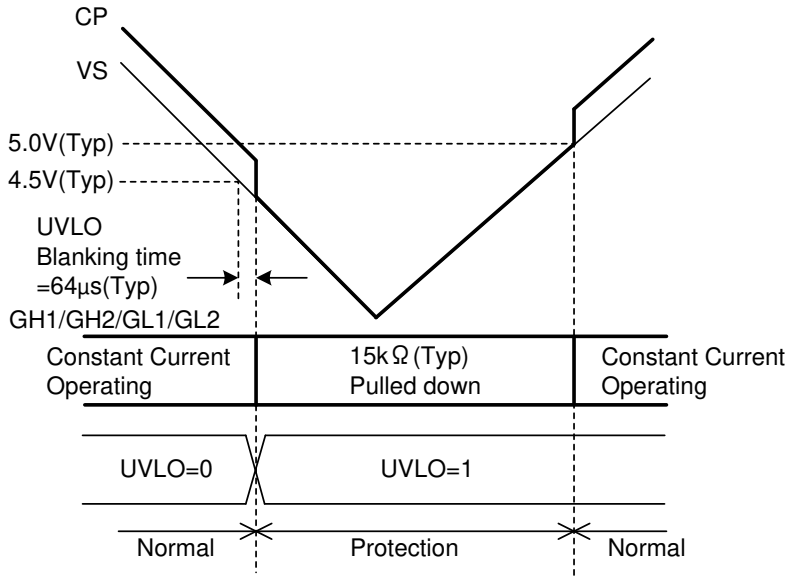


Figure 17. VS UVLO Timing Chart (Auto Recovery)

2. Latch

When the VS terminal voltage drops below 4.5V (Typ), all driver outputs are pulled down with 15kΩ (Typ), the charge pump stops charging and the UVLO Status Read register is set '1'. When the VS terminal voltage rises above 5.0V (Typ) this condition remains until UVLO Status Read register is cleared via "Clear Status" command register. In addition, a 64µs (Typ) UVLO Blanking time is programmed to reject any noise. When the VS terminal voltage drops below 4.5V (Typ), the BD16950EFV starts counting the blanking time. After that, the driver outputs are pulled down with 15kΩ (Typ) and the UVLO register is set to '1'.

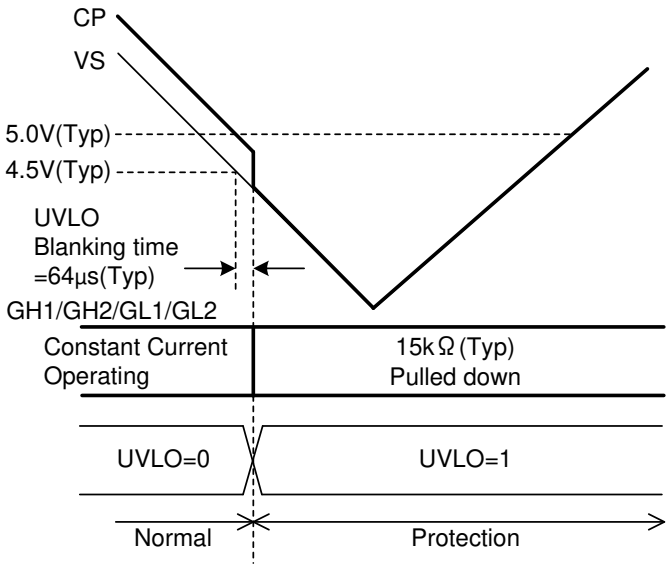


Figure 18. VS UVLO Timing Chart (Latch)

3.UVLO Disable

In this setting, normal operation continues when VS terminal voltage drops below 4.5V (Typ).

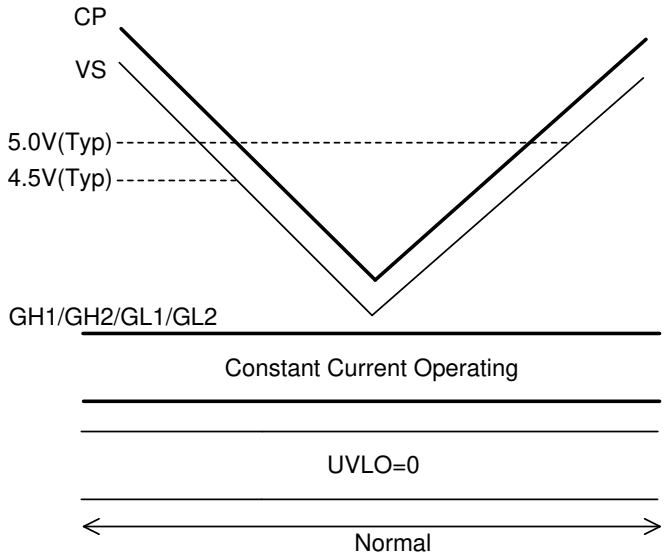


Figure 19. VS UVLO Timing Chart (UVLO Disable)

VS Over Voltage Protection (OVP)

Similar to the UVLO settings, the over-voltage protection function (OVP) also has three settings: Auto recovery, Latch and OVP disable, which can be set by the SPI register.

1.Auto Recovery

When the VS terminal voltage rises above 22V (Typ), all driver outputs are pulled down with 15kΩ (Typ), the charge pump stops and the OVP Status Read register is set to '1'. When VS terminal voltage drops below 21V (Typ), the driver outputs come back, the charge pump restarts and the BD16950EFV returns to the normal operation mode. The Status Read register latches OVP=1. In order to reset this register, it has to be cleared via "Clear Status" command register. Caution should be taken to never exceed the absolute maximum power supply voltage, which could destroy the IC. In addition, a 64µs (Typ) OVP Blanking time is programmed to reject noise. As soon as the VS terminal voltage rises above 22V (Typ), the BD16950EFV starts counting the blanking time. After that, the driver outputs are pulled down with 15kΩ (Typ) and the OVP register is set to '1'. In addition, when the Half-Bridge control No.2 mode register (Figure 29) is set by SPI in an OVP event, the driver outputs can be controlled in the 'Braking' mode.

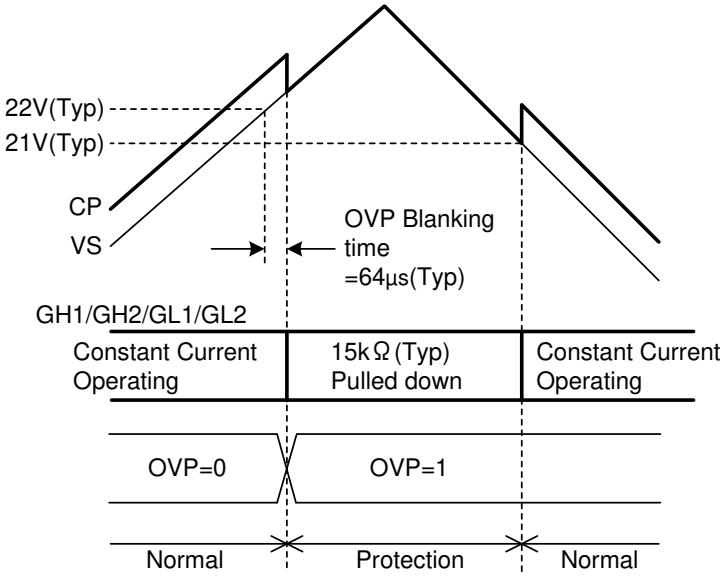


Figure 20. VS OVP Timing Chart (Auto Recovery)

2.Latch

When the VS terminal voltage rises above 22V (Typ), all driver outputs are pulled down with 15kΩ (Typ), the charge pump stops and the OVP Status Read register is set to '1'. When VS terminal voltage drops above 21V (Typ), this condition remains until the OVP Status Read register is cleared via "Clear Status" command register. In addition, a 64µs (Typ) OVP Blanking time is programmed to reject noise. VS terminal voltage above 22V (Typ), BD16950EFV count the blanking time. After that, the driver outputs are pulled down with 15kΩ (Typ) and OVP register is set "1". In addition, when the control No.2 mode register (Figure 29) is set by SPI in an OVP event, the driver outputs can be controlled in the 'Braking' mode.

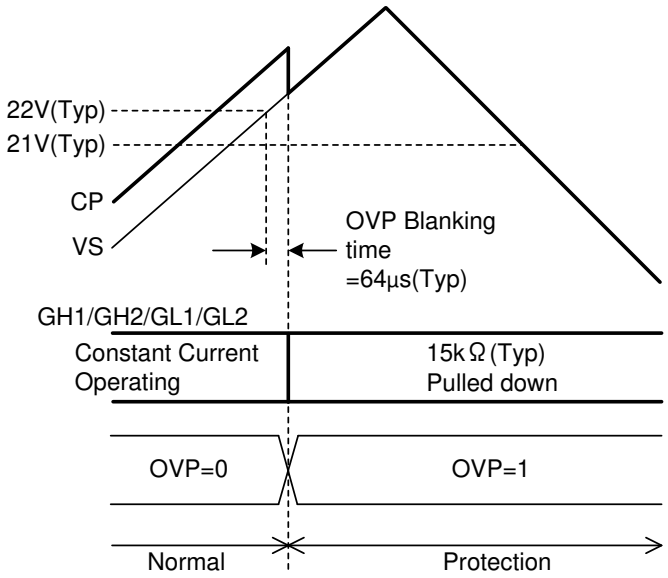


Figure 21. VS OVP Timing Chart (Latch)

3.OVP Disable

In this setting, when VS terminal voltage is above 22V (Typ), normal operation continues and Status Read is OVP=0.

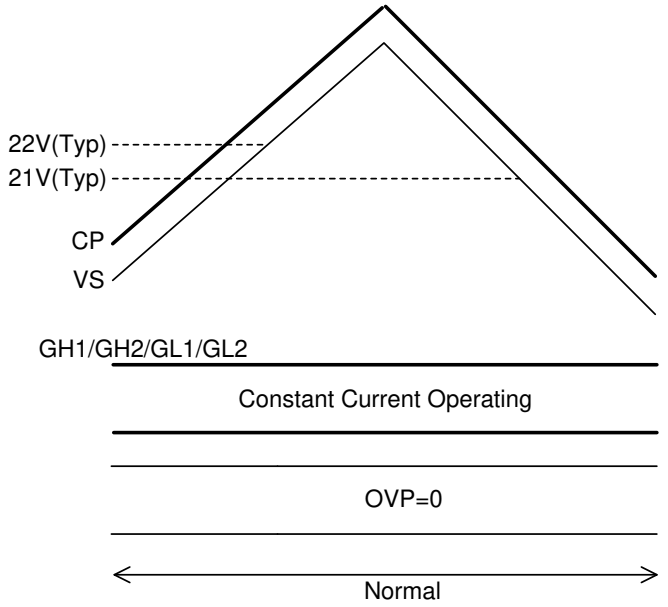


Figure 22. VS OVP Timing Chart (OVP Disable)

Thermal Shut Down (TSD)

When the junction temperature rises above 175°C (Typ) all driver outputs are pulled down with 15kΩ (Typ), the charge pump stops and the SPI is uncommunicable (SO output is all '1' output). In that case the TSD register is set to '1'. The SPI registers hold their values. When the junction temperature falls below 160°C (Typ), the BD16950EFV returns to normal operation mode and SPI is communicable. There is a 15°C hysteresis. In order to reset this flag, it has to be cleared via "Clear Status" command register.

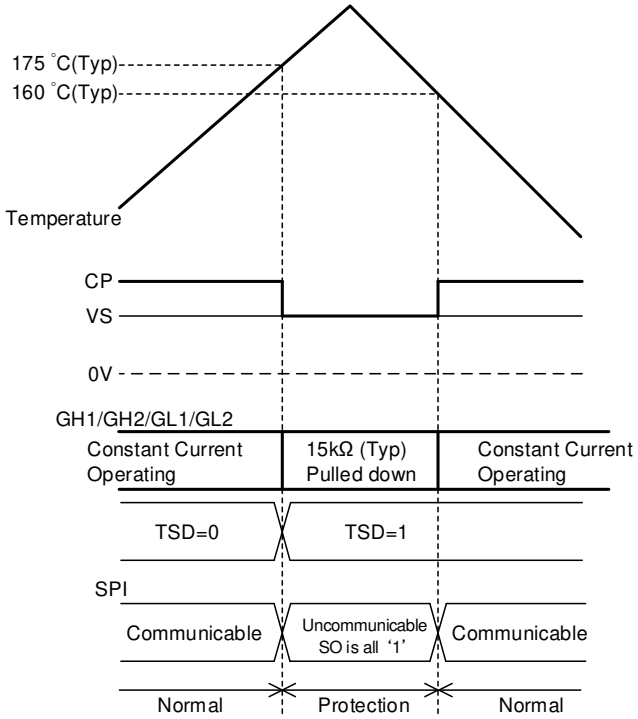


Figure 23. TSD Timing Chart

Thermal Warning (TW)

Before the TSD thermal shut down temperature is detected, the BD16950EFV can warn the MCU when the junction temperature rises above 137.5°C (Typ). In that case the TW register is set to '1'. The MCU can confirm that the IC is heating-up abnormally by reading the register TW. The MCU can turn OFF the charge pump (CPEN=0) or the driver outputs (DRVEN=0) before a TSD is detected. BD16950EFV releases the thermal warning TW when the junction temperature falls below 117.5°C (Typ). The Status Read remains latched TW=1. In order to reset TW register, it has to be cleared via "Clear Status" command.

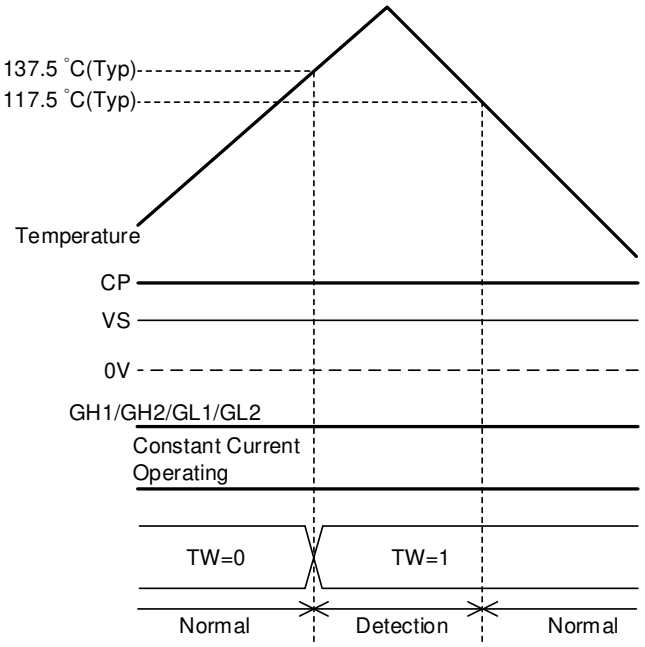


Figure 24. TW Timing Chart

Over Current Protection (OCP)

When the drain-source voltage of one (or more) external MOSFETs of the Half-bridge exceeds the OCP detection threshold setting value, the BD16950EFV detects over current. Only those outputs at which an over current is detected, will be turned OFF. The OCP detection threshold setting value can be set by the SPI register. Setting ranges are 200mV, 300mV, 400mV, 500mV, 750mV, 1000mV, 1250mV and 1500mV. High side (Drain-SH1 and Drain-SH2) and Low side (SH1-SL and SH2-SL) OCP detection levels can be individually set to different values. For each of the four external MOSFETs, there is an individual OCP Status flag (OCP_HS1, OCP_HS2, OCP_LS1 and OCP_LS2).

There is a latch mode and an auto recovery mode for the driver output OFF operation in case an over current is detected. Latch or auto recovery can be selected by the SPI register. OCP function is effective at No.2 mode, No.3 mode, No.4 mode, No.6 mode and No.9 mode (Mode Setting Ch2, Ch1).

To reject noise, the OCP Filter time setting can be set by the SPI register for both the auto recovery mode and the OCP latch mode. OCP Filter time setting ranges are 1µs to 64µs with steps of 1µs. OCP Filter time is the same for all output drivers.

The OCP Filter time starts when the drain-source voltage of the external MOSFET V_{DS} is higher than the OCP detection threshold voltage. When the setting value of Filter time exceeds the on time set by the PWM, the BD16950EFV cannot detect over current.

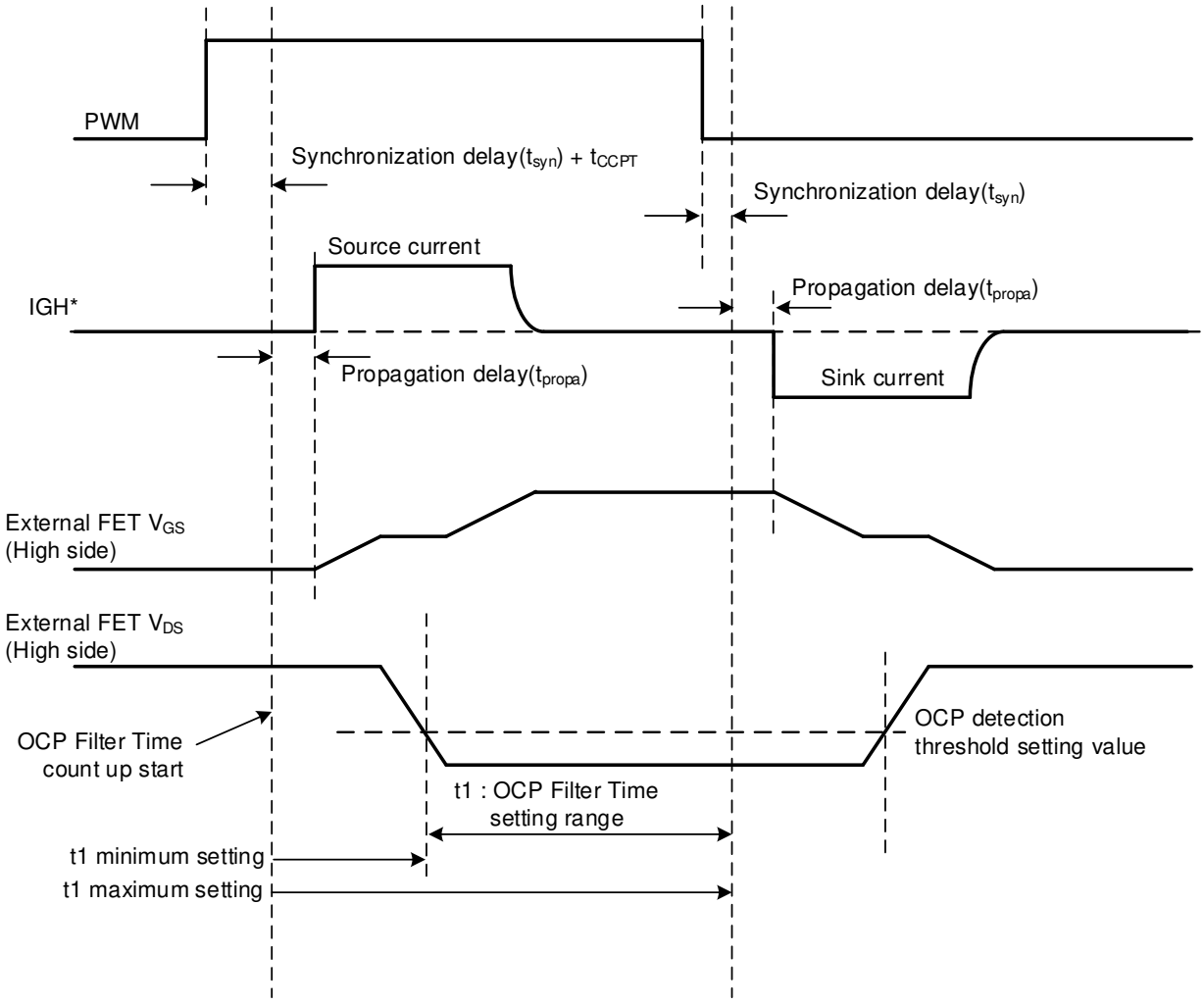


Figure 25. OCP Timing Chart

In latch mode, the BD16950EFV turns OFF (latched) the driver output when over current is detected. In this case, this output is actively driven low at the constant current 31mA setting and the OCP Status Read register is set to '1'. For each of the four external MOSFETs, there is an OCP Status Read register of OCP_HS1, OCP_HS2, OCP_LS1 and OCP_LS2. The OCP register corresponding detected over current is latched to '1'. In order to reset the OCP register and release the driver output, it has to be cleared via Clear Status Command. When the BD16950EFV detects an OCP condition, the charge pump stays active.

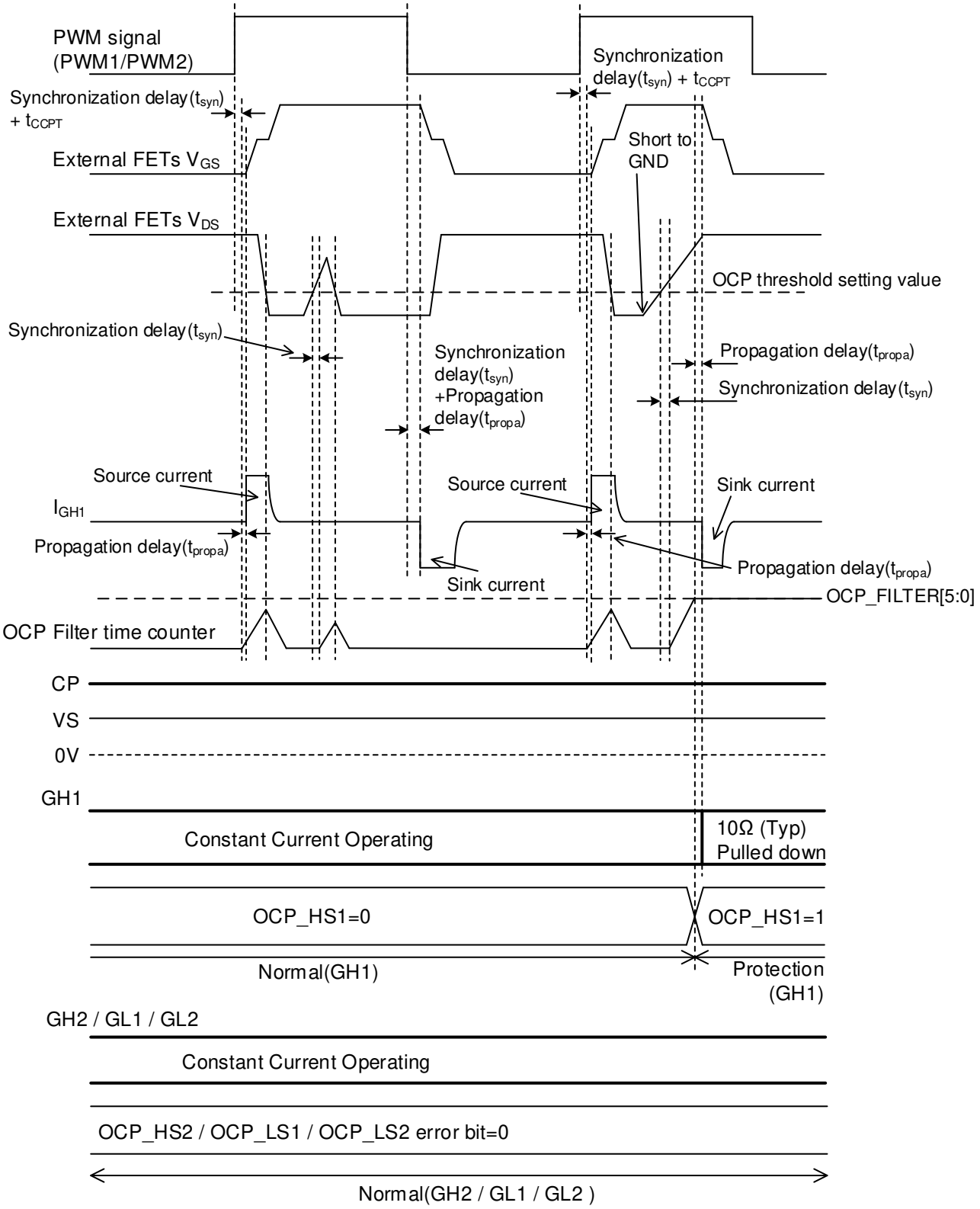
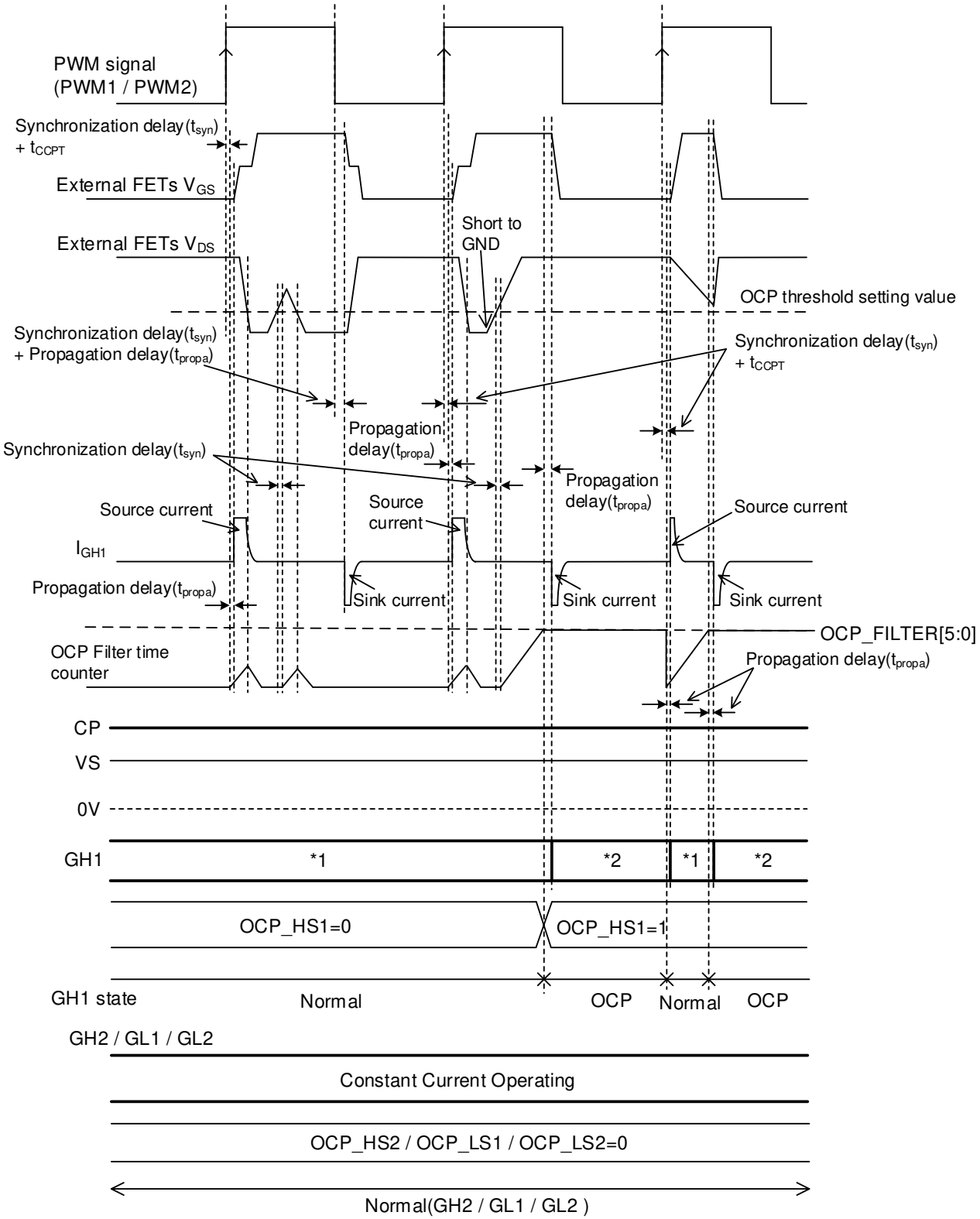


Figure 26. OCP Timing Chart (Latch)

In the auto recovery mode, the BD16950EFV turns OFF (latched) the driver output when over current is detected. After that, the driver output recovers from this OCP condition at the rising edge of the PWM signal (from PWM1 or PWM2 terminals). Then the detection output is actively driven low at the constant current 31mA setting and the OCP register is set to '1'. For each of the four external MOSFETs, there is an OCP Status Read register : OCP_HS1, OCP_HS2, OCP_LS1 and OCP_LS2. The OCP register bit corresponding to the output which detects over current is latched to "1". In order to release the driver output and reset the OCP register, it has to be cleared via Clear Status Command. When the BD16950EFV detects an OCP condition, the charge pump stays active.



*1 : Constant Current setting value

*2 : 10Ω (Typ) Pulled down

Figure 27. OCP Timing Chart (Auto Recovery)

DRAIN Under Voltage Protection(UVP)

When the DRAIN terminal voltage drops under 4.9V (Typ), DRAIN under voltage is detected. Therefore, GH1 and GH2 terminal are changed to 31mA sink setting. In other words, high side external MOSFET's become OFF. The states of high side driver GH1 and GH2 move to DRAIN under voltage protection1 states. Low side driver GL1 and GL2 stay in Normal states. UVP has same specification with OCP. The filter time of DRAIN under voltage protection is the same as the OCP_FILTER. There are latch mode and auto recovery mode for the driver output OFF operation when UVP is detected. In other words, when OCP is selected to latch mode, UVP becomes the latch mode. When OCP and UVP are detected at the same time, UVP is high priority. OCP_HS1 or OCP_HS2 Bit is changed, too. If GH1 is source setting (e.g. figure 33) and GH2 is sink setting, OCP_HS1 bit is changed to 1. If GH1 is sink setting (e.g. figure 30) and GH2 is source setting, OCP_HS2 bit is changed to 1. UVP function is become effective other than No.1 mode (Mode Setting Ch2, Ch1).

Register Map

Registers can be set using 16-bit SPI command (R/W bit+7bit Address+8bit data). The following table lists the addresses, Read/Write(R/W) possibility, the corresponding registers and default values of the registers.

Description	MSB	Address	Data bit							LSB	Default Value
	15	14-8	7	6	5	4	3	2	1	0	7-0
Software POR	W	000_0000	1	1	0	1	0	1	1	1	NA
Enable Register	R/W	000_0001	x	x	x	x	x	EN	CPEN	DRVEN	0000_0000
Mode Setting Ch2, Ch1	R/W	000_0010	CH2_ MODE [3]	CH2_ MODE [2]	CH2_ MODE [1]	CH2_ MODE [0]	CH1_ MODE [3]	CH1_ MODE [2]	CH1_ MODE [1]	CH1_ MODE [0]	0000_0000
Protection Mode Setting	R/W	000_0011	OCPLA_ H2	OCPLA_ L2	OCPLA_ H1	OCPLA_ L1	UVLOLA	OVPLA	UVLOM	OVPM	1111_1100
Half-Bridge Motor Op. Setting1	R/W	000_0100	x	x	x	CUR_ SOURCE [4]	CUR_ SOURCE [3]	CUR_ SOURCE [2]	CUR_ SOURCE [1]	CUR_ SOURCE [0]	0001_1111
Half-Bridge Motor Op. Setting2	R/W	000_0101	x	x	x	CUR_ SINK [4]	CUR_ SINK [3]	CUR_ SINK [2]	CUR_ SINK [1]	CUR_ SINK [0]	0001_1111
Half-Bridge Motor Op. Setting3	R/W	000_0110	x	x	CCPT[5]	CCPT[4]	CCPT[3]	CCPT[2]	CCPT[1]	CCPT[0]	0011_1111
OCP and UVP Setting	R/W	000_0111	x	x	OCPHD [2]	OCPHD [1]	OCPHD [0]	OCPLD [2]	OCPLD [1]	OCPLD [0]	0000_0000
OCP Filter Time Setting	R/W	000_1000	x	x	OCP_ FILTER [5]	OCP_ FILTER [4]	OCP_ FILTER [3]	OCP_ FILTER [2]	OCP_ FILTER [1]	OCP_ FILTER [0]	0000_0000
Status Read/Clear Status	R/W	000_1001	OCP_ HS1	OCP_ HS2	OCP_ LS1	OCP_ LS2	x	x	x	x	0000_0000

Note: x: Don't care

Address =00h <Software POR>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
00h	R/W	1	1	0	1	0	1	1	1
Initial Value	00h	0	0	0	0	0	0	0	0

This is Software POR command. It will set all setting register, error register(Global status register bits) and counter(blanking time) to default value.
Note default value for POR register is 1.
When EN is “1”, software POR can be used.
If the data does not match, this command is ignored, so the registers settings are unchanged.

Address =01h <Enable Register>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
01h	R/W	x	x	x	x	x	EN	CPEN	DRVEN
Initial Value	00h	0	0	0	0	0	0	0	0

Bit[2]: **EN** Enable for all analog blocks
0 : Sleep mode
1 : Normal mode

Bit[1]: **CPEN** Enable for Charge pump circuit
0 : Charge pump disable.
1 : Charge pump enable.
When CPEN is ‘0’, GH1, GH2, GL1, GL1 and GL2 are pulled down with 15kΩ resistors. It is also possible to control the driver in braking mode at normal state.

Bit[0]: **DRVEN** Enable for Half-bridge Drivers
0 : Drivers disable. GH1, GH2, GL1 and GL2 are pulled down at 10Ω.
1 : Drivers enable. GH1, GH2, GL1 and GL2 are synchronous with PWM1 or PWM2 input.

Address =02h <Mode Set Register>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
02h	R/W	CH2_ MODE[3]	CH2_ MODE[2]	CH2_ MODE[1]	CH2_ MODE[0]	CH1_ MODE[3]	CH1_ MODE[2]	CH1_ MODE[1]	CH1_ MODE[0]
Initial Value	00h	0	0	0	0	0	0	0	0

CH2_MODE[3:0] Defines mode settings for Channel2(GH2, GL2).

CH1_MODE[3:0] Defines mode settings for Channel1(GH1, GL1).

The table below describes various mode settings for Channel1. Mode for channel2 can be independently set following the same table using CH2_MODE [3:0] registers.

Mode Configuration								
NO	CH1_ MODE[3]	CH1_ MODE[2]	CH1_ MODE[1]	CH1_ MODE[0]	GH1	GL1	Channel Control	Channel1 Use Case
1	0	0	0	0	OFF	OFF	Independent Control	High Impedance
2	0	1	0	0	OFF	$\overline{PWM}$		Active low PWM Control of a VS connected load1
3	0	0	0	1	OFF	ON		Active low DC control of a VS connected load 1
4	0	1	1	0	PWM	OFF		Active high PWM control of a GND connected load 2
5	0	1	0	1	PWM	ON		Active high PWM control of load2 & active low DC control of load1
6	0	0	1	0	ON	OFF		Active high DC control of a GND connected load 2
7	0	1	1	1	ON	$\overline{PWM}$		Active high DC control of load2 & active low PWM control of load1
8	0	0	1	1	ON	ON		Active high DC control of load2 & active low DC control of load1
9	1	0	0	0	PWM with AFW(PWM)		Half-Bridge Control	Half-Bridge-Mode (PWM=high->GH1=ON: PWM=Low-> GH1=OFF)

Note: In Direct Control (DC) mode, PWM pin is either LOW or HIGH continuously. There is no PWM in DC mode.
Any other input command will put the driver into High impedance mode.

Half-Bridge Control Mode

For the high side and low side gate drivers of the BD16950EFV, there are 9 mode settings which can be set by the SPI register. In the pictures below, these modes are shown. No.1 is OFF pull down mode. No.4 and No.9 are PWM mode. No.3, No.6 and No.8 are Direct Control mode. No.5 and No.7 are PWM & Direct Control mode. No.2 is Braking mode.
No.1 to No.8 can control the high-side gate driver and low-side gate driver independently. No.9 can control the high-side gate driver and low-side gate driver as the Half-Bridge. BD16950EFV can select various modes.
Therefore, these modes allow the BD16950EFV to supports various applications. In addition, the GH1 and GL1 outputs are synchronized to the PWM1 input. GH2 and GL2 outputs are synchronized to PWM2. When Mode2 is set by SPI during an OVP detection, the driver outputs can be controlled in the Braking mode. When Inductive loads are used, SH1 and SH2 terminals might exceed their absolute maximum ratings. Therefore, the SH1 and SH2 terminals must be connected to a protection diode as illustrated by the diagrams below(Figure29 to Figure 35). The minimum current and voltage requirements of the diode are depending on the corresponding absolute maximum ratings of the SH1 and SH2 terminals.

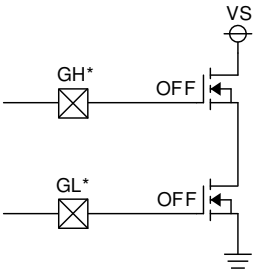


Figure 28. No.1 Mode

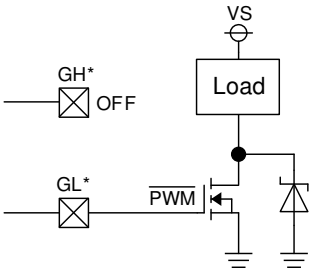


Figure 29. No.2 Mode (Braking Mode)

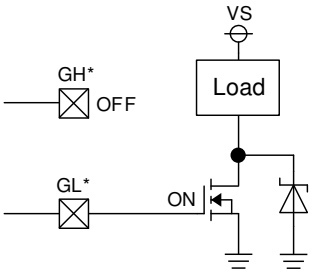


Figure 30. No.3 Mode

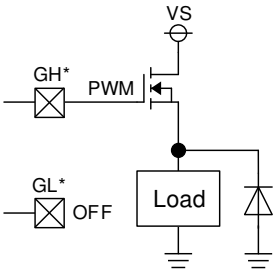


Figure 31. No.4 Mode

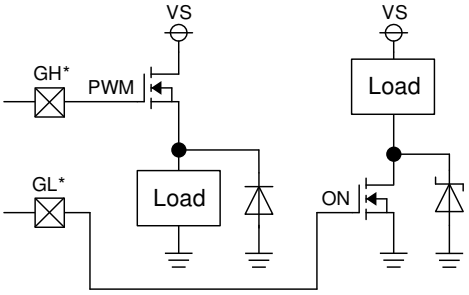


Figure 32. No.5 Mode

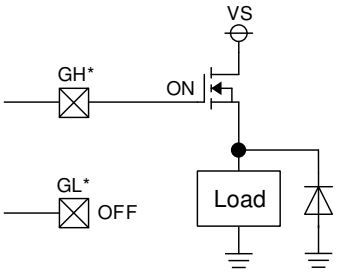


Figure 33. No.6 Mode

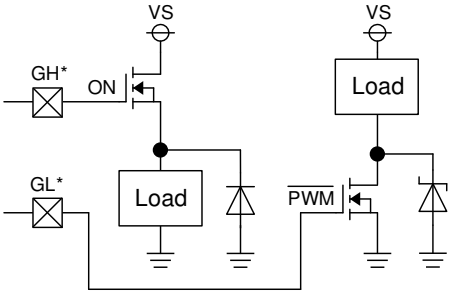


Figure 34. No.7 Mode

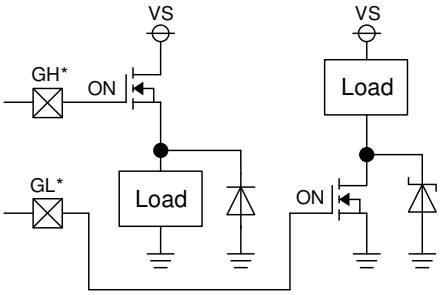


Figure 35. No.8 Mode

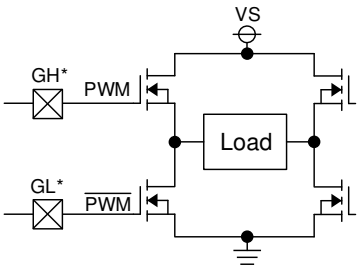


Figure 36. No.9 Mode

Address =03h <Protection Mode Setting>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
03h	R/W	OCPLA_H2	OCPLA_L2	OCPLA_H1	OCPLA_L1	UVLOLA	OVPLA	UVLOM	OVPM
Initial Value	FCh	1	1	1	1	1	1	0	0

Bit[7] : **OCPLA_H2** Mode select of Over Current and Under Voltage Protection (GH2)
0 : Auto recovery
1 : Latch

Bit[6] : **OCPLA_L2** Mode select of Over Current Protection (GL2)
0 : Auto recovery
1 : Latch

Bit[5] : **OCPLA_H1** Mode select of Over Current and Under Voltage Protection (GH1)
0 : Auto recovery
1 : Latch

Bit[4] : **OCPLA_L1** Mode select of Over Current Protection (GL1)
0 : Auto recovery
1 : Latch

Bit[3] : **UVLOLA** Mode select of Under Voltage Lock Out (VS)
0 : Auto recovery
1 : Latch

Bit[2] : **OVPLA** Mode select of Over Voltage Protection (VS)
0 : Auto recovery
1 : Latch

Bit[1] : **UVLOM** Mode select of Under Voltage Protection (VS)
0 : Under Voltage Lock Out is enabled
1 : Under Voltage Lock Out is disabled

Bit[0] : **OVPM** Mode select of Over Voltage Protection (VS)
0 : Over Voltage Protection is enabled
1 : Over Voltage Protection is disabled

Address =04h <Half-Bridge Motor Operating Setting 1>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
04h	R/W	x	x	x	CUR_ SOURCE[4]	CUR_ SOURCE[3]	CUR_ SOURCE[2]	CUR_ SOURCE[1]	CUR_ SOURCE[0]
Initial Value	1Fh	0	0	0	1	1	1	1	1

Bit[4:0]: **CUR_SOURCE** configure source current to control external MOSFET gate slew rate

CUR_SOURCE	Source Current
00000	Drivers off (0mA)
00001	1mA
00010	2mA
…	…
01111	15mA
10000	16mA
10001	17mA
…	…
11110	30mA
11111	31mA

Source current does not include the pull-down current due to the 15 kΩ resistor.

Address =05h <Half-Bridge Motor Operating Setting 2>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
05h	R/W	x	x	x	CUR_ SINK[4]	CUR_ SINK[3]	CUR_ SINK[2]	CUR_ SINK[1]	CUR_ SINK[0]
Initial Value	1Fh	0	0	0	1	1	1	1	1

Bit[4:0]: **CUR_SINK** configure sink current to control external MOSFET gate slew rate

CUR	Sink Current
00000	Drivers off (0mA)
00001	1mA
00010	2mA
…	…
01111	15mA
10000	16mA
10001	17mA
…	…
11110	30mA
11111	31mA

Sink current does not include the pull-down current due to the 15 kΩ resistor.

Address =06h <Half-Bridge Motor Operating Setting 3>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
06h	R/W	x	x	CCPT[5]	CCPT[4]	CCPT[3]	CCPT[2]	CCPT[1]	CCPT[0]
Initial Value	3Fh	0	0	1	1	1	1	1	1

Bit[5:0]: **CCPT** Configure Cross Current Protection Time.

CCPT[5:0]	Cross Current Protection Time
00h	0.25 µs
01h	0.50 µs
02h	0.75 µs
03h	1.00 µs
04h	1.25 µs
05h	1.50 µs
06h	1.75 µs
07h	2.00 µs
08h	2.25 µs
09h	2.50 µs
0Ah	2.75 µs
0Bh	3.00 µs
0Ch	3.25 µs
0Dh	3.50 µs
0Eh	3.75 µs
0Fh	4.00 µs
10h	5.00 µs
11h	6.00 µs
12h	7.00 µs
13h	8.00 µs
14h	9.00 µs
15h	10.00 µs
16h	11.00 µs
17h	12.00 µs
18h	14.00 µs
19h	16.00 µs
1Ah	18.00 µs
1Bh	20.00 µs
1Ch	22.00 µs
1Dh	24.00 µs
1Eh	26.00 µs
1Fh	28.00 µs
20h	30.00 µs
21h	32.00 µs
22h	34.00 µs
23h	36.00 µs
24h	38.00 µs
25h	40.00 µs
26h	42.00 µs
27h	44.00 µs
28h	46.00 µs
29h	48.00 µs
2Ah	50.00 µs
2Bh	52.00 µs
2Ch	54.00 µs
2Dh	56.00 µs
2Eh	58.00 µs
2Fh	60.00 µs
30h	62.00 µs
31h	64.00 µs
32h	66.00 µs
33h	68.00 µs
34h	70.00 µs
35h	72.00 µs
36h	74.00 µs
37h	76.00 µs
38h	78.00 µs
39h	80.00 µs
3Ah	82.00 µs
3Bh	84.00 µs
3Ch	86.00 µs
3Dh	88.00 µs
3Eh	90.00 µs
3Fh	92.00 µs

Address =07h <OCP>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
07h	R/W	x	x	OCPHD[2]	OCPHD[1]	OCPHD[0]	OCPLD[2]	OCPLD[1]	OCPLD[0]
Initial Value	00h	0	0	0	0	0	0	0	0

OCPHD[2:0] Configure OCP of High side
OCPLD[2:0] Configure OCP of Low side

OCPHD/OCPLD	V_{ocp} (mV) (V_{ds})
000	200
001	300
010	400
011	500
100	750
101	1000
110	1250
111	1500

Address =08h <OCP Filter Time Setting >

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
08h	R/W	x	x	OCP_ FILTER[5]	OCP_ FILTER[4]	OCP_ FILTER[3]	OCP_ FILTER[2]	OCP_ FILTER[1]	OCP_ FILTER[0]
Initial Value	00h	0	0	0	0	0	0	0	0

Bits[5:0]: OCP_FILTER configure OCP and DRAIN under voltage protection filter time setting.

OCP_FILTER/UVP_FILTER	Filter Time (t_{ocp_filter})
00h	1µs
01h	2µs
02h	3µs
03h	4µs
04h	5µs
05h	6µs
06h	7µs
07h	8µs
08h	9µs
09h	10µs
0Ah	11µs
0Bh	12µs
0Ch	13µs
0Dh	14µs
…	…
3Eh	63µs
3Fh	64µs

Address =09h <Status Read/Clear Status>

Address	R/W	DATA bit							
		7	6	5	4	3	2	1	0
09h	R	OCP_HS1	OCP_HS2	OCP_LS1	OCP_LS2	x	x	x	x
Initial Value	00h	0	0	0	0	0	0	0	0

Bit[7] : **OCP_HS1**
0 : Normal
1 : Over current detected in H bridge driver channel 1 (Between Drain, SH1 terminal)
Bit[6] : **OCP_HS2**
0 : Normal
1 : Over current detected in H bridge driver channel 2 (Between Drain, SH2 terminal)
Bit[5] : **OCP_LS1**
0 : Normal
1 : Over current detected in H bridge driver channel 1 (Between SH1, SL terminal)
Bit[4] : **OCP_LS2**
0 : Normal
1 : Over current detected in H bridge driver channel 2 (Between SH2, SL terminal)

When DRAIN under voltage protection (UVP) is detected, OCP_HS1 or OCP_HS2 Bit is set. If GH1 is source setting (e.g. figure 33) and GH2 is sink setting, OCP_HS1 bit is changed to 1. If GH1 is sink setting (e.g. figure 30) and GH2 is source setting, OCP_HS2 bit is changed to 1.

Status Read: R/W=1(Note 1): Status bits are read.
Clear Status: R/W=0(Note 1): Status bits are read and then reset to '0'. All of the Global status register bits are also reset to '0'.
Data-bits input during read and write operations are don't care.
The Status Read is possible in EN=0 and EN=1, but the Clear Status is only EN=1, not available in EN=0.
(Note1) please see figure.37 and 38.

Global Status Register:

Bits of this register are defined as follows:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	OCPx	UVLO	OVP	SPI_FAIL	TSD	TW	POR

Bit[6] : **OCPx**
- Logical OR between bits OCP_HS1, OCP_HS2, OCP_LS1, OCP_LS2 and DRAIN under voltage protection

Bit[5] : **UVLO**
0 : Normal
1 : Under voltage Lock Out detection from monitoring VS terminal

Bit[4]: **OVP**
0 : Normal
1 : Over Voltage Protection detection from monitoring VS terminal

Bit[3]: **SPI_FAIL**
Status of last SPI communication; this bit shall be set when the previous SPI command was not accepted by the device because of:
- wrong number of SPI clocks
- wrong address
When a communication error is detected, register settings are unchanged.

Bit[2] : **TSD**
0 : Normal
1 : Thermal Shutdown detection

Bit[1] : **TW**
0 : Normal
1 : Thermal Warning detection

Bit[0] : **POR**
0 : Normal
1 : Power On Reset occurs from monitoring VCC terminal

During each SPI command, the first 8-bit that appear on SO pin after CSB goes 'Low' are the Global status register bits.

Reset Terminal and Command

The chip has several reset sequences as follows.

Reset Sequence	Setting(note 1)	Error flags (note 2)	Counter(note 3)
RSTB = L	Reset	Reset	Reset
VCCPOR	Reset	Reset	Reset
EN register = 0	Hold	Hold	Reset
Software POR	Reset	Reset	Reset

(Note1) All registers with the exception of the Status Read and the Global status.

(Note2)The error flags are the Status Read and the Global status resisters .

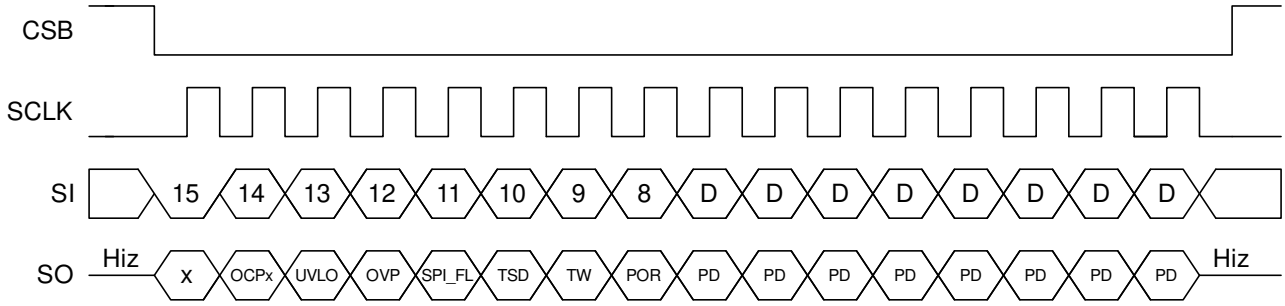
(Note3) This logic block which counts time for Blanking time, filter time and cross current protection time.

Serial Communication:

The serial port is used to write data, read diagnostic status and configure settings of the chip by transferring the data to the desired address. During normal operation an 8-bit serial address followed by 8-bit serial data is written into the 16-bit shift register. The shift register advances on SCLK rising edge. Depending on the address, valid data is conveyed from or to the appropriate register or a command is interpreted. When a read address is latched data is read out from a storage register and shifted out of SO to the microcontroller.

Write Register

The write register protocol is shown below. For input pins we use CSB, SCLK and SI. When CSB is Low, data is accepted. Data (SI) is latched at the rising edge of the clock (SCLK) and sent to the register after 16-bit command is completely received. For write operation, the highest rank bit (MSB) must be Low. The next 7 bits are address settings, the 8 lowest bits are data. On SO, after CSB goes Low, the first 8-bits shifted out during send operation are the Global status register bits and the next 8-bits are the values of the register.

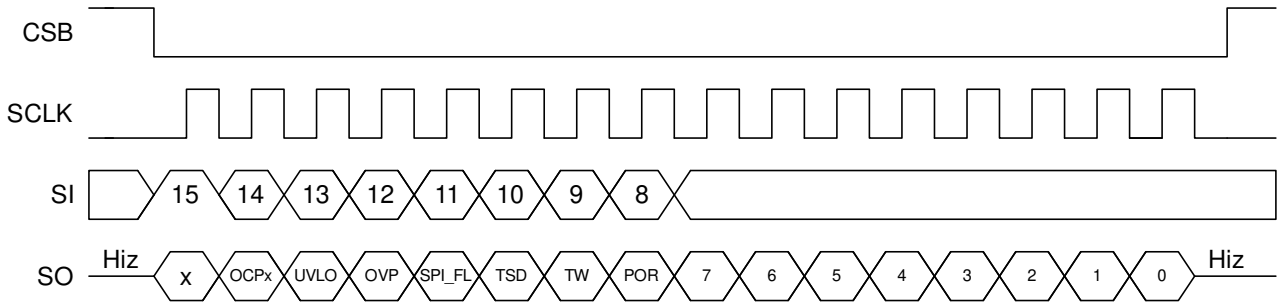


D : Data to be written in registers addressed by bits 14:8
PD: Previous data in the registers addressed by bits 14:8

Figure 37. Register Write Protocol

Read Register

Reading–out from the registers is shown below. For read operation, the highest rank bit (MSB) must be High. After that, the 7 bits address is send followed by 8 data bits (data value is ‘don’t care’). The first 8-bits shifted out on SO during send operation are the Global status register bits and the next 8-bits shifted out are the values of the register addressed.



X : don't care

Figure 38. Register Read-Out Protocol

SPI Timing Chart

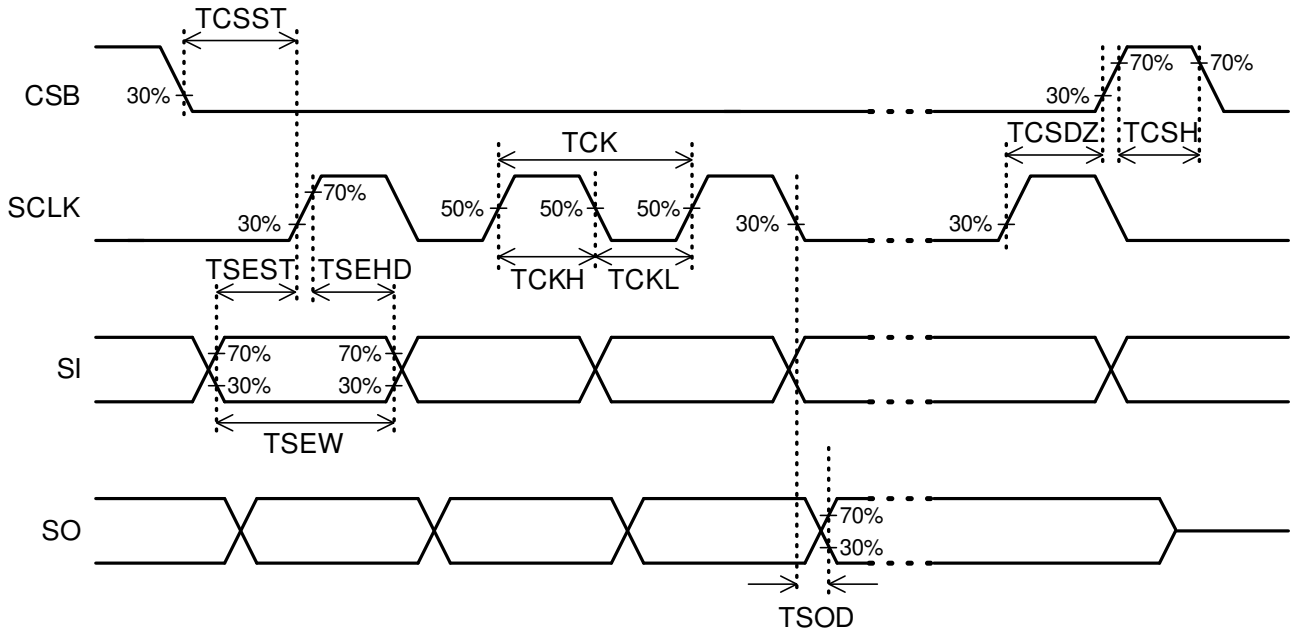


Figure 39. SPI Timing Diagram

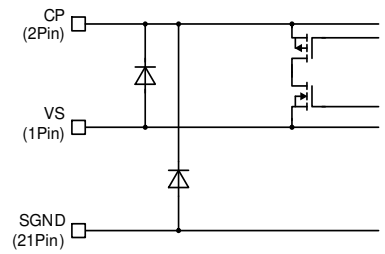
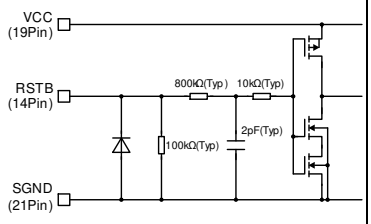
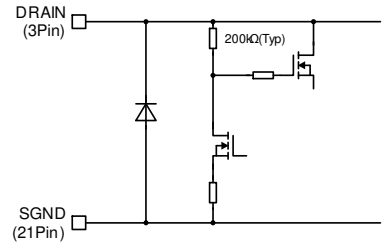
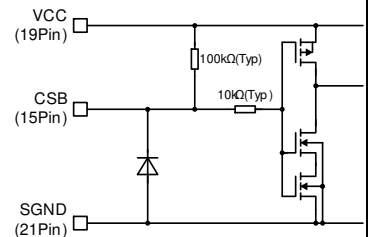
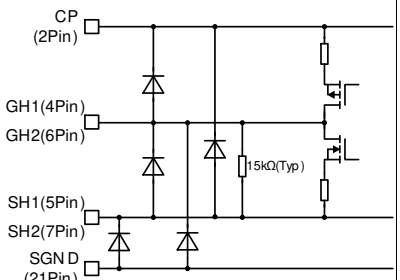
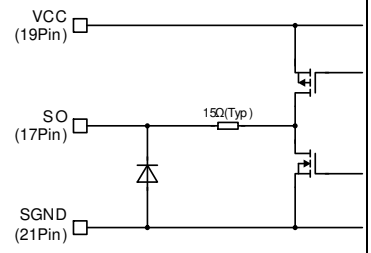
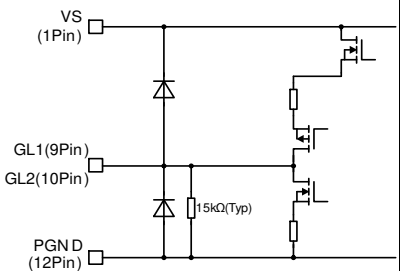
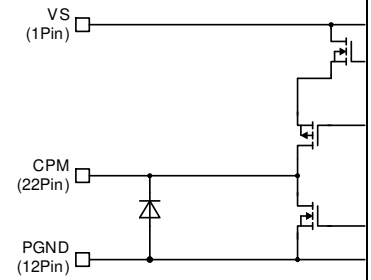
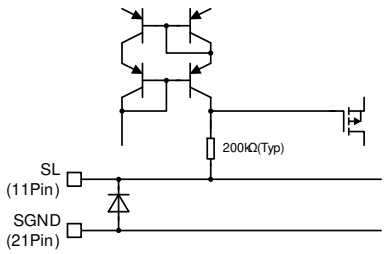
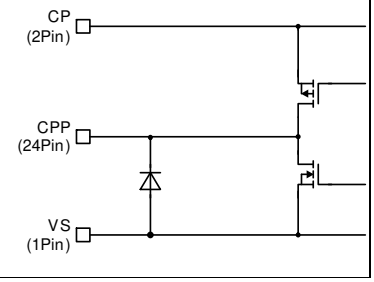
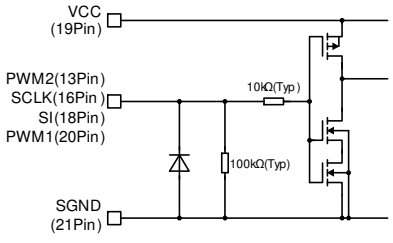
I/O SIGNAL's TIMING RULE (-40°C ≤ Tj ≤+150°C VCC=3.0 to 5.5V)

Parameter	Symbol	Min	Max	Unit
SCLK Period	TCK	142	-	ns
SCLK High Pulse Width	TCKH	65	-	ns
SCLK Low Pulse Width	TCKL	65	-	ns
SI High and Low Pulse Width	TSEW	135	-	ns
SI Setup Time Prior to SCLK Rise	TSEST	55	-	ns
SI Hold Time After SCLK Rise	TSEHD	55	-	ns
CSB High Pulse Width	TCSH	2	-	µs
CSB Setup Time	TCSST	50	-	ns
SCLK Rise Edge to CSB Rise Edge	TCSDZ	120	-	ns
SO Delay Time	TSOD	-	60	ns

I/O signal's timing diagram shows the absolute minimal timing and the SO output signal's maximum delay time

The timings are valid for a 7MHz clock signal. The input High Going threshold voltage (V_{TH}) is 0.7x VCC on the rising edge and (V_{TH}) 0.3x VCC on the falling edge for all digital pins. See electrical characteristics on page 8.

I/O Equivalence Circuit

Pin No.	Pin name	Equivalence circuit	Pin No.	Pin name	Equivalence circuit
2	CP		14	RSTB	
3	DRAIN		15	CSB	
4 5 6 7	GH1 SH1 GH2 SH2		17	SO	
9 10	GL1 GL2		22	CPM	
11	SL		24	CPP	
13 16 18 20	PWM2 SCLK SI PWM1				

Resistance values shown in the diagrams above represent a typical limit, respectively

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

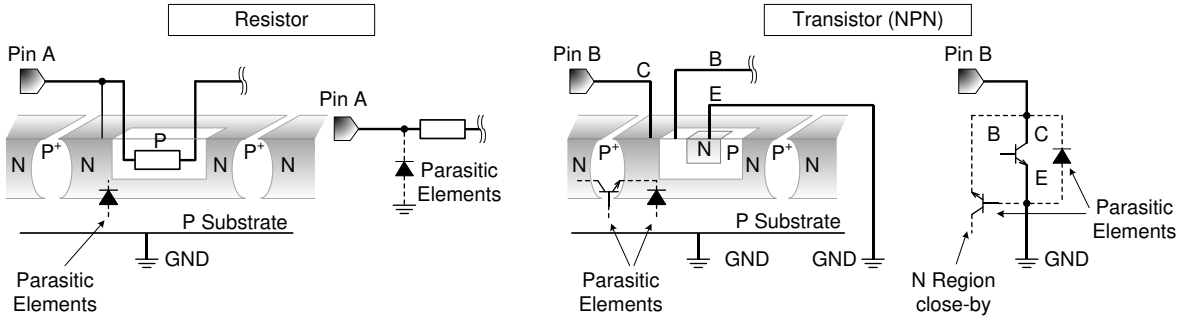


Figure 40. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

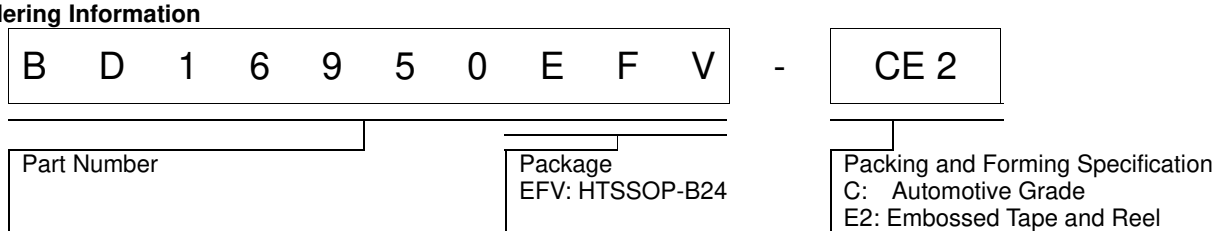
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.

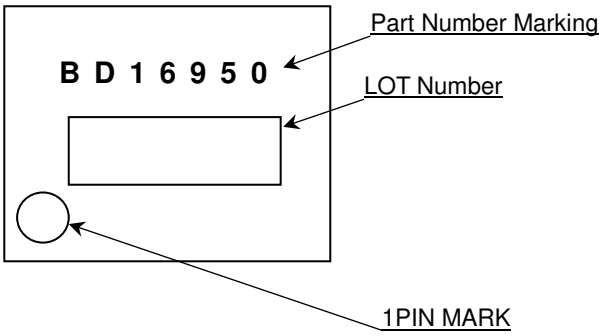
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information



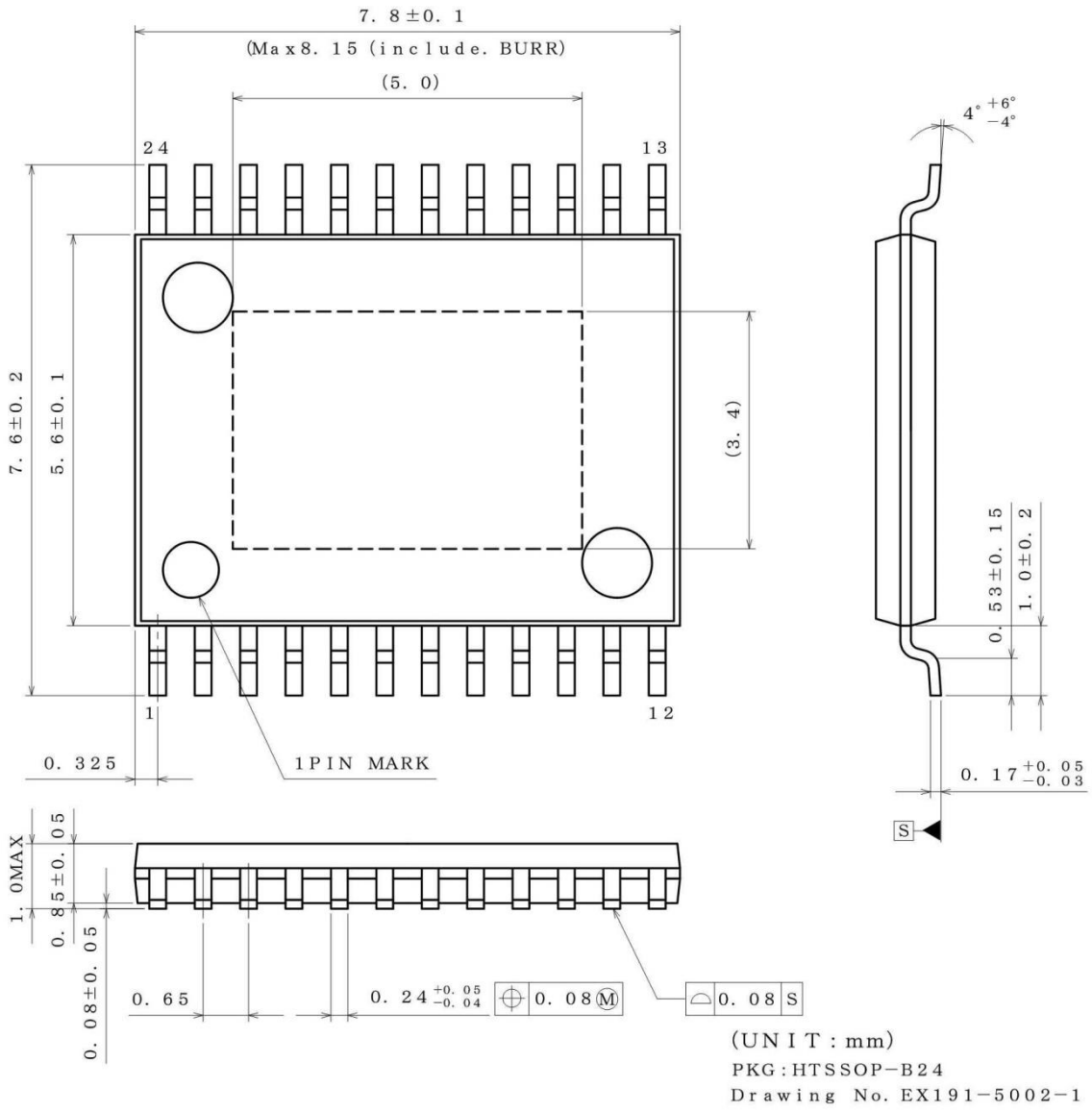
Marking Diagrams

HTSSOP-B24 (TOP VIEW)



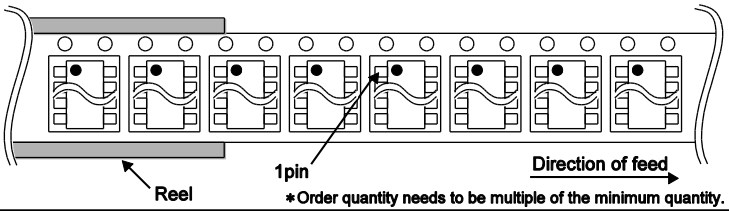
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
01-Mar-2017	001	New release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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