

# BLF7G10L-250; BLF7G10LS-250

Power LDMOS transistor

Rev. 6 — 7 November 2016

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

250 W LDMOS power transistor for base station applications at frequencies from 869 MHz to 960 MHz.

**Table 1. Typical performance**

Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing = 5 MHz. Typical RF performance at  $T_{case} = 25\text{ }^{\circ}\text{C}$ .

Test signal	f (MHz)	I <sub>Dq</sub> (mA)	V <sub>DS</sub> (V)	P <sub>L(AV)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	ACPR (dBc)
2-carrier W-CDMA	869 to 894 <a href="#">[1]</a>	1800	30	60	19.5	27.4	-35.6
2-carrier W-CDMA	920 to 960 <a href="#">[2]</a>	1800	30	60	19.5	30.5	-34

[1] In a common source class-AB application test circuit.

[2] In a common source class-AB production test circuit.

### 1.2 Features and benefits

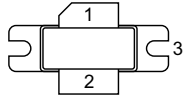
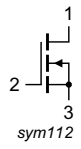
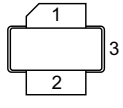
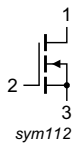
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (869 MHz to 960 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use (input and output)
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 869 MHz to 960 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF7G10L-250 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <span style="color: blue;">[1]</span>		
<b>BLF7G10LS-250 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <span style="color: blue;">[1]</span>		

[1] Connected to flange

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G10L-250	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF7G10LS-250	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$ ; $P_L = 60\text{ W (CW)}$ ; $V_{DS} = 30\text{ V}$ ; $I_{Dq} = 1800\text{ mA}$	0.38	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 3.3\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 330\text{ A}$	1.50	1.9	2.30	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 30\text{ V}; I_D = 1.8\text{ A}$	1.63	2.03	2.43	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	5	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	56	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	0.5	mA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 11.55\text{ A}$	-	22	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 11.55\text{ A}$	-	57	-	m $\Omega$

**Table 7. RF characteristics**

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH;  $f_1 = 920\text{ MHz}; f_2 = 925\text{ MHz}; f_3 = 955\text{ MHz}; f_4 = 960\text{ MHz}$ ; RF performance at  $V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 60\text{ W}$	18.5	19.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 60\text{ W}$	-	-15.5	-10	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 60\text{ W}$	27	30.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 60\text{ W}$	-	-34	-31	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF7G10L-250 and BLF7G10LS-250 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}; P_L = 200\text{ W (CW)}; f = 920\text{ MHz to }960\text{ MHz}$ .

### 7.2 Impedance information

**Table 8. Typical impedance information**

$I_{Dq} = 1800\text{ mA}$ ; main transistor  $V_{DS} = 30\text{ V}$ .  $Z_S$  and  $Z_L$  defined in [Figure 1](#).

f	$Z_S$	$Z_L$
(MHz)	( $\Omega$ )	( $\Omega$ )
925	3.1 – j3.3	1.0 – j1.7
942	3.2 – j3.3	1.0 – j1.6
960	3.4 – j3.5	0.9 – j1.4

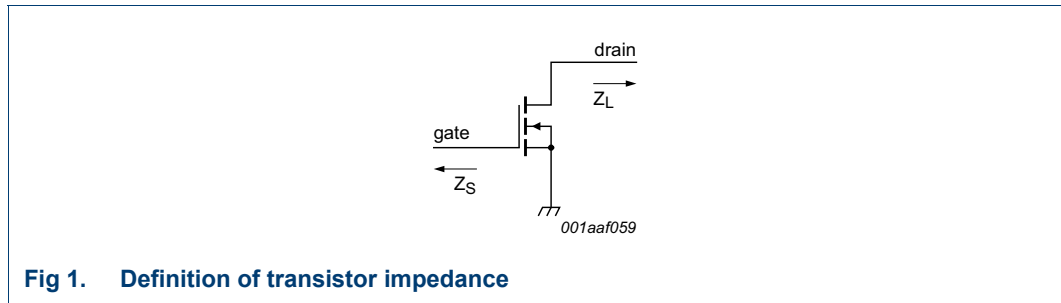


Fig 1. Definition of transistor impedance

### 7.3 Circuit

The figure shows two PCB layout diagrams. The left diagram shows the top layer with components C7, C8, C2, C1, C9, C10, and C3. The right diagram shows the bottom layer with components C5, C11, C12, C15, C4, C6, C13, C14, and C16. The transistor is labeled 'BLF7G10L(S)-250' and the reference number 'aaa-001570' is at the bottom right.

Printed-Circuit Board (PCB): Rogers RO3006;  $\epsilon_r = 6.15$  F/m; thickness = 0.635 mm; thickness copper plating = 35  $\mu\text{m}$ .  
 The vias can be used as a reference to place components.  
 The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be provided.  
 See [Table 9](#) for list of components.

Fig 2. Component layout

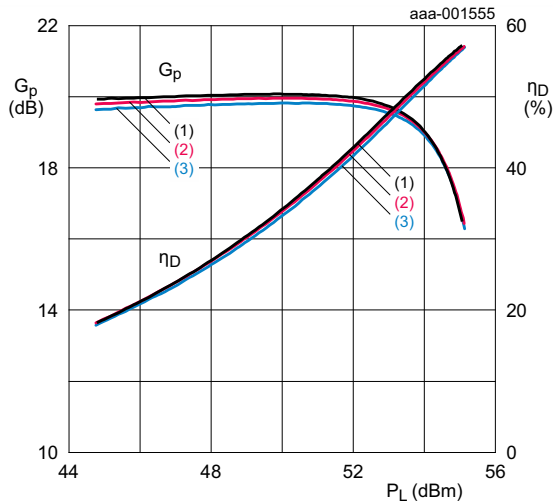
Table 9. List of components

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	82 pF	ATC800B
C7, C9, C12, C14	multilayer ceramic chip capacitor	10 $\mu\text{F}$	Murata
C8, C10, C11, C13	multilayer ceramic chip capacitor	1 $\mu\text{F}$	Murata
C15, C16	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	

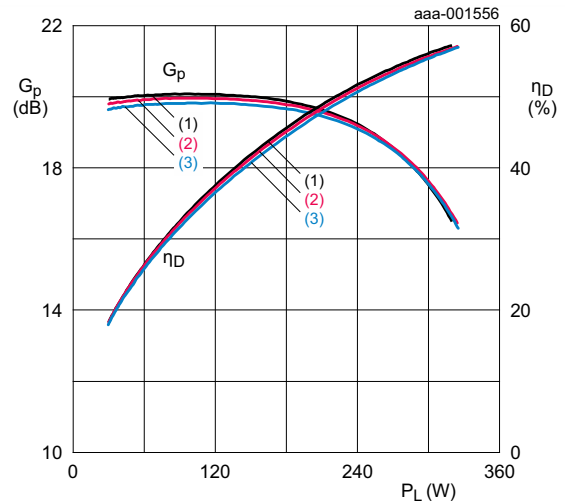
7.4 Graphs

7.4.1 CW pulsed



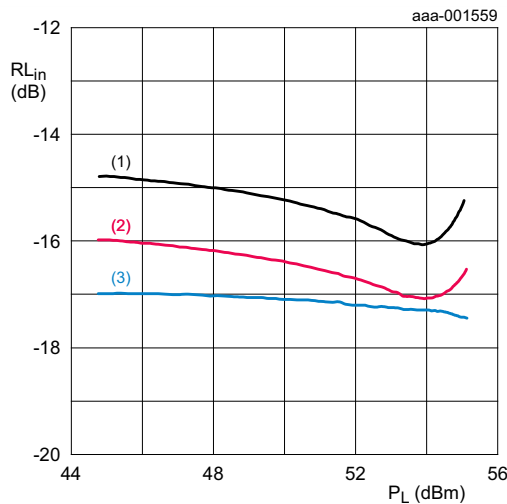
$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}$ .  
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

**Fig 3. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}$ .  
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

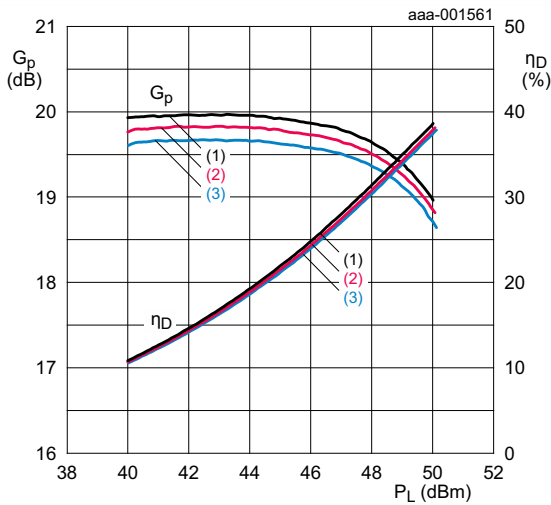
**Fig 4. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}$ .  
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

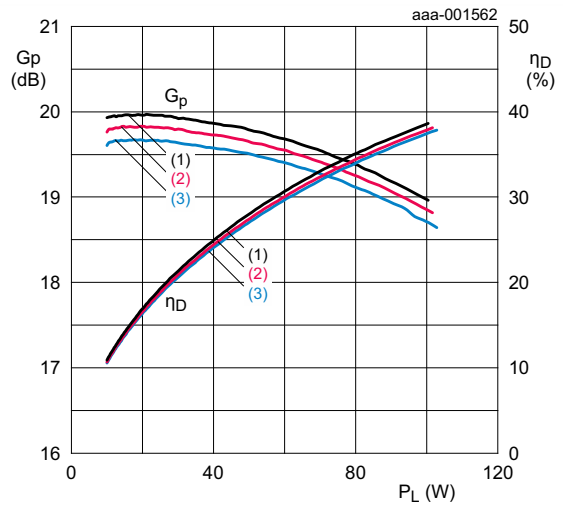
**Fig 5. Input return loss as a function of output power; typical values**

7.4.2 2-Carrier W-CDMA



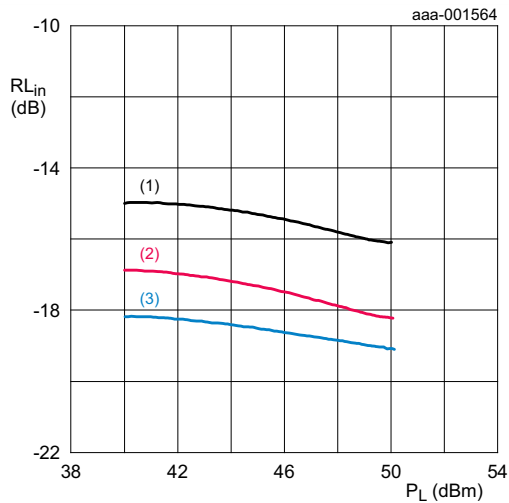
$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}.$   
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

**Fig 6. Power gain and drain efficiency as function of output power; typical values**



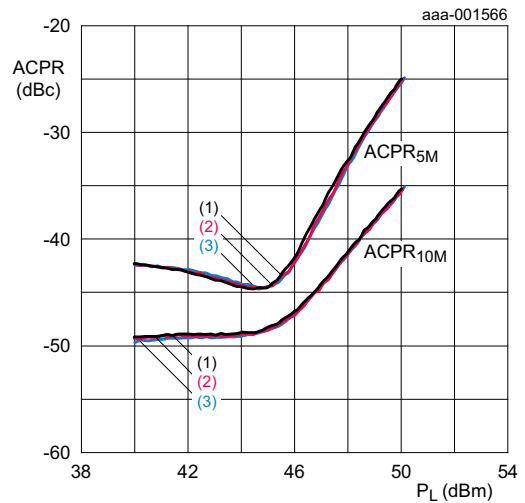
$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}.$   
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

**Fig 7. Power gain and drain efficiency as function of output power; typical values**



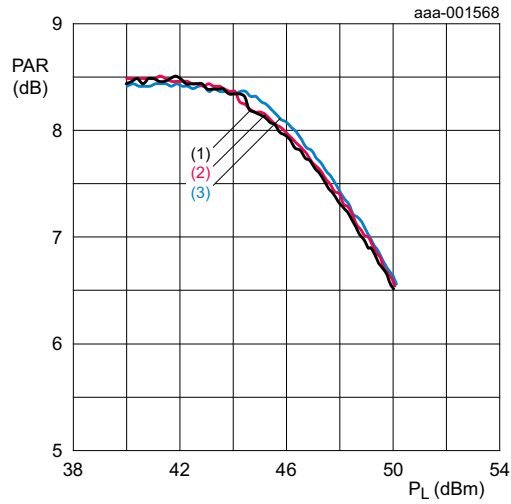
$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}.$   
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

**Fig 8. Input return loss as a function of output power; typical values**



$V_{DS} = 30\text{ V}; I_{Dq} = 1800\text{ mA}.$   
 (1)  $f = 920\text{ MHz}$   
 (2)  $f = 940\text{ MHz}$   
 (3)  $f = 960\text{ MHz}$

**Fig 9. Adjacent channel power ratio (5 MHz and 10 MHz) as function of output power; typical values**



$V_{DS} = 30\text{ V}$ ;  $I_{Dq} = 1800\text{ mA}$ .

- (1)  $f = 920\text{ MHz}$
- (2)  $f = 940\text{ MHz}$
- (3)  $f = 960\text{ MHz}$

**Fig 10. Peak-to-average ratio as a function of output power; typical values**

### 8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

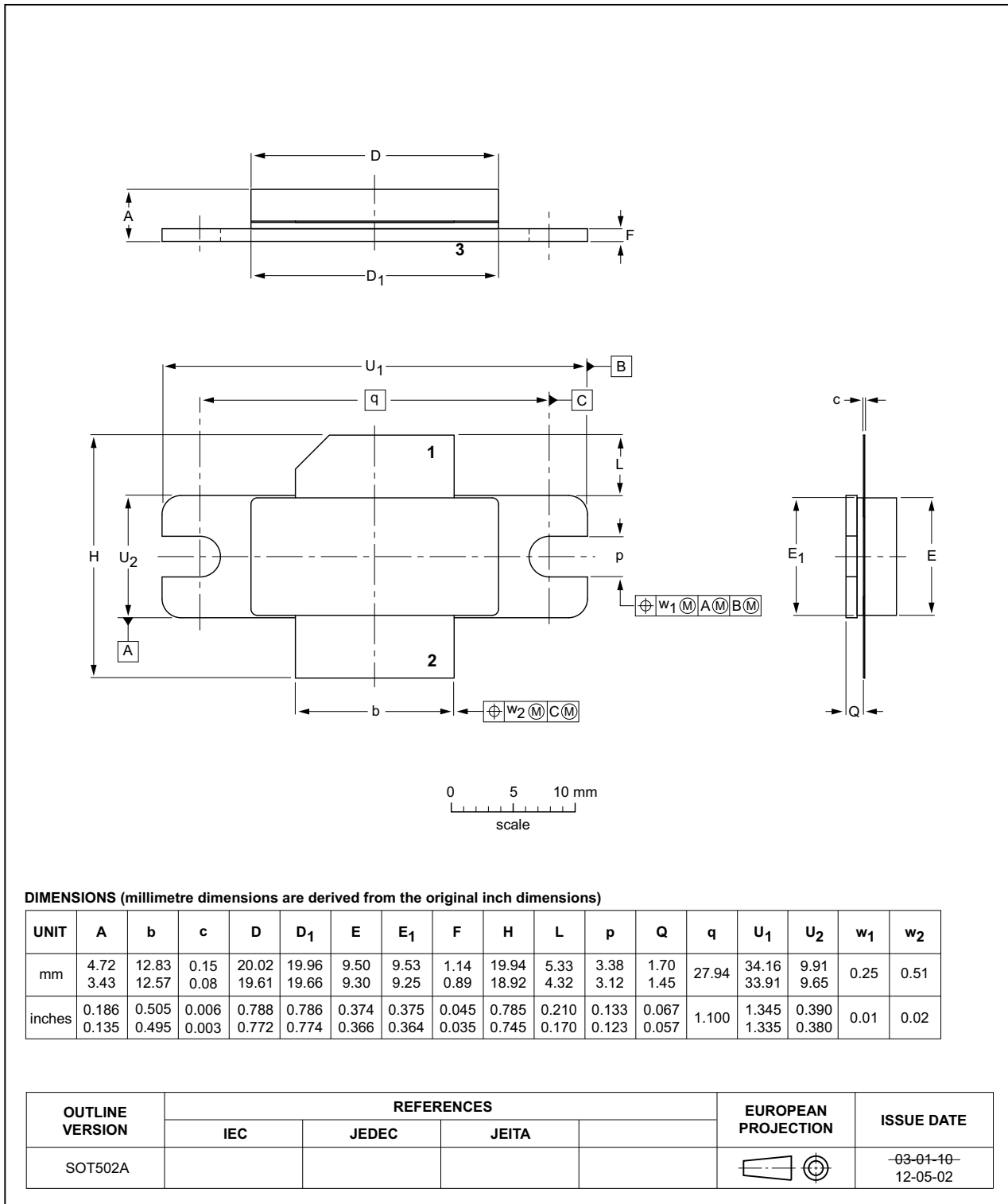


Fig 11. Package outline SOT502A



Earless flanged ceramic package; 2 leads

SOT502B

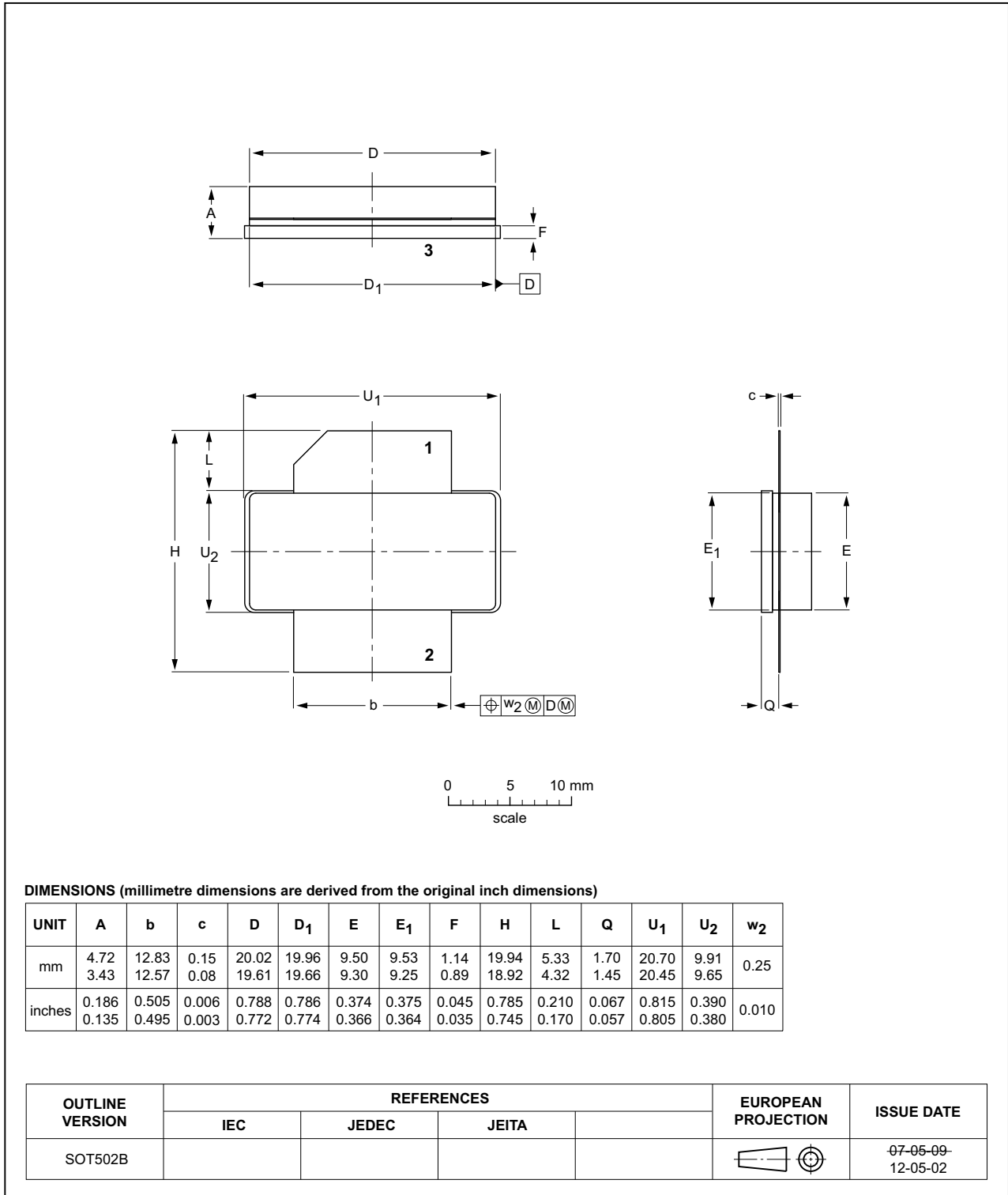


Fig 12. Package outline SOT502B

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G10L-250_7G10LS-250 v.6	20161107	Product data sheet	-	BLF7G10L-250_7G10LS-250 v.5
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 6 on page 3</a>: added <math>V_{GSq}</math> parameter to table</li> </ul>			
BLF7G10L-250_7G10LS-250 v.5	20150901	Product data sheet	-	BLF7G10L-250_7G10LS-250 v.4
BLF7G10L-250_7G10LS-250 v.4	20120913	Product data sheet	-	BLF7G10L-250_7G10LS-250 v.3
BLF7G10L-250_7G10LS-250 v.3	20120216	Product data sheet	-	BLF7G10L-250_7G10LS-250 v.2
BLF7G10L-250_7G10LS-250 v.2	20111114	Preliminary data sheet	-	BLF7G10L-250_7G10LS-250 v.1
BLF7G10L-250_7G10LS-250 v.1	20110225	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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