19-1614; Rev 0; 6/00

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

SiGe, Variable IIP3, Low-Noise Amplifier in UCSP Package

General Description

The MAX2374 silicon-germanium (SiGe), switchable-gain, variable-linearity, low-noise amplifier (LNA) is designed for cellular-band, code-division multiple-access (CDMA). It can be used for applications such as TDMA and PDC or wherever high dynamic range and low noise are required. This LNA provides a high intermodulation intercept point (IIP3), which is adjustable to meet specific system requirements by selecting an appropriate external resistor. To achieve high gain and low noise, the LNA is packaged in a tiny ultra-chip-scale package (UCSP) with six solder bumps. The LNA operates from a +2.7V to +5.5V single supply and consumes just 8.5mA while achieving a +6.2dBm input IIP3. Supply current reduces to less than 1µA in shutdown mode.

The MAX2374 provides two gain modes. High-gain mode optimizes system sensitivity, while low-gain mode optimizes system linearity.

Applications

CDMA Phones

TDMA Phones

Wireless Local Loop (WLL)

GSM Handsets

Land Mobile Radio

Wireless Data

Pin Configuration appears at end of data sheet.

Features

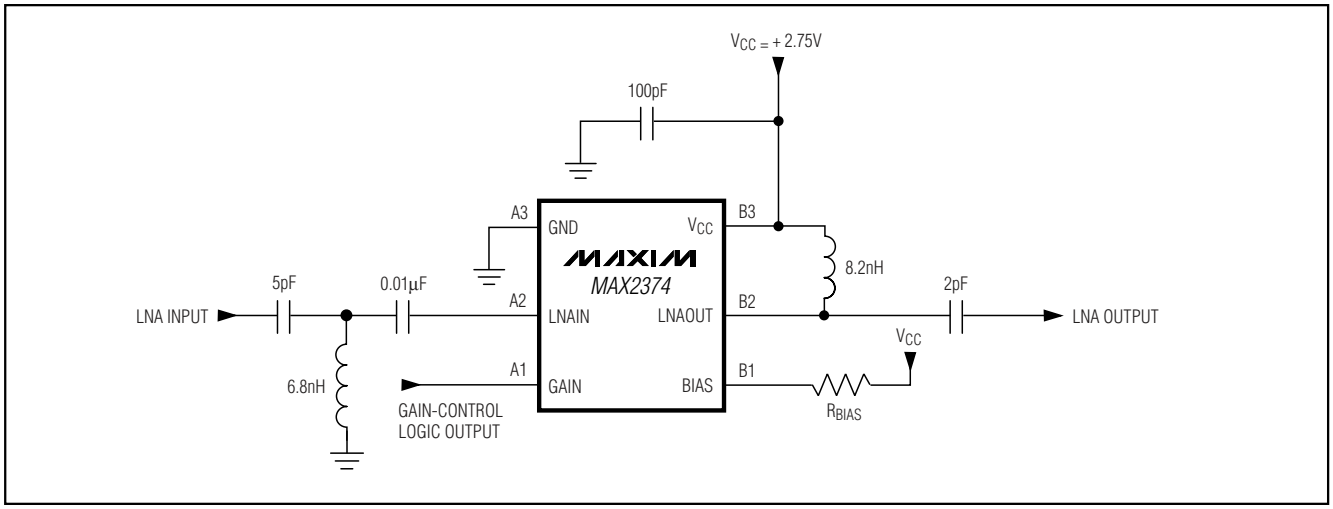
- **+2.7V to +5.5V Single Supply**
- **Low Operating Current**
  - **8.5mA for High Linearity**
  - **4.5mA for Paging**
  - **4.1mA in Low-Gain, High-Linearity Mode**
- **Low Noise Figure: 1.5dB Cellular**
- **Adjustable IIP3**
- **Two Gain Settings**
- **< 1µA Shutdown Mode**
- **Ultra-Small 6-Bump UCSP (1mm x 1.5mm)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX2374EBT	-40°C to +85°C	6 UCSP*	AAB

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

Typical Application Circuit



SiGe, Variable IIP3, Low-Noise Amplifier in UCSP Package

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
GAIN, BIAS Voltage to GND.....-0.3V to (V_{CC} + 0.3V)
GAIN, BIAS Current .....±10mA
RF Input Power
LNAIN .....+10dBm
LNAOUT to GND .....-0.3V to (V_{CC} + 0.6V)
Continuous Power Dissipation (T_A = +85°C) 540mW
Operating Temperature Range
MAX2374 .....-40°C to +85°C
Storage Temperature.....-65°C to +150°C
Junction Temperature .....+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, R_{BIAS} = 20kΩ, V_{GAIN} = high, LNAOUT = V_{CC}, no input signals at LNAIN, T_A = -40°C to +85°C. Typical values are at V_{CC} = +2.75V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Voltage		2.7		5.5	V
Supply Current	V_{CC} = 2.75V		8.5	10.5	mA
	V_{CC} = 5.5V		10.5		
	R_{BIAS} = 10kΩ		15		
	R_{BIAS} = 43kΩ		4.5		
	GAIN = 0.6V, V_{CC} = 2.75V		4.5	5.5	
Shutdown Supply Current	BIAS = open circuit		0.1	1	µA
GAIN CONTROL INPUT					
Input Logic Voltage High		1.5			V
Input Logic Voltage Low				0.6	V
Input Current		-5		5	µA
BIAS Pin Voltage (Note 2)			V_{CC} - 1.16		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = +2.7V to +5.5V, P_{LNAIN} = -30dBm, V_{GAIN} = high, f_{LNAIN} = 881MHz, R_{BIAS} = 20kΩ, T_A = +25°C. Typical values are at V_{CC} = +2.75V, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Recommended Operating Frequency Range (Note 3)			750		1000	MHz
Input and Output Return Loss	Input and output ports externally matched to 50Ω			14		dB
Reverse Isolation	V_{GAIN} = high			-20		dB
	V_{GAIN} = low			-9		
Output 1dB Compression	V_{CC} = 2.75V	V_{GAIN} = high		6		dBm
		V_{GAIN} = low		-3.5		
Maximum Stable Load VSWR	All modes, f ≤ 6.5GHz		10:1			

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = +2.7V to +5.5V, P_{LNAIN} = -30dBm, V_{GAIN} = high, f_{LNAIN} = 881MHz, R_{BIAS} = 18kΩ, T_A = +25°C. Typical values are at V_{CC} = +2.75V, unless otherwise noted.) (Note 2)

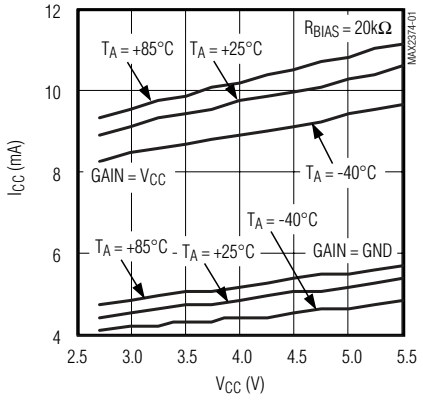
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
HIGH-GAIN MODE (GAIN = V_{CC})						
Gain	T_A = +25°C		13.8	15	15.6	dB
	T_A = -40°C to +85°C		12.5		17	
Noise Figure	V_{CC} = 2.75V			1.5	1.7	dB
Input Third-Order Intercept Point (Note 4)	MAX2374	R_{BIAS} = 10kΩ		7.2		dBm
		R_{BIAS} = 20kΩ	4.5	6.2		
		R_{BIAS} = 43kΩ		4.2		
LOW-GAIN MODE (GAIN = GND)						
Gain	T_A = -40°C to +85°C	T_A = +25°C	0.4	1.2	2	dB
		T_A = -40°C to +85°C	-1		3.5	
Noise Figure				3	3.5	dB
Input Third-Order Intercept Point (Note 4)	MAX2374	R_{BIAS} = 10kΩ		10.5		dBm
		R_{BIAS} = 20kΩ	5.8	7.2		
		R_{BIAS} = 43kΩ		1		

Note 1: Production tested at T_A = +25°C. Maximum and minimum limits are guaranteed by design and characterization.
Note 2: Guaranteed by design and characterization.
Note 3: Operation over this frequency range is possible with a matching network tuned to the desired operating frequency.
Note 4: Measured with two-tone test with P_{LNAIN} = -25dBm per tone, f1 = 881MHz, f2 = 881.9MHz.

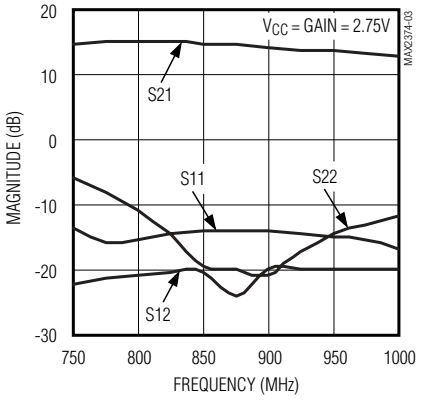
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CC} = +2.7V to +5.5V, P_{LNAIN} = -30dBm, f_{LNAIN} = 881MHz, R_{BIAS} = 20kΩ, T_A = +25°C, unless otherwise noted.)

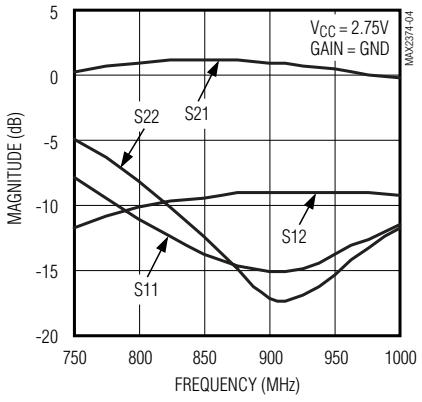
ICC vs. VCC AND TEMPERATURE



S21, S11, S22, S12 vs. FREQUENCY



S21, S11, S22, S12 vs. FREQUENCY

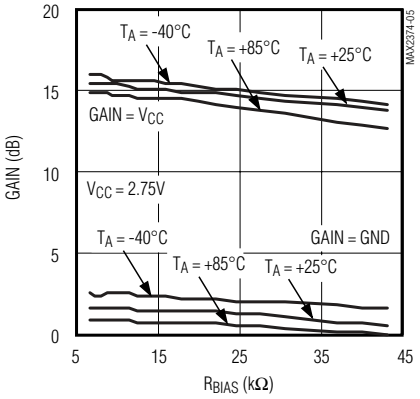


SiGe, Variable IIP3, Low-Noise Amplifier in UCSP Package

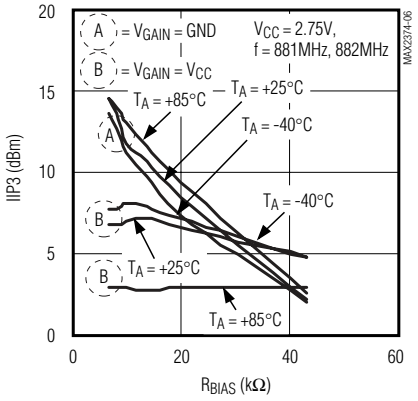
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = +2.7V to +5.5V, P_{LNAIN} = -30dBm, f_{LNAIN} = 881MHz, R_{BIAS} = 20kΩ, T_A = +25°C, unless otherwise noted.)

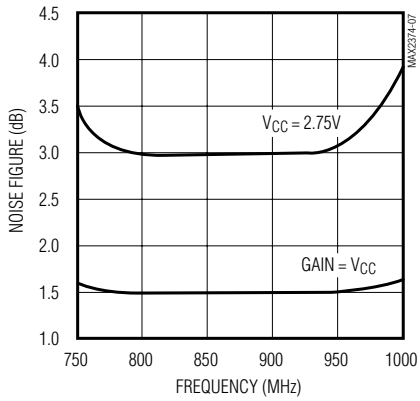
GAIN vs. R_{BIAS} AND TEMPERATURE



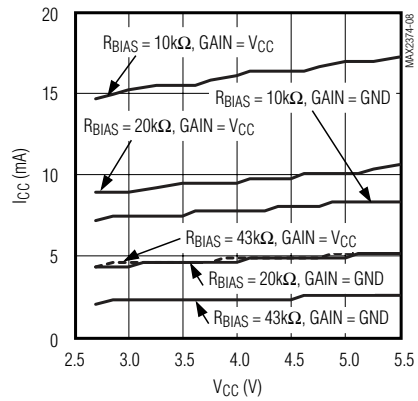
IIP3 vs. R_{BIAS} AND TEMPERATURE



NOISE FIGURE vs. FREQUENCY



CURRENT vs. VOLTAGE AND R_{BIAS}



Pin Description

PIN	NAME	FUNCTION
A3	GND	Ground
A2	LNAIN	LNA Input Port. Blocking capacitor is required, which may be used as part of the matching network.
A1	GAIN	Gain-Control Logic Input. Drive high for high-gain mode. Drive low for low-gain mode.
B1	BIAS	LNA Bias Setting Pin. For nominal bias, connect 20kΩ resistor to V_{CC}. Adjust the resistor value to alter the linearity of the LNA.
B2	LNAOUT	LNA Output Port. This port requires an external pullup inductor, which may be used as part of the matching network.
B3	V_{CC}	Supply Voltage Input. Bypass with a 100pF capacitor to GND.

Table 1a. S-Parameters (V_{CC} = V_{GAIN} = 2.75V)

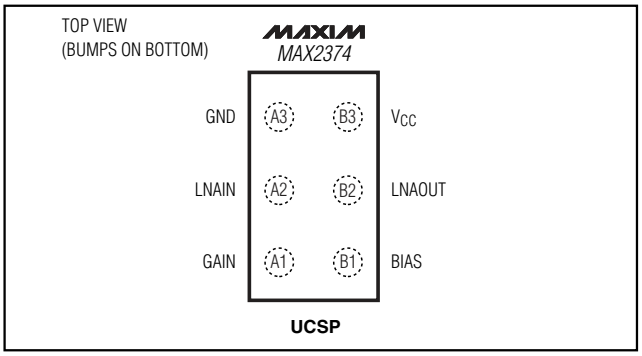
FREQ (MHz)	S11		S21		S12		S22	
	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE
50	0.929	-11.89	12.84	-151.3	0.007	123.5	0.908	78.8
250	0.728	-49	9.83	122.73	0.026	69	0.842	-20.2
500	0.571	-77.5	6.19	79.42	0.041	47.6	0.728	-54.8
750	0.524	-101	4.21	49.35	0.053	33.3	0.68	-81
1000	0.529	-123.7	3.12	24.18	0.06	21	0.671	-105
1250	0.568	-145.2	2.38	1	0.063	11.19	0.68	-128
1500	0.612	-165	1.77	-19.2	0.057	5.042	0.704	-150
1750	0.639	176	1.46	-35	0.061	15	0.732	-171
2000	0.652	163	1.07	-51	0.094	17	0.697	162
2250	0.664	149	1.01	-60.5	0.161	-12.9	0.626	158.7
2500	0.691	139	0.892	-77	0.1	-45.4	0.689	146.5
2750	0.716	125	0.781	-91.7	0.078	-37	0.693	128
3000	0.72	111.5	0.662	-104	0.074	-33.3	0.686	110

Table 1b. S-Parameters (V_{CC} = 2.75V, V_{GAIN} = GND)

FREQ (MHz)	S11		S21		S12		S22	
	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE	MAGNITUDE	ANGLE
50	0.987	-8.93	1.25	-148.7	0.01	127	0.374	85.8
250	0.916	-42.4	1.21	128.8	0.06	85.7	0.471	1.23
500	0.8	-77	1	72.4	0.14	52.2	0.596	-42
750	0.75	-106	0.772	28.18	0.189	19.6	0.659	-82
1000	0.754	-132.7	0.583	-6.87	0.2	-9.33	0.689	-117.3
1250	0.782	-158	0.429	-34.5	0.184	-30.7	0.694	-147.5
1500	0.803	180	0.301	-54	0.146	-47	0.695	-173
1750	0.811	159.5	0.228	-66	0.117	-53.4	0.681	164.6
2000	0.797	141.5	0.148	-66	0.096	-42.5	0.629	141.7
2250	0.739	126.3	0.196	-62	0.175	-47	0.534	140
2500	0.745	112	0.156	-89	0.123	-77.2	0.623	126.35
2750	0.701	92.4	0.096	-83	0.082	-63.3	0.6	103.2
3000	0.591	73	0.112	-73.48	0.103	-62.8	0.566	85.8

SiGe, Variable IIP3, Low-Noise Amplifier in UCSP Package

Pin Configuration



Detailed Description

The MAX2374 SiGe LNA is packaged in a UCSP package in order to deliver high gain, high linearity, and low noise in the smallest package possible. The special feature of this LNA is that its linearity is adjusted by an external resistor, R_{BIAS}. The LNA has two digitally controllable gain modes to increase system dynamic range. Digital high at GAIN selects the high-gain mode, and digital low selects the low-gain mode.

Adjust the LNA bias current to control the amplifier's linearity. The resistor R_{BIAS} connected between BIAS and V_{CC} controls the LNA current. The amplifier's linearity is directly related to the operating current. Increasing the bias current of the LNA increases the IIP3. V_{BIAS} is approximately constant at V_{CC} - 1.16V. Connecting a resistor from BIAS to V_{CC} results in a supply current that can be calculated as follows:

$$V_{CC} = (\text{High Gain}) \simeq (150 - 1.16V) / R_{BIAS}$$

I_{BIAS} can be set by a fixed resistor to V_{CC} as described above, or it can be generated with a switched network.

To operate the LNA in high-gain/high-linearity mode, set R_{BIAS} = 20kΩ and drive GAIN high. Do this in the presence of a transmit signal to minimize cross-modulation. To operate the LNA in low-gain/low-linearity mode, set R_{BIAS} = 43kΩ and drive GAIN high. This mode draws less current and should be used in the absence of a transmit signal (paging mode). Shutdown of the IC is accomplished by switching R_{BIAS} to open circuit.

Layout Issues

Design the layout for the IC to be as compact as possible to minimize the parasitics. The chip-scale IC package uses a bump pitch of 0.5mm (19.7mil) and bump diameter of 0.3mm (~12mil). Therefore, lay out the solder-pad spacing on 0.5mm (19.7mil) centers, using a pad size of 0.25mm (~10mil) and a solder mask opening of 0.33mm (13mil). Round or square pads are permissible. Connect multiple vias from the ground plane as close to the ground pins as possible.

Install capacitors as close as possible to the IC supply voltage pin and supply end of the series inductor. Place the ground end of these capacitors near the IC GND pins to provide a low-impedance return path for the signal current.

Prototype Chip Installation

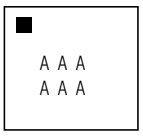
Alignment keys on the PC board around the area where the chip is located will be helpful in the prototype assembly process. It is better to align the chip on the board before any other components are placed, and then place the board on a hot plate or hot surface until the solder starts melting. Remove the board from the hot plate without disturbing the position of the chip, and let it cool down to room temperature before processing the board further.

UCSP Reliability

The ultra-chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally well as a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package.

Performance through operating-life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for UCSP packages. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged product lead frame. Solder joint contact integrity must be considered. Comprehensive reliability tests have been performed and are available upon request. In conclusion, the UCSP performs reliably through environmental stresses.

Marking Information



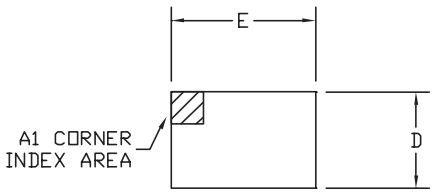
ORIENTATION
PRODUCT ID CODE
LOT CODE

Chip Information

TRANSISTOR COUNT: 296

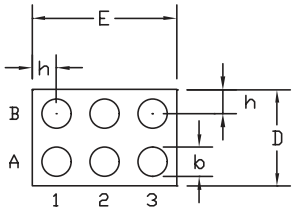
Package Information

6L,UCSP.EPS

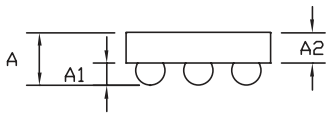


TOP VIEW

SYMBOL	DIMENSIONS
A	0.022 ±.002
D	0.040 ±.002
E	0.059 ±.002
e	0.0197 BASIC
b	ø 0.0120 BASIC
A1	0.009±.0015
A2	0.013 Ref.
h	0.010 Ref.



BOTTOM VIEW



SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. MEETS JEDEC MO195.

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 6L UCSP, 3x2

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0097	A	1/1

NOTES