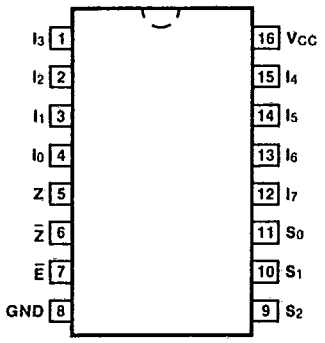
T-66-21-53

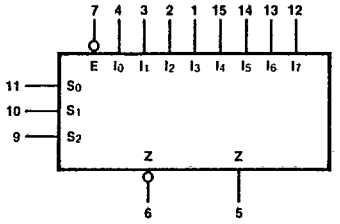
54/74151A
54S/74S151
54LS/74LS151
8-INPUT MULTIPLEXER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '151 is a high speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The '151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74151APC, 74S151PC 74LS151PC		9B
Ceramic DIP (D)	A	74151ADC, 74S151DC 74LS151DC	54151ADM, 54S151DM 54LS151DM	6B
Flatpak (F)	A	74151AFC, 74S151FC 74LS151FC	54151AFM, 54S151FM 54LS151FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I0 — I7	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
S0 — S2	Select Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Ē	Enable Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
Z	Data Output	20/10	25/12.5	10/5.0 (2.5)
Z̄	Inverted Data Output	20/10	25/12.5	10/5.0 (2.5)

FUNCTIONAL DESCRIPTION — The '151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

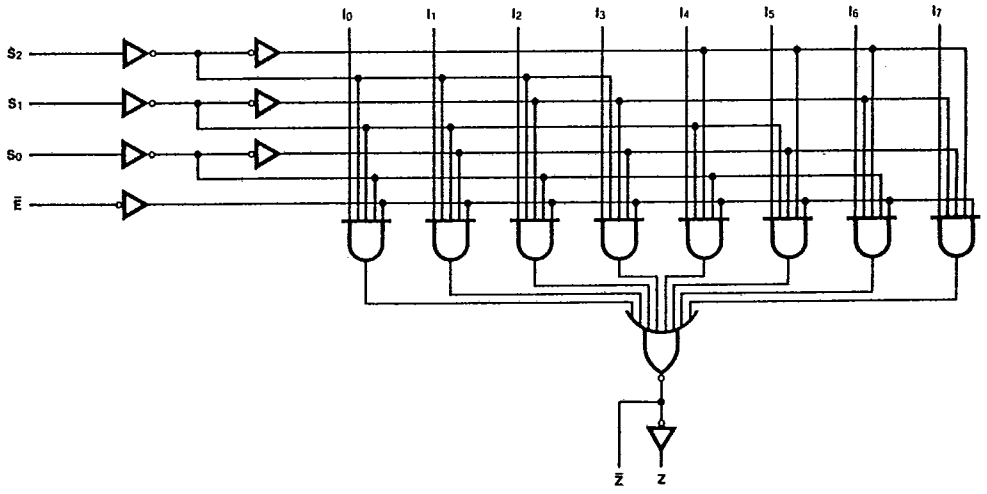
The '151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the '151 can provide any logic function of four variables and its negation.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current	XM	-20	-55	-40	-100	-20	-100	mA	V_{CC} = Max
		XC	-18	-55	-40	-100	-20	-100		
I_{CC}	Power Supply Current			48		70		10	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay		26		15		23	ns	Figs. 3-1, 3-20
t_{PHL}	S_n to $\overline{Z}$		30		13.5		34		
t_{PLH}	Propagation Delay		38		18		48	ns	Figs. 3-1, 3-20
t_{PHL}	S_n to Z		38		18		30		
t_{PLH}	Propagation Delay		21		13		24	ns	Figs. 3-1, 3-5
t_{PHL}	$\overline{E}$ to $\overline{Z}$		23		12		30		
t_{PLH}	Propagation Delay		33		16.5		42	ns	Figs. 3-1, 3-4
t_{PHL}	$\overline{E}$ to Z		33		18		32		
t_{PLH}	Propagation Delay		14		7.0		21	ns	Figs. 3-1, 3-4
t_{PHL}	I_n to $\overline{Z}$		14		7.0		20		
t_{PLH}	Propagation Delay		20		12		32	ns	Figs. 3-1, 3-5
t_{PHL}	I_n to Z		27		12		26		