HARRIS SEMICONDUCTOR

IH5216
8-Channel Differential Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5216 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI547 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any channel pair or none at all. These 4 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI547**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5216MJI	−55°C to +125°C	28 pin CERDIP
IH5216CJI	0°C to +70°C	28 pin CERDIP
IH5216CPI	0°C to +70°C	28 pin Plastic DIP

TRUTH TABLE

A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

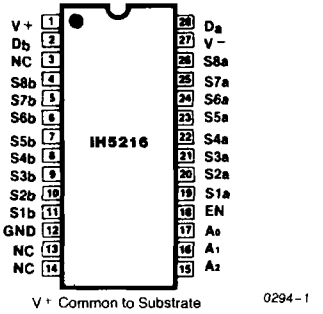

Figure 1: Pin Configuration (Outline dwgs JI, PI)

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NOTE. All typical values have been characterized but are not tested

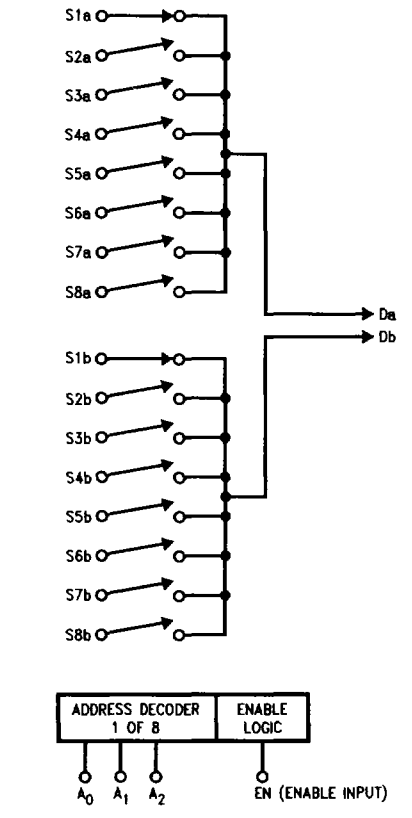

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

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ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix ..... 0°C to +70°C
M Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
M Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation*
28-Pin CERDIP Package** 1200mW
28-Pin Plastic Package*** 625mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 16mW/°C above 75°C

***Derate 8.3mV/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	16	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	Ω
		16	$V_D = -10V$ $I_S = -100\mu A$		900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$, $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	16	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		16	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.05		±1.0	±100		±2.0	±100	
		1	$V_D = -10V, V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$	±0.1		±2.0	±100		±4.0	±100	
		16	$V_{S(All)} = V_D = -10V$		±0.1		±2.0	±100		±4.0	±100	
FAULT												
I_S with Power OFF	S	16	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$ or $5V$		±1.0		±2.0			±5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		±1.0		±2.0			±5.0		

NOTE: All typical values have been characterized but are not tested.

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ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits						Units
					M Suffix			C Suffix			
					−55°C	25°C	125°C	0°C	25°C	70°C	
INPUT											
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1 A_2, A_3 or EN	4	$V_A = 0V$	0.01		−10	−30		−10	−30	µA
		4	$V_A = 15V$	0.01		10	30		10	30	
DYNAMIC											
$t_{transition}$	D		See Figure 3	0.3		1					µs
t_{open}	D		See Figure 4	0.2							
$t_{on(EN)}$	D		See Figure 5	0.6		1.5					
$t_{off(EN)}$	D			0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D		$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$. See Figure 6	25							ns
"OFF" Isolation	D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, f = 500kHz	60							dB
$C_{s(off)}$	S		$V_S = 0V$	$V_{EN} = 0V$, f = 140kHz to 1 MHz	5						pF
$C_{D(off)}$	D		$V_D = 0V$		25						
$C_{DS(off)}$	D to S		$V_S = 0V$, $V_D = 0V$		1						
SUPPLY											
Supply Current +	I^+	1	All $V_A = 0V/5V$ $V_{EN} = 5V$	0.5		0.6			1.0		mA
Supply Current −	I^-	1		0.02		0.6			1.0		

NOTE: All typical values have been characterized but are not tested.

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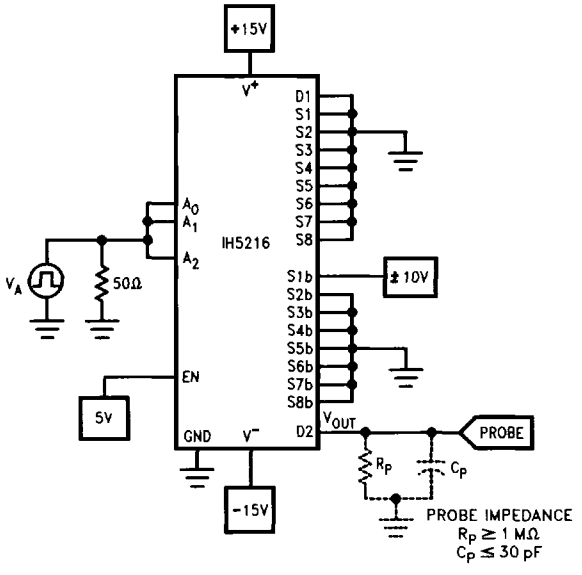

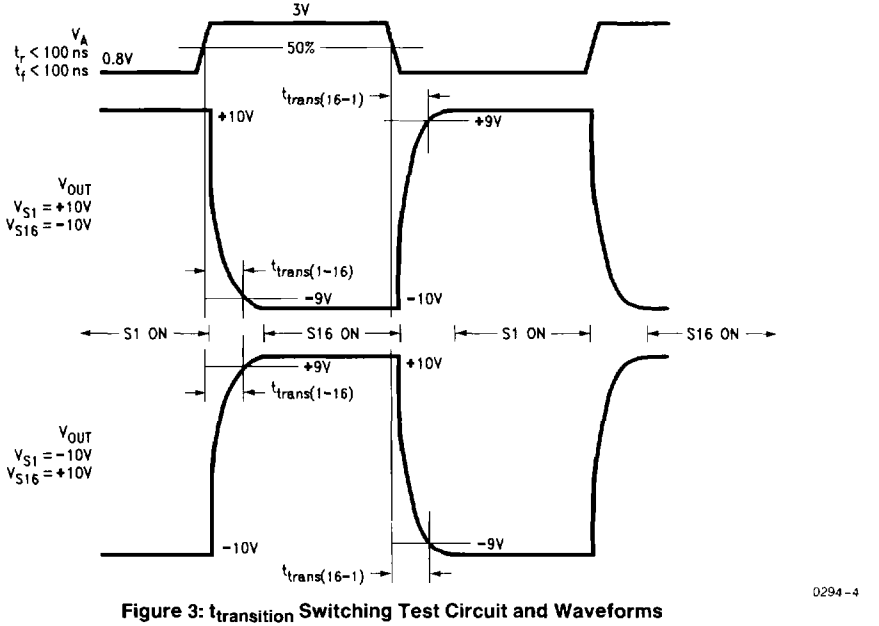

Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

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NOTE: All typical values have been characterized but are not tested.

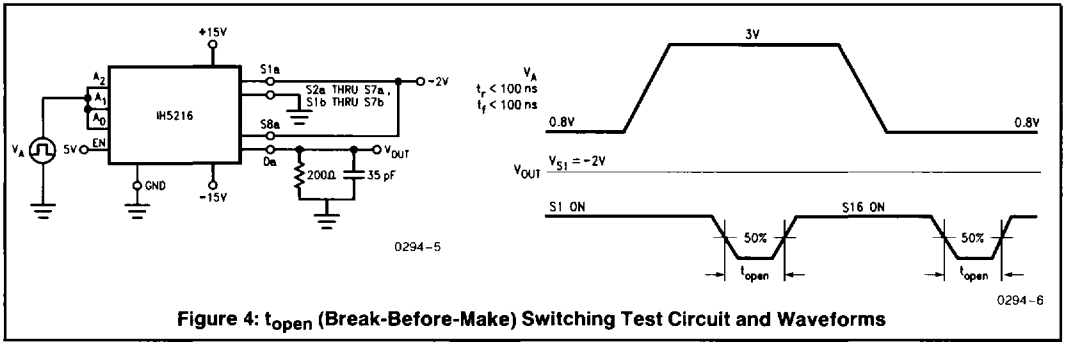

Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

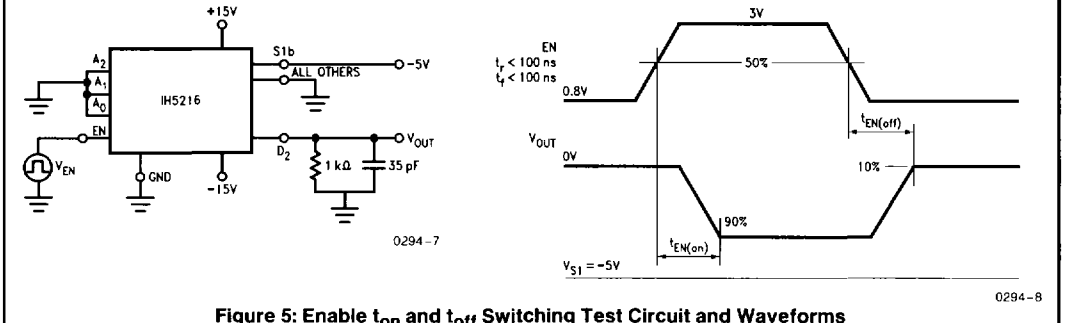

Figure 5: Enable t_{on} and t_{off} Switching Test Circuit and Waveforms

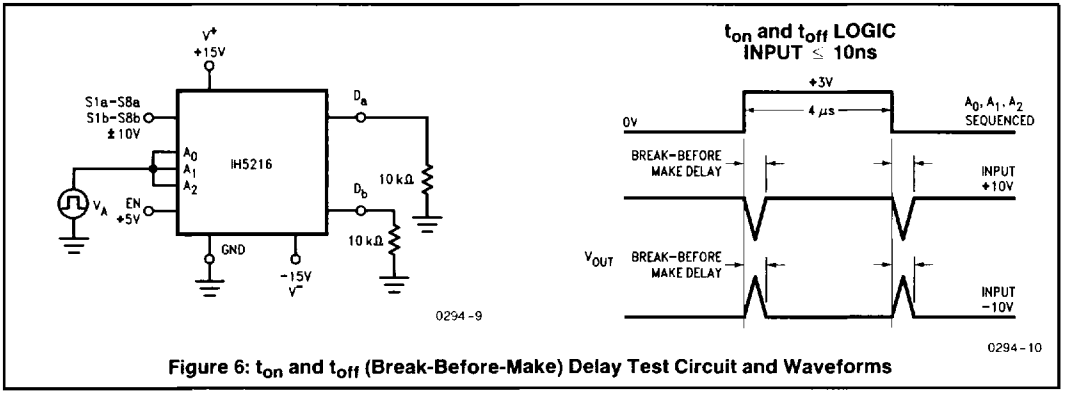

Figure 6: t_{on} and t_{off} (Break-Before-Make) Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested

DETAILED DESCRIPTION

The IH5216, like all Harris' multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5216 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5216 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.

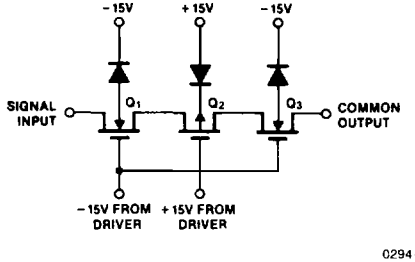

Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

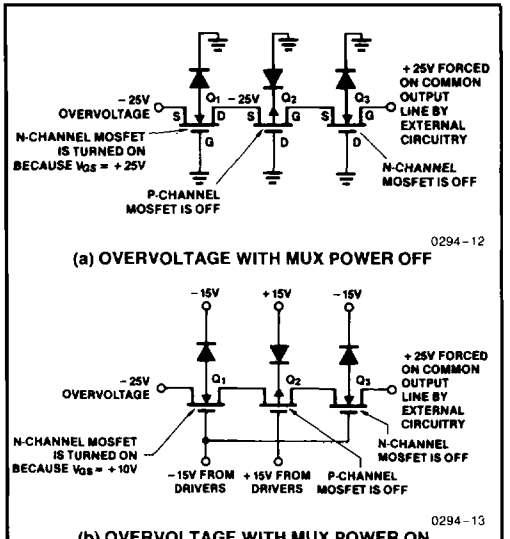

Figure 8: Overvoltage Protection

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

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NOTE: All typical values have been characterized but are not tested.

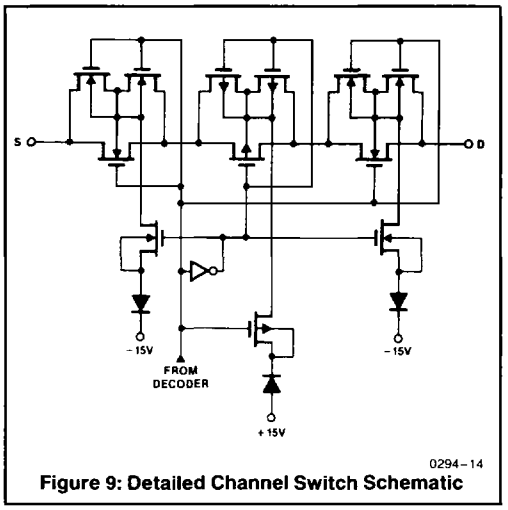

Figure 9: Detailed Channel Switch Schematic

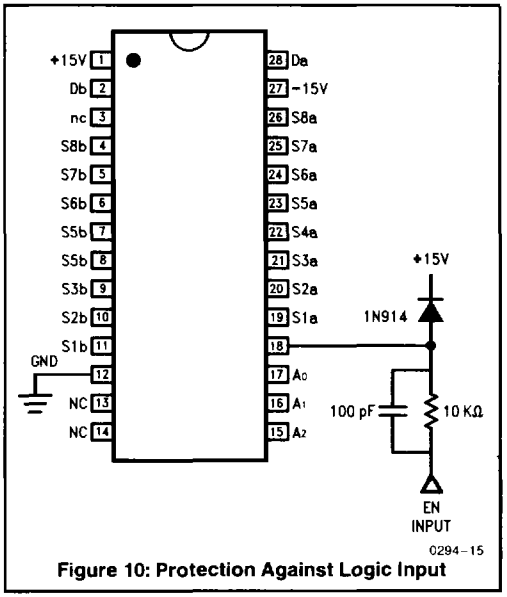

Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5216 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

USING THE IH5216 WITH SUPPLIES OTHER THAN ±15V

The IH5216 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

NOTE: All typical values have been characterized but are not tested

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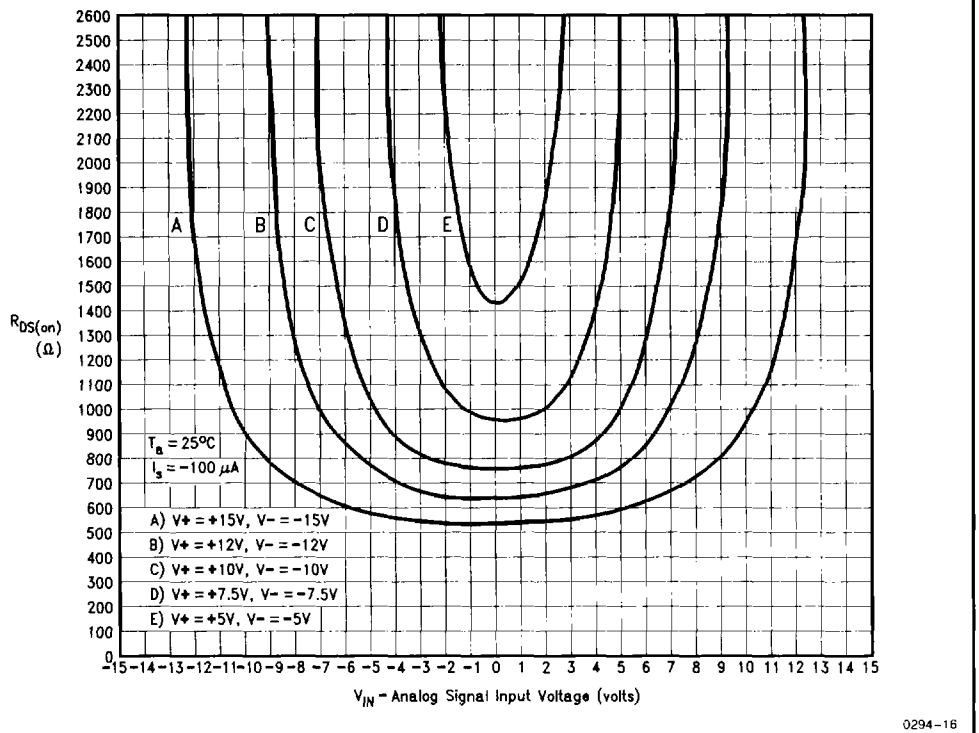

Figure 11: $r_{DS(on)}$ vs Signal Input Voltage @ $T_A = +25°C$

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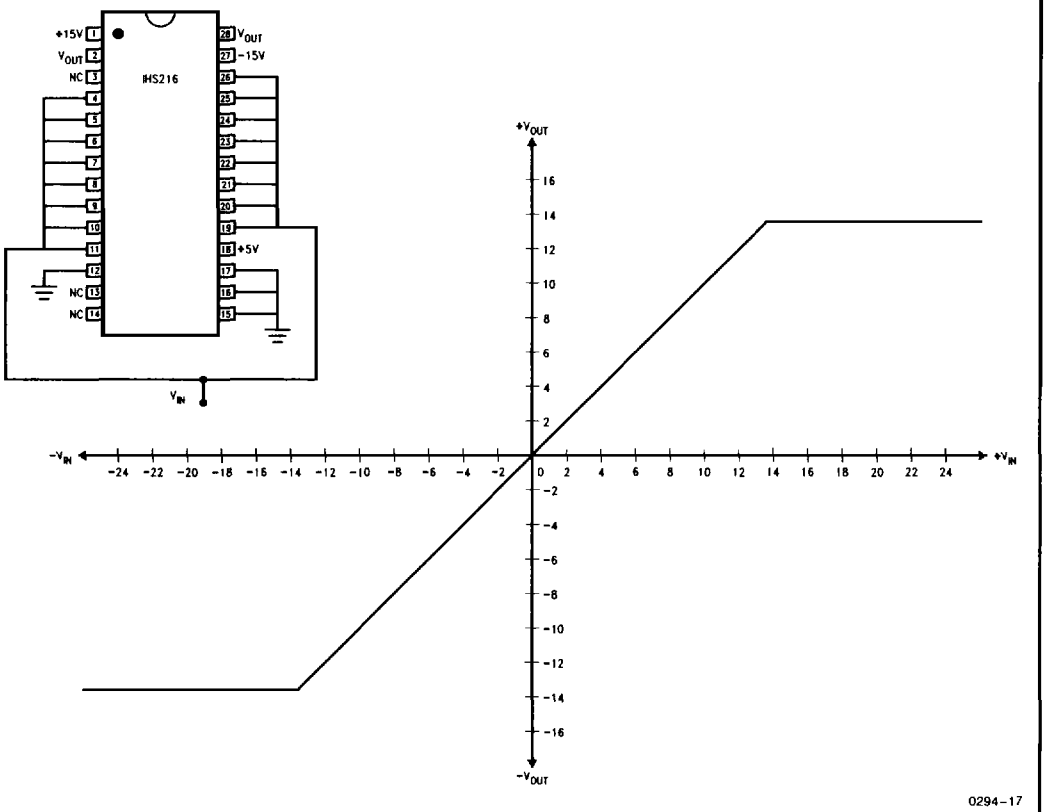

Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar

NOTE: All typical values have been characterized but are not tested.

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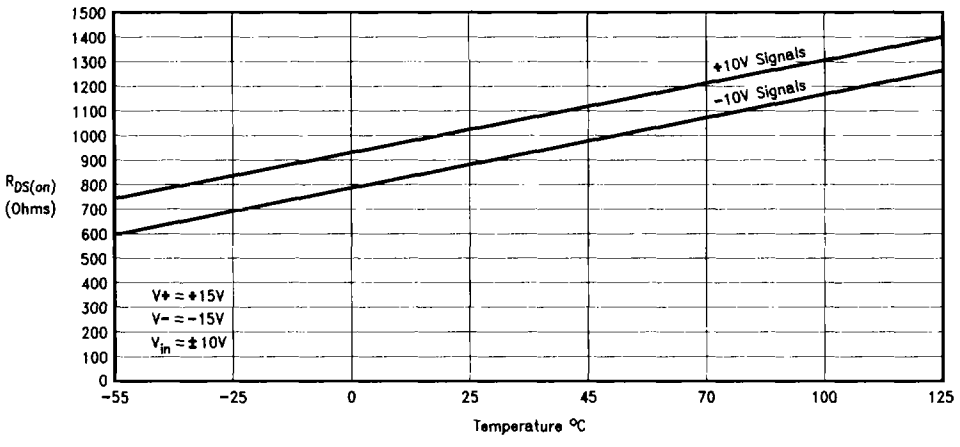

Figure 13: Typical $R_{DS(on)}$ Variation vs Temperature

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NOTE: All typical values have been characterized but are not tested

IH5216 APPLICATIONS

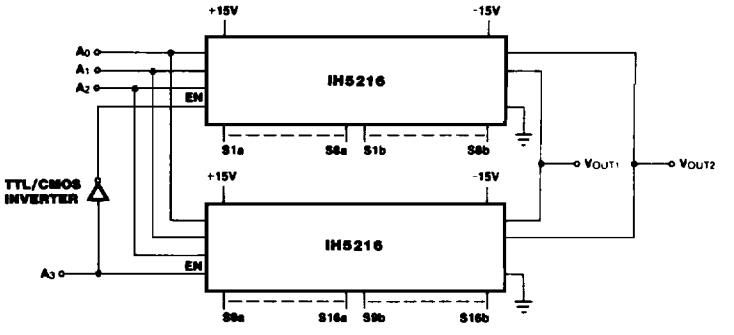

Figure 14: 2 of 32 Channel Multiplexer Using 2 IH5216s

TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

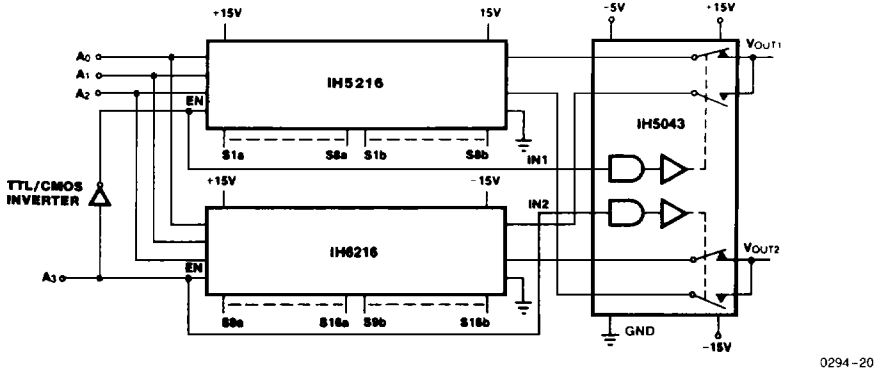

Figure 15: 2 of 32 Multiplexer Using Two IH5216s, and An IH5043 for Submultiplexing

NOTE: All typical values have been characterized but are not tested

General note on expandability

*Figures 14, 15, and 16 show how the IH5216 is expand-*ed. Figure 14 shows a 2 of 32 multiplexer, using 2 IH5216s. Corresponding output points of each of the IH5216s are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 7 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 7 $I_{D(off)}$s or about 0.45nA at room temperature. Throughput speed will be typically 0.6μs for t_{on} and 0.4μs for t_{off}, with throughput channel resistance in the 950Ω area.

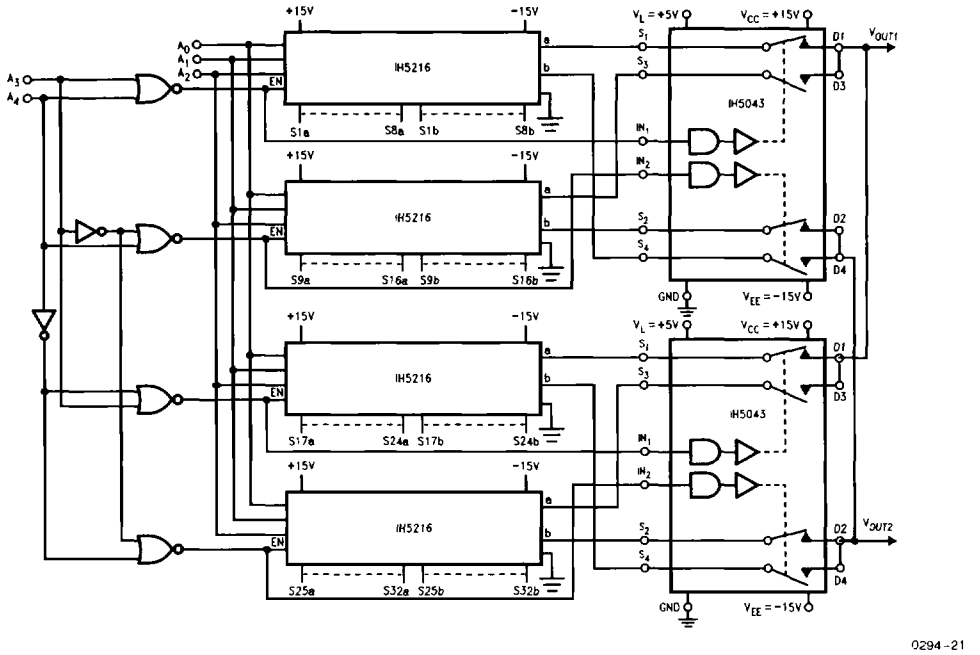

Figure 16: 2 of 64 Multiplexer Using 4 IH5216s and 2 IH5043s as Submultiplexers

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NOTE: All typical values have been characterized but are not tested

Figure 15 shows the 2 of 32 MUX, with a second tier of submultiplexing added to reduce leakage and output capacitance. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases throughput channel resistance from the 900 ohms of Figure 14 to about 950 ohms for Figure 15. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Figure 16 shows a 2 of 64 MUX using 2 tier MUXing (similar to Figure 15). The IH5043 is used for the second tier of MUXing. Each V_{out} point will see 7 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.45nA. Throughput channel resistance will be in the 950Ω area and throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the second tier of the MUX because it will switch the same AC signals as the 5216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the 5216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 14 and 15 show the EN pin used as the A_3 input. TTL and the Enable input is CMOS compatible.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles through Proper Device Selection"

NOTE: All typical values have been characterized but are not tested